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PRODUCT SPECIFICATIONS

SHARP®

Integrated Circuits Group

LH28F320BJE-PBTL90

Flash Memory

32M (2M × 16/4M × 8)

(Model No.: LHF32J06)

Spec No.: EL121090A

Issue Date: October 25, 2000

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●Please direct all queries regarding the products covered herein to a sales representative of the company.

CONTENTS

LH28F320BJE-PBTL90
32M-BIT (2Mbit ×16 / 4Mbit ×8)
Boot Block Flash MEMORY

- Low Voltage Operation
  - V_{CC}=V_{CCW}=2.7V-3.6V Single Voltage
- OTP(One Time Program) Block
  - 3963 word + 4 word Program only array
- User-Configurable ×8 or ×16 Operation
- High-Performance Read Access Time
  - 90ns(V_{CC}=2.7V-3.6V)
- Operating Temperature
  - 0°C to +70°C
- Low Power Management
  - Typ. 4µA (V_{CC}=3.0V) Standby Current
  - Automatic Power Savings Mode Decreases I_{CCR} in Static Mode
  - Typ. 120µA (V_{CC}=3.0V, T_A=+25°C, f=32kHz) Read Current
- Optimized Array Blocking Architecture
  - Two 4K-word (8K-byte) Boot Blocks
  - Six 4K-word (8K-byte) Parameter Blocks
  - Sixty-three 32K-word (64K-byte) Main Blocks
  - Bottom Boot Location
- Extended Cycling Capability
  - Minimum 100,000 Block Erase Cycles
- Enhanced Automated Suspend Options
  - Word/Byte Write Suspend to Read
  - Block Erase Suspend to Word/Byte Write
  - Block Erase Suspend to Read
- Enhanced Data Protection Features
  - Absolute Protection with $V_{CCW} \leq V_{CCWLK}$
  - Block Erase, Full Chip Erase, Word/Byte Write and Lock-Bit Configuration Lockout during Power Transitions
  - Block Locking with Command and WP#
  - Permanent Locking
- Automated Block Erase, Full Chip Erase, Word/Byte Write and Lock-Bit Configuration
  - Command User Interface (CUI)
  - Status Register (SR)
- SRAM-Compatible Write Interface
- Industry-Standard Packaging
  - 48-Lead TSOP
- ETOX™* Nonvolatile Flash Technology
- CMOS Process (P-type silicon substrate)
- Not designed or rated as radiation hardened

SHARP's LH28F320BJE-PBTL90 Flash memory is a high-density, low-cost, nonvolatile, read/write storage solution for a wide range of applications.

LH28F320BJE-PBTL90 can operate at V_{CC}=2.7V-3.6V and V_{CCW}=2.7V-3.6V or 11.7V-12.3V. Its low voltage operation capability realize battery life and suits for cellular phone application.

Its Boot, Parameter and Main-blocked architecture, low voltage and extended cycling provide for highly flexible component suitable for portable terminals and personal computers. Its enhanced suspend capabilities provide for an ideal solution for code + data storage applications.

For secure code storage applications, such as networking, where code is either directly executed out of flash or downloaded to DRAM, the LH28F320BJE-PBTL90 offers four levels of protection: absolute protection with $V_{CCW} \leq V_{CCWLK}$, selective hardware block locking or flexible software block locking. These alternatives give designers ultimate control of their code security needs.

The LH28F320BJE-PBTL90 is manufactured on SHARP's 0.25µm ETOX™* process technology. It come in industry-standard package: the 48-lead TSOP, ideal for board constrained applications.

*ETOX is a trademark of Intel Corporation.

1 INTRODUCTION

This datasheet contains LH28F320BJE-PBTL90 specifications. Section 1 provides a flash memory overview. Sections 2, 3, 4 and 5 describe the memory organization and functionality. Section 6 covers electrical specifications.

1.1 Features

Key enhancements of LH28F320BJE-PBTL90 boot block Flash memory are:

- •Single low voltage operation
- •Low power consumption
- •Enhanced Suspend Capabilities
- •Boot Block Architecture

Please note following:

- •V_{CCWLK} has been lowered to 1.0V to support 2.7V-3.6V block erase, full chip erase, word/byte write and lock-bit configuration operations. The V_{CCW} voltage transitions to GND is recommended for designs that switch V_{CCW} off during read operation.

1.2 Product Overview

The LH28F320BJE-PBTL90 is a high-performance 32M-bit Boot Block Flash memory organized as 2M-word of 16 bits or 4M-byte of 8 bits. The 2M-word/4M-byte of data is arranged in two 4K-word/8K-byte boot blocks, six 4K-word/8K-byte parameter blocks and sixty-three 32K-word/64K-byte main blocks which are individually erasable, lockable and unlockable in-system. The memory map is shown in Figure 3.

The dedicated V_{CCW} pin gives complete data protection when $V_{CCW} \leq V_{CCWLK}$.

A Command User Interface (CUI) serves as the interface between the system processor and internal operation of the device. A valid command sequence written to the CUI initiates device automation. An internal Write State Machine (WSM) automatically executes the algorithms and timings necessary for block erase, full chip erase, word/byte write and lock-bit configuration operations.

A block erase operation erases one of the device's 32K-word/64K-byte blocks typically within 1.2s (3V V_{CC}, 3V V_{CCW}), 4K-word/8K-byte blocks typically within 0.6s (3V V_{CC}, 3V V_{CCW}) independent of other blocks. Each block can be independently erased minimum 100,000 times. Block erase suspend mode allows system software to suspend block erase to read or write data from any other block.

Writing memory data is performed in word/byte increments of the device's 32K-word blocks typically within 33µs (3V V_{CC}, 3V V_{CCW}), 64K-byte blocks typically within 31µs (3V V_{CC}, 3V V_{CCW}), 4K-word blocks typically within 36µs (3V V_{CC}, 3V V_{CCW}), 8K-byte blocks typically within 32µs (3V V_{CC}, 3V V_{CCW}). Word/byte write suspend mode enables the system to read data or execute code from any other flash memory array location.

Individual block locking uses a combination of bits, seventy-one block lock-bits, a permanent lock-bit and WP# pin, to lock and unlock blocks. Block lock-bits gate block erase, full chip erase and word/byte write operations, while the permanent lock-bit gates block lock-bit modification and locked block alternation. Lock-bit configuration operations (Set Block Lock-Bit, Set Permanent Lock-Bit and Clear Block Lock-Bits commands) set and cleared lock-bits.

The status register indicates when the WSM's block erase, full chip erase, word/byte write or lock-bit configuration operation is finished.

The RY/BY# output gives an additional indicator of WSM activity by providing both a hardware signal of status (versus software polling) and status masking (interrupt masking for background block erase, for example). Status polling using RY/BY# minimizes both CPU overhead and system power consumption. When low, RY/BY# indicates that the WSM is performing a block erase, full chip erase, word/byte write or lock-bit configuration. RY/BY#-high Z indicates that the WSM is ready for a new command, block erase is suspended (and word/byte write is inactive), word/byte write is suspended, or the device is in reset mode.

The access time is 90ns (t_{AVQV}) over the operating temperature range (0°C to +70°C) and V_{CC} supply voltage range of 2.7V-3.6V.

The Automatic Power Savings (APS) feature substantially reduces active current when the device is in static mode (addresses not switching). In APS mode, the typical I_{CCR} current is 4µA (CMOS) at 3.0V V_{CC}.

When CE# and RP# pins are at V_{CC}, the I_{CC} CMOS standby mode is enabled. When the RP# pin is at GND, reset mode is enabled which minimizes power consumption and provides write protection. A reset time (t_{PHQV}) is required from RP# switching high until outputs are valid. Likewise, the device has a wake time (t_{PHEL}) from RP#-high until writes to the CUI are recognized. With RP# at GND, the WSM is reset and the status register is cleared.

Please do not execute reprogramming "0" for the bit which has already been programed "0". Overwrite operation may generate unerasable bit. In case of reprogramming "0" to the data which has been programed "1".

- Program "0" for the bit in which you want to change data from "1" to "0".
- Program "1" for the bit which has already been programmed "0".

For example, changing data from "10111101" to "10111100" requires "11111110" programming.

1.3 Product Description

1.3.1 Package Pinout

LH28F320BJE-PBTL90 Boot Block Flash memory is available in 48-lead TSOP package (see Figure 2).

1.3.2 Block Organization

This product features an asymmetrically-blocked architecture providing system memory integration. Each erase block can be erased independently of the others up to 100,000 times. For the address locations of the blocks, see the memory map in Figure 3.

Boot Blocks: The boot block is intended to replace a dedicated boot PROM in a microprocessor or microcontroller-based system. This boot block 4K words (4,096words) features hardware controllable write-protection to protect the crucial microprocessor boot code from accidental modification. The protection of the boot block is controlled using a combination of the V_{CCW}, RP#, WP# pins and block lock-bit.

Parameter Blocks: The boot block architecture includes parameter blocks to facilitate storage of frequently update small parameters that would normally require an EEPROM. By using software techniques, the word-rewrite functionality of EEPROMs can be emulated. Each boot block component contains six parameter blocks of 4K words (4,096 words) each. The protection of the parameter block is controlled using a combination of the V_{CCW}, RP# and block lock-bit.

Main Blocks: The reminder is divided into main blocks for data or code storage. Each 32M-bit device contains sixty-three 32K words (32,768 words) blocks. The protection of the main block is controlled using a combination of the V_{CCW}, RP# and block lock-bit.

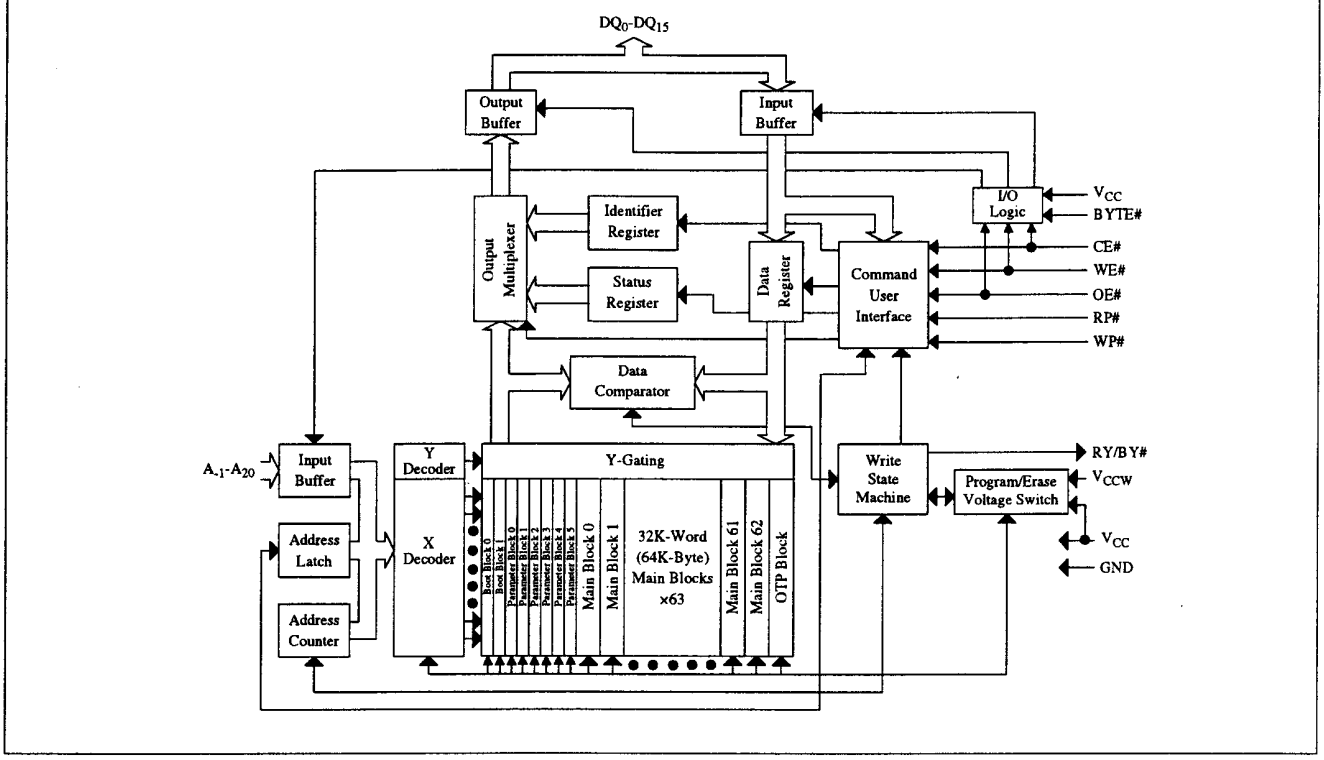


Figure 1. Block Diagram

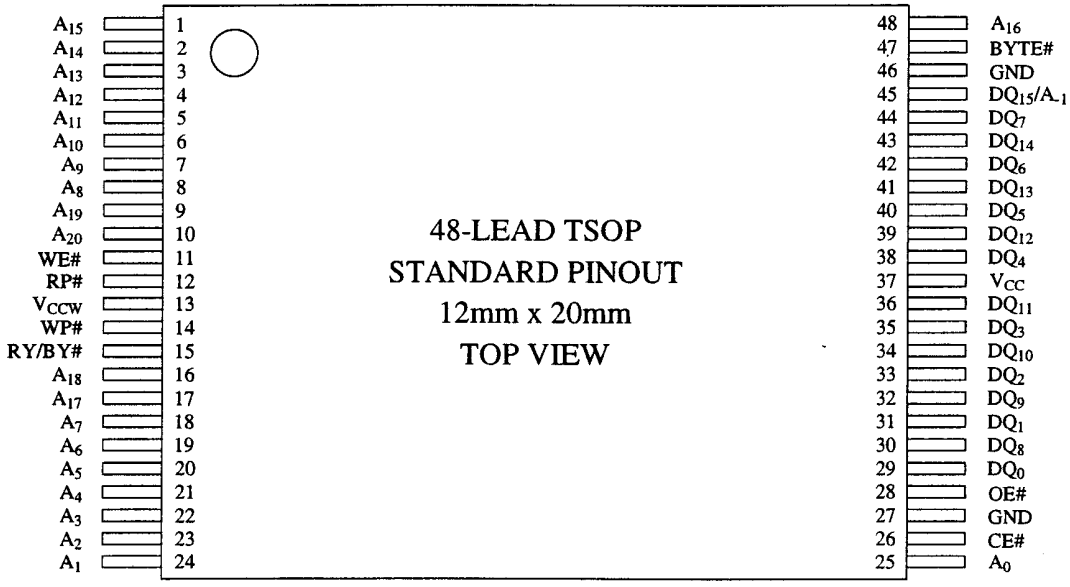


Figure 2. TSOP 48-Lead Pinout

Table 1. Pin Descriptions

Symbol	Type	Name and Function
A_{-1} A_0-A_{20}	INPUT	ADDRESS INPUTS: Inputs for addresses during read and write operations. Addresses are internally latched during a write cycle. A_{-1}: Lower address input while BYTE# is V_{IL}. A_{-1} pin changes DQ_{15} pin while BYTE# is V_{IH}. A_{15}-A_{20}: Main Block Address. A_{12}-A_{20}: Boot and Parameter Block Address.
DQ_0-DQ_{15}	INPUT/ OUTPUT	DATA INPUT/OUTPUTS: Inputs data and commands during CUI write cycles; outputs data during memory array, status register and identifier code read cycles. Data pins float to high-impedance when the chip is deselected or outputs are disabled. Data is internally latched during a write cycle. DQ_8-DQ_{15} pins are not used while byte mode (BYTE#=V_{IL}). Then, DQ_{15} pin changes A_{-1} address input.
CE#	INPUT	CHIP ENABLE: Activates the device's control logic, input buffers, decoders and sense amplifiers. CE#-high deselects the device and reduces power consumption to standby levels.
RP#	INPUT	RESET: Resets the device internal automation. RP#-high enables normal operation. When driven low, RP# inhibits write operations which provides data protection during power transitions. Exit from reset mode sets the device to read array mode. RP# must be V_{IL} during power-up.
OE#	INPUT	OUTPUT ENABLE: Gates the device's outputs during a read cycle.
WE#	INPUT	WRITE ENABLE: Controls writes to the CUI and array blocks. Addresses and data are latched on the rising edge of the WE# pulse.
WP#	INPUT	WRITE PROTECT: When WP# is V_{IL}, boot blocks cannot be written or erased. When WP# is V_{IH}, locked boot blocks can not be written or erased. WP# is not affected parameter and main blocks.
BYTE#	INPUT	BYTE ENABLE: BYTE# V_{IL} places device in byte mode (×8). All data is then input or output on DQ_{0-7}, and DQ_{8-15} float. BYTE# V_{IH} places the device in word mode (×16), and turns off the A_{-1} input buffer.
RY/BY#	OPEN DRAIN OUTPUT	READY/BUSY#: Indicates the status of the internal WSM. When low, the WSM is performing an internal operation (block erase, full chip erase, word/byte write or lock-bit configuration). RY/BY#-high Z indicates that the WSM is ready for new commands, block erase is suspended, and word/byte write is inactive, word/byte write is suspended, or the device is in reset mode.
V_{CCW}	SUPPLY	BLOCK ERASE, FULL CHIP ERASE, WORD/BYTE WRITE OR LOCK-BIT CONFIGURATION POWER SUPPLY: For erasing array blocks, writing words/bytes or configuring lock-bits. With $V_{CCW} \leq V_{CCWLK}$, memory contents cannot be altered. Block erase, full chip erase, word/byte write and lock-bit configuration with an invalid V_{CCW} (see 6.2.3 DC Characteristics) produce spurious results and should not be attempted. Applying 12V±0.3V to V_{CCW} during erase/write can only be done for a maximum of 1000 cycles on each block. V_{CCW} may be connected to 12V±0.3V for a total of 80 hours maximum.
V_{CC}	SUPPLY	DEVICE POWER SUPPLY: Do not float any power pins. With $V_{CC} \leq V_{LKO}$, all write attempts to the flash memory are inhibited. Device operations at invalid V_{CC} voltage (see 6.2.3 DC Characteristics) produce spurious results and should not be attempted.
GND	SUPPLY	GROUND: Do not float any ground pins.

Bottom Boot

$[A_{20}\text{-}A_0]$			$[A_{20}\text{-}A_{-1}]$
0FFFFF	32KW/64KB Main Block	30	1FFFFF
0F8000			1F0000
0F7FFF	32KW/64KB Main Block	29	1EFFFF
0F0000			1E0000
0EFFFF	32KW/64KB Main Block	28	1DFFFF
0E8000			1D0000
0E7FFF	32KW/64KB Main Block	27	1CFFFF
0E0000			1C0000
0DFFFF	32KW/64KB Main Block	26	1BFFFF
0D8000			1B0000
0D7FFF	32KW/64KB Main Block	25	1AFFFF
0D0000			1A0000
0CFFFF	32KW/64KB Main Block	24	19FFFF
0C8000			190000
0C7FFF	32KW/64KB Main Block	23	18FFFF
0C0000			180000
0BFFFF	32KW/64KB Main Block	22	17FFFF
0B8000			170000
0B7FFF	32KW/64KB Main Block	21	16FFFF
0B0000			160000
0AFFFF	32KW/64KB Main Block	20	15FFFF
0A8000			150000
0A7FFF	32KW/64KB Main Block	19	14FFFF
0A0000			140000
09FFFF	32KW/64KB Main Block	18	13FFFF
098000			130000
097FFF	32KW/64KB Main Block	17	12FFFF
090000			120000
08FFFF	32KW/64KB Main Block	16	11FFFF
088000			110000
087FFF	32KW/64KB Main Block	15	10FFFF
080000			100000
07FFFF	32KW/64KB Main Block	14	0FFFFF
078000			0F0000
077FFF	32KW/64KB Main Block	13	0EFFFF
070000			0E0000
06FFFF	32KW/64KB Main Block	12	0DFFFF
068000			0D0000
067FFF	32KW/64KB Main Block	11	0CFFFF
060000			0C0000
05FFFF	32KW/64KB Main Block	10	0BFFFF
058000			0B0000
057FFF	32KW/64KB Main Block	9	0AFFFF
050000			0A0000
04FFFF	32KW/64KB Main Block	8	09FFFF
048000			090000
047FFF	32KW/64KB Main Block	7	08FFFF
040000			080000
03FFFF	32KW/64KB Main Block	6	07FFFF
038000			070000
037FFF	32KW/64KB Main Block	5	06FFFF
030000			060000
02FFFF	32KW/64KB Main Block	4	05FFFF
028000			050000
027FFF	32KW/64KB Main Block	3	04FFFF
020000			040000
01FFFF	32KW/64KB Main Block	2	03FFFF
018000			030000
017FFF	32KW/64KB Main Block	1	02FFFF
010000			020000
00FFFF	32KW/64KB Main Block	0	01FFFF
008000			010000
007FFF	4KW/8KB Parameter Block	5	00FFFF
007000			00E000
006FFF	4KW/8KB Parameter Block	4	00DFFF
006000			00C000
005FFF	4KW/8KB Parameter Block	3	00BFFF
005000			00A000
004FFF	4KW/8KB Parameter Block	2	009FFF
004000			008000
003FFF	4KW/8KB Parameter Block	1	007FFF
003000			006000
002FFF	4KW/8KB Parameter Block	0	005FFF
002000			004000
001FFF	4KW/8KB Boot Block	1	003FFF
001000			002000
000FFF	4KW/8KB Boot Block	0	001FFF
000000			000000

$[A_{20}\text{-}A_0]$			$[A_{20}\text{-}A_{-1}]$
1FFFFF	32KW/64KB Main Block	62	3FFFFF
1F8000			3F0000
1F7FFF	32KW/64KB Main Block	61	3EFFFF
1F0000			3E0000
1EFFFF	32KW/64KB Main Block	60	3DFFFF
1E8000			3D0000
1E7FFF	32KW/64KB Main Block	59	3CFFFF
1E0000			3C0000
1DFFFF	32KW/64KB Main Block	58	3BFFFF
1D8000			3B0000
1D7FFF	32KW/64KB Main Block	57	3AFFFF
1D0000			3A0000
1CFFFF	32KW/64KB Main Block	56	39FFFF
1C8000			390000
1C7FFF	32KW/64KB Main Block	55	38FFFF
1C0000			380000
1BFFFF	32KW/64KB Main Block	54	37FFFF
1B8000			370000
1B7FFF	32KW/64KB Main Block	53	36FFFF
1B0000			360000
1AFFFF	32KW/64KB Main Block	52	35FFFF
1A8000			350000
1A7FFF	32KW/64KB Main Block	51	34FFFF
1A0000			340000
19FFFF	32KW/64KB Main Block	50	33FFFF
198000			330000
197FFF	32KW/64KB Main Block	49	32FFFF
190000			320000
18FFFF	32KW/64KB Main Block	48	31FFFF
188000			310000
187FFF	32KW/64KB Main Block	47	30FFFF
180000			300000
17FFFF	32KW/64KB Main Block	46	2FFFFF
178000			2F0000
177FFF	32KW/64KB Main Block	45	2EFFFF
170000			2E0000
16FFFF	32KW/64KB Main Block	44	2DFFFF
168000			2D0000
167FFF	32KW/64KB Main Block	43	2CFFFF
160000			2C0000
15FFFF	32KW/64KB Main Block	42	2BFFFF
158000			2B0000
157FFF	32KW/64KB Main Block	41	2AFFFF
150000			2A0000
14FFFF	32KW/64KB Main Block	40	29FFFF
148000			290000
147FFF	32KW/64KB Main Block	39	28FFFF
140000			280000
13FFFF	32KW/64KB Main Block	38	27FFFF
138000			270000
137FFF	32KW/64KB Main Block	37	26FFFF
130000			260000
12FFFF	32KW/64KB Main Block	36	25FFFF
128000			250000
127FFF	32KW/64KB Main Block	35	24FFFF
120000			240000
11FFFF	32KW/64KB Main Block	34	23FFFF
118000			230000
117FFF	32KW/64KB Main Block	33	22FFFF
110000			220000
10FFFF	32KW/64KB Main Block	32	21FFFF
108000			210000
107FFF	32KW/64KB Main Block	31	20FFFF
100000			200000

Figure 3. Memory Map

2 PRINCIPLES OF OPERATION

The LH28F320BJE-PBTL90 flash memory includes an on-chip WSM to manage block erase, full chip erase, word/byte write and lock-bit configuration functions. It allows for: fixed power supplies during block erase, full chip erase, word/byte write and lock-bit configuration, and minimal processor overhead with RAM-like interface timings.

After initial device power-up or return from reset mode (see section 3 Bus Operations), the device defaults to read array mode. Manipulation of external memory control pins allow array read, standby and output disable operations.

Status register and identifier codes can be accessed through the CUI independent of the V_{CCW} voltage. High voltage on V_{CCW} enables successful block erase, full chip erase, word/byte write and lock-bit configurations. All functions associated with altering memory contents–block erase, full chip erase, word/byte write, lock-bit configuration, status and identifier codes–are accessed via the CUI and verified through the status register.

Commands are written using standard microprocessor write timings. The CUI contents serve as input to the WSM, which controls the block erase, full chip erase, word/byte write and lock-bit configuration. The internal algorithms are regulated by the WSM, including pulse repetition, internal verification and margining of data. Addresses and data are internally latched during write cycles. Writing the appropriate command outputs array data, accesses the identifier codes or outputs status register data.

Interface software that initiates and polls progress of block erase, full chip erase, word/byte write and lock-bit configuration can be stored in any block. This code is copied to and executed from system RAM during flash memory updates. After successful completion, reads are again possible via the Read Array command. Block erase suspend allows system software to suspend a block erase to read/write data from/to blocks other than that which is suspend. Word/byte write suspend allows system software to suspend a word/byte write to read data from any other flash memory array location.

2.1 Data Protection

When $V_{CCW} \leq V_{CCWLK}$, memory contents cannot be altered. The CUI, with two-step block erase, full chip erase, word/byte write or lock-bit configuration command sequences, provides protection from unwanted operations even when high voltage is applied to V_{CCW}. All write functions are disabled when V_{CC} is below the write lockout voltage V_{LKO} or when RP# is at V_{IL}. The device's block locking capability provides additional protection from inadvertent code or data alteration by gating block erase, full chip erase and word/byte write operations. Refer to Table 5 for write protection alternatives.

3 BUS OPERATION

The local CPU reads and writes flash memory in-system. All bus cycles to or from the flash memory conform to standard microprocessor bus cycles.

3.1 Read

Information can be read from any block, identifier codes or status register independent of the V_{CCW} voltage. RP# can be at V_{IH}.

The first task is to write the appropriate read mode command (Read Array, Read Identifier Codes or Read Status Register) to the CUI. Upon initial device power-up or after exit from reset mode, the device automatically resets to read array mode. Six control pins dictate the data flow in and out of the component: CE#, OE#, BYTE#, WE#, RP# and WP#. CE# and OE# must be driven active to obtain data at the outputs. CE# is the device selection control, and when active enables the selected memory device. OE# is the data output (DQ_0-DQ_{15}) control and when active drives the selected memory data onto the I/O bus. BYTE# is the device I/O interface mode control. WE# must be at V_{IH}, RP# must be at V_{IH}, and BYTE# and WP# must be at V_{IL} or V_{IH}. Figure 16, 17 illustrates read cycle.

3.2 Output Disable

With OE# at a logic-high level (V_{IH}), the device outputs are disabled. Output pins (DQ_0-DQ_{15}) are placed in a high-impedance state.

3.3 Standby

CE# at a logic-high level (V_{IH}) places the device in standby mode which substantially reduces device power consumption. DQ_0-DQ_{15} outputs are placed in a high-impedance state independent of OE#. If deselected during block erase, full chip erase, word/byte write or lock-bit configuration, the device continues functioning, and consuming active power until the operation completes.

3.4 Reset

RP# at V_{IL} initiates the reset mode.

In read modes, RP#-low deselects the memory, places output drivers in a high-impedance state and turns off all internal circuits. RP# must be held low for a minimum of 100ns. Time t_{PHQV} is required after return from reset mode until initial memory access outputs are valid. After this wake-up interval, normal operation is restored. The CUI is reset to read array mode and status register is set to 80H.

During block erase, full chip erase, word/byte write or lock-bit configuration modes, RP#-low will abort the operation. RY/BY# remains low until the reset operation is complete. Memory contents being altered are no longer valid; the data may be partially erased or written. Time t_{PHWL} is required after RP# goes to logic-high (V_{IH}) before another command can be written.

As with any automated device, it is important to assert RP# during system reset. When the system comes out of reset, it expects to read from the flash memory. Automated flash memories provide status information when accessed during block erase, full chip erase, word/byte write or lock-bit configuration modes. If a CPU reset occurs with no flash memory reset, proper CPU initialization may not occur because the flash memory may be providing status information instead of array data. SHARP's flash memories allow proper CPU initialization following a system reset through the use of the RP# input. In this application, RP# is controlled by the same RESET# signal that resets the system CPU.

3.5 Read Identifier Codes

The read identifier codes operation outputs the manufacturer code, device code, block lock configuration codes for each block and the permanent lock configuration code (see Figure 4). Using the manufacturer and device codes, the system CPU can automatically match the device with its proper algorithms. The block lock and permanent lock configuration codes identify locked and unlocked blocks and permanent lock-bit setting.

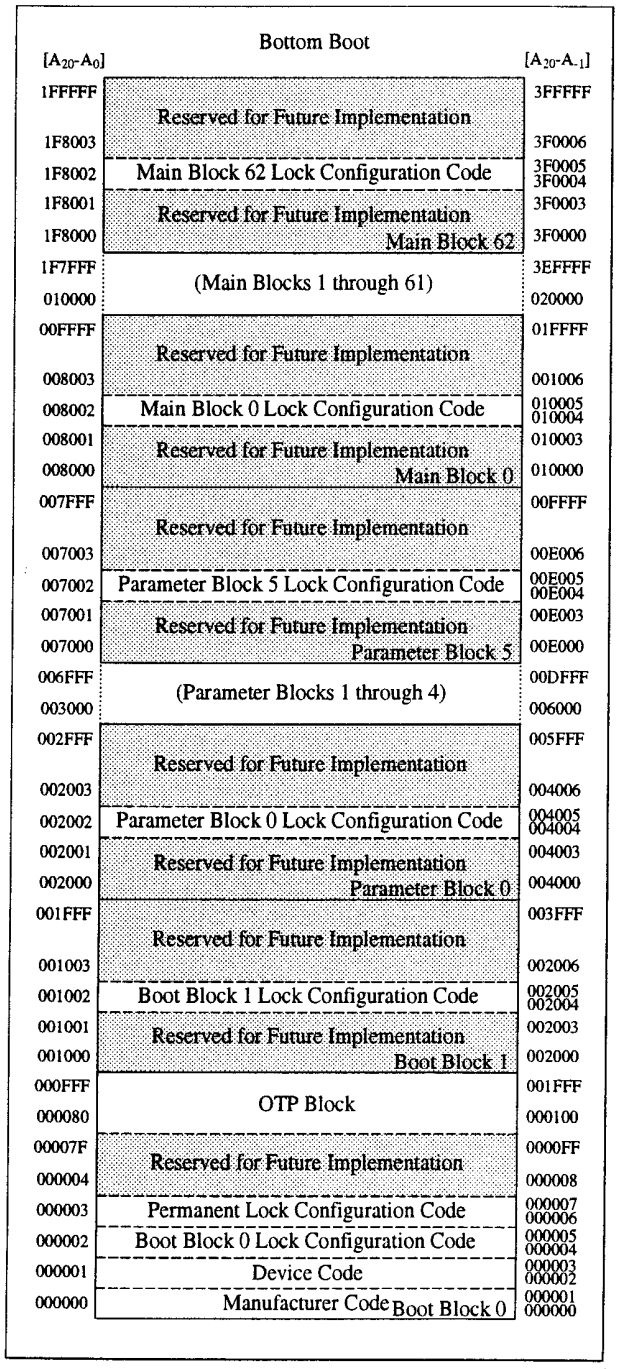


Figure 4. Device Identifier Code Memory Map

3.6 OTP(One Time Program) Block

The OTP block is a special block that can not be erased. The block is divided into two parts. One is a factory program area where a unique number can be written according to customer requirements in SHARP factory. This factory program area is "READ ONLY" (Already locked). The other is a customer program area that can be used by customers. This customer program area can be locked. After locking, this customer program area is protected permanently.

The OTP block is read in Configuration Read Mode by writing Read Identifier Codes command(90H). To return to Read Array Mode, write Read Array command(FFH).

The OTP block is programmed by writing OTP Program command(C0H). First write OTP Program command and then write data with address to the device (See Figure 5). If OTP program is failed, SR.4(WORD/BYTE WRITE AND SET LOCK-BIT STATUS) bit is set to "1". And if this OTP block is locked, SR.1(DEVICE PROTECT STATUS) bit is set to "1" too.

The OTP block is also locked by writing OTP Program command(C0H). First write OTP Program command and then write data "FFFDH" with address "80H" to the device. Address "80H" of OTP block is OTP lock information. Bit 0 of address "80H" means factory program area lock status("1" is "NOT LOCKED", "0" is "LOCKED"). Bit 1 of address "80H" means customer program area lock status. The OTP lock information can not be cleared, after once it is set.

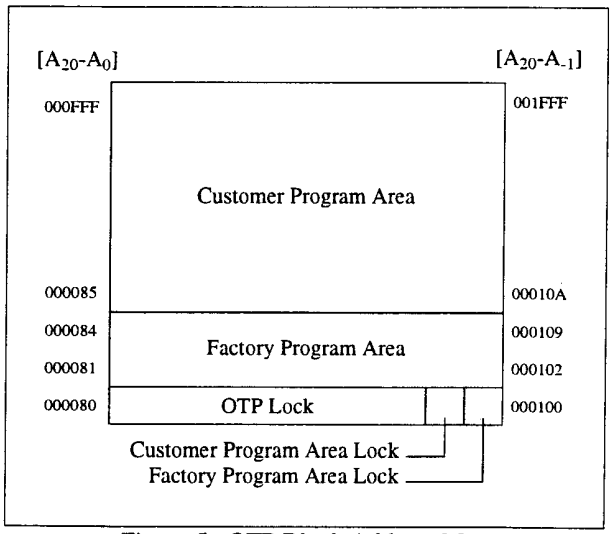


Figure 5. OTP Block Address Map

3.7 Write

Writing commands to the CUI enable reading of device data and identifier codes. They also control inspection and clearing of the status register. When V_{CC}=2.7V-3.6V and V_{CCW}=$V_{CCWH1/2}$, the CUI additionally controls block erase, full chip erase, word/byte write and lock-bit configuration.

The Block Erase command requires appropriate command data and an address within the block to be erased. The Full Chip Erase command requires appropriate command data and an address within the device. The Word/Byte Write command requires the command and address of the location to be written. Set Permanent and Block Lock-Bit commands require the command and address within the device (Permanent Lock) or block within the device (Block Lock) to be locked. The Clear Block Lock-Bits command requires the command and address within the device.

The CUI does not occupy an addressable memory location. It is written when WE# and CE# are active. The address and data needed to execute a command are latched on the rising edge of WE# or CE# (whichever goes high first). Standard microprocessor write timings are used. Figures 18 and 19 illustrate WE# and CE# controlled write operations.

4 COMMAND DEFINITIONS

When the V_{CCW} voltage ≤V_{CCWLK}, read operations from the status register, identifier codes, or blocks are enabled. Placing $V_{CCWH1/2}$ on V_{CCW} enables successful block erase, full chip erase, word/byte write and lock-bit configuration operations.

Device operations are selected by writing specific commands into the CUI. Table 3 defines these commands.

Table 2.1. Bus Operations (BYTE#=V_{IH})(1,2)

Mode	Notes	RP#	CE#	OE#	WE#	Address	V_{CCW}	DQ_{0-15}	RY/BY#(3)
Read	8	V_{IH}	V_{IL}	V_{IL}	V_{IH}	X	X	D_{OUT}	X
Output Disable		V_{IH}	V_{IL}	V_{IH}	V_{IH}	X	X	High Z	X
Standby		V_{IH}	V_{IH}	X	X	X	X	High Z	X
Reset	4	V_{IL}	X	X	X	X	X	High Z	High Z
Read Identifier Codes	8	V_{IH}	V_{IL}	V_{IL}	V_{IH}	See Figure 4, 5	X	Note 5	High Z
Write	6,7,8	V_{IH}	V_{IL}	V_{IH}	V_{IL}	X	X	D_{IN}	X

Table 2.2. Bus Operations (BYTE#=V_{IL})(1,2)

Mode	Notes	RP#	CE#	OE#	WE#	Address	V_{CCW}	DQ_{0-7}	RY/BY#(3)
Read	8	V_{IH}	V_{IL}	V_{IL}	V_{IH}	X	X	D_{OUT}	X
Output Disable		V_{IH}	V_{IL}	V_{IH}	V_{IH}	X	X	High Z	X
Standby		V_{IH}	V_{IH}	X	X	X	X	High Z	X
Reset	4	V_{IL}	X	X	X	X	X	High Z	High Z
Read Identifier Codes	8	V_{IH}	V_{IL}	V_{IL}	V_{IH}	See Figure 4, 5	X	Note 5	High Z
Write	6,7,8	V_{IH}	V_{IL}	V_{IH}	V_{IL}	X	X	D_{IN}	X

NOTES:
1. Refer to DC Characteristics. When V_{CCW}≤V_{CCWLK}, memory contents can be read, but not altered.
2. X can be V_{IL} or V_{IH} for control pins and addresses, and V_{CCWLK} or $V_{CCWH1/2}$ for V_{CCW}. See DC Characteristics for V_{CCWLK} voltages.
3. RY/BY# is V_{OL} when the WSM is executing internal block erase, full chip erase, word/byte write or lock-bit configuration algorithms. It is High Z during when the WSM is not busy, in block erase suspend mode (with word/byte write inactive), word/byte write suspend mode or reset mode.
4. RP# at GND±0.2V ensures the lowest power consumption.
5. See Section 4.2 for read identifier code data.
6. Command writes involving block erase, full chip erase, word/byte write or lock-bit configuration are reliably executed when V_{CCW}=$V_{CCWH1/2}$ and V_{CC}=2.7V-3.6V.
7. Refer to Table 3 for valid D_{IN} during a write operation.
8. Never hold OE# low and WE# low at the same timing.

Table 3. Command Definitions[10]

Command	Bus Cycles Req'd.	Notes	First Bus Cycle			Second Bus Cycle		
			Oper[1]	Addr[2]	Data[3]	Oper[1]	Addr[2]	Data[3]
Read Array/Reset	1		Write	X	FFH			
Read Identifier Codes	≥2	4	Write	X	90H	Read	IA	ID
Read Status Register	2		Write	X	70H	Read	X	SRD
Clear Status Register	1		Write	X	50H			
Block Erase	2	5	Write	X	20H	Write	BA	D0H
Full Chip Erase	2		Write	X	30H	Write	X	D0H
Word/Byte Write	2	5,6	Write	X	40H or 10H	Write	WA	WD
Block Erase and Word/Byte Write Suspend	1	5	Write	X	B0H			
Block Erase and Word/Byte Write Resume	1	5	Write	X	D0H			
Set Block Lock-Bit	2	8	Write	X	60H	Write	BA	01H
Clear Block Lock-Bits	2	7,8	Write	X	60H	Write	X	D0H
Set Permanent Lock-Bit	2	9	Write	X	60H	Write	X	F1H
OTP Program	2		Write	X	C0H	Write	OA	OD

NOTES:
1. BUS operations are defined in Table 2.1 and Table 2.2.
2. X=Any valid address within the device.
   IA=Identifier Code Address: see Figure 4.
   BA=Address within the block being erased.
   WA=Address of memory location to be written.
   OA=Address of OTP block to be written: see Figure 5.
3. ID=Data read from identifier codes.
   SRD=Data read from status register. See Table 6 for a description of the status register bits.
   WD=Data to be written at location WA. Data is latched on the rising edge of WE# or CE# (whichever goes high first).
   OD=Data to be written at location OA. Data is latched on the rising edge of WE# or CE# (whichever goes high first).
4. Following the Read Identifier Codes command, read operations access manufacturer, device, block lock configuration and permanent lock configuration codes. See Section 4.2 for read identifier code data.
5. If WP# is V_{IL}, boot blocks are locked without block lock-bits state. If WP# is V_{IH}, boot blocks are locked by block lock-bits. The parameter and main blocks are locked by block lock-bits without WP# state.
6. Either 40H or 10H are recognized by the WSM as the word/byte write setup.
7. The clear block lock-bits operation simultaneously clears all block lock-bits.
8. If the permanent lock-bit is set, Set Block Lock-Bit and Clear Block Lock-Bits commands can not be done.
9. Once the permanent lock-bit is set, permanent lock-bit reset is unable.
10. Commands other than those shown above are reserved by SHARP for future device implementations and should not be used.

4.1 Read Array Command

Upon initial device power-up and after exit from reset mode, the device defaults to read array mode. This operation is also initiated by writing the Read Array command. The device remains enabled for reads until another command is written. Once the internal WSM has started a block erase, full chip erase, word/byte write or lock-bit configuration the device will not recognize the Read Array command until the WSM completes its operation unless the WSM is suspended via an Erase Suspend or Word/Byte Write Suspend command. The Read Array command functions independently of the V_{CCW} voltage and RP# can be V_{IH}.

4.2 Read Identifier Codes Command

The identifier code operation is initiated by writing the Read Identifier Codes command. Following the command write, read cycles from addresses shown in Figure 4 retrieve the manufacturer, device, block lock configuration and permanent lock configuration codes (see Table 4 for identifier code values). To terminate the operation, write another valid command. Like the Read Array command, the Read Identifier Codes command functions independently of the V_{CCW} voltage and RP# can be V_{IH}. Following the Read Identifier Codes command, the following information can be read:

Table 4. Identifier Codes

Code	Address(2) [A_{20}-A_0]	Data(3) [DQ_7-DQ_0]
Manufacture Code	00000H	B0H
Device Code	00001H	E3H
Block Lock Configuration	BA(1)+2	
•Block is Unlocked		DQ_0=0
•Block is Locked		DQ_0=1
•Reserved for Future Use		DQ_{1-7}
Permanent Lock Configuration	00003H	
•Device is Unlocked		DQ_0=0
•Device is Locked		DQ_0=1
•Reserved for Future Use		DQ_{1-7}

NOTE:
1. BA selects the specific block lock configuration code to be read. See Figure 4 for the device identifier code memory map.
2. A_{-1} don't care in byte mode.
3. DQ_{15}-DQ_8 outputs 00H in word mode.

4.3 Read Status Register Command

The status register may be read to determine when a block erase, full chip erase, word/byte write or lock-bit configuration is complete and whether the operation completed successfully. It may be read at any time by writing the Read Status Register command. After writing this command, all subsequent read operations output data from the status register until another valid command is written. The status register contents are latched on the falling edge of OE# or CE#, whichever occurs. OE# or CE# must toggle to V_{IH} before further reads to update the status register latch. The Read Status Register command functions independently of the V_{CCW} voltage. RP# can be V_{IH}.

4.4 Clear Status Register Command

Status register bits SR.5, SR.4, SR.3 or SR.1 are set to "1"s by the WSM and can only be reset by the Clear Status Register command. These bits indicate various failure conditions (see Table 6). By allowing system software to reset these bits, several operations (such as cumulatively erasing multiple blocks or writing several words/bytes in sequence) may be performed. The status register may be polled to determine if an error occurred during the sequence.

To clear the status register, the Clear Status Register command (50H) is written. It functions independently of the applied V_{CCW} Voltage. RP# can be V_{IH}. This command is not functional during block erase or word/byte write suspend modes.

4.5 Block Erase Command

Erase is executed one block at a time and initiated by a two-cycle command. A block erase setup is first written, followed by an block erase confirm. This command sequence requires appropriate sequencing and an address within the block to be erased (erase changes all block data to FFFFH/FFH). Block preconditioning, erase, and verify are handled internally by the WSM (invisible to the system). After the two-cycle block erase sequence is written, the device automatically outputs status register data when read (see Figure 6). The CPU can detect block erase completion by analyzing the output data of the RY/BY# pin or status register bit SR.7.

When the block erase is complete, status register bit SR.5 should be checked. If a block erase error is detected, the status register should be cleared before system software attempts corrective actions. The CUI remains in read status register mode until a new command is issued.

This two-step command sequence of set-up followed by execution ensures that block contents are not accidentally erased. An invalid Block Erase command sequence will result in both status register bits SR.4 and SR.5 being set to "1". Also, reliable block erasure can only occur when V_{CC}=2.7V-3.6V and V_{CCW}=$V_{CCWH1/2}$. In the absence of this high voltage, block contents are protected against erasure. If block erase is attempted while $V_{CCW} \leq V_{CCWLK}$, SR.3 and SR.5 will be set to "1". Successful block erase requires for boot blocks that WP# is V_{IH} and the corresponding block lock-bit be cleared. In parameter and main blocks case, it must be cleared the corresponding block lock-bit. If block erase is attempted when the excepting above conditions, SR.1 and SR.5 will be set to "1".

4.6 Full Chip Erase Command

This command followed by a confirm command erases all of the unlocked blocks. A full chip erase setup (30H) is first written, followed by a full chip erase confirm (D0H). After a confirm command is written, device erases the all unlocked blocks block by block. This command sequence requires appropriate sequencing. Block preconditioning, erase and verify are handled internally by the WSM (invisible to the system). After the two-cycle full chip erase sequence is written, the device automatically outputs status register data when read (see Figure 7). The CPU can detect full chip erase completion by analyzing the output data of the RY/BY# pin or status register bit SR.7.

When the full chip erase is complete, status register bit SR.5 should be checked. If erase error is detected, the status register should be cleared before system software attempts corrective actions. The CUI remains in read status register mode until a new command is issued. If error is detected on a block during full chip erase operation, WSM stops erasing. Full chip erase operation start from lower address block, finish the higher address block. Full chip erase can not be suspended.

This two-step command sequence of set-up followed by execution ensures that block contents are not accidentally erased. An invalid Full Chip Erase command sequence will result in both status register bits SR.4 and SR.5 being set to "1". Also, reliable full chip erasure can only occur when V_{CC}=2.7V-3.6V and V_{CCW}=$V_{CCWH1/2}$. In the absence of this high voltage, block contents are protected against erasure. If full chip erase is attempted while $V_{CCW} \leq V_{CCWLK}$, SR.3 and SR.5 will be set to "1". Successful full chip erase requires for boot blocks that WP# is V_{IH} and the corresponding block lock-bit be cleared. In parameter and main blocks case, it must be cleared the corresponding block lock-bit. If all blocks are locked, SR.1 and SR.5 will be set to "1".

4.7 Word/Byte Write Command

Word/Byte write is executed by a two-cycle command sequence. Word/Byte write setup (standard 40H or alternate 10H) is written, followed by a second write that specifies the address and data (latched on the rising edge of WE#). The WSM then takes over, controlling the word/byte write and write verify algorithms internally. After the word/byte write sequence is written, the device automatically outputs status register data when read (see Figure 8). The CPU can detect the completion of the word/byte write event by analyzing the RY/BY# pin or status register bit SR.7.

When word/byte write is complete, status register bit SR.4 should be checked. If word/byte write error is detected, the status register should be cleared. The internal WSM verify only detects errors for "1"s that do not successfully write to "0"s. The CUI remains in read status register mode until it receives another command.

Reliable word/byte writes can only occur when V_{CC}=2.7V-3.6V and V_{CCW}=$V_{CCWH1/2}$. In the absence of this high voltage, memory contents are protected against word/byte writes. If word/byte write is attempted while $V_{CCW} \leq V_{CCWLK}$, status register bits SR.3 and SR.4 will be set to "1". Successful word/byte write requires for boot blocks that WP# is V_{IH} and the corresponding block lock-bit be cleared. In parameter and main blocks case, it must be cleared the corresponding block lock-bit. If word/byte write is attempted when the excepting above conditions, SR.1 and SR.4 will be set to "1".

4.8 Block Erase Suspend Command

The Block Erase Suspend command allows block-erase interruption to read or word/byte write data in another block of memory. Once the block erase process starts, writing the Block Erase Suspend command requests that the WSM suspend the block erase sequence at a predetermined point in the algorithm. The device outputs status register data when read after the Block Erase Suspend command is written. Polling status register bits SR.7 and SR.6 can determine when the block erase operation has been suspended (both will be set to "1"). RY/BY# will also transition to High Z. Specification t_{WHRZ2} defines the block erase suspend latency.

When Block Erase Suspend command write to the CUI, if block erase was finished, the device places read array mode. Therefore, after Block Erase Suspend command write to the CUI, Read Status Register command (70H) has to write to CUI, then status register bit SR.6 should be checked for places the device in suspend mode.

At this point, a Read Array command can be written to read data from blocks other than that which is suspended. A Word/Byte Write command sequence can also be issued during erase suspend to program data in other blocks. Using the Word/Byte Write Suspend command (see Section 4.9), a word/byte write operation can also be suspended. During a word/byte write operation with block erase suspended, status register bit SR.7 will return to "0" and the RY/BY# output will transition to V_{OL}. However, SR.6 will remain "1" to indicate block erase suspend status.

The only other valid commands while block erase is suspended are Read Status Register and Block Erase Resume. After a Block Erase Resume command is written to the flash memory, the WSM will continue the block erase process. Status register bits SR.6 and SR.7 will automatically clear and RY/BY# will return to V_{OL}. After the Erase Resume command is written, the device automatically outputs status register data when read (see Figure 9). V_{CCW} must remain at $V_{CCWH1/2}$ (the same V_{CCW} level used for block erase) while block erase is suspended. RP# must also remain at V_{IH}. WP# must also remain at V_{IL} or V_{IH} (the same WP# level used for block erase). Block erase cannot resume until word/byte write operations initiated during block erase suspend have completed.

If the time between writing the Block Erase Resume command and writing the Block Erase Suspend command is shorter than t_{ERES} and both commands are written repeatedly, a longer time is required than standard block erase until the completion of the operation.

4.9 Word/Byte Write Suspend Command

The Word/Byte Write Suspend command allows word/byte write interruption to read data in other flash memory locations. Once the word/byte write process starts, writing the Word/Byte Write Suspend command requests that the WSM suspend the Word/Byte write sequence at a predetermined point in the algorithm. The device continues to output status register data when read after the Word/Byte Write Suspend command is written. Polling status register bits SR.7 and SR.2 can determine when the word/byte write operation has been suspended (both will be set to "1"). RY/BY# will also transition to High Z. Specification t_{WHRZ1} defines the word/byte write suspend latency.

When Word/Byte Write Suspend command write to the CUI, if word/byte write was finished, the device places read array mode. Therefore, after Word/Byte Write Suspend command write to the CUI, Read Status Register command (70H) has to write to CUI, then status register bit SR.2 should be checked for places the device in suspend mode.

At this point, a Read Array command can be written to read data from locations other than that which is suspended. The only other valid commands while word/byte write is suspended are Read Status Register and Word/Byte Write Resume. After Word/Byte Write Resume command is written to the flash memory, the WSM will continue the word/byte write process. Status register bits SR.2 and SR.7 will automatically clear and RY/BY# will return to V_{OL}. After the Word/Byte Write Resume command is written, the device automatically outputs status register data when read (see Figure 10). V_{CCW} must remain at $V_{CCWH1/2}$ (the same V_{CCW} level used for word/byte write) while in word/byte write suspend mode. RP# must also remain at V_{IH}. WP# must also remain at V_{IL} or V_{IH} (the same WP# level used for word/byte write).

If the time between writing the Word/Byte Write Resume command and writing the Word/Byte Write Suspend command is short and both commands are written repeatedly, a longer time is required than standard word/byte write until the completion of the operation.

4.10 Set Block and Permanent Lock-Bit Commands

A flexible block locking and unlocking scheme is enabled via a combination of block lock-bits, a permanent lock-bit and WP# pin. The block lock-bits and WP# pin gates program and erase operations while the permanent lock-bit gates block-lock bit modification. With the permanent lock-bit not set, individual block lock-bits can be set using the Set Block Lock-Bit command. The Set Permanent Lock-Bit command, sets the permanent lock-bit. After the permanent lock-bit is set, block lock-bits and locked block contents cannot altered. See Table 5 for a summary of hardware and software write protection options.

Set block lock-bit and permanent lock-bit are executed by a two-cycle command sequence. The set block or permanent lock-bit setup along with appropriate block or device address is written followed by either the set block lock-bit confirm (and an address within the block to be locked) or the set permanent lock-bit confirm (and any device address). The WSM then controls the set lock-bit algorithm. After the sequence is written, the device automatically outputs status register data when read (see Figure 11). The CPU can detect the completion of the set lock-bit event by analyzing the RY/BY# pin output or status register bit SR.7.

When the set lock-bit operation is complete, status register bit SR.4 should be checked. If an error is detected, the status register should be cleared. The CUI will remain in read status register mode until a new command is issued.

This two-step sequence of set-up followed by execution ensures that lock-bits are not accidentally set. An invalid Set Block or Permanent Lock-Bit command will result in status register bits SR.4 and SR.5 being set to "1". Also, reliable operations occur only when V_{CC}=2.7V-3.6V and V_{CCW}=$V_{CCWH1/2}$. In the absence of this high voltage, lock-bit contents are protected against alteration.

A successful set block lock-bit operation requires that the permanent lock-bit be cleared. If it is attempted with the permanent lock-bit set, SR.1 and SR.4 will be set to "1" and the operation will fail.

4.11 Clear Block Lock-Bits Command

All set block lock-bits are cleared in parallel via the Clear Block Lock-Bits command. With the permanent lock-bit not set, block lock-bits can be cleared using only the Clear Block Lock-Bits command. If the permanent lock-bit is set, block lock-bits cannot cleared. See Table 5 for a summary of hardware and software write protection options.

Clear block lock-bits operation is executed by a two-cycle command sequence. A clear block lock-bits setup is first written. After the command is written, the device automatically outputs status register data when read (see Figure 12). The CPU can detect completion of the clear block lock-bits event by analyzing the RY/BY# Pin output or status register bit SR.7.

When the operation is complete, status register bit SR.5 should be checked. If a clear block lock-bit error is detected, the status register should be cleared. The CUI will remain in read status register mode until another command is issued.

This two-step sequence of set-up followed by execution ensures that block lock-bits are not accidentally cleared. An invalid Clear Block Lock-Bits command sequence will result in status register bits SR.4 and SR.5 being set to "1". Also, a reliable clear block lock-bits operation can only occur when V_{CC}=2.7V-3.6V and V_{CCW}=$V_{CCWH1/2}$. If a clear block lock-bits operation is attempted while V_{CCW}≤V_{CCWLK}, SR.3 and SR.5 will be set to "1". In the absence of this high voltage, the block lock-bits content are protected against alteration. A successful clear block lock-bits operation requires that the permanent lock-bit is not set. If it is attempted with the permanent lock-bit set, SR.1 and SR.5 will be set to "1" and the operation will fail.

If a clear block lock-bits operation is aborted due to V_{CCW} or V_{CC} transitioning out of valid range or RP# active transition, block lock-bit values are left in an undetermined state. A repeat of clear block lock-bits is required to initialize block lock-bit contents to known values. Once the permanent lock-bit is set, it cannot be cleared.

4.12 OTP Program Command

OTP program is executed by a two-cycle command sequence. OTP program command(C0H) is written, followed by a second write cycle that specifies the address and data (latched on the rising edge of WE#). The WSM then takes over, controlling the OTP program and program verify algorithms internally. After the OTP program command sequence is completed, the device automatically outputs status register data when read (see Figure 13). The CPU can detect the completion of the OTP program by analyzing the output data of the RY/BY# pin or status register bit SR.7.

When OTP program is completed, status register bit SR.4 should be checked. If OTP program error is detected, the status register should be cleared. The internal WSM verify only detects errors for "1"s that do not successfully program to "0"s. The CUI remains in read status register mode until it receives other commands.

Reliable OTP program can be executed only when V_{CC}=2.7V-3.6V and V_{CCW}=$V_{CCWH1/2}$. In the absence of this voltage, memory contents are protected against OTP programs. If OTP program is attempted while $V_{CCW} \leq V_{CCWLK}$, status register bits SR.3 and SR.4 is set to "1". If OTP write is attempted when the OTP Lock-bit is set, SR.1 and SR.4 is set to "1".

4.13 Block Locking by the WP#

This Boot Block Flash memory architecture features two hardware-lockable boot blocks so that the kernel code for the system can be kept secure while other blocks are programmed or erased as necessary.

The lockable two boot blocks are locked when WP#=V_{IL}; any program or erase operation to a locked block will result in an error, which will be reflected in the status register. For top configuration, the top two boot blocks are lockable. For the bottom configuration, the bottom two boot blocks are lockable. If WP# is V_{IH} and block lock-bit is not set, boot block can be programmed or erased normally (Unless V_{CCW} is below V_{CCWLK}). WP# is valid only two boot blocks, other blocks are not affected.

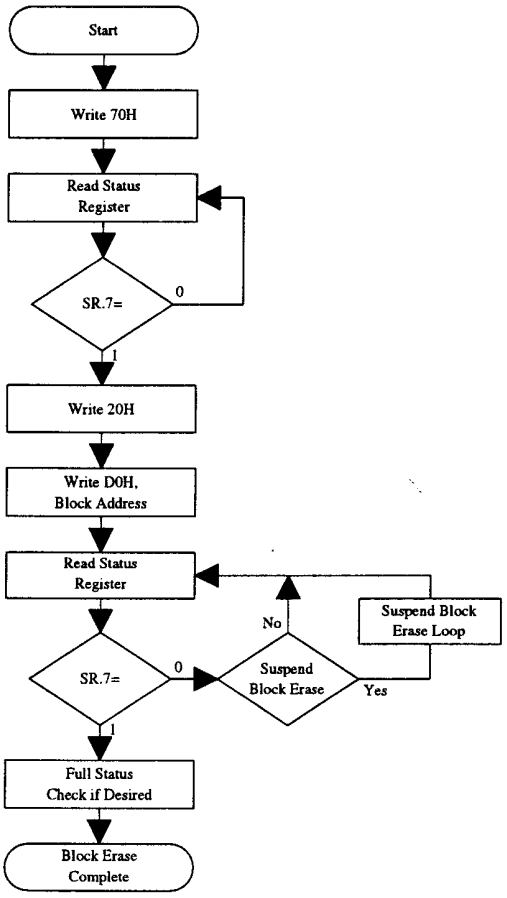
Table 5. Write Protection Alternatives

Operation	V_{CCW}	RP#	Permanent Lock-Bit	Block Lock-bit	WP#	Effect
Block Erase or Word/Byte Write	$\leq V_{CCWLK}$	X	X	X	X	All Blocks Locked.
	$>V_{CCWLK}$	V_{IL}	X	X	X	All Blocks Locked.
		V_{IH}	X	0	V_{IL}	2 Boot Blocks Locked.
					V_{IH}	Block Erase and Word/Byte Write Enabled.
				1	V_{IL}	Block Erase and Word/Byte Write Disabled.
					V_{IH}	Block Erase and Word/Byte Write Disabled.
Full Chip Erase	$\leq V_{CCWLK}$	X	X	X	X	All Blocks Locked.
	$>V_{CCWLK}$	V_{IL}	X	X	X	All Blocks Locked.
		V_{IH}	X	X	V_{IL}	All Unlocked Blocks are Erased. 2 Boot Blocks and Locked Blocks are NOT Erased.
					V_{IH}	All Unlocked Blocks are Erased, Locked Blocks are NOT Erased.
Set Block Lock-Bit	$\leq V_{CCWLK}$	X	X	X	X	Set Block Lock-Bit Disabled.
	$>V_{CCWLK}$	V_{IL}	X	X	X	Set Block Lock-Bit Disabled.
		V_{IH}	0	X	X	Set Block Lock-Bit Enabled.
			1	X	X	Set Block Lock-Bit Disabled.
Clear Block Lock-Bits	$\leq V_{CCWLK}$	X	X	X	X	Clear Block Lock-Bits Disabled.
	$>V_{CCWLK}$	V_{IL}	X	X	X	Clear Block Lock-Bits Disabled.
		V_{IH}	0	X	X	Clear Block Lock-Bits Enabled.
			1	X	X	Clear Block Lock-Bits Disabled.
Set Permanent Lock-Bit	$\leq V_{CCWLK}$	X	X	X	X	Set Permanent Lock-Bit Disabled.
	$>V_{CCWLK}$	V_{IL}	X	X	X	Set Permanent Lock-Bit Disabled.
		V_{IH}	X	X	X	Set Permanent Lock-Bit Enabled.

Table 6. Status Register Definition

WSMS	BESS	ECBLBS	WBWSLBS	VCCWS	WBWSS	DPS	R
7	6	5	4	3	2	1	0

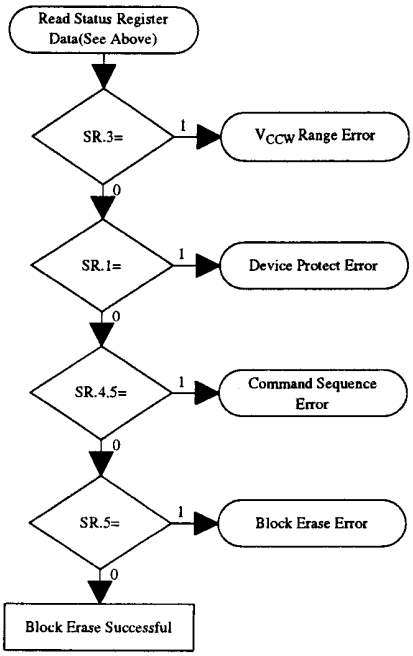
	NOTES:
SR.7 = WRITE STATE MACHINE STATUS (WSMS) 1 = Ready 0 = Busy	Check RY/BY# or SR.7 to determine block erase, full chip erase, word/byte write or lock-bit configuration completion. SR.6-0 are invalid while SR.7="0".
SR.6 = BLOCK ERASE SUSPEND STATUS (BESS) 1 = Block Erase Suspended 0 = Block Erase in Progress/Completed	
SR.5 = ERASE AND CLEAR BLOCK LOCK-BITS STATUS (ECBLBS) 1 = Error in Block Erase, Full Chip Erase or Clear Block Lock-Bits 0 = Successful Block Erase, Full Chip Erase or Clear Block Lock-Bits	If both SR.5 and SR.4 are "1"s after a block erase, full chip erase or lock-bit configuration attempt, an improper command sequence was entered.
SR.4 = WORD/BYTE WRITE AND SET LOCK-BIT STATUS (WBWSLBS) 1 = Error in Word/Byte Write or Set Block/Permanent Lock-Bit 0 = Successful Word/Byte Write or Set Block/Permanent Lock-Bit	SR.3 does not provide a continuous indication of V_{CCW} level. The WSM interrogates and indicates the V_{CCW} level only after Block Erase, Full Chip Erase, Word/Byte Write or Lock-Bit Configuration command sequences. SR.3 is not guaranteed to reports accurate feedback only when $V_{CCW} \neq V_{CCWH1/2}$.
SR.3 = V_{CCW} STATUS (VCCWS) 1 = V_{CCW} Low Detect, Operation Abort 0 = V_{CCW} OK	
SR.2 = WORD/BYTE WRITE SUSPEND STATUS (WBWSS) 1 = Word/Byte Write Suspended 0 = Word/Byte Write in Progress/Completed	SR.1 does not provide a continuous indication of permanent and block lock-bit and WP# values. The WSM interrogates the permanent lock-bit, block lock-bit and WP# only after Block Erase, Full Chip Erase, Word/Byte Write or Lock-Bit Configuration command sequences. It informs the system, depending on the attempted operation, if the block lock-bit is set, permanent lock-bit is set and/or WP# is V_{IL}. Reading the block lock and permanent lock configuration codes after writing the Read Identifier Codes command indicates permanent and block lock-bit status.
SR.1 = DEVICE PROTECT STATUS (DPS) 1 = Block Lock-Bit, Permanent Lock-Bit and/or WP# Lock Detected, Operation Abort 0 = Unlock	
SR.0 = RESERVED FOR FUTURE ENHANCEMENTS (R)	SR.0 is reserved for future use and should be masked out when polling the status register.



Bus Operation	Command	Comments
Write	Read Status Register	Data=70H Addr=X
Read		Status Register Data
Standby		Check SR.7 1=WSM Ready 0=WSM Busy
Write	Erase Setup	Data=20H Addr=X
Write	Erase Confirm	Data=D0H Addr=Within Block to be Erased
Read		Status Register Data
Standby		Check SR.7 1=WSM Ready 0=WSM Busy

Repeat for subsequent block erasures.
Full status check can be done after each block erase or after a sequence of block erasures.
Write FFH after the last operation to place device in read array mode.

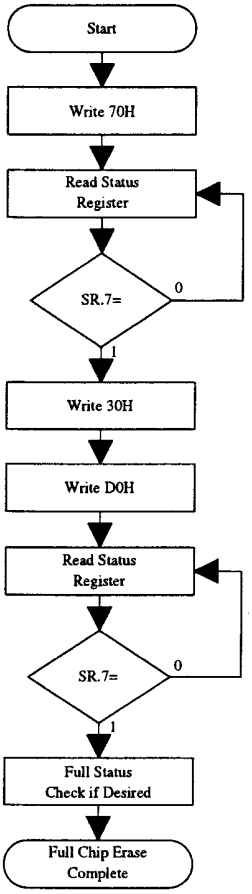
FULL STATUS CHECK PROCEDURE



Bus Operation	Command	Comments
Standby		Check SR.3 1=V_{CCW} Error Detect
Standby		Check SR.1 1=Device Protect Detect
Standby		Check SR.4,5 Both 1=Command Sequence Error
Standby		Check SR.5 1=Block Erase Error

SR.5, SR.4, SR.3 and SR.1 are only cleared by the Clear Status Register Command in cases where multiple blocks are erased before full status is checked.
If error is detected, clear the Status Register before attempting retry or other error recovery.

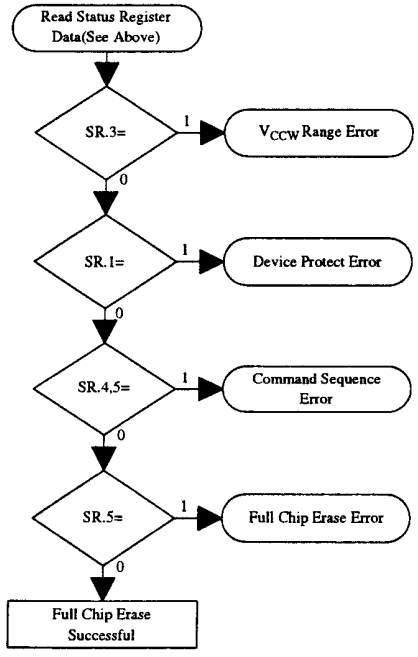
Figure 6. Automated Block Erase Flowchart



Bus Operation	Command	Comments
Write	Read Status Register	Data=70H Addr=X
Read		Status Register Data
Standby		Check SR.7 1=WSM Ready 0=WSM Busy
Write	Full Chip Erase Setup	Data=30H Addr=X
Write	Full Chip Erase Confirm	Data=D0H Addr=X
Read		Status Register Data
Standby		Check SR.7 1=WSM Ready 0=WSM Busy

Full status check can be done after each full chip erase.
Write FFH after the last operation to place device in read array mode.

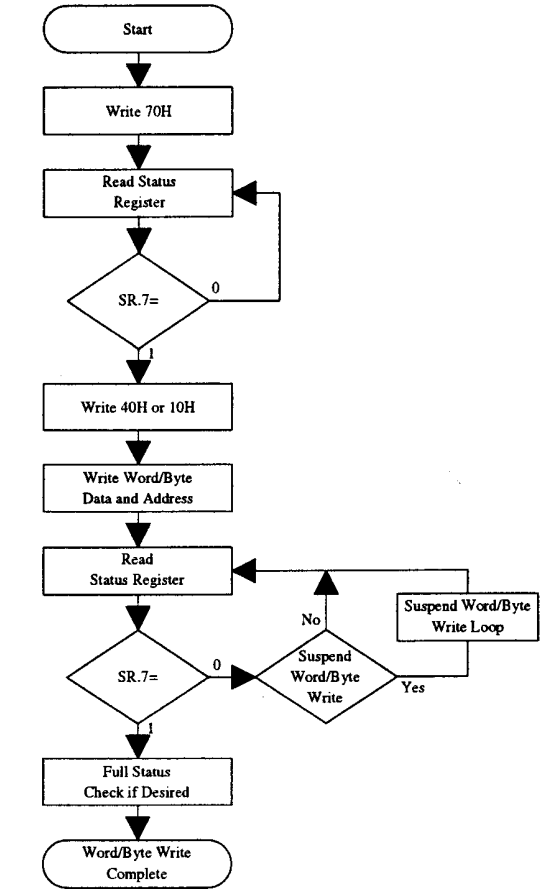
FULL STATUS CHECK PROCEDURE



Bus Operation	Command	Comments
Standby		Check SR.3 1=V_{CCW} Error Detect
Standby		Check SR.1 1=Device Protect Detect (All Blocks are locked)
Standby		Check SR.4,5 Both 1=Command Sequence Error
Standby		Check SR.5 1=Full Chip Erase Error

SR.5, SR.4, SR.3 and SR.1 are only cleared by the Clear Status Register Command in cases where multiple blocks are erased before full status is checked.
If error is detected, clear the Status Register before attempting retry or other error recovery.

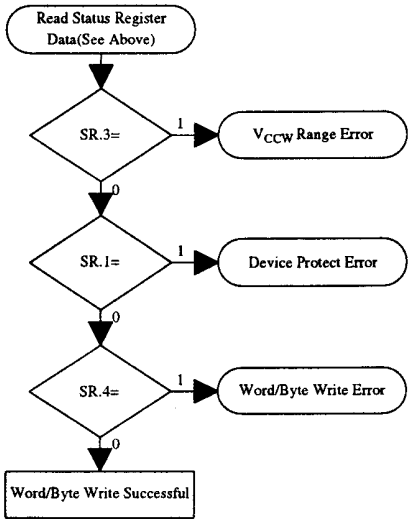
Figure 7. Automated Full Chip Erase Flowchart



Bus Operation	Command	Comments
Write	Read Status Register	Data=70H Addr=X
Read		Status Register Data
Standby		Check SR.7 1=WSM Ready 0=WSM Busy
Write	Setup Word/Byte Write	Data=40H or 10H Addr=X
Write	Word/Byte Write	Data=Data to Be Written Addr=Location to Be Written
Read		Status Register Data
Standby		Check SR.7 1=WSM Ready 0=WSM Busy

Repeat for subsequent word/byte writes.
SR full status check can be done after each word/byte write, or after a sequence of word/byte writes.
Write FFH after the last word/byte write operation to place device in read array mode.

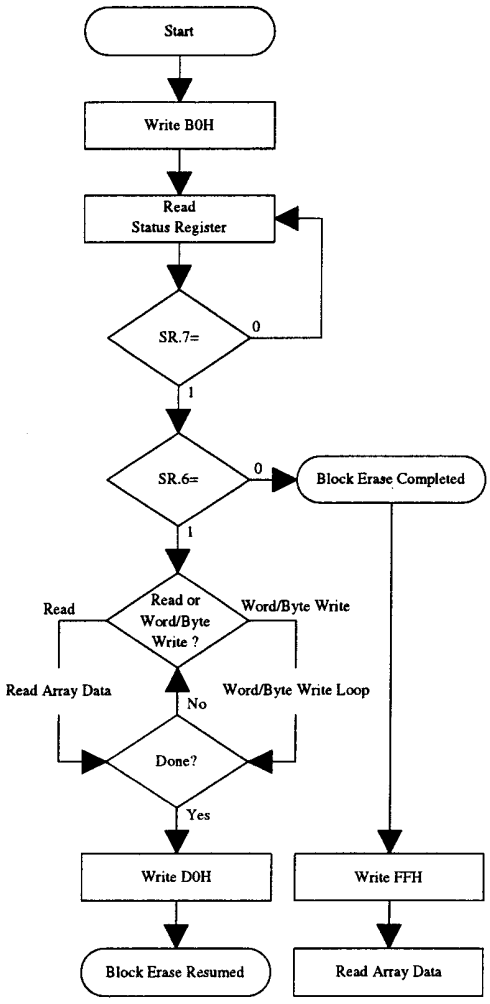
FULL STATUS CHECK PROCEDURE



Bus Operation	Command	Comments
Standby		Check SR.3 1=V_{CCW} Error Detect
Standby		Check SR.1 1=Device Protect Detect
Standby		Check SR.4 1=Data Write Error

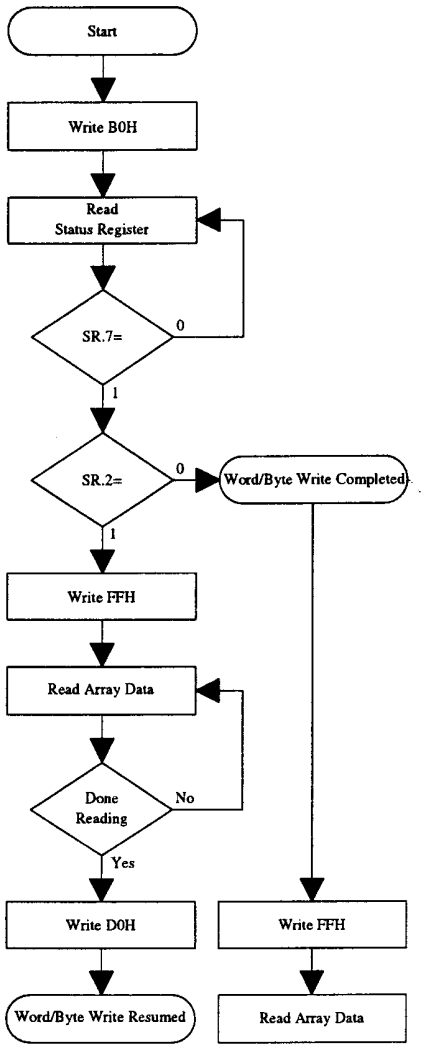
SR.4, SR.3 and SR.1 are only cleared by the Clear Status Register command in cases where multiple locations are written before full status is checked.
If error is detected, clear the Status Register before attempting retry or other error recovery.

Figure 8. Automated Word/Byte Write Flowchart



Bus Operation	Command	Comments
Write	Erase Suspend	Data=B0H Addr=X
Read		Status Register Data Addr=X
Standby		Check SR.7 1=WSM Ready 0=WSM Busy
Standby		Check SR.6 1=Block Erase Suspended 0=Block Erase Completed
Write	Erase Resume	Data=D0H Addr=X

Figure 9. Block Erase Suspend/Resume Flowchart



Bus Operation	Command	Comments
Write	Word/Byte Write Suspend	Data=B0H Addr=X
Read		Status Register Data Addr=X
Standby		Check SR.7 1=WSM Ready 0=WSM Busy
Standby		Check SR.2 1=Word/Byte Write Suspended 0=Word/Byte Write Completed
Write	Read Array	Data=FFH Addr=X
Read		Read Array locations other than that being written.
Write	Word/Byte Write Resume	Data=D0H Addr=X

Figure 10. Word/Byte Write Suspend/Resume Flowchart