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LH5116/H

CMOS 16K (2K × 8) Static RAM

FEATURES

- 2,048 × 8 bit organization
- Access time: 100 ns (MAX.)
- Power consumption:
 - Operating: 220 mW (MAX.)
 - Standby: 5.5 μW (MAX.)
- Single +5 V power supply
- Fully-static operation
- TTL compatible I/O
- Three-state outputs
- Wide temperature range available
LH5116H: -40 to +85°C
- Packages:
 - 24-pin, 600-mil DIP
 - 24-pin, 300-mil SK-DIP
 - 24-pin, 450-mil SOP

DESCRIPTION

The LH5116/H are static RAMs organized as 2,048 × 8 bits. It is fabricated using silicon-gate CMOS process technology. It features high speed access in read mode using output enable (t_{OE}).

PIN CONNECTIONS

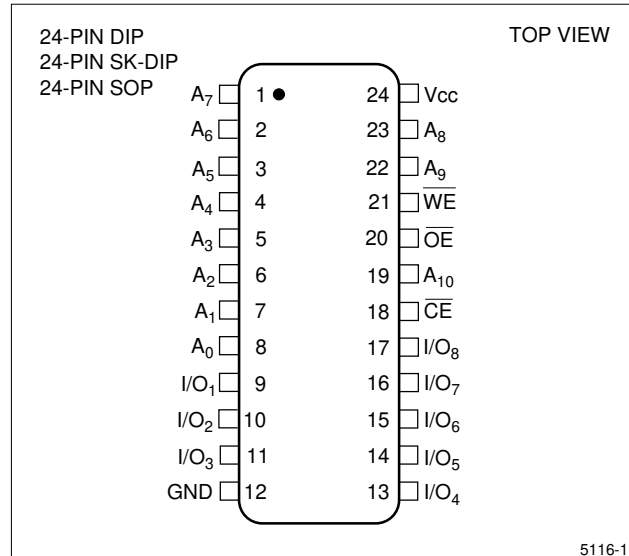


Figure 1. Pin Connections for DIP, SK-DIP, and SOP Packages

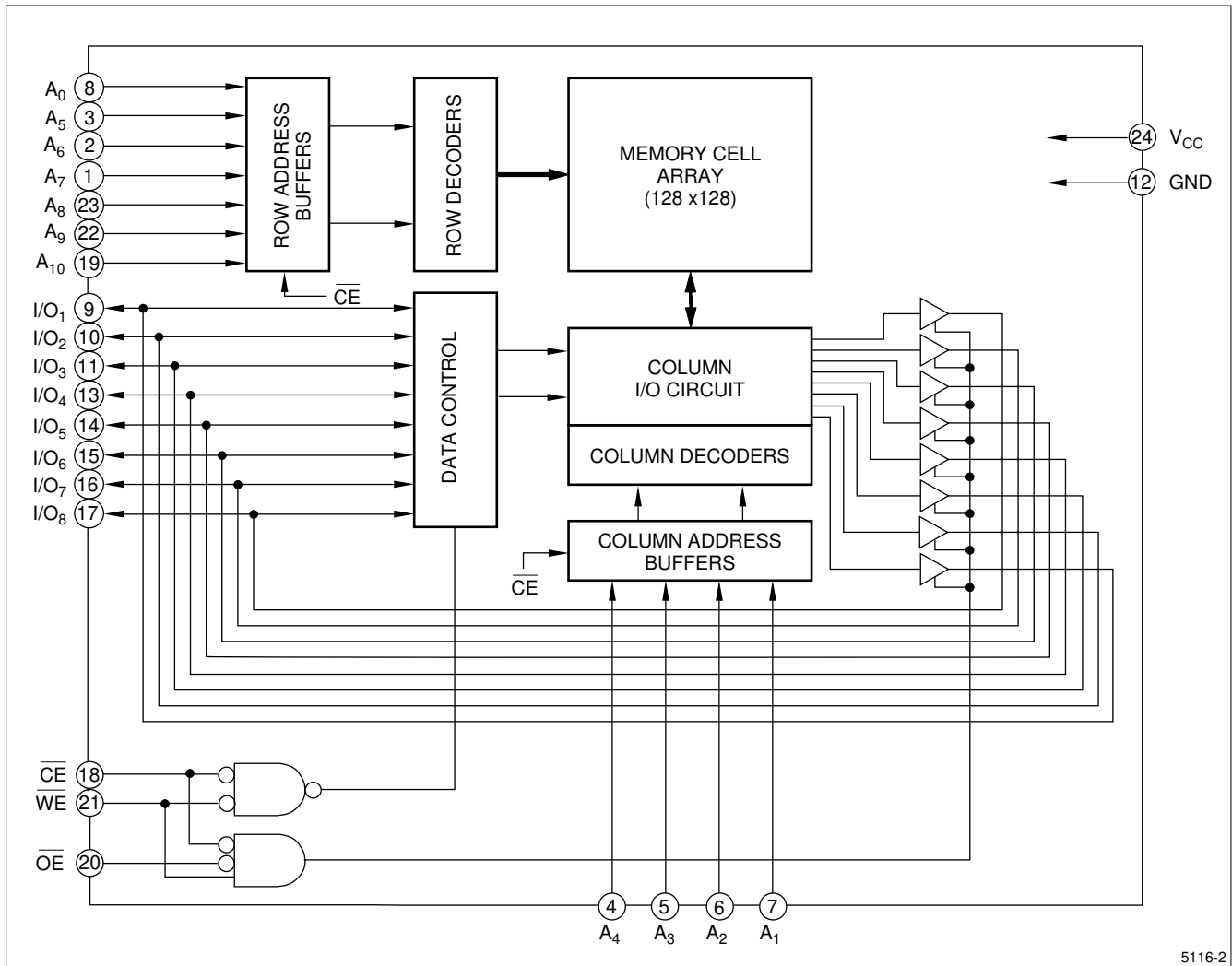


Figure 2. LH5116/H Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME
A ₀ - A ₁₀	Address input
CE	Chip Enable input
OE	Output Enable input
WE	Write Enable input

SIGNAL	PIN NAME
I/O ₁ - I/O ₈	Data input/output
V _{CC}	Power supply
GND	Ground

TRUTH TABLE

CE	OE	WE	MODE	I/O ₁ - I/O ₈	SUPPLY CURRENT	NOTE
L	X	L	Write	D _{IN}	Operating (I _{CC})	1
L	L	H	Read	D _{OUT}	Operating (I _{CC})	
H	X	X	Deselect	High-Z	Standby (I _{SB})	1
L	H	X	Outputs disable	High-Z	Operating (I _{CC})	1

NOTE:
1. X = H or L

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT	NOTE
Supply voltage	V _{CC}	-0.3 to +7.0	V	1
Input voltage	V _{IN}	-0.3 to V _{CC} + 0.3	V	1
Operating temperature	T _{opr}	0 to +70	°C	2
		-40 to +85		3
Storage temperature	T _{stg}	-55 to +150	°C	

NOTES:

1. The maximum applicable voltage on any pin with respect to GND.
2. Applied to the LH5116/D/NA
3. Applied to the LH5116H/HD/HN

RECOMMENDED OPERATING CONDITIONS ¹

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V _{CC}	4.5	5.0	5.5	V
Input voltage	V _{IH}	2.2		V _{CC} + 0.3	V
	V _{IL}	-0.3		0.8	V

NOTE:

1. T_A = 0 to 70°C (LH5116/D/NA), T_A = -40 to +85°C (LH5116H/HD/HN)

DC CHARACTERISTICS ¹ (V_{CC} = 5 V ±10%)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Output 'LOW' voltage	V _{OL}	I _{OL} = 2.1 mA			0.4	V	
Output 'HIGH' voltage	V _{OH}	I _{OH} = -1.0 mA	2.4			V	
Input leakage current	I _{LI}	V _{IN} = 0 V to V _{CC}	-1.0		1.0	μA	
Output leakage current	I _{LO}	CE = V _{IH} , V _{I/O} = 0 V to V _{CC}	-1.0		1.0	μA	
Operating current	I _{CC1}	Outputs open (OE = V _{CC})		25	30	mA	2
	I _{CC2}	Outputs open (OE = V _{IH})		30	40	mA	3
Standby current	I _{SB}	CE ≥ V _{CC} - 0.2 V All other input pins = 0 V to V _{CC}			1.0	μA	4
					0.2		

NOTES:

1. T_A = 0 to 70°C (LH5116/D/NA), T_A = -40 to +85°C (LH5116H/HD/HN)
2. CE = 0 V; all other input pins = 0 V to V_{CC}
3. CE = V_{IL}; all other input pins = V_{IL} to V_{IH}
4. T_A = 25°C

AC CHARACTERISTICS ¹**(1) READ CYCLE (V_{CC} = 5 V ±10%)**

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
Read cycle time	t _{RC}	100			ns	
Address access time	t _{AA}			100	ns	
Chip enable access time	t _{ACE}			100	ns	
Chip enable Low to output in Low-Z	t _{CLZ}	10			ns	2
Output enable access time	t _{OE}			40	ns	
Output enable Low to output in Low-Z	t _{OLZ}	10			ns	2
Chip disable to output in High-Z	t _{CHZ}	0		40	ns	2
Output disable to output in High-Z	t _{OHZ}	0		40	ns	2
Output hold time	t _{OH}	10			ns	

NOTES:

1. T_A = 0 to 70°C (LH5116/NA/D), T_A = -40 to 85°C (LH5116H/HD/HN).
2. Active output to high-impedance and high-impedance to output active tests specified for a ±200 mV transition from steady state levels into the test load.

(2) WRITE CYCLE ¹ ($V_{CC} = 5\text{ V} \pm 10\%$)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
Write cycle time	t_{WC}	100			ns	
Chip enable to end of write	t_{CW}	80			ns	
Address valid time	t_{AW}	80			ns	
Address setup time	t_{AS}	0			ns	
Write pulse width	t_{WP}	60			ns	
Write recovery time	t_{WR}	10			ns	
Output active from end of write	t_{OW}	10			ns	2
WE Low to output in High-Z	t_{WHZ}	0		30	ns	2
Data valid to end of write	t_{DW}	30			ns	
Data hold time	t_{DH}	10			ns	
Output enable to output in High-Z	t_{OHZ}	0		40	ns	2
Output active from end of write	t_{OW}	10			ns	2

NOTES:

- $T_A = 0$ to $+70^\circ\text{C}$ (LH5116/D/NA), $T_A = -40$ to $+85^\circ\text{C}$ (LH5116H/HD/HN)
- Active output to high-impedance and high-impedance to output active tests specified for a ± 200 mV transition from steady state levels into the test load.

AC TEST CONDITIONS

PARAMETER	MODE	NOTE
Input voltage amplitude	0.8 V to 2.2 V	
Input rise/fall time	10 ns	
Timing reference level	1.5 V	
Output load condition	1TTL + C_L (100 pF)	1

NOTE:

- Includes scope and jig capacitance.

DATA RETENTION CHARACTERISTICS ¹

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Data retention voltage	V_{CCDR}	$CE \geq V_{CCRC} - 0.2\text{ V}$	2.0		5.5	V	
Data retention current	I_{CCDR}	$CE \geq V_{CCDR} - 0.2\text{ V}$, $V_{CCDR} = 2.0\text{ V}$			1.0 0.2	μA	2
Chip disable to data retention	t_{CDR}		0			ns	
Recovery time	t_R		t_{RC}			ns	3

NOTES:

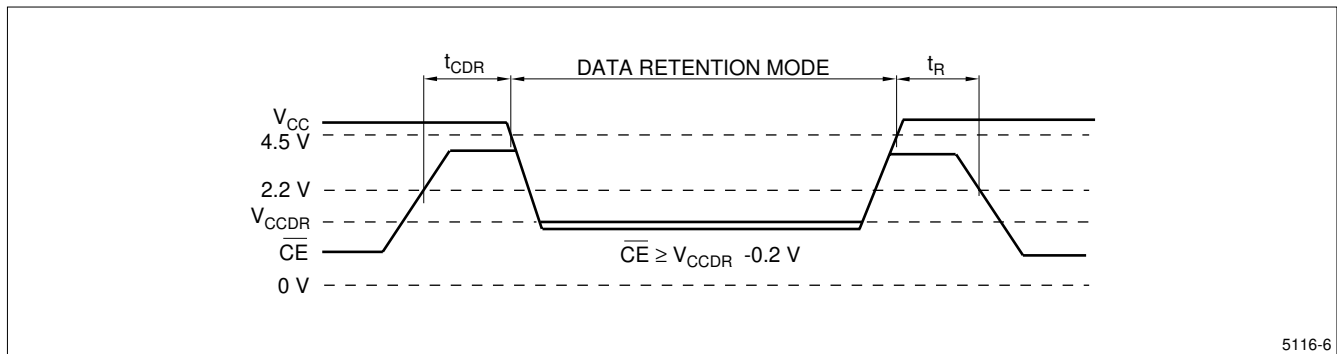
- $T_A = 0$ to $+70^\circ\text{C}$ (LH5116/D/NA), $T_A = -40$ to $+85^\circ\text{C}$ (LH5116H/HD/HN)
- $T_A = 25^\circ\text{C}$
- t_{RC} = Read cycle time

CAPACITANCE ¹ ($f = 1\text{ MHz}$, $T_A = 25^\circ\text{C}$)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input capacitance	C_{IN}	$V_{IN} = 0\text{ V}$			7	pF
Input/output capacitance	$C_{I/O}$	$V_{I/O} = 0\text{ V}$			10	pF

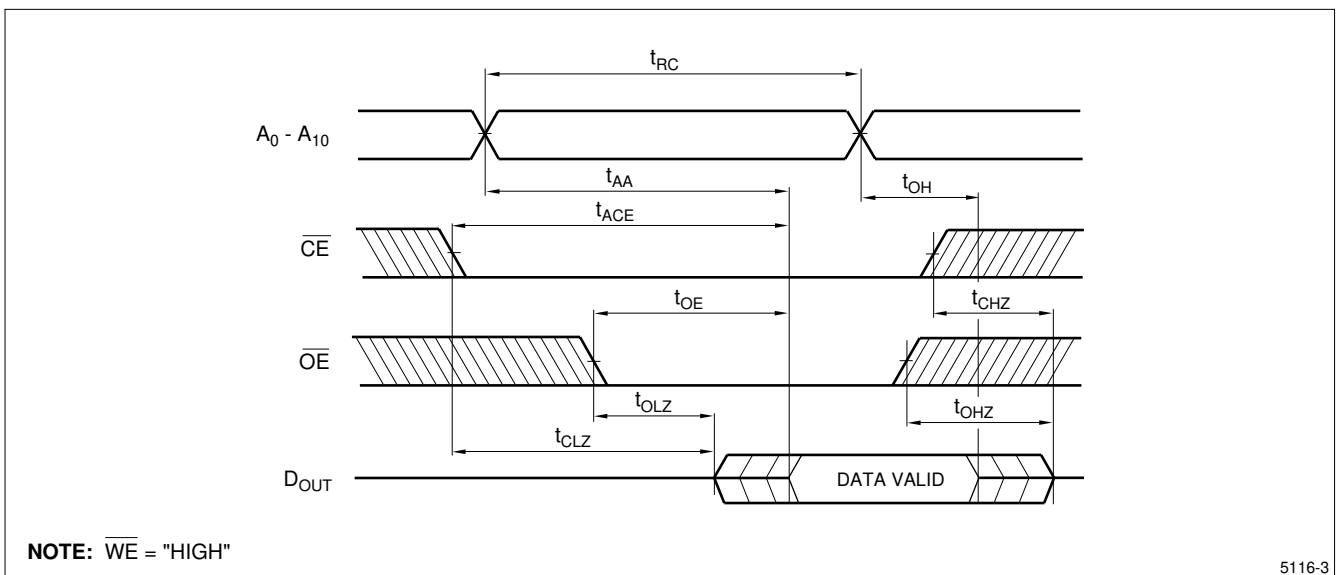
NOTE:

- This parameter is sampled and not production tested.



5116-6

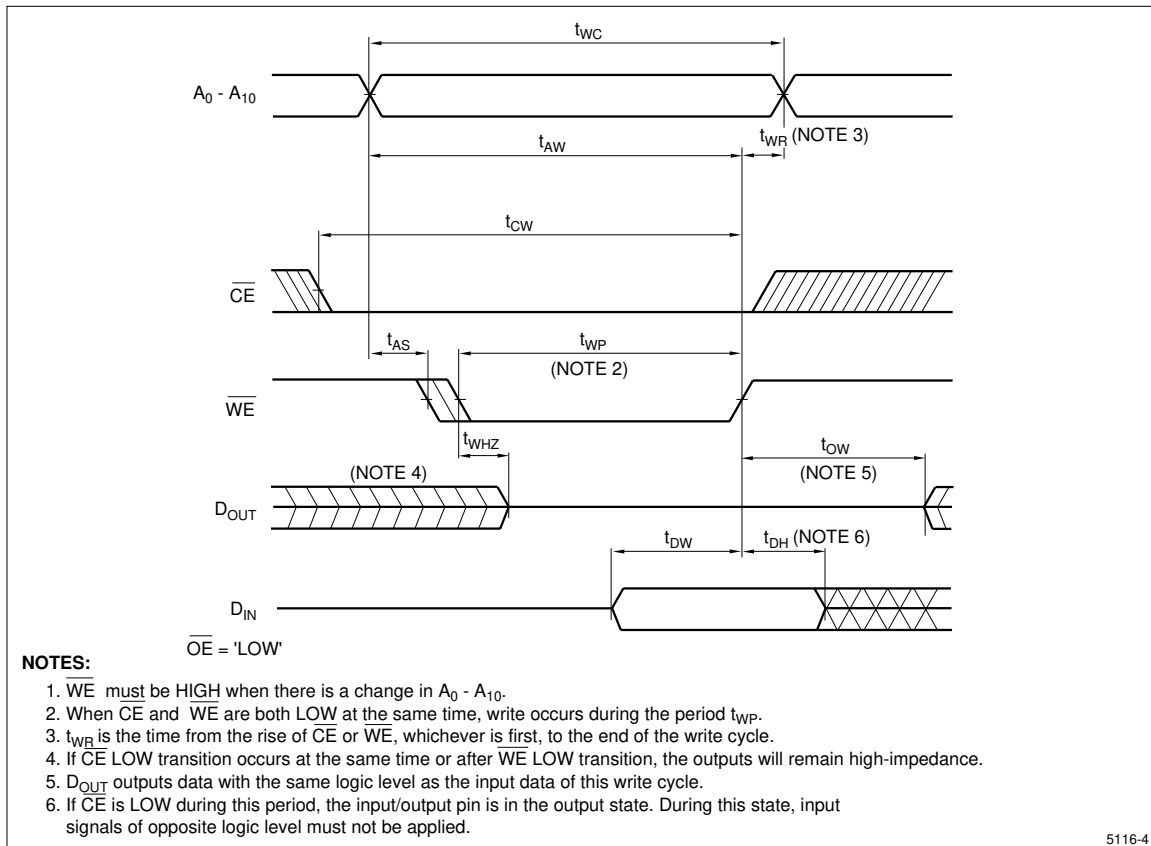
Figure 3. Low Voltage Data Retention



NOTE: \overline{WE} = "HIGH"

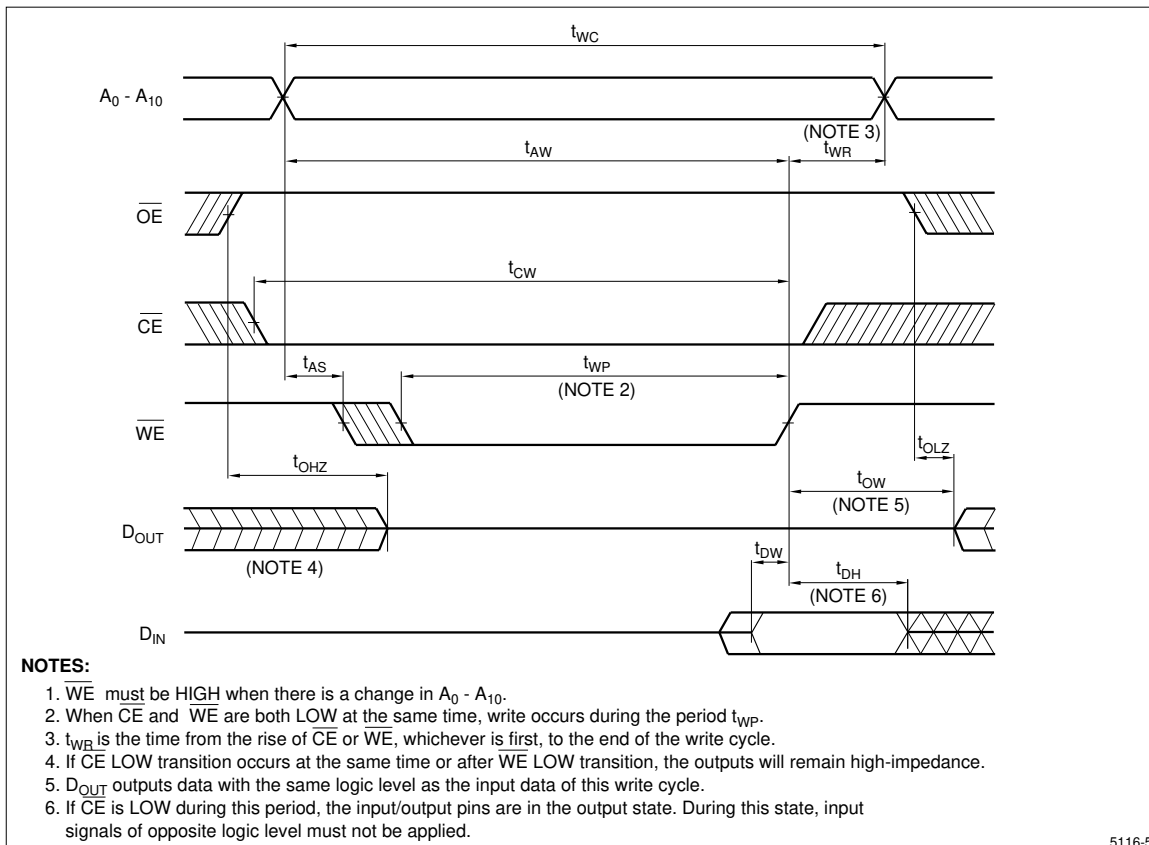
5116-3

Figure 4. Read Cycle



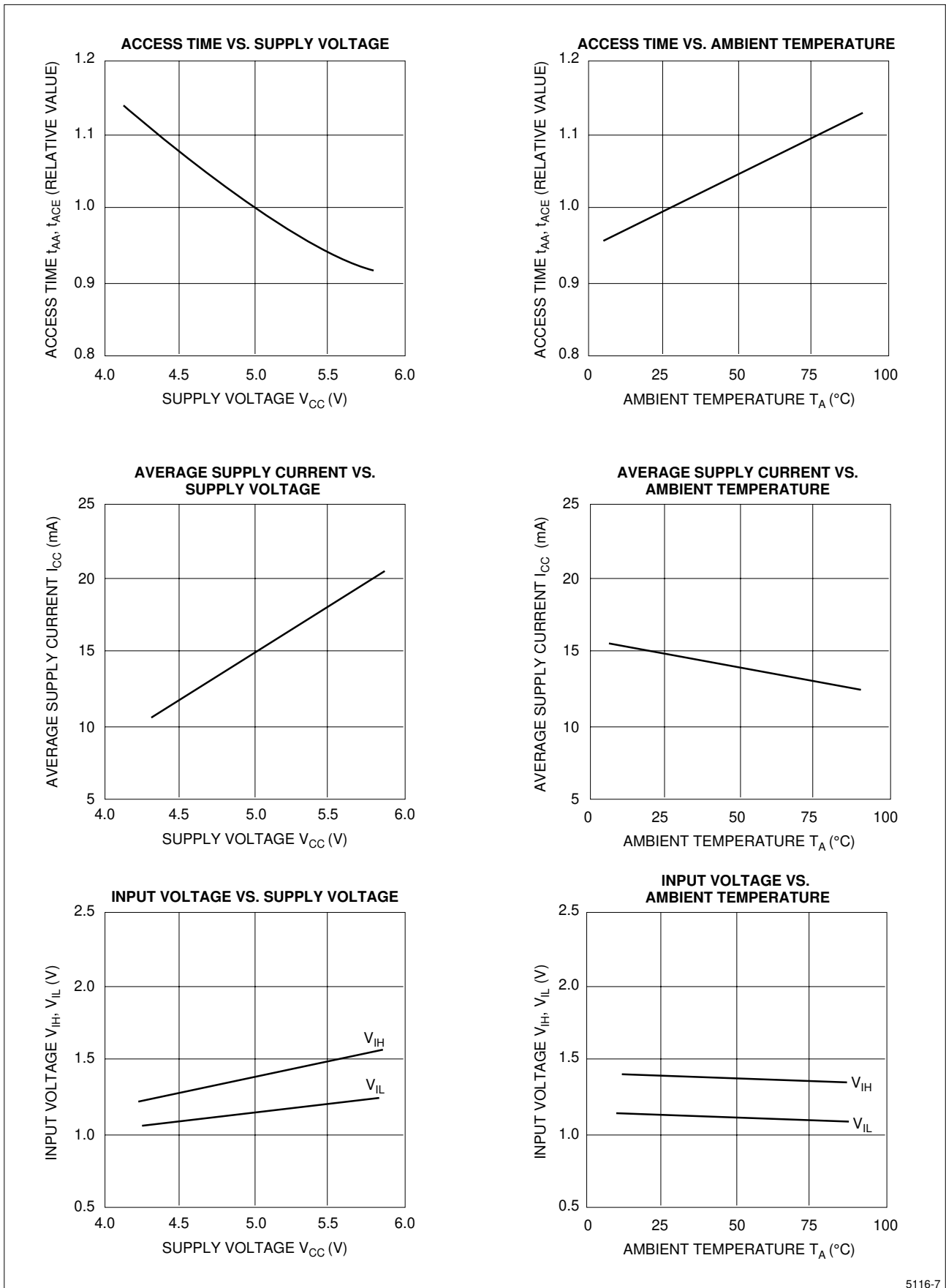
5116-4

Figure 5. Write Cycle 1



5116-5

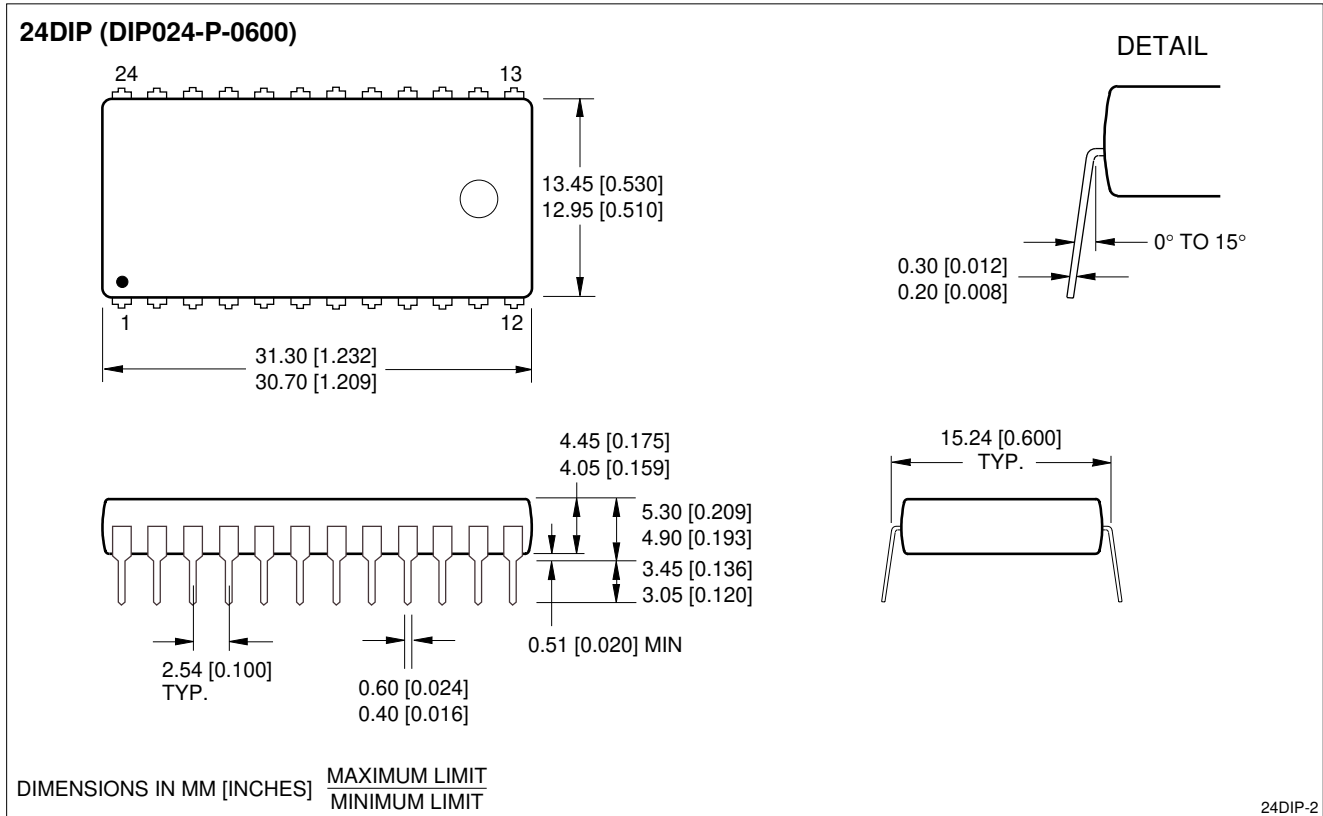
Figure 6. Write Cycle 2



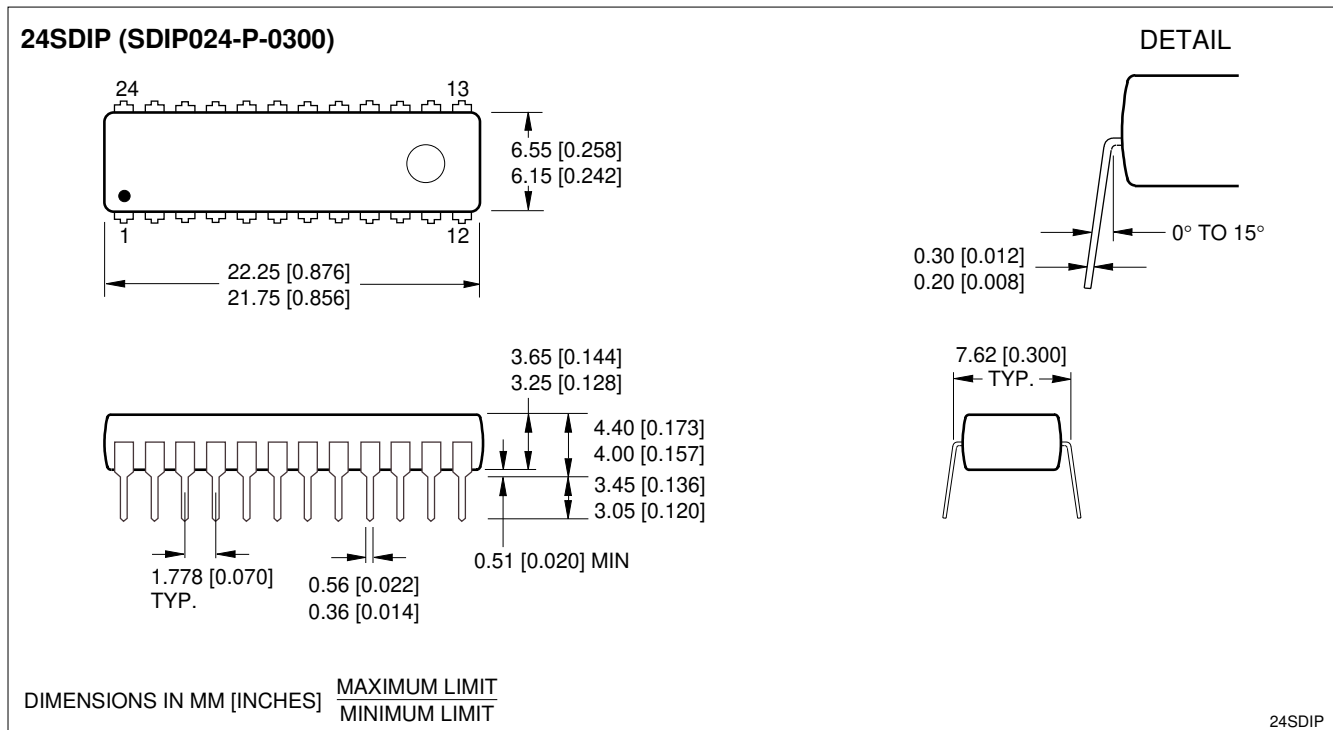
5116-7

Figure 7. Electrical Characteristic Curves
 ($V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$ unless otherwise specified)

PACKAGE DIAGRAMS

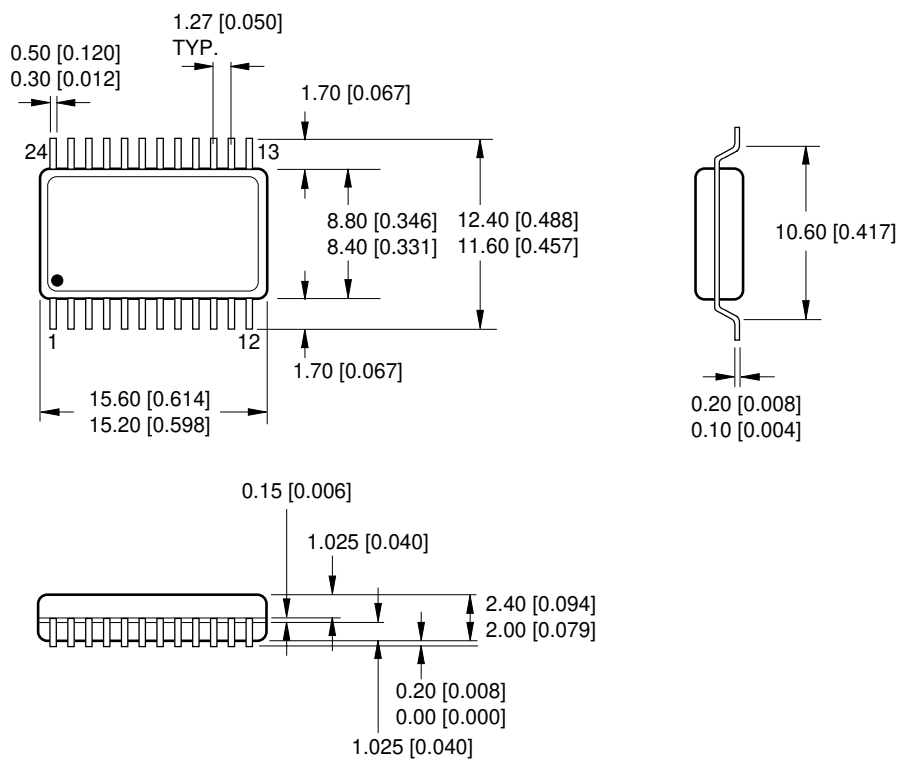


24-pin, 600-mil DIP



24-pin, 300-mil SK-DIP

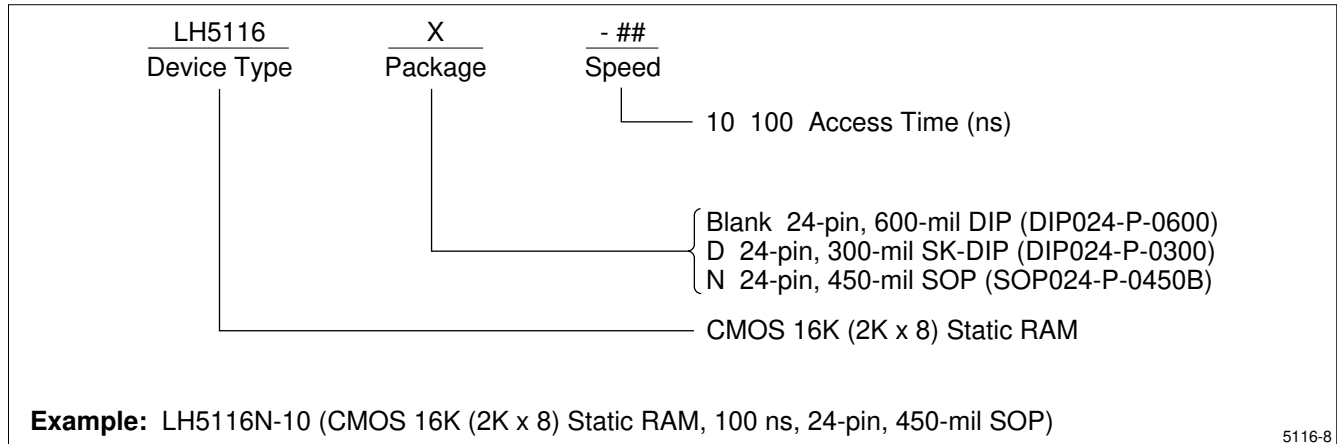
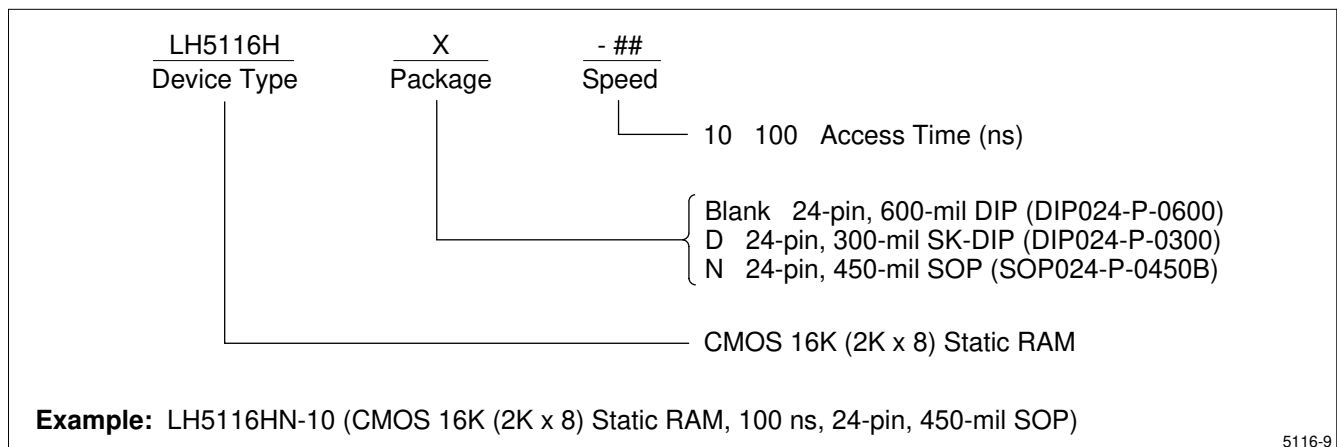
24SOP (SOP024-P-0450B)



DIMENSIONS IN MM [INCHES] MAXIMUM LIMIT
 MINIMUM LIMIT

24SOP

24-pin, 450-mil SOP

ORDERING INFORMATION ($T_A = 0^\circ\text{C}$ to 70°C)ORDERING INFORMATION ($T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$)

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