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APPROVED BY:	DATE

SHARP

INTEGRATED CIRCUITS GROUP
SHARP CORPORATION

SPECIFICATION

SPEC No. EL 6 3 7 3 2 B
FILE No.
ISSUE July 13, 1988
PAGE 8 Pages
REPRESENTATIVE DEPARTMENT

DEVICE SPECIFICATION FOR

16K CMOS STATIC RAM (2,048 X 8bit)

MODEL No.

LH5116NA-10

CUSTOMERS APPROVAL

DATE

BY

PRESENTED
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1. General Description

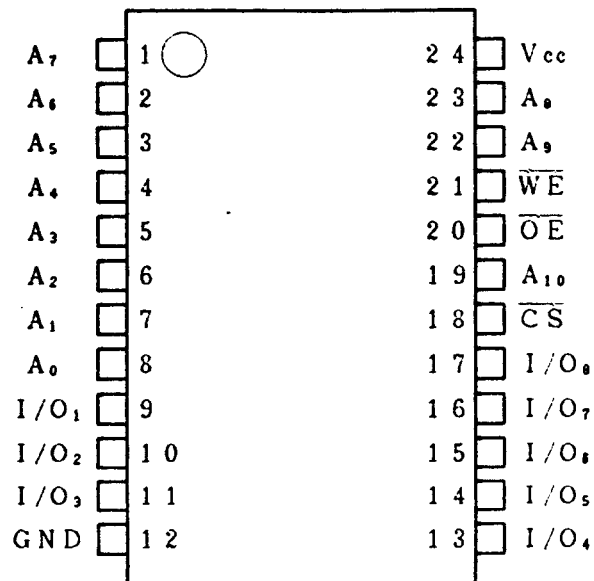
The LH5116NA-10 is a static RAM organized as 16,384(2,048 word x 8bit) fabricated with a CMOS silicon gate process.

It's main features include:

Features

- Access time (MAX.) and dissipation current (MAX.)
100 ns / 40 mA
- Single 5 V power supply ($5 V \pm 10\%$)
- Full static operation requiring no clock and refresh cycle
- All input and output TTL compatible
- Three state output
- Pin configuration is compatible with industry standard
16K EPROM/MASK ROM
- Standard 24-pin Small-Outline Package (SOP)

2. Pin Configuration

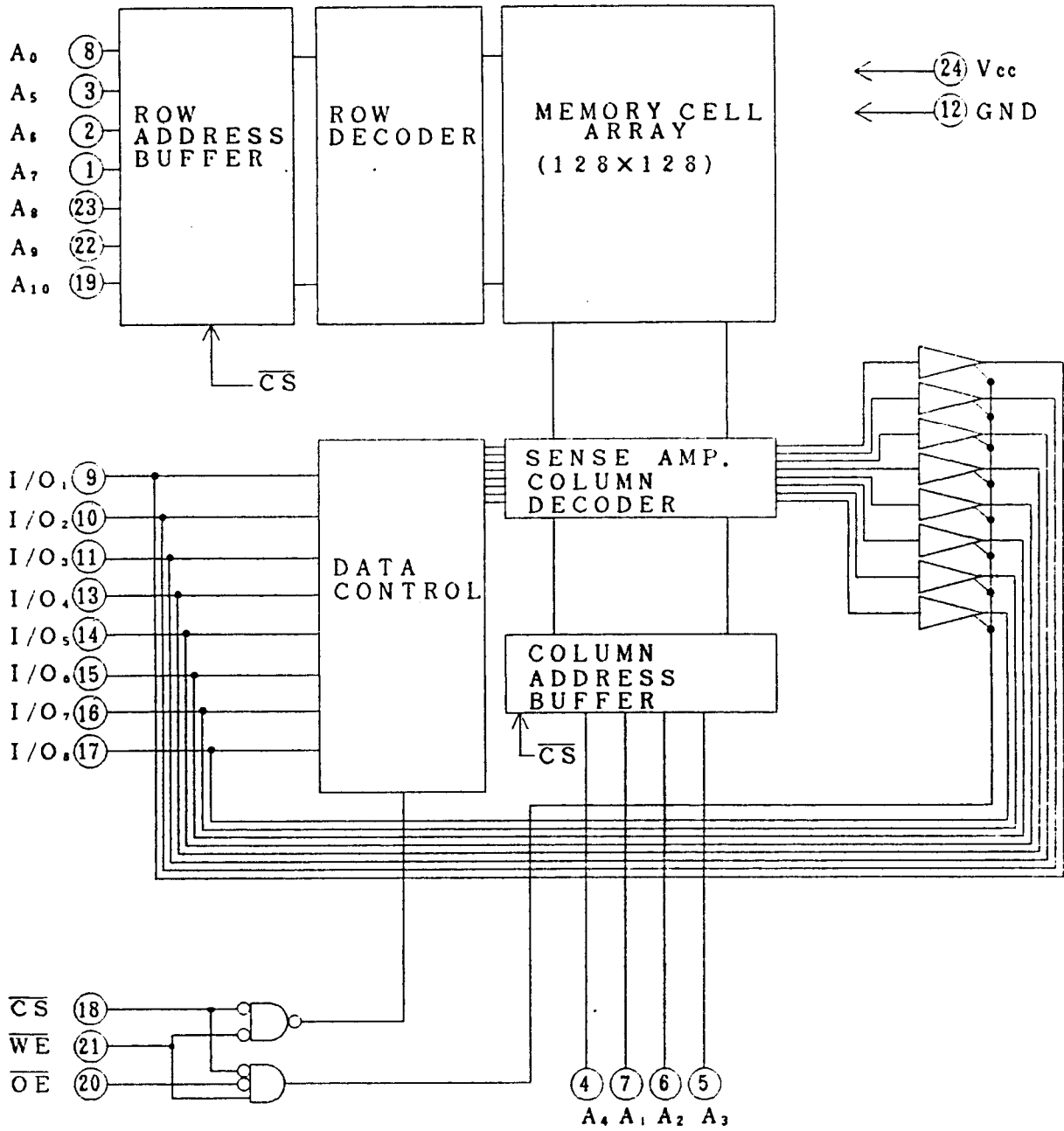


Pin name	Signal
A ₀ ~ A ₁₀	Address input
\overline{CS}	Chip select
\overline{OE}	Output enable
\overline{WE}	Write enable
I/O ₁ ~ I/O ₈	Data input/output
V _{CC}	Power supply
GND	Ground

3. Operating Mode

\overline{CS}	\overline{WE}	\overline{OE}	Mode	I/O ₁ ~ I/O ₈	Supply current
H	X	X	Deselect	High impedance	Standby (I _{CC} L)
L	L	X	Write	Data input	Operating(I _{CC})
L	H	L	Read	Data output	Operating(I _{CC})
L	X	H	Output disable	High impedance	Operating(I _{CC})

4. Block Diagram



5. Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply voltage	V _{CC}	-0.3~+7.0	V
Input voltage	V _{IN}	-0.3~V _{CC} +0.3	V
Operating temperature	T _{opr}	0~+70	°C
Storage temperature	T _{str}	-55~+150	°C

6. DC Electrical Characteristics

V_{CC}=5V±10%, T_a=0~+70°C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input "LOW" voltage	V _{IL}		-0.3		0.8	V
Input "HIGH" voltage	V _{IH}		2.2		V _{CC} +0.3	V
Output "LOW" voltage	V _{OL}	I _{OL} =2.1mA			0.4	V
Output "HIGH" voltage	V _{OH}	I _{OH} =-1.0mA	2.4			V
Input leakage current	I _{LI}	V _{IN} =0~V _{CC}			1.0	μA
Output leakage current	I _{LO}	$\overline{CS} = V_{IH}, V_{I/O} = 0V \sim V_{CC}$			1.0	μA
Dissipation current 1	I _{CC1}	$\overline{CS} = 0V$, other input is 0V~V _{CC} , I _{I/O} =0mA, ($\overline{OE} = V_{CC}$)		2.5	3.0	mA
Dissipation current 2	I _{CC2}	$\overline{CS} = V_{IL}$, other input is V _{IL} ~V _{IH} , I _{I/O} =0mA, ($\overline{OE} = V_{IH}$)		3.0	4.0	mA
Standby Dissipation current	I _{CCL}	$\overline{CS} \geq V_{CC} - 0.2V$ other input is 0V~V _{CC}			1.0	μA
					0.2*	μA

Note)* T_a=25°C

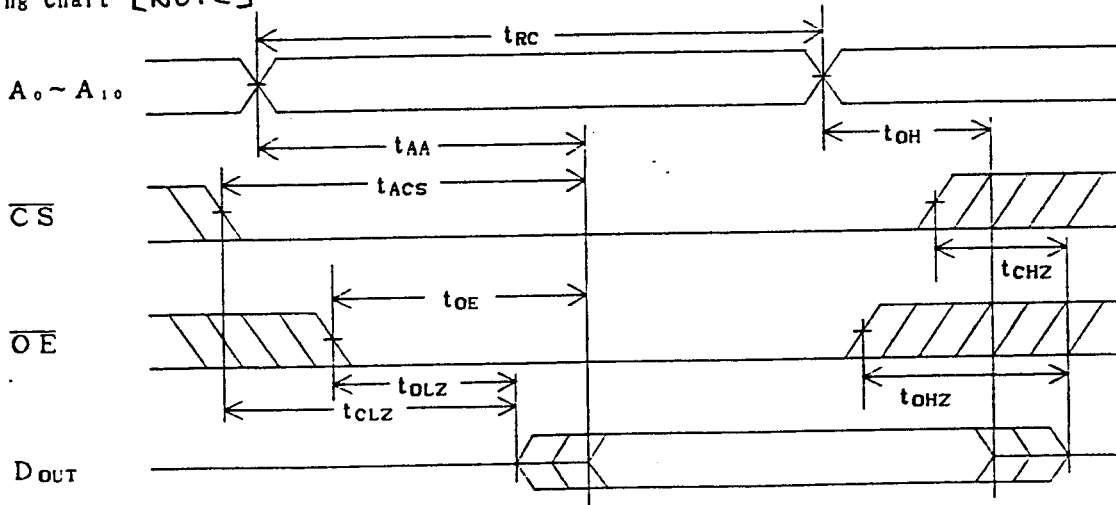
7. AC Characteristics

Read cycle

$V_{CC} = 5V \pm 10\%$, $T_a = 0 \sim +70^\circ C$

Parameter	Symbol	MIN	MAX	Unit
Read cycle time	t_{RC}	100		ns
Address access time	t_{AA}		100	ns
Chip enable access time	t_{ACS}		100	ns
Output floating hold time with respect to chip select	t_{CLZ}	10		ns
Output enable access time	t_{OE}		40	ns
Output floating hold time with respect to output enable	t_{OLZ}	10		ns
Output floating time with respect to chip select	t_{CHZ}	0	40	ns
Output floating time with respect to output enable	t_{OHZ}	0	40	ns
Previous read data valid with respect to address change	t_{OH}	10		ns

Timing Chart [NOTE]



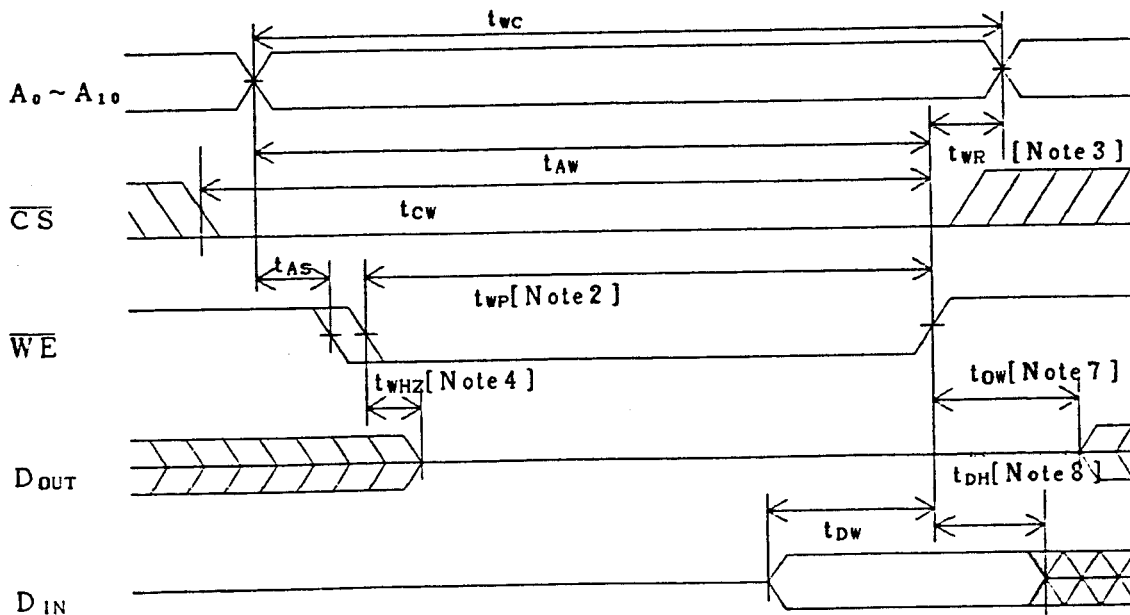
Note) \overline{WE} is "High" level during the read cycle

Write Cycle

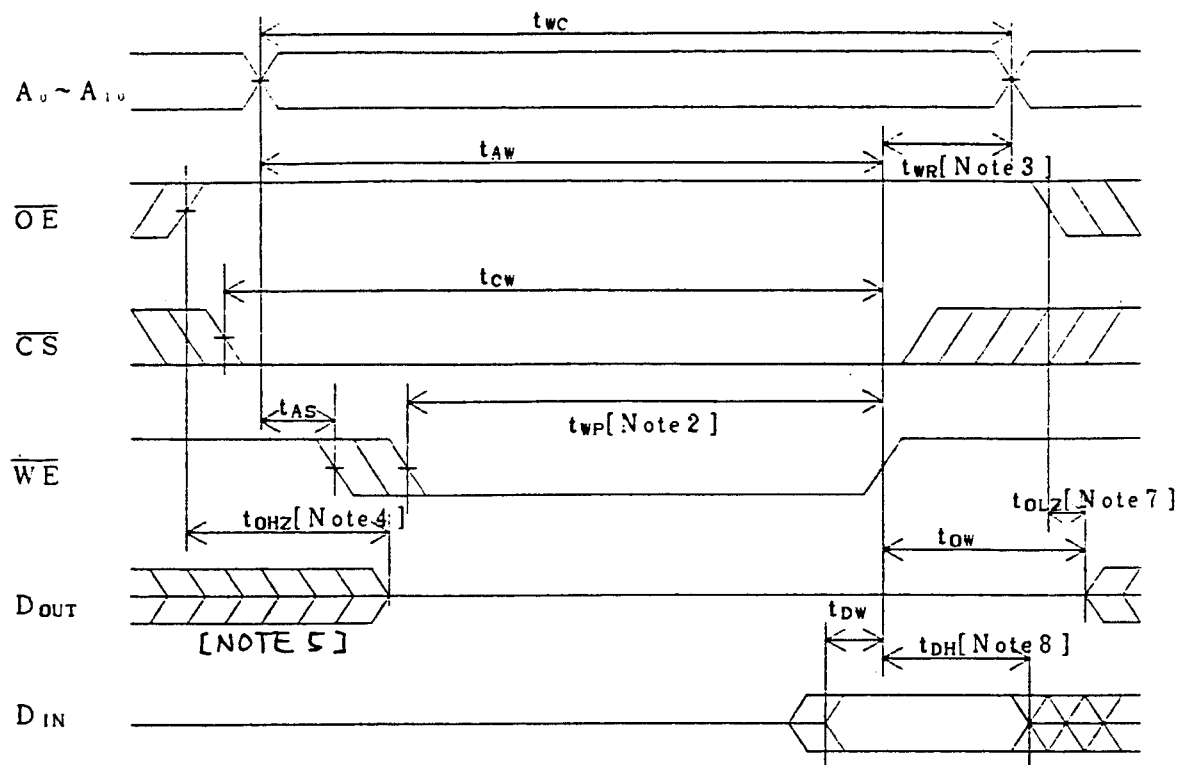
$V_{CC} = 5V \pm 10\%$, $T_a = 0 \sim +70^\circ C$

Parameter	Symbol	MIN	MAX	Unit
Write cycle	t _{wc}	100		ns
Chip enable to write	t _{cw}	80		ns
Write delay	t _{AW}	80		ns
Address setup time	t _{AS}	0		ns
Write pulse width	t _{WP}	60		ns
Write recovery	t _{WR}	10		ns
Output floating time with respect to write pulse	t _{WHZ}		30	ns
Data setup time	t _{DW}	30		ns
Data hold time	t _{DH}	10		ns
Output floating time with respect to write	t _{OW}	10		ns
Output hold time with respect to output enable	t _{OHZ}		40	ns

Timing Chart(No.1)[Note1,6]

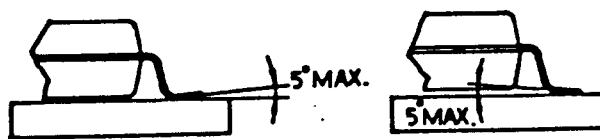
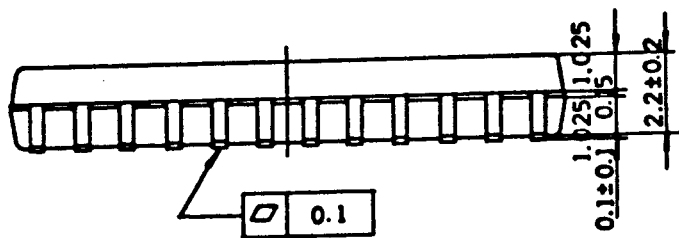
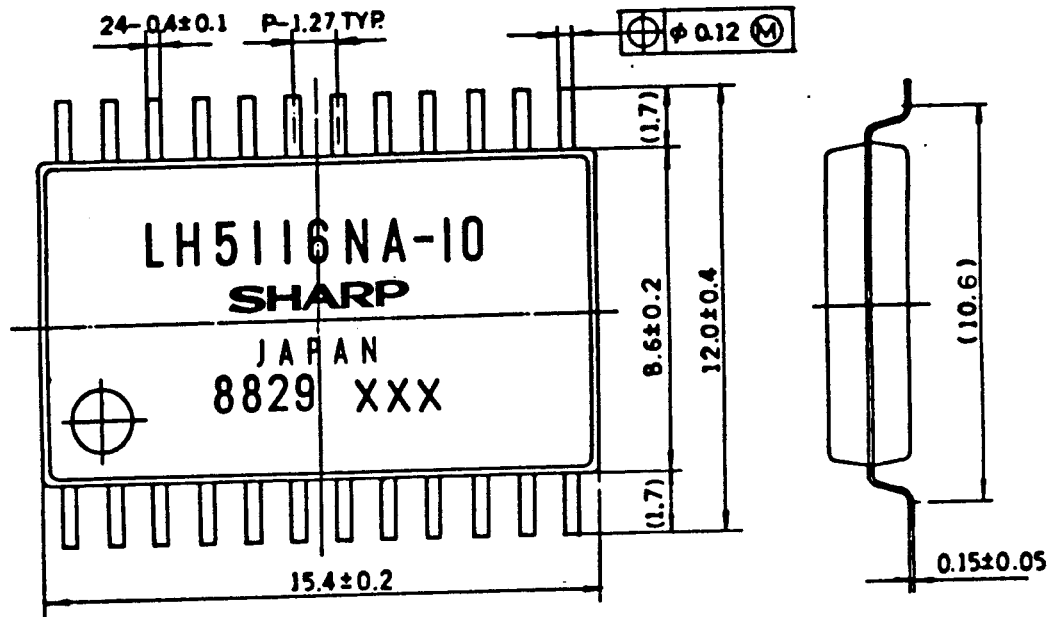


Timing Chart (No.2) [Note 1]



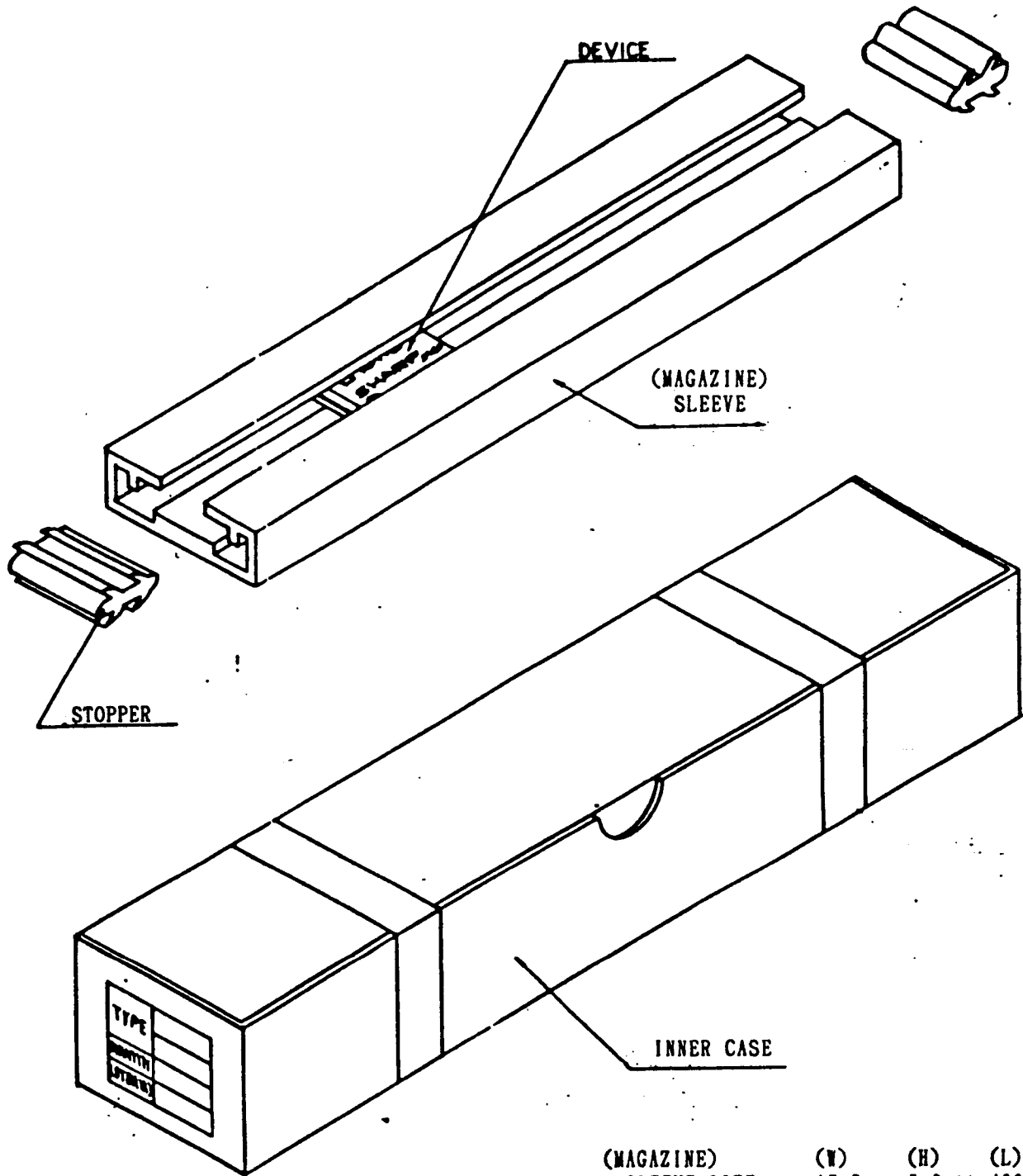
[NOTE]

- \overline{WE} must be High when $A_0 \sim A_{10}$ switch between high and low.
- Write cycle occurs during a overlapping period of $\overline{CS} = \text{Low}$ and $\overline{WE} = \text{Low}(t_{wp})$.
- t_{wr} represents the time interval between the earliest rising edge of \overline{CS} or \overline{WE} and the end of write cycle.
- Since during this period, I/O pins assume output state, no input signal 180° out of phase with an output signal is admitted.
- If the rising edge of \overline{CS} occurs simultaneously with or after the falling edge of \overline{WE} the output buffer assume high impedance state.
- \overline{OE} must be kept Low level.
- D_{OUT} generates data in phase with input data for the write cycle.
- If both \overline{CS} remain Low during this period, I/O pins assume output state. At this point, no data input signal 180° out of phase with an output signal.



Plastic body dimensions do not include burr of resin.

適用機種 APPLICABLE MODEL		LH5116NA		尺度 SCALE	5 / 1	單位 UNIT	1 = 1 / 1mm	△			
板厚 THICKNESS		数量 PIECES		材質 MATERIAL		仕上 FINISH		名称 NAME			
						TIN PLATING		SOT24BP			
日付 DATE		'88. 7 . 12		設計 DESIGN		製図 DRAW		校对 CHECK		承認 APPROVE	
				SHARP CORPORATION		IC		図号 DRAWING No.		AA941-001	



(MAGAZINE) SLEEVE SIZE : (W) 17.5 (H) 5.6 (L) 490
 CASE SIZE : (W) 80 (H) 62 (L) 510

適用機種 APPLICABLE MODEL		尺規 SCALE		單位 UNIT		△			
LH5116NA		/		1 = 1/1 mm		△			
板厚 THICKNESS		枚数 PIECES		材質 MATERIAL		仕上 FINISH		名称 NAME	
								28SOP, 24SOP EXTERNAL APPEARANCE OF PACKING	
日付 DATE		'88. 7 . 12		設計者 DESIGNER		I.C. 番号 IC NO.		コード CODE	
設計 DESIGN		描圖 DRAW		校核 CHECK		承認 APPROVE		図番 DRAWING NO.	
SHARP CORPORATION								BJ 2 0:0 - 0 1 1 1	

AC Characteristics Test Conditions

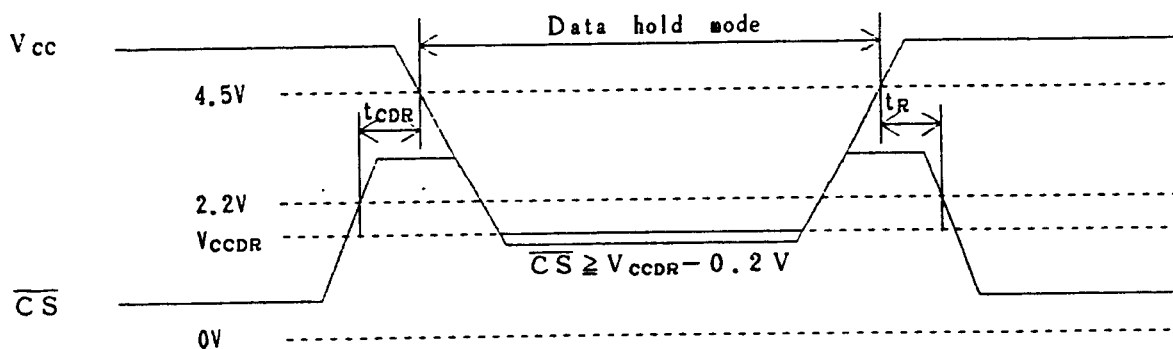
項 目	条 件
Input pulse level	$V_{IN} = 2.2V, V_{IL} = 0.8V$
Input rise and fall time	10 ns
I/O timing reference level	1.5 V
Output load	100 pF + 1 TTL

8. Data Hold Characteristics at Low Supply voltage

$T_a = 0 \sim +70^\circ C$

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Data hold supply voltage	V_{CCDR}	$\overline{CS} \geq V_{CCDR} - 0.2V$	2.0			V
Data hold supply current	I_{CCDR}	$\overline{CS} \geq V_{CCDR} - 0.2V$ $V_{CCDR} = 2V$			1.0 0.2**	μA μA
Chip Select Setup time	t_{CDR}		0			ns
Chip Select Hold time	t_R		t_{RC}^*			ns

Note *Read cycle time **at $T_a = 25^\circ C$



9. Pin Capacitances

$T_a = 25^\circ C, f = 1MHz$

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit
Input capacitance	C_I	$V_I = 0V$			7	pF
I/O capacitance	$C_{I/O}$	$V_{I/O} = 0V$			10	pF

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