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PRODUCT SPECIFICATION

SHARP

Integrated Circuits Group

LH5116NA-10F

16K SRAM

(Model Number: LH5116NC)

Spec. Issue Date: Oct. 22, 2004

Spec No: EL16X148

SHARP

SPEC No.	EL16X148
ISSUE:	Oct. 22. 2004

To;

SPECIFICATIONS

Product Type 16k SRAM

LH5116NA-10F

Model No. (LH5116NC)

*This specifications contains 20 pages including the cover and appendix.
If you have any objections, please contact us before issuing purchasing order.

CUSTOMER ACCEPTANCE

DATE:

BY:

PRESENTED

BY: M. Okada

M. OKADA
Dept. General Manager

REVIEWED BY: M. Kawai

PREPARED BY: T. Morimura

Product Development Dept. 3
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Integrated Circuits Group
SHARP CORPORATION

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● When using the products covered herein, please observe the conditions written herein and the precautions outlined in the following paragraphs. In no event shall the company be liable for any damages resulting from failure to strictly adhere to these conditions and precautions.

(1) The products covered herein are designed and manufactured for the following application areas. When using the products covered herein for the equipment listed in Paragraph (2), even for the following application areas, be sure to observe the precautions given in Paragraph (2). Never use the products for the equipment listed in Paragraph (3).

- Office electronics
- Instrumentation and measuring equipment
- Machine tools
- Audiovisual equipment
- Home appliances
- Communication equipment other than for trunk lines

(2) Those contemplating using the products covered herein for the following equipment which demands high reliability, should first contact a sales representative of the company and then accept responsibility for incorporating into the design fail-sale operation, redundancy, and other appropriate measures for ensuring reliability and safety of the equipment and the overall system.

- Control and safety devices for airplanes, trains, automobiles, and other transportation equipment
- Mainframe computers
- Traffic control systems
- Gas leak detectors and automatic cutoff devices
- Rescue and security equipment
- Other safety devices and safety equipment, etc.

(3) Do not use the products covered herein for the following equipment which demands extremely high performance in terms of functionality, reliability, or accuracy.

- Aerospace equipment
- Communications equipment for trunk lines
- Control equipment for the nuclear power industry
- Medical equipment related to life support, etc.

(4) Please direct all queries and comments regarding the interpretation of the above three Paragraphs to a sales representative of the company.

● Please direct all queries regarding the products covered herein to a sales representative of the company.

Contents

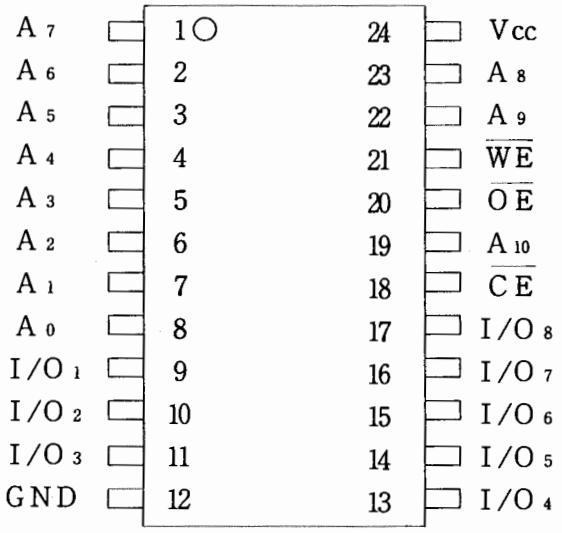
1.Description

The LH5116NA-10F is a static RAM organized as 2,048×8 bit with provides low-power standby mode.
It is fabricated using silicon-gate CMOS process technology.

Features

- ○Access Time ・・・・ 100 ns (Max.)
- ○Operating current ・・・・ 40 mA (Max.)
- ○Standby current ・・・・ 1.0 μA (Max.)
- ○Data retention current ・・・・ 0.2 μA (Max. V_{CCDR}=2V, Ta=25℃)
- ○Wide operating voltage range ・・・・ 4.5 V to 5.5 V
- ○Operating temperature ・・・・ 0℃ to +70℃
- ○Fully static operation
- ○Three-state output
- ○Not designed or rated as radiation hardened
- ○24 pin SOP (SOP24-P-450) plastic package
- ○P-type bulk silicon

2.Pin Configuration



(Top View)

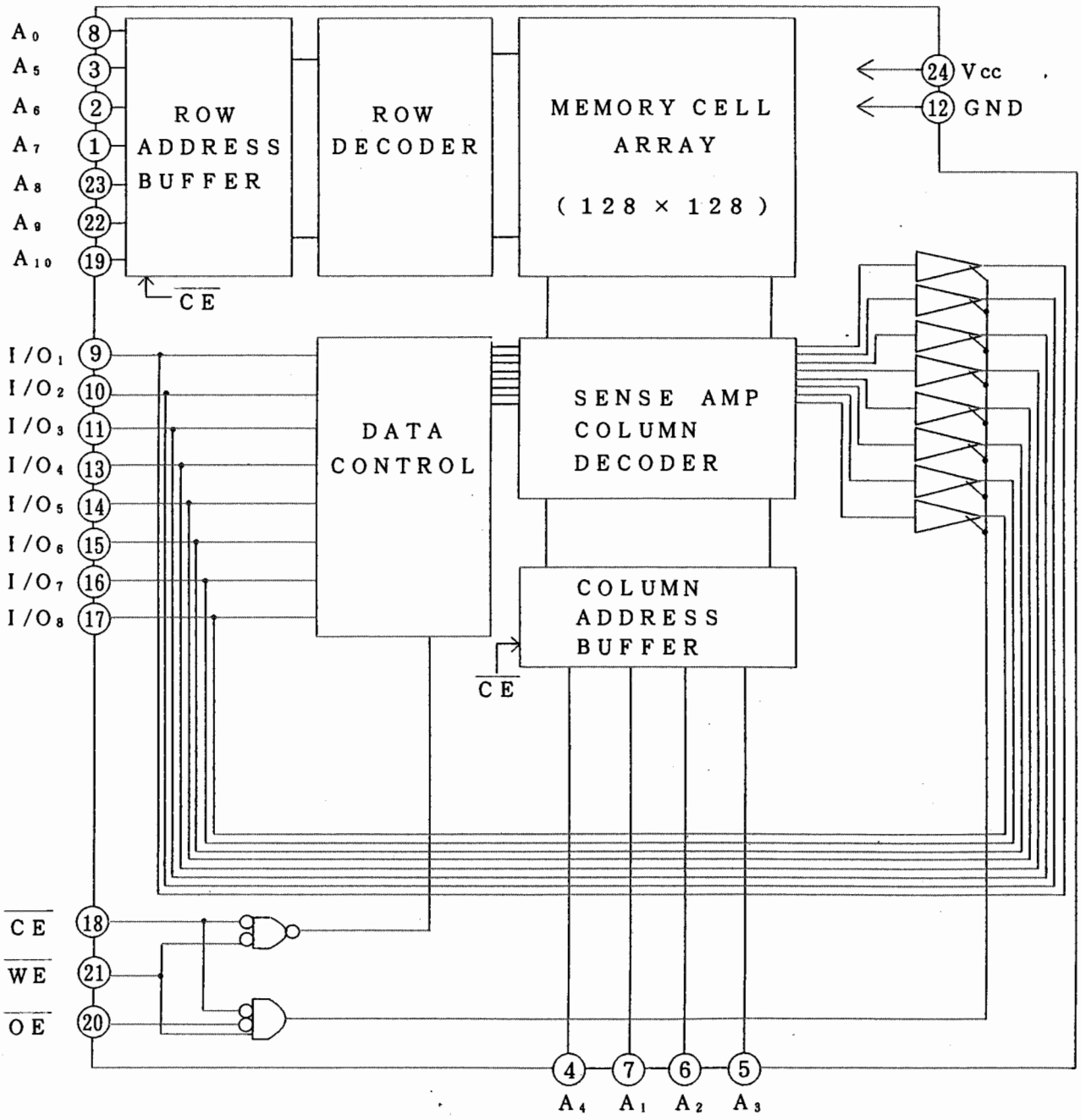
Pin Name	Function
A_0 to A_{10}	Address inputs
$\overline{CE}$	Chip enable
$\overline{WE}$	Write enable
$\overline{OE}$	Output enable
I/O_1 to I/O_8	Data inputs/outputs
Vcc	Power supply
GND	Ground

3. Truth Table

$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	Mode	I/O_1 to I/O_8	Supply current
H	*	*	Standby	High impedance	Standby (I_{SB})
L	H	L	Read	Data output	Active (I_{CC})
L	*	H	Output disable	High impedance	Active (I_{CC})
L	L	*	Write	Data Input	Active (I_{CC})

(*=Don't Care, L=Low, H=High)

4. Block Diagram



5. Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Supply voltage(*1)	Vcc	−0.3 to +7.0	V
Input voltage(*1)	V_{IN}	−0.3 (*2) to Vcc+0.3	V
Operating temperature	T_{opr}	0 to +70	℃
Storage temperature	T_{stg}	−55 to +150	℃

Note) *1. The maximum applicable voltage on any pin with respect to GND.
*2. Undershoot of −3.0V is allowed width of pulse bellow 50ns.

6. Recommended DC Operating Conditions

(Ta = 0℃ to +70℃)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	Vcc	4.5	5.0	5.5	V
Input voltage	V_{IH}	2.2		Vcc+0.3	V
	V_{IL}	−0.3 (*3)		0.8	V

Note) *3. Undershoot of −3.0V is allowed width of pulse below 50ns.

7. DC Electrical Characteristics

(Ta= 0℃ to +70℃, Vcc= 4.5V to 5.5V)

Parameter	Symbol	Conditions	Min.	Typ. (*4)	Max.	Unit
Input leakage current	I_{LI}	V_{IN} =0V to Vcc	−1.0		1.0	μA
Output leakage current	I_{LO}	$\overline{CE}$ =V_{IH} $V_{I/O}$ =0V to Vcc	−1.0		1.0	μA
Operating supply current	I_{CC1}	$\overline{CE}$ =0V, Other input is 0V to Vcc $I_{I/O}$ =0mA, ($\overline{OE}$ =Vcc)		25	30	mA
	I_{CC2}	$\overline{CE}$ =V_{IL}, Other input is V_{IL} to V_{IH} $I_{I/O}$ =0mA, ($\overline{OE}$ =V_{IH})		30	40	mA
Standby current	I_{SB}	$\overline{CE}$ ≧Vcc−0.2V, Ta=25℃			0.2	μA
		Other input is 0V to Vcc			1.0	μA
Output voltage	V_{OL}	I_{OL}= 2.1mA			0.4	V
	V_{OH}	I_{OH}=−1.0mA	2.4			V

Note) *4. Typical values at Vcc=5.0V, Ta=25℃.

8. AC Electrical Characteristics

AC Test Conditions

Input pulse level	0.8V to 2.2V
Input rise and fall time	10ns
Input and Output timing Ref. level	1.5V
Output load	1TTL+C_L (100pF) (*5)

Note) *5. Including scope and jig capacitance.

Read cycle

(Ta= 0℃ to +70℃, Vcc=4.5V to 5.5V)

Parameter	Symbol	Min.	Max.	Unit	
Read cycle time	t_{RC}	100		ns	
Address access time	t_{AA}		100	ns	
$\overline{CE}$ access time	t_{ACE}		100	ns	
Output enable to output valid	t_{OE}		40	ns	
Output hold from address change	t_{OH}	10		ns	
$\overline{CE}$ Low to output active	t_{CLZ}	10		ns	*6
$\overline{OE}$ Low to output active	t_{OLZ}	10		ns	*6
$\overline{CE}$ High to output in High impedance	t_{CHZ}	0	40	ns	*6
$\overline{OE}$ High to output in High impedance	t_{OHZ}	0	40	ns	*6

Write cycle

(Ta= 0℃ to +70℃, Vcc=4.5V to 5.5V)

Parameter	Symbol	Min.	Max.	Unit	
Write cycle time	t_{WC}	100		ns	
$\overline{CE}$ Low to end of write	t_{CW}	80		ns	
Address valid to end of write	t_{AW}	80		ns	
Address setup time	t_{AS}	0		ns	
Write pulse width	t_{WP}	60		ns	
Write recovery time	t_{WR}	10		ns	
Input data setup time	t_{DW}	30		ns	
Input data hold time	t_{DH}	10		ns	
$\overline{WE}$ High to output active	t_{OW}	10		ns	*6
$\overline{WE}$ Low to output in High impedance	t_{WHZ}	0	30	ns	*6
$\overline{OE}$ High to output in High impedance	t_{OHZ}	0	40	ns	*6

Note) *6. Active output to High impedance and High impedance to output active tests specified for a ±200mV transition from steady state levels into the test load.

9.Data Retention Characteristics

(Ta= 0℃ to +70℃)

Parameter	Symbol	Conditions		Min.	Typ. (*7)	Max.	Unit
Data Retention supply voltage	V_{CCDR}	$\overline{CE} \geqq V_{CCDR}-0.2V$		2.0		5.5	V
Data Retention supply current	I_{CCDR}	$V_{CCDR}=2.0V$	Ta=25℃			0.2	μA
		$\overline{CE} \geqq V_{CCDR}-0.2V$				1.0	μA
Chip enable setup time	t_{CDR}			0			ns
Chip enable hold time	t_R			(*8) t_{RC}			ns

Note) *7. Typical values at Ta=25℃

*8. Read Cycle

10.Pin Capacitance

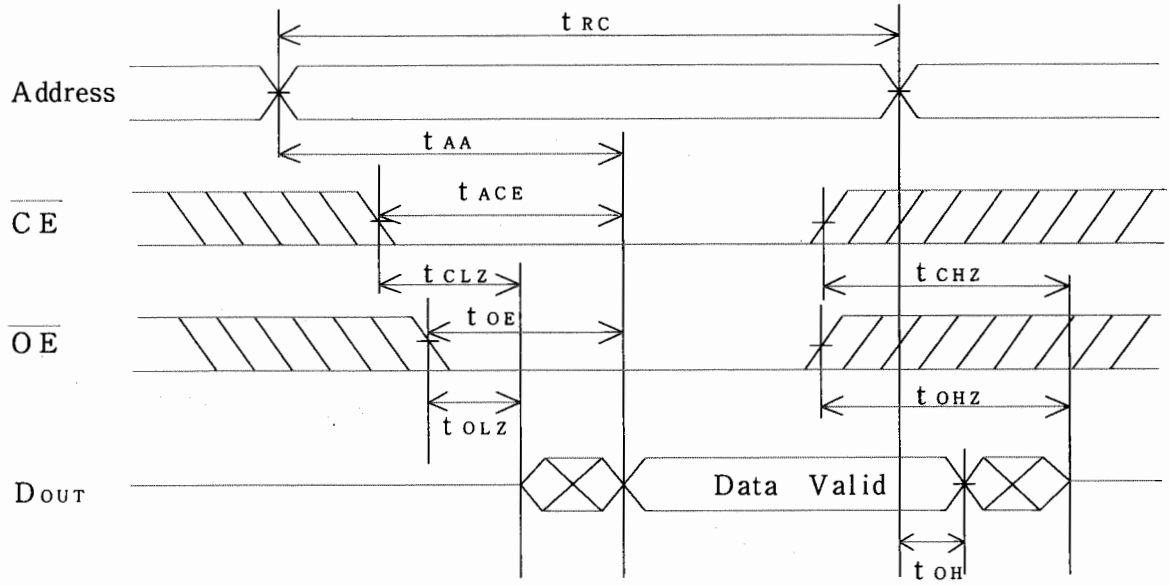
(Ta=25℃, f=1MHz)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	
Input capacitance	C_{IN}	$V_{IN}=0V$			7	pF	*9
I/O capacitance	$C_{I/O}$	$V_{I/O}=0V$			10	pF	*9

Note) *9.This parameter is sampled and not production tested.

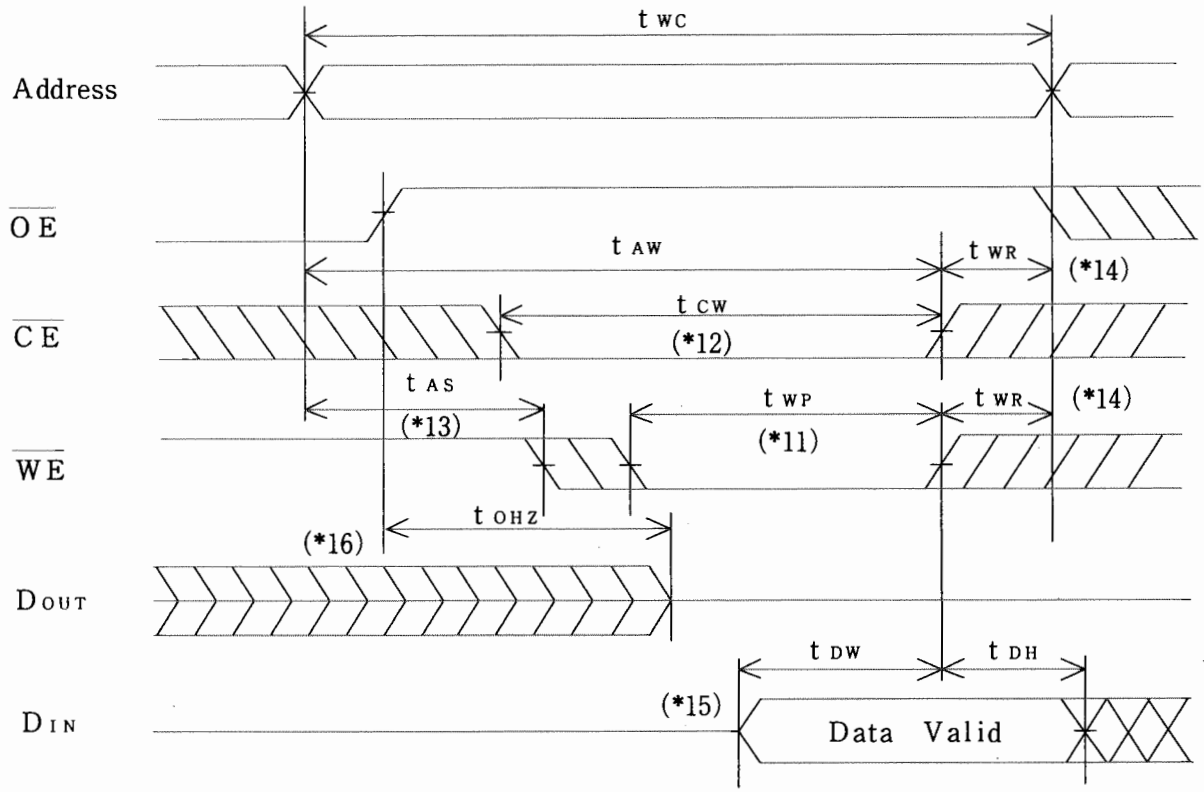
11. Timing Chart

Read cycle timing chart (*10)

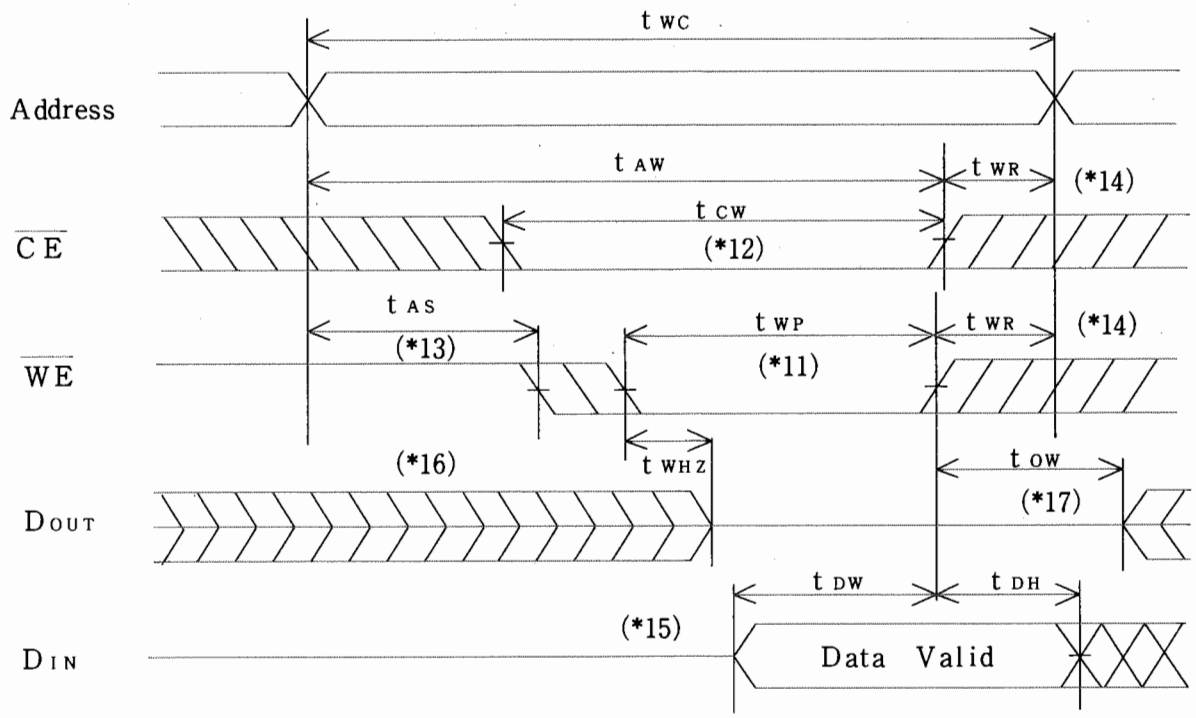


Note) *10. $\overline{WE}$ is high for Read cycle.

Write cycle timing chart ($\overline{OE}$ Controlled)



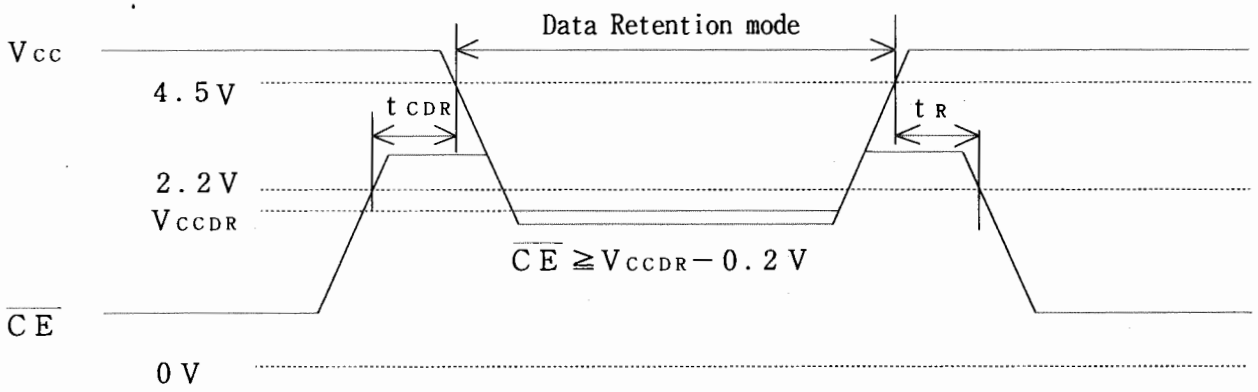
Write cycle timing chart ($\overline{OE}$ Low fixed)



Note) * 11. A write occurs during the overlap of a low $\overline{CE}$, and a low $\overline{WE}$,
A write begins at the latest transition among $\overline{CE}$ going low, and $\overline{WE}$ going low.
A write ends at the earliest transition among $\overline{CE}$ going high, and $\overline{WE}$ going high.
t_{WP} is measured from the beginning of write to the end of write.

* 12. t_{CW} is measured from the later of $\overline{CE}$ going low to the end of write.
* 13. t_{AS} is measured from the address valid to the beginning of write.
* 14. t_{WR} is measured from the end of write to the address change.
* 15. During this period, I/O pins are in the output state, therefore the input signals of opposite phase to the outputs must not be applied.
* 16. If $\overline{CE}$ goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, the outputs remain in high impedance state.
* 17. If $\overline{CE}$ goes high simultaneously with $\overline{WE}$ going high or before $\overline{WE}$ going high, the outputs remain in high impedance state.

Data Retention timing chart ($\overline{CE}$ Controlled)



12 Package and packing specification

[Applicability]

This specification applies to IC package of the LEAD-FREE delivered as a standard specification.

1.Storage Conditions.

1-1.Storage conditions required before opening the dry packing.

- Normal temperature : 5～40℃
- Normal humidity : 80%(Relative humidity) max.

*"Humidity" means "Relative humidity"

1-2.Storage conditions required after opening the dry packing.

In order to prevent moisture absorption after opening, ensure the following storage conditions apply:

(1) Storage conditions for one-time soldering. (Convection reflow*1, IR/Convection reflow.*1, or Manual soldering.)

- Temperature : 5～25℃
- Humidity : 60% max.
- Period : 96 hours max. after opening.

(2) Storage conditions for one-time soldering . (Solder dipping .)

- Temperature : 5～25℃
- Humidity : 60% Max.
- Period : 96 hours max. after opening.

(3) Storage conditions for two-time soldering. (Convection reflow*1, IR/Convection reflow.*1)

a. Storage conditions following opening and prior to performing the 1st reflow.

- Temperature : 5～25℃
- Humidity : 60% max.
- Period : 96 hours max. after opening.

b. Storage conditions following completion of the 1st reflow and prior to performing the 2nd reflow.

- Temperature : 5～25℃
- Humidity : 60% max.
- Period : 96 hours max. after completion of the 1st reflow.

*1:Air or nitrogen environment.

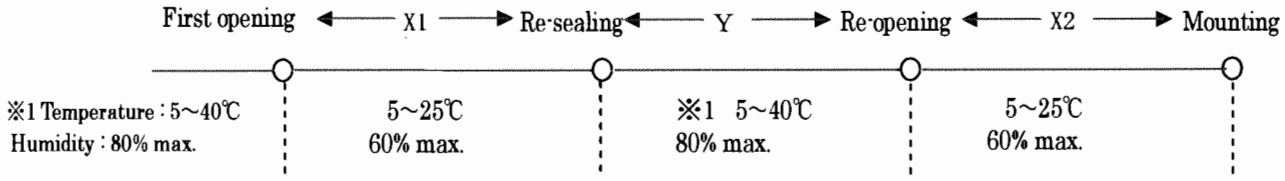
1-3.Temporary storage after opening.

To re-store the devices before soldering, do so only once and use a dry box or place desiccant (with a blue humidity indicator) with the devices and perform dry packing again using heat-sealing.

The storage period, temperature and humidity must be as follows :

(1) Storage temperature and humidity.

※1 : External atmosphere temperature and humidity of the dry packing.



(2) Storage period.

- X1＋X2 : Refer to Section 1-2(1),(2), and (3)a , depending on the mounting method.
- Y : Two weeks max.

2. Baking Condition.

(1) Situations requiring baking before mounting.

- Storage conditions exceed the limits specified in Section 1-2 or 1-3.
- Humidity indicator in the desiccant was already red (pink) when opened.
  (Also for re-opening.)

(2) Recommended baking conditions.

- Baking temperature and period : 120℃ for 16～24 hours or 150℃ for 5～10 hours.
- The above baking conditions do not apply since the magazines are not heat-resistant . Replace the devices on heat-resistant magazine .

(3) Storage after baking.

- After baking, store the devices in the environment specified in Section 1-2 and mount immediately.

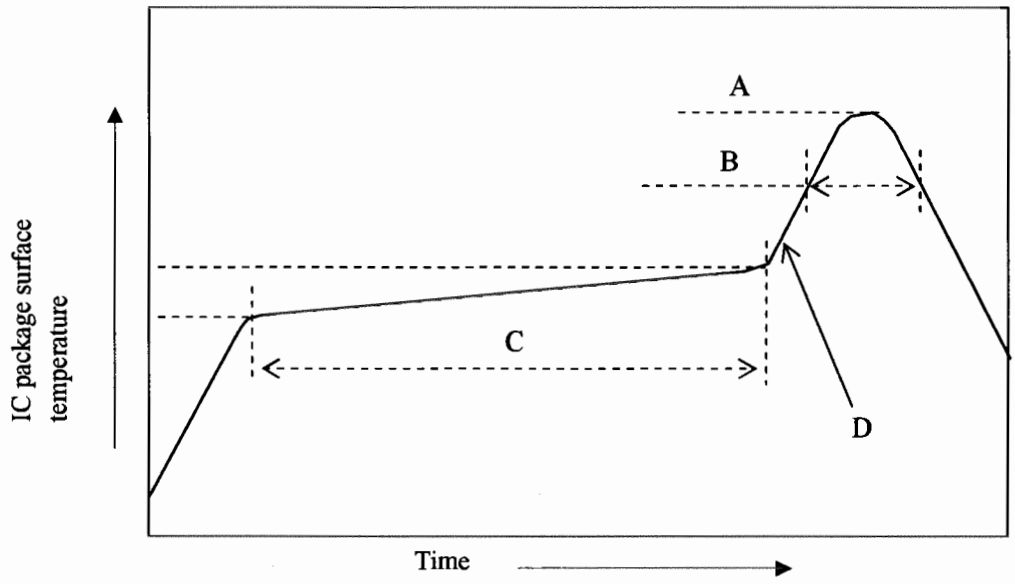
3. Surface mount conditions.

The following soldering condition are recommended to ensure device quality.

3-1.Soldering.

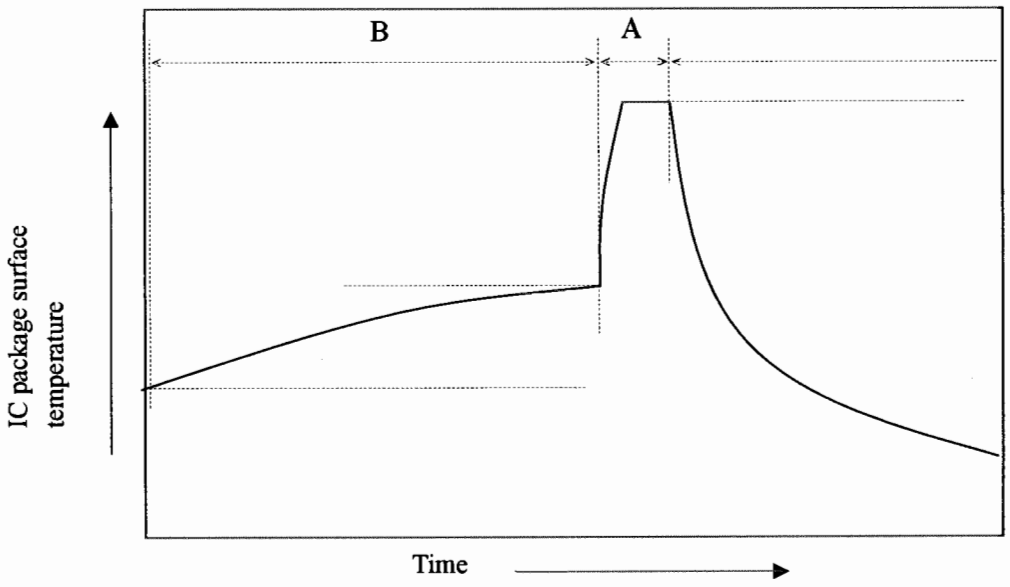
(1) Convection reflow or IR/Convection. (one-time soldering or two-time soldering in air or nitrogen environment)

- Temperature and period :
  - A) Peak temperature. 250℃ max.
  - B) Heating temperature. 40 to 60 seconds as 220℃
  - C) Preheat temperature. It is 150 to 200℃, and is 120±30 seconds
  - D) Temperature increase rate. It is 1 to 3℃/seconds
- Measuring point : IC package surface.
- Temperature profile :



(2) Solder dipping. (one-time dipping only)

- Temperature and period :
  - A) Peak temperature. 260℃ max. for 10 seconds Max.
  - B) Preheat temperature of 120 to 150℃ for 120±60 seconds
- Measuring point :
  - A) Solder bath.
  - B) IC package surface.
- Temperature profile:



(3) Manual soldering (soldering iron) (one-time soldering only)

Soldering iron should only touch the IC's outer leads.

- Temperature and period :
  350℃ max. for 3 seconds / pin max.
  (Soldering iron should only touch the IC's outer leads.)
- Measuring point : Soldering iron tip.

4. Condition for removal of residual flux.

(1) Ultrasonic washing power : 25 watts / liter max.

(2) Washing time : Total 1 minute max.

(3) Solvent temperature : 15～40℃

5. Package outline specification.

Refer to the attached drawing.

(Plastic body dimensions do not include burr of resin.)

The contents of LEAD-FREE TYPE application of the specifications. (*2)

6. Markings.

6-1.Marking details. (The information on the package should be given as follows.)

(1) Product name : LH5116NA-10F

(2) Company name : SHARP

(3) Date code : (Example) YYWW XXX

YY → Denotes the production year. (Last two digits of the year.)

WW → Denotes the production week. (01・02・～・52・53)

XXX → Denotes the production ref. code (1～3 digits).

(4) "JAPAN" indicates the country of origin.

6-2.Marking layout.

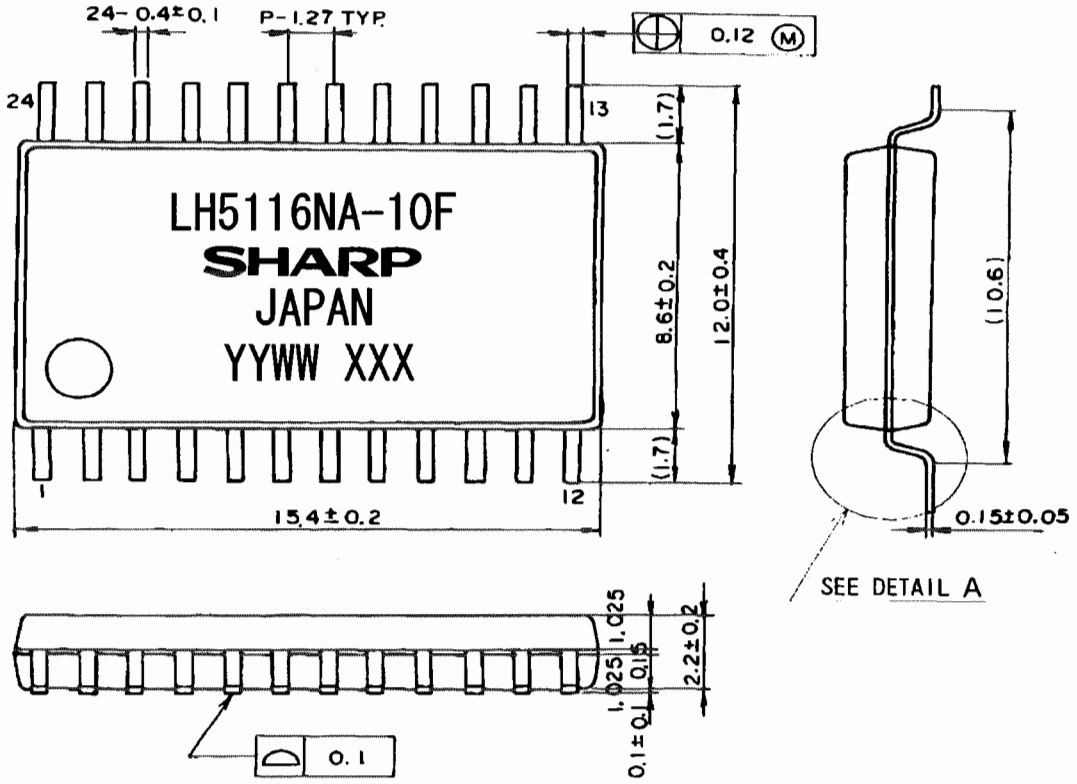
The layout is shown in the attached drawing.

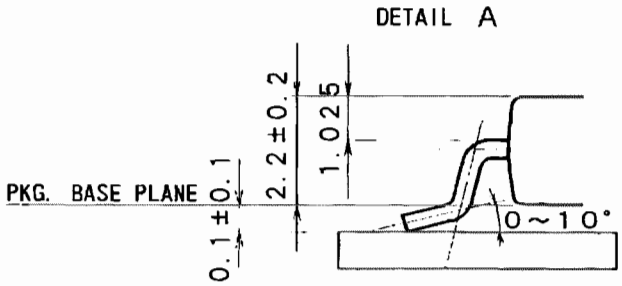
(However, this layout does not specify the size of the marking character and marking position.)

*2 The contents of LEAD-FREE TYPE application of the specifications.

LEAD FINISH or BALL TYPE	LEAD-FREE TYPE (Sn-Bi)
DATE CODE	They are those with an underline.
The word of " LEAD FREE" is printed on the packing label	Printed

(Note) It is those with an underline printing in a date code because of a LEAD-FREE type.





SOP024-P-0450-AA941

LEAD TYPE	LEAD FINISH	LEAD MATERIAL
	Sn-Bi PLATING	42Alloy

NAME	SOP024-P-0450			NOTE : Plastic body dimensions do not include burr of resin.
DRAWING NO.	AA941	UNIT	mm	

20041022

7.Packing Specifications(Dry packing for surface mount packages.)

7-1.Packing materials.

Material name	Material specifications	Purpose
Inner carton	Gardboard (1200 devices / inner carton max.)	Packing the devices.
Magazine	Anti-static treated plastic (30 devices / magazine)	Securing the devices.
Stopper	Plastic or rubber	Securing the devices.
Cap	Plastic (2 caps / bag)	Securing the magazine.
Laminated aluminum bag	Aluminum polyethylene	Keeping the devices dry.
Desiccant	Silica gel	Keeping the devices dry.
Label	Paper	Indicates part number, quantity , and packed date .
Outer carton	Gardboard (4800 devices / outer carton max.)	Outer packing.

(Devices must be placed on the magazine in the same direction.)

7-2.Outline dimension of magazine.

Refer to the attached drawing.

7-3.Outline dimension of carton.

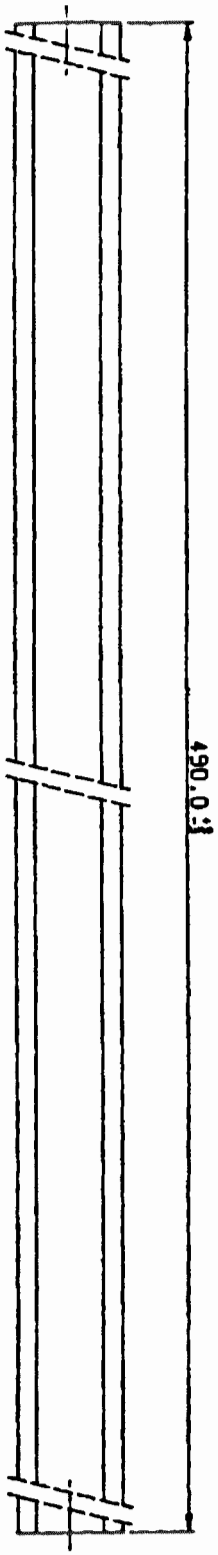
Refer to the attached drawing.

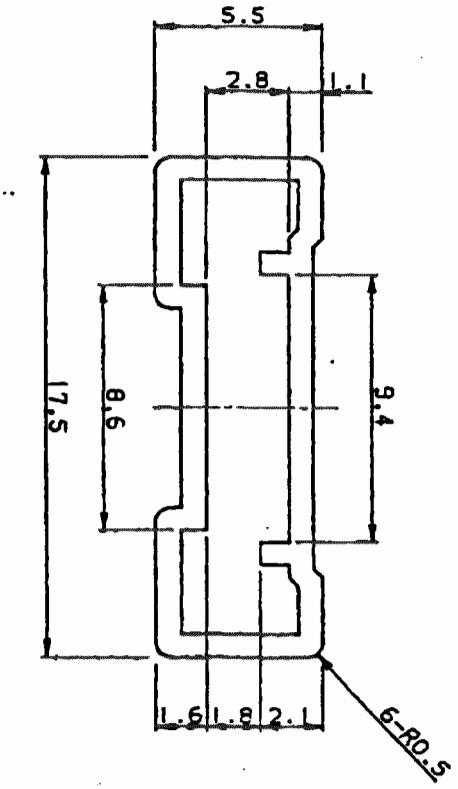
8.Precautions for use.

(1) Opening must be done on an anti-ESD treated workbench.
All workers must also have undergone anti- ESD treatment.

(2) The magazines have undergone either conductive or anti-ESD treatment.
If another magazine is used , make sure it has also undergone conductive or anti-ESD treatment.

(3) The devices should be mounted within one year of the date of delivery.



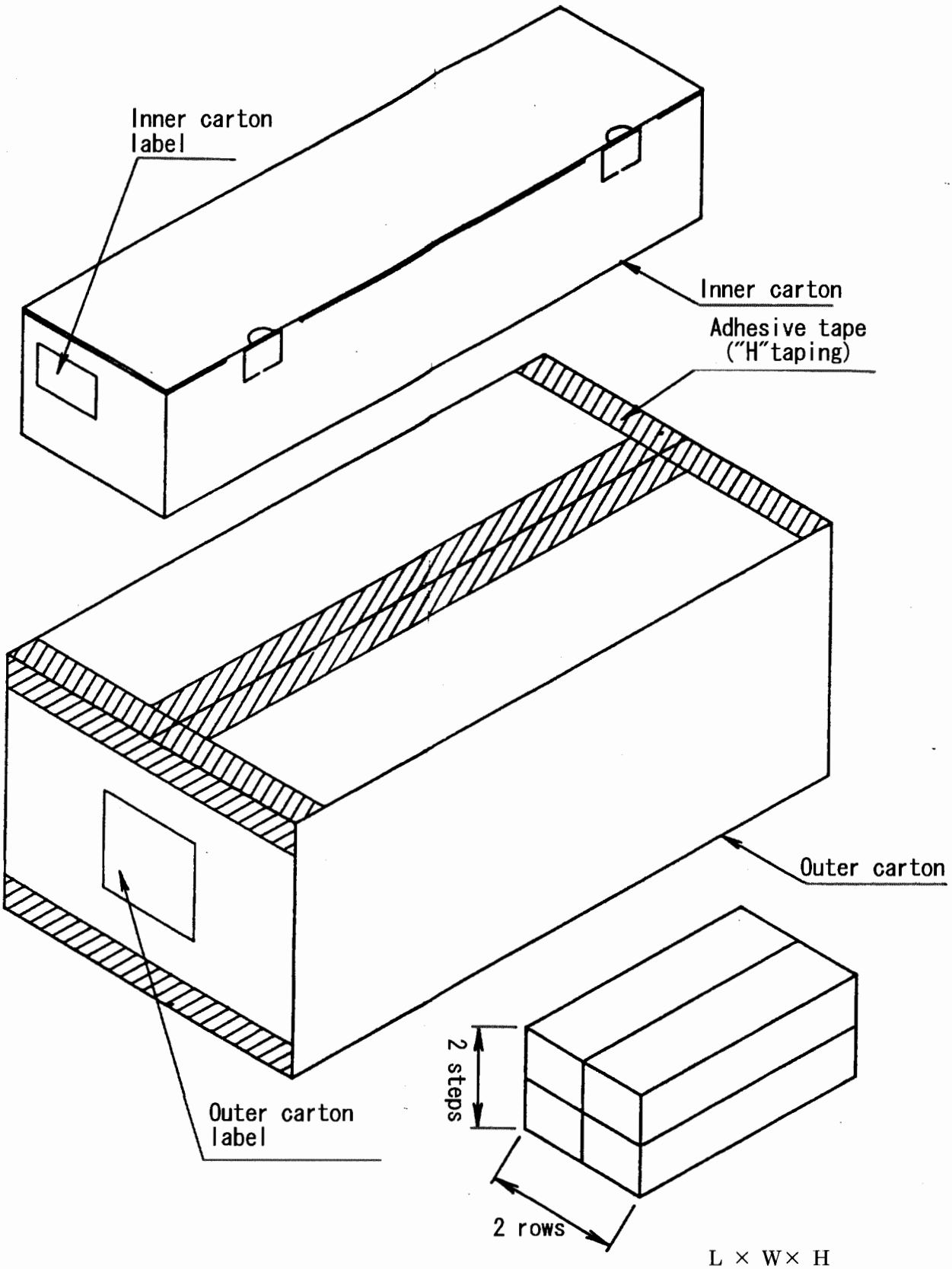


注記 ：マガジン（スリーブ）両側のストッパーは、ゴムストッパーとする。指示無き寸法公差は全て±0.4mmとする。

NOTES : Stopper which is set at the both ends of magazine(sleeve) is made of rubber.
All tolerances are ±0.4mm unless otherwise specified.

名称 Name	SOP28SPN-A2			備考 Note
Drawing no.	CV607	単位 Unit	mm	

20041022



L × W× H

Inner carton - Outer dimensions : 575×125×110

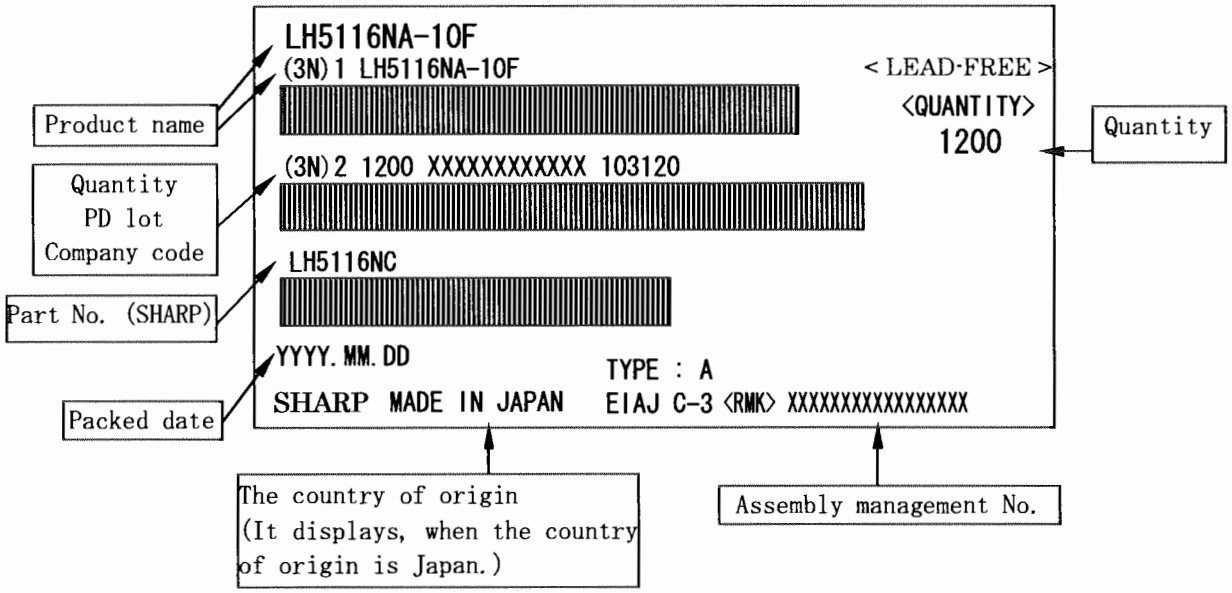
Outer carton - Outer dimensions : 605×265×260

名称 NAME	Packing specifications			備考 NOTE 出荷数量が端数の場合、本仕様と異なることがあります。 There is a possibility different from this specification when the number of shipments is fractions.
DRAWING NO.	BJ535	単位 UNIT	mm	

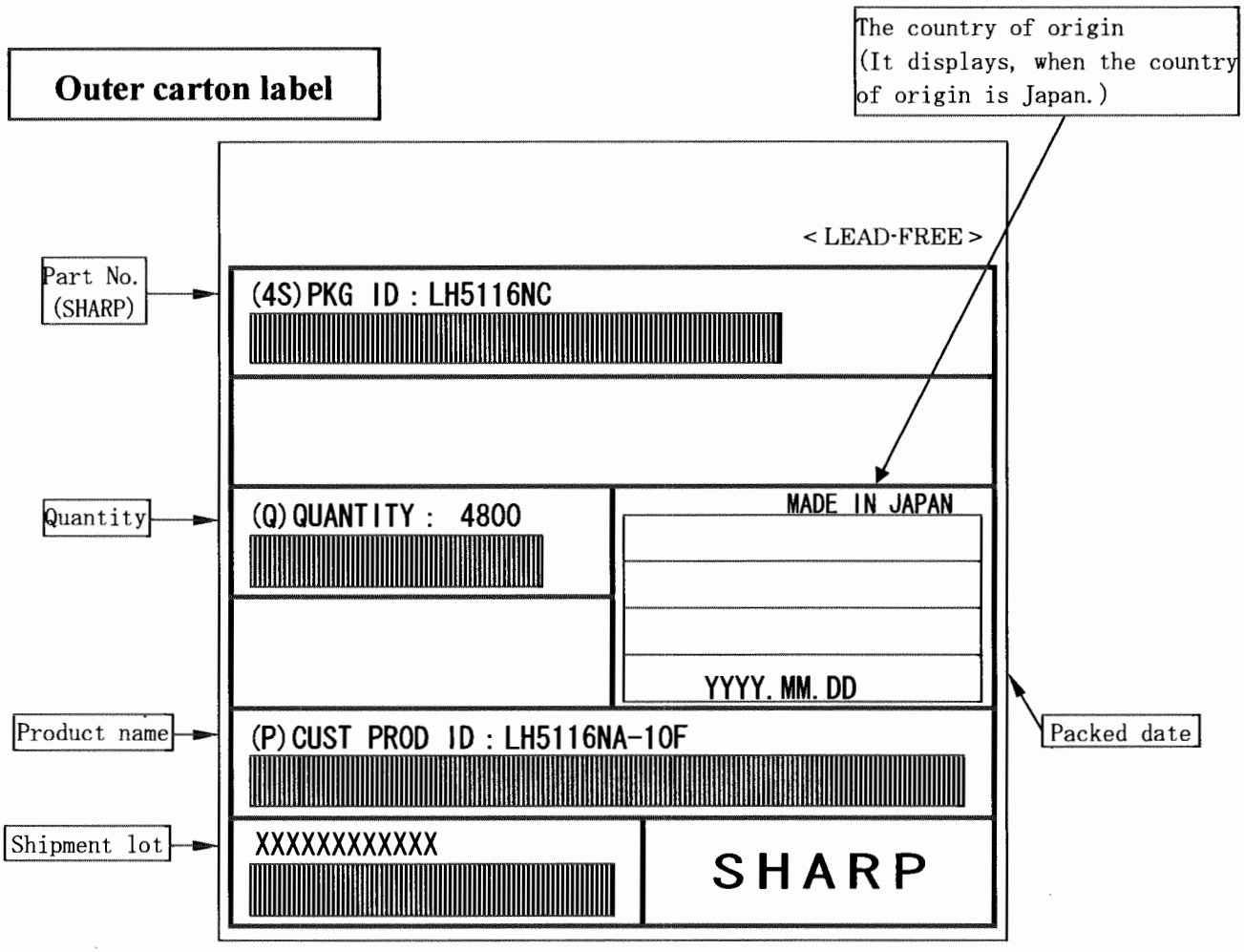
20041022

(Note) The <LEAD-FREE> display shows a lead-free article.

Inner carton label



Outer carton label



(Former) EIAJ B Standard conforming

20041022

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