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FEATURES

- ARM922T™ Core:
 - 32-bit ARM9TDMI™ RISC Core (200 MHz)
 - 16KB Cache: 8KB Instruction Cache and 8KB Data Cache
 - MMU (Windows CE™ Enabled)
- 80KB On-Chip Memory
- Programmable Interrupt Controller
- External Bus Interface
 - 100 MHz
 - Asynchronous SRAM/ROM/Flash
 - Synchronous DRAM/Flash
 - PCMCIA
 - CompactFlash
- Clock and Power Management
 - 32.768 kHz and 14.7456 MHz Oscillators
 - Programmable PLL
- Low Power Modes (Typical)
 - Run (125 mA), Halt (25 mA), Standby (42 µA)
- Programmable LCD Controller
 - Up to 1,024 × 768 Resolution
 - Supports STN, Color STN, AD-TFT, HR-TFT, TFT
 - Up to 64 k-Colors and 15 Gray Shades
- DMA (10 Channels)
 - AC97
 - MMC
 - USB
- USB Device Interface (USB 1.1)
- Synchronous Serial Port (SSP)
 - Motorola SPI™
 - Texas Instruments SSI
 - National MICROWIRE™
- Three Programmable Timers
- Three UARTs
 - Classic IrDA (115 kbit/s)
- Smart Card Interface (ISO7816)
- Two DC-to-DC Converters
- MultiMediaCard™ Interface
- AC97 Codec Interface
- Smart Battery Monitor Interface
- Real Time Clock (RTC)
- Up to 60 General Purpose I/Os
- Watchdog Timer
- JTAG Debug Interface and Boundary Scan
- Operating Voltage
 - 1.8 V Core
 - 3.3 V Input/Output
- 5 V Tolerant Digital Inputs (except oscillator pins)
 - Oscillator pins P15, P16, R13, and T13 are 1.8 V ± 10%.
- Operating Temperature
 - 0°C to +70°C Commercial
 - -40°C to +85°C Industrial (With Clock Frequency Reduction)
- 256-Ball PBGA or 256-Ball CABGA Package

DESCRIPTION

The LH7A400, powered by an ARM922T, is a complete System-on-Chip with a high level of integration to satisfy a wide range of requirements and expectations.

This high degree of integration lowers overall system costs, reduces development cycle time and accelerates product introduction.

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National Semiconductor MICROWIRE is a trademark of National Semiconductor Corporation.

Windows CE is a trademark of Microsoft Corporation.

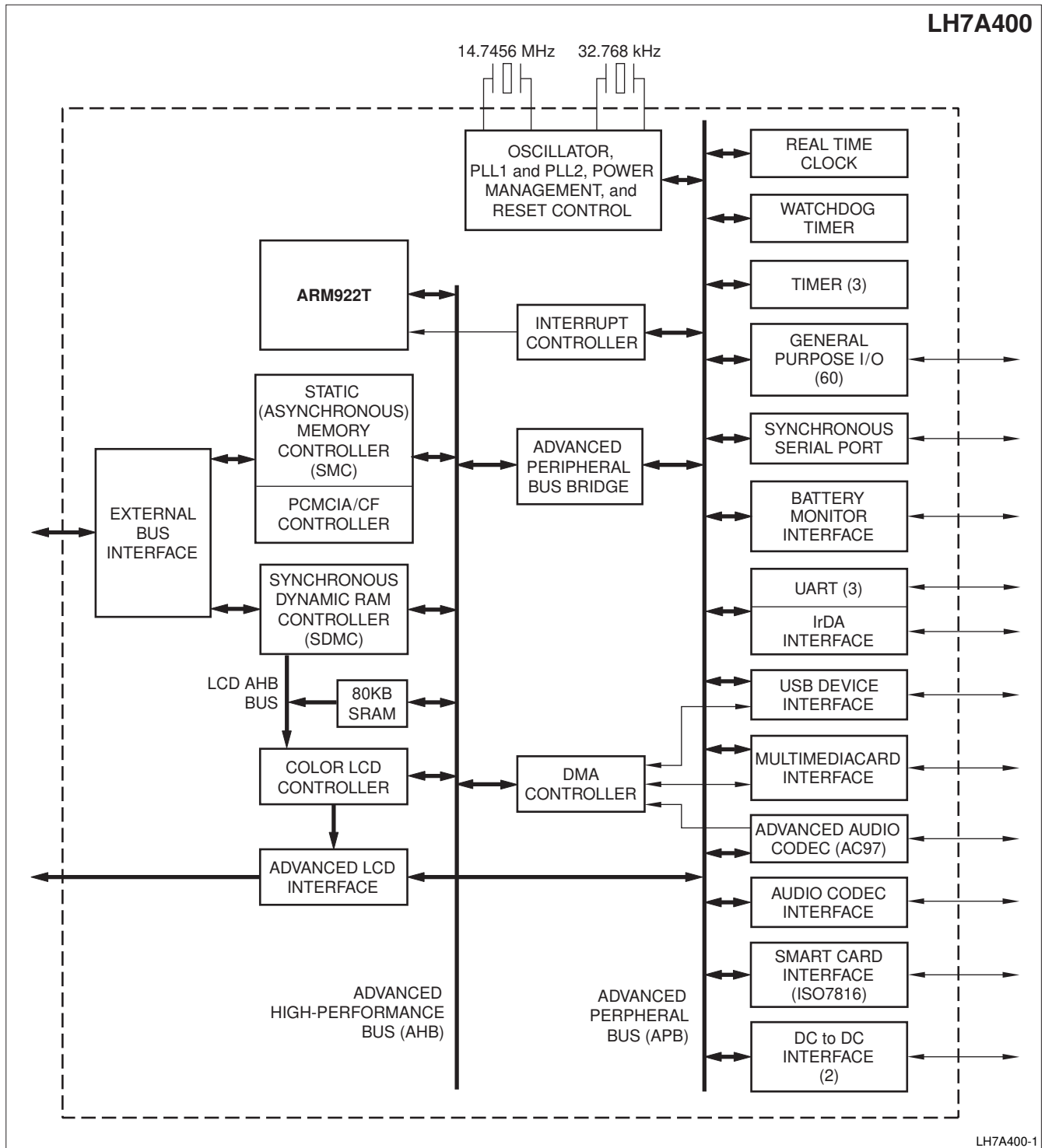


Figure 1. LH7A400 Block Diagram

Table 1. Functional Pin List

PBGA PIN	CABGA PIN	SIGNAL	DESCRIPTION	RESET STATE	STANDBY STATE	OUTPUT DRIVE
G7	C10	VDD	I/O Ring Power			
F1	F9					
K7	F11					
M1	F14					
M5	G8					
T6	H13					
R14	J9					
M14	K15					
J11	L7					
J12	N6					
F13	N8					
B14	N12					
E10	N13					
B8	P11					
H7	B8	VSS	I/O Ring Ground			
G3	C6					
K4	D5					
N5	D13					
P6	E8					
T14	F7					
R16	G13					
N16	H9					
K13	J14					
H9	K7					
C15	L8					
A11	L10					
E8	L12					
A5	M11					
F7	M14					
E1	C4	VDDC	Core Power			
J4	D7					
P3	D10					
T8	F4					
K9	F10					
L13	J4					
E15	J8					
D12	K8					
A7	L6					
H5	G7	VSSC	Core Ground			
M3	H4					
L9	H8					
T10	L4					
N15	L9					
H12	N3					
B15	N7					
C9	N10					
G6	R5					

Table 1. Functional Pin List (Cont'd)

PBGA PIN	CABGA PIN	SIGNAL	DESCRIPTION	RESET STATE	STANDBY STATE	OUTPUT DRIVE
R11	P12	VDDA	Analog Power for PLL			
N12	M10					
P12	R13	VSSA	Analog Ground for PLL			
T11	N11					
D3	E4	nPOR	Power On Reset	Input	Input	
H6	D1	nURESET	User Reset; should be pulled HIGH for normal or JTAG operation.	Input (Schmitt)	Input	
D4	E2	WAKEUP	Wake Up	Input (Schmitt)	Input	
E4	F2	nPWRFL	Power Fail Signal	Input (Schmitt)	Input	
C2	D2	nEXTPWR	External Power	Input (Schmitt)	Input	
R13	R14	XTALIN	14.7456 MHz Crystal Oscillator pins. An external clock source can be connected to XTALIN leaving XTALOUT open.	Input	Input	
T13	R15	XTALOUT		LOW	LOW	
P16	N14	XTAL32IN	32.768 kHz Real Time Clock Crystal Oscillator pins. An external clock source can be connected to XTAL32IN leaving XTAL32OUT open.	Input	Input	
P15	M13	XTAL32OUT		Output	Output	
P14	M12	CLKEN	External Oscillator Clock Enable Output	LOW	LOW	8 mA
J6	J5	PGMCLK	Programmable Clock (14.7456 MHz MAX.)	LOW	LOW	8 mA
K11	P14	nCS0	Asynchronous Memory Chip Select 0	HIGH	HIGH	12 mA
K10	P16	nCS1	Asynchronous Memory Chip Select 1	HIGH	HIGH	12 mA
P13	N15	nCS2	Asynchronous Memory Chip Select 2	HIGH	HIGH	12 mA
M12	N16	nCS3/ nMMSPICS	<ul style="list-style-type: none"> • Asynchronous Memory Chip Select 3 • MultiMediaCard SPI Mode Chip Select 	HIGH: nCS3	HIGH	12 mA

Table 1. Functional Pin List (Cont'd)

PBGA PIN	CABGA PIN	SIGNAL	DESCRIPTION	RESET STATE	STANDBY STATE	OUTPUT DRIVE
L12	L11	D0	Data Bus	LOW	LOW	12 mA
M15	L13	D1				
N13	L14	D2				
L16	K11	D3				
L15	L16	D4				
L14	K14	D5				
H11	J15	D6				
K12	J12	D7				
J15	J10	D8				
J13	H16	D9				
J10	H14	D10				
H15	H11	D11				
H13	G16	D12				
G15	G9	D13				
G11	G14	D14				
G12	G12	D15				
F15	F15	D16				
F12	E15	D17				
E14	D16	D18				
D16	F12	D19				
H10	E13	D20				
D14	D14	D21				
F10	E12	D22				
A16	B16	D23				
A14	D12	D24				
B13	A16	D25				
C13	B13	D26				
E12	B14	D27				
G10	C12	D28				
B12	A14	D29				
B11	B12	D30				
D11	A12	D31				
M16	M15	A0/nWE1	<ul style="list-style-type: none"> Asynchronous Address Bus Asynchronous Memory Write Byte Enable 1 	HIGH: nWE1	HIGH	12 mA
N14	M16	A1/nWE2	<ul style="list-style-type: none"> Asynchronous Address Bus Asynchronous Memory Write Byte Enable 2 	HIGH: nWE2	HIGH	12 mA

Table 1. Functional Pin List (Cont'd)

PBGA PIN	CABGA PIN	SIGNAL	DESCRIPTION	RESET STATE	STANDBY STATE	OUTPUT DRIVE
M13	L15	A2/SA0	<ul style="list-style-type: none"> Asynchronous Address Bus Synchronous Address Bus 	LOW	LOW	12 mA
K16	K12	A3/SA1		LOW	LOW	12 mA
K15	K13	A4/SA2		LOW	LOW	12 mA
K14	K16	A5/SA3		LOW	LOW	12 mA
J8	J13	A6/SA4		LOW	LOW	12 mA
J16	J11	A7/SA5		LOW	LOW	12 mA
J14	J16	A8/SA6		LOW	LOW	12 mA
J9	H15	A9/SA7		LOW	LOW	12 mA
H16	H10	A10/SA8		LOW	LOW	12 mA
H14	H12	A11/SA9		LOW	LOW	12 mA
G16	G15	A12/SA10		LOW	LOW	12 mA
G14	G10	A13/SA11		LOW	LOW	12 mA
G13	G11	A14/SA12		LOW	LOW	12 mA
F16	F16	A15/SA13		LOW	LOW	12 mA
F14	E16	A16/SB0	<ul style="list-style-type: none"> Asynchronous Address Bus Synchronous Device Bank Address 0 	LOW	LOW	12 mA
E16	F13	A17/SB1	<ul style="list-style-type: none"> Asynchronous Address Bus Synchronous Device Bank Address 1 	LOW	LOW	12 mA
E13	E14	A18	Asynchronous Address Bus	LOW	LOW	12 mA
F11	D15	A19				
D15	C16	A20				
C16	C15	A21				
B16	C14	A22				
A15	B15	A23				
A13	E11	A24				
G8	D8	A25/SCIO	<ul style="list-style-type: none"> Asynchronous Memory Address Bus Smart Card Interface I/O (Data) 	LOW: A25	LOW	12 mA
F8	B7	A26/SCCLK	<ul style="list-style-type: none"> Asynchronous Memory Address Bus Smart Card Interface Clock 	LOW: A26	LOW	12 mA
A8	A7	A27/SCRST	<ul style="list-style-type: none"> Asynchronous Memory Address Bus Smart Card Interface Reset 	LOW: A27	LOW	12 mA
D8	C8	nOE	Asynchronous Memory Output Enable	HIGH	HIGH	12 mA
C8	F8	nWE0	Asynchronous Memory Write Byte Enable 0	HIGH	HIGH	12 mA
D10	D9	nWE3	Asynchronous Memory Write Byte Enable 3	HIGH	HIGH	8 mA
B10	E9	CS6/SCKE1_2	<ul style="list-style-type: none"> Asynchronous Memory Chip Select 6 Synchronous Memory Clock Enable 1 OR 2 	LOW: CS6	LOW	12 mA
C10	A10	CS7/SCKE0	<ul style="list-style-type: none"> Asynchronous Memory Chip Select 7 Synchronous Memory Clock Enable 0 	LOW: CS7	LOW	12 mA
G9	A11	SCKE3	Synchronous Memory Clock Enable 3	LOW	LOW	12 mA
A10	B10	SCLK	Synchronous Memory Clock	LOW	LOW	20 mA (sink) 12 mA (source)
C14	C13	nSCS0	Synchronous Memory Chip Select 0	HIGH	HIGH	12 mA
D13	A15	nSCS1	Synchronous Memory Chip Select 1	HIGH	HIGH	12 mA
E11	D11	nSCS2	Synchronous Memory Chip Select 2	HIGH	HIGH	12 mA
A12	E10	nSCS3	Synchronous Memory Chip Select 3	HIGH	HIGH	12 mA
C12	A13	nSWE	Synchronous Memory Write Enable	HIGH	HIGH	12 mA
C11	B11	nCAS	Synchronous Memory Column Address Strobe Signal	HIGH	HIGH	12 mA

Table 1. Functional Pin List (Cont'd)

PBGA PIN	CABGA PIN	SIGNAL	DESCRIPTION	RESET STATE	STANDBY STATE	OUTPUT DRIVE
F9	C11	nRAS	Synchronous Memory Row Address Strobe Signal	HIGH	HIGH	12 mA
A9	C9	DQM0	Synchronous Memory Data Mask 0	HIGH	HIGH	12 mA
B9	A9	DQM1	Synchronous Memory Data Mask 1	HIGH	HIGH	12 mA
D9	B9	DQM2	Synchronous Memory Data Mask 2	HIGH	HIGH	12 mA
E9	A8	DQM3	Synchronous Memory Data Mask 3	HIGH	HIGH	12 mA
J5	K1	PA0/LCDVD16	<ul style="list-style-type: none"> GPIO Port A LCD Data bit 16. This CLCDC output signal is always LOW. 	Input: PA0	No Change	8 mA
K1	K2	PA1/LCDVD17	<ul style="list-style-type: none"> GPIO Port A LCD Data bit 17. This CLCDC output signal is always LOW. 	Input: PA1	No Change	8 mA
K2	K3	PA2	GPIO Port A	Input	No Change	8 mA
K3	K4	PA3				
K5	K6	PA4				
L1	K5	PA5				
L2	L1	PA6				
L3	L2	PA7				
L4	L3	PB0/UARTRX1	<ul style="list-style-type: none"> GPIO Port B UART1 Receive Data Input 	Input: PB0	No Change	8 mA
L5	M1	PB1/UARTTX3	<ul style="list-style-type: none"> GPIO Port B UART3 Transmit Data Out 	Input: PB1	LOW if UART3 is Enabled, otherwise No Change	8 mA
L7	M2	PB2/UARTRX3	<ul style="list-style-type: none"> GPIO Port B UART3 Receive Data In 	Input: PB2	No Change	8 mA
M2	M3	PB3/UARTCTS3	<ul style="list-style-type: none"> GPIO Port B UART3 Clear to Send 	Input: PB3	No Change	8 mA
M4	L5	PB4/UARTDCD3	<ul style="list-style-type: none"> GPIO Port B UART3 Data Carrier Detect 	Input: PB4	No Change	8 mA
N1	N1	PB5/UARTDSR3	<ul style="list-style-type: none"> GPIO Port B UART3 Data Set Ready 	Input: PB5	No Change	8 mA
N2	N2	PB6/SWID/SMBD	<ul style="list-style-type: none"> GPIO Port B Single Wire Data Smart Battery Data 	Input: PB6	Input if SMB is Enabled, otherwise No Change	8 mA
N3	M4	PB7/SMBCLK	<ul style="list-style-type: none"> GPIO Port B Smart Battery Clock 	Input: PB7	Input if SMB is Enabled, otherwise No Change	8 mA
P1	P1	PC0/UARTTX1	<ul style="list-style-type: none"> GPIO Port C UART1 Transmit Data Output 	LOW: PC0	No Change	12 mA
P2	P2	PC1/LCDPS	<ul style="list-style-type: none"> GPIO Port C HR-TFT Power Save 	LOW: PC1	No Change	12 mA
R1	R1	PC2/LCDVDDEN	<ul style="list-style-type: none"> GPIO Port C HR-TFT Power Sequence Control 	LOW: PC2	No Change	12 mA
K6	M5	PC3/LCDREV	<ul style="list-style-type: none"> GPIO Port C HR-TFT Gray Scale Voltage Reverse 	LOW: PC3	No Change	12 mA
L8	P3	PC4/LCDSPS	<ul style="list-style-type: none"> GPIO Port C HR-TFT Reset Row Driver Counter 	LOW: PC4	No Change	12 mA
T1	N4	PC5/LCDCLS	<ul style="list-style-type: none"> GPIO Port C HR-TFT Row Driver Clock 	LOW: PC5	No Change	12 mA

Table 1. Functional Pin List (Cont'd)

PBGA PIN	CABGA PIN	SIGNAL	DESCRIPTION	RESET STATE	STANDBY STATE	OUTPUT DRIVE
T2	R2	PC6/LCDHRLP	<ul style="list-style-type: none"> • GPIO Port C • LCD Latch Pulse 	LOW: PC6	No Change	12 mA
R2	N5	PC7/LCDSPL	<ul style="list-style-type: none"> • GPIO Port C • LCD Start Pulse Left 	LOW: PC7	No Change	12 mA
M11	M9	PD0/LCDVD8	<ul style="list-style-type: none"> • GPIO Port D • LCD Video Data Bus 	LOW: PD0	LOW if Dual-Panel LCD is Enabled; otherwise, No Change	12 mA
L11	K10	PD1/LCDVD9		LOW: PD1		
K8	P10	PD2/LCDVD10		LOW: PD2		
N11	T11	PD3/LCDVD11		LOW: PD3		
R9	T12	PD4/LCDVD12		LOW: PD4		
T9	R11	PD5/LCDVD13		LOW: PD5		
P10	R12	PD6/LCDVD14		LOW: PD6		
R10	T13	PD7/LCDVD15		LOW: PD7		
L10	T9	PE0/LCDVD4	<ul style="list-style-type: none"> • GPIO Port E • LCD Video Data Bus 	Input: PE0	LOW if 8-bit LCD is Enabled, otherwise No Change	12 mA
N10	K9	PE1/LCDVD5		Input: PE1		
M9	T10	PE2/LCDVD6		Input: PE2		
M10	R10	PE3/LCDVD7		Input: PE3		
A6	A5	PF0/INT0	<ul style="list-style-type: none"> • GPIO Port F • External FIQ Interrupt. Interrupts can be level or edge triggered and are internally debounced. 	Input: PF0 (Schmitt)	No Change	8 mA
B6	B4	PF1/INT1	<ul style="list-style-type: none"> • GPIO Port F • External IRQ Interrupts. Interrupts can be level or edge triggered and are internally debounced. 	Input: PF1 (Schmitt)	No Change	8 mA
C6	E7	PF2/INT2		Input: PF2 (Schmitt)	No Change	8 mA
H8	B3	PF3/INT3	<ul style="list-style-type: none"> • GPIO Port F • External IRQ Interrupt. Interrupts can be level or edge triggered and are internally debounced. 	Input: PF3 (Schmitt)	No Change	8 mA
B5	C5	PF4/INT4/SCVCCEN	<ul style="list-style-type: none"> • GPIO Port F • External IRQ Interrupt. Interrupts can be level or edge triggered and are internally debounced. • Smart Card Supply Voltage Enable 	Input: PF4 (Schmitt)	LOW if SCI is Enabled; otherwise, No Change	8 mA
D6	D6	PF5/INT5/SCDETECT	<ul style="list-style-type: none"> • GPIO Port F • External IRQ Interrupt. Interrupts can be level or edge triggered and are internally debounced. • Smart Card Detection 	Input: PF5 (Schmitt)	No Change	8 mA
E6	A4	PF6/INT6/PCRDY1	<ul style="list-style-type: none"> • GPIO Port F • External IRQ Interrupt. Interrupts can be level or edge triggered and are internally debounced. • Ready for Card 1 for PC Card (PCMCIA or CompactFlash) in single or dual card mode 	Input: PF6 (Schmitt)	No Change	8 mA
C5	A3	PF7/INT7/PCRDY2	<ul style="list-style-type: none"> • GPIO Port F • External IRQ Interrupt. Interrupts can be level or edge triggered and are internally debounced. • Ready for Card 2 for PC Card (PCMCIA or CompactFlash) in single or dual card mode 	Input: PF7 (Schmitt)	No Change	8 mA
R3	M6	PG0/nPCOE	<ul style="list-style-type: none"> • GPIO Port G • Output Enable for PC Card (PCMCIA or CompactFlash) in single or dual card mode 	LOW: PG0	No Change	8 mA
T3	T1	PG1/nPCWE	<ul style="list-style-type: none"> • GPIO Port G • Write Enable for PC Card (PCMCIA or CompactFlash) in single or dual card mode 	LOW: PG1	No Change	8 mA

Table 1. Functional Pin List (Cont'd)

PBGA PIN	CABGA PIN	SIGNAL	DESCRIPTION	RESET STATE	STANDBY STATE	OUTPUT DRIVE
L6	P4	PG2/nPCIOR	<ul style="list-style-type: none"> GPIO Port G I/O Read Strobe for PC Card (PCMCIA or CompactFlash) in single or dual card mode 	LOW: PG2	No Change	8 mA
M6	R3	PG3/nPCIOW	<ul style="list-style-type: none"> GPIO Port G I/O Write Strobe for PC Card (PCMCIA or CompactFlash) in single or dual card mode 	LOW: PG3	No Change	8 mA
N6	T2	PG4/nPCREG	<ul style="list-style-type: none"> GPIO Port G Register Memory Access for PC Card (PCMCIA or CompactFlash) in single or dual card mode 	LOW: PG4	No Change	8 mA
M7	P5	PG5/nPCCE1	<ul style="list-style-type: none"> GPIO Port G Card Enable 1 for PC Card (PCMCIA or CompactFlash) in single or dual card mode. This signal and nPCCE2 are used by the PC Card for decoding low and high byte accesses. 	LOW: PG5	No Change	8 mA
M8	R4	PG6/nPCCE2	<ul style="list-style-type: none"> GPIO Port G Card Enable 2 for PC Card (PCMCIA or CompactFlash) in single or dual card mode. This signal and nPCCE1 are used by the PC Card for decoding low and high byte accesses. 	LOW: PG6	No Change	8 mA
N4	T3	PG7/PCDIR	<ul style="list-style-type: none"> GPIO Port G Direction for PC Card (PCMCIA or CompactFlash) in single or dual card mode 	LOW: PG7	No Change	8 mA
P4	P6	PH0/ PCRESET1	<ul style="list-style-type: none"> GPIO Port H Reset Card 1 for PC Card (PCMCIA or CompactFlash) in single or dual card mode 	Input: PH0	No Change	8 mA
R4	T4	PH1/CFA8/ PCRESET2	<ul style="list-style-type: none"> GPIO Port H Address Bit 8 for PC Card (CompactFlash) in single card mode Reset Card 2 for PC Card (PCMCIA or CompactFlash) in dual card mode 	Input: PH1	No Change	8 mA
T4	M7	PH2/ nPCSLOTE1	<ul style="list-style-type: none"> GPIO Port H Enable Card 1 for PC Card (PCMCIA or CompactFlash) in single or dual card mode. This signal is used for gating other control signals to the appropriate PC Card. 	Input: PH2	No Change	8 mA
N7	T5	PH3/CFA9/ PCMCIAA25/ nPCSLOTE2	<ul style="list-style-type: none"> GPIO Port H Address Bit 9 for PC Card (CompactFlash) in single card mode Address Bit 25 for PC Card (PCMCIA) in single card mode Enable Card 2 for PC Card (PCMCIA or CompactFlash) in dual card mode. This signal is used for gating other control signals to the appropriate PC Card. 	Input: PH3	No Change	8 mA
P8	R6	PH4/ nPCWAIT1	<ul style="list-style-type: none"> GPIO Port H WAIT Signal for Card 1 for PC Card (PCMCIA or CompactFlash) in single or dual card mode 	Input: PH4	No Change	8 mA
P5	R7	PH5/CFA10/ PCMCIAA24/ nPCWAIT2	<ul style="list-style-type: none"> GPIO Port H Address Bit 10 for PC Card (CompactFlash) in single card mode Address Bit 24 for PC Card (PCMCIA) in single card mode WAIT Signal for Card 2 for PC Card (PCMCIA or CompactFlash) in dual card mode 	Input: PH5	No Change	8 mA

Table 1. Functional Pin List (Cont'd)

PBGA PIN	CABGA PIN	SIGNAL	DESCRIPTION	RESET STATE	STANDBY STATE	OUTPUT DRIVE
R5	P7	PH6/ AC97RESET	<ul style="list-style-type: none"> • GPIO Port H • Audio Codec (AC97) Reset 	Input: PH6	No Change	8 mA
T5	T6	PH7/nPC- STATRE	<ul style="list-style-type: none"> • GPIO Port H • Status Read Enable for PC Card (PCMCIA or CompactFlash) in single or dual card mode 	Input: PH7	No Change	8 mA
R6	T7	LCDFP	LCD Frame Synchronization pulse	LOW	LOW	12 mA
R8	R9	LCDLP	LCD Line Synchronization pulse	LOW	LOW	12 mA
P9	P9	LCDENAB/ LCDM	<ul style="list-style-type: none"> • LCD TFT Data Enable • LCD STN AC Bias 	LOW: LCDENAB	LOW	12 mA
N9	N9	LCDDCLK	LCD Data Clock	LOW	LOW	12 mA
P7	M8	LCDVD0	LCD Video Data Bus	LOW	LOW	12 mA
R7	P8	LCDVD1				
T7	R8	LCDVD2				
N8	T8	LCDVD3				
T15	T16	USBDP	USB Data Positive (Differential Pair)	Input	Input	75 mA (NOM.)
T16	R16	USBDN	USB Data Negative (Differential Pair)	Input	Input	75 mA (NOM.)
E7	C7	nPWME0	DC-DC Converter Pulse Width Modulator 0 Enable	Input	Input	
D7	A6	nPWME1	DC-DC Converter Pulse Width Modulator 1 Enable	Input	Input	
C7	B6	PWM0	DC-DC Converter Pulse Width Modulator 0 Output during normal operation and Polarity Selection input at reset	Input	Input	8 mA
B7	B5	PWM1	DC-DC Converter Pulse Width Modulator 1 Output during normal operation and Polarity Selection input at reset	Input	Input	8 mA
C4	A2	ACBITCLK	<ul style="list-style-type: none"> • Audio Codec (AC97) Clock • Audio Codec (ACI) Clock 	Input	Input	
D5	A1	ACOUT	<ul style="list-style-type: none"> • Audio Codec (AC97) Output • Audio Codec (ACI) Output 	LOW	LOW	8 mA
B4	B2	ACSYNC	<ul style="list-style-type: none"> • Audio Codec (AC97) Synchronization • Audio Codec (ACI) Synchronization 	LOW	LOW	8 mA
A4	E6	ACIN	<ul style="list-style-type: none"> • Audio Codec (AC97) Input • Audio Codec (ACI) Input 	Input	Input	
A3	C3	MMCCLK/ MMSPICLK	<ul style="list-style-type: none"> • MultiMediaCard Clock (20 MHz MAX.) • MultiMediaCard SPI Mode Clock 	LOW: MMCCLK	LOW	8 mA
B3	B1	MMCCMD/ MMSPIDIN	<ul style="list-style-type: none"> • MultiMediaCard Command • MultiMediaCard SPI Mode Data Input 	Input: MMCCMD	Input	8 mA
A2	D4	MMCDATA/ MMSPIDOUT	<ul style="list-style-type: none"> • MultiMediaCard Data • MultiMediaCard SPI Mode Data Output 	Input: MMCDATA	Input	8 mA
E2	E1	UARTCTS2	UART2 Clear to Send Signal. This pin is an output for JTAG boundary scan only.	Input	Input	
E3	F3	UARTDCD2	UART2 Data Carrier Detect Signal. This pin is output for JTAG boundary scan only.	Input	Input	
E5	G4	UARTDSR2	UART2 Data Set Ready Signal	Input	Input	
F2	G5	UARTIRTX1	IrDA Transmit	LOW	LOW	8 mA
F3	G6	UARTIRRX1	IrDA Receive. This pin is an output for JTAG boundary scan only.	Input	Input	
F4	F1	UARTTX2	UART2 Transmit Data Output	HIGH	HIGH	8 mA

Table 1. Functional Pin List (Cont'd)

PBGA PIN	CABGA PIN	SIGNAL	DESCRIPTION	RESET STATE	STANDBY STATE	OUTPUT DRIVE
J7	G3	UARTRX2	UART2 Receive Data Input. This pin is an output for JTAG boundary scan only.	Input	Input	
H4	J3	SSPCLK	Synchronous Serial Port Clock	LOW	LOW	8 mA
J1	J6	SSPRX	Synchronous Serial Port Receive	Input	Input	
J2	J7	SSPTX	Synchronous Serial Port Transmit	LOW	LOW	8 mA
J3	J2	SSPFRM/ nSSPFRM	Synchronous Serial Port Frame Sync	HIGH:	Output	8 mA
F6	G2	COL0	Keyboard Interface	HIGH	HIGH	8 mA
F5	G1	COL1				
G1	H3	COL2				
G2	H5	COL3				
G4	H6	COL4				
G5	H7	COL5				
H1	H2	COL6				
H2	H1	COL7				
H3	J1	TBUZ	Timer Buzzer (254 kHz MAX.)	LOW	LOW	8 mA
C3	F5	MEDCHG	Boot Device Media Change. Used with WIDTH0 and WIDTH1 to specify boot memory device.	Input (Schmitt)	Input	
P11	T14	WIDTH0	External Memory Width Pins. Also, used with MEDCHG to specify the boot memory device size. These pins have weak internal pull-up resistors.	Input (Schmitt) with pull-up	Input with pull-up	
R12	T15	WIDTH1				
D1	E3	BATOK	Battery OK	Input (Schmitt)	Input	
D2	F6	nBATCHG	Battery Change	Input (Schmitt)	Input	
A1	E5	TDI	JTAG Data In. This signal is internally pulled-up to VDD.	Input with Pull-up	Input with Pull-up	
B1	C2	TCK	JTAG Clock. This signal should be externally pulled-up to VDD.	Input	Input	
B2	D3	TDO	JTAG Data Out. This signal should be externally pulled up to VDD with a 33 k Ω resistor.	Input	No Change	4 mA
C1	C1	TMS	JTAG Test Mode select. This signal is internally pulled-up to VDD.	Input with Pull-up	Input with Pull-up	
T12	P15	nTEST0	Test Pin 0. Internally pulled up to VDD. For Normal mode, leave open. For JTAG mode, tie to GND. See Table 2.	Input with Pull-up	Input with Pull-up	
R15	P13	nTEST1	Test Pin 1. internally pulled up to VDD. For Normal and JTAG mode, leave open. See Table 2.	Input with Pull-up	Input with Pull-up	

NOTES: *Signals beginning with 'n' are Active LOW.

Table 2. nTest Pin Function

MODE	nTEST0	nTEST1	nURESET
JTAG	0	1	1
Normal	1	1	x

Table 3. LCD Data Multiplexing

PBGA PIN	CABGA PIN	LCD DATA SIGNAL	STN						TFT	AD-TFT/ HR-TFT	
			MONO 4-BIT		MONO 8-BIT		COLOR				
			SINGLE PANEL	DUAL PANEL	SINGLE PANEL	DUAL PANEL	SINGLE PANEL	DUAL PANEL			
K1	K2	LCDVD17									LOW
J5	K1	LCDVD16									LOW
R10	T13	LCDVD15				MLSTN7		CLSTN7	Intensity	Intensity	
P10	R12	LCDVD14				MLSTN6		CLSTN6	BLUE4	BLUE4	
T9	R11	LCDVD13				MLSTN5		CLSTN5	BLUE3	BLUE3	
R9	T12	LCDVD12				MLSTN4		CLSTN4	BLUE2	BLUE2	
N11	T11	LCDVD11				MLSTN3		CLSTN3	BLUE1	BLUE1	
K8	P10	LCDVD10				MLSTN2		CLSTN2	BLUE0	BLUE0	
L11	K10	LCDVD9				MLSTN1		CLSTN1	GREEN4	GREEN4	
M11	M9	LCDVD8				MLSTN0		CLSTN0	GREEN3	GREEN3	
M10	R10	LCDVD7		MLSTN3	MUSTN7	MUSTN7	CUSTN7	CUSTN7	GREEN2	GREEN2	
M9	T10	LCDVD6		MLSTN2	MUSTN6	MUSTN6	CUSTN6	CUSTN6	GREEN1	GREEN1	
N10	K9	LCDVD5		MLSTN1	MUSTN5	MUSTN5	CUSTN5	CUSTN5	GREEN0	GREEN0	
L10	T9	LCDVD4		MLSTN0	MUSTN4	MUSTN4	CUSTN4	CUSTN4	RED4	RED4	
N8	T8	LCDVD3	MUSTN3	MUSTN3	MUSTN3	MUSTN3	CUSTN3	CUSTN3	RED3	RED3	
T7	R8	LCDVD2	MUSTN2	MUSTN2	MUSTN2	MUSTN2	CUSTN2	CUSTN2	RED2	RED2	
R7	P8	LCDVD1	MUSTN1	MUSTN1	MUSTN1	MUSTN1	CUSTN1	CUSTN1	RED1	RED1	
P7	M8	LCDVD0	MUSTN0	MUSTN0	MUSTN0	MUSTN0	CUSTN0	CUSTN0	RED0	RED0	

NOTES:

1. The Intensity bit is identically generated for all three colors.
2. MU = Monochrome Upper
3. CU = Color Upper
4. CL = Color Lower

Table 4. 256-Ball PBGA Package Numerical Pin List

BGA PIN	SIGNAL	RESET STATE	STANDBY STATE
A1	TDI	Input with Pull-up	Input with Pull-up
A2	MMCDATA/MMSPIDOUT	Input: MMSPIDOUT	LOW
A3	MMCCLK/MMSPICK	LOW: MMSPICK	LOW
A4	ACIN	Input	Input
A5	VSS		
A6	PF0/INT0	Input: PF0	No Change
A7	VDDC		
A8	A27/SCRST	LOW: A27	LOW
A9	DQM0	HIGH	LOW
A10	SCLK	LOW	LOW
A11	VSS		
A12	nSCS3	HIGH	HIGH
A13	A24	LOW	LOW
A14	D24	LOW	LOW
A15	A23	LOW	LOW
A16	D23	LOW	LOW
B1	TCK	Input	Input
B2	TDO	Input	No Change
B3	MMCCMD/MMSPIDIN	Input: MMSPIDIN	LOW
B4	ACSYNC	LOW	LOW
B5	PF4/INT4/SCVCCEN	Input: PF4	LOW if SCI is Enabled; otherwise, No Change
B6	PF1/INT1	Input: PF1	No Change
B7	PWM1	Input	Input
B8	VDD		
B9	DQM1	HIGH	LOW
B10	CS6/SCKE1_2	LOW: CS6	LOW
B11	D30	LOW	LOW
B12	D29	LOW	LOW
B13	D25	LOW	LOW
B14	VDD		
B15	VSSC		
B16	A22	LOW	LOW
C1	TMS	Input with Pull-up	Input with Pull-up
C2	nEXTPWR	Input	Input
C3	MEDCHG	Input	Input
C4	ACBITCLK	Input	Input
C5	PF7/INT7/PCRDY2	Input: PF7	No Change
C6	PF2/INT2	PF2/INT2	No Change
C7	PWM0	Input	Input
C8	nWE0	HIGH	HIGH
C9	VSSC		
C10	CS7/SCKE0	LOW: CS7	LOW
C11	nCAS	HIGH	HIGH
C12	nSWE	HIGH	HIGH
C13	D26	LOW	LOW

Table 4. 256-Ball PBGA Package Numerical Pin List (Cont'd)

BGA PIN	SIGNAL	RESET STATE	STANDBY STATE
C14	nSCS0	HIGH	HIGH
C15	VSS		
C16	A21	LOW	LOW
D1	BATOK	Input	Input
D2	nBATCHG	Input	Input
D3	nPOR	Input	Input
D4	WAKEUP	Input	Input
D5	ACOUT	LOW	LOW
D6	PF5/INT5/SCDETECT	Input: PF5	No Change
D7	nPWME1	Input	Input
D8	nOE	HIGH	HIGH
D9	DQM2	HIGH	LOW
D10	nWE3	HIGH	HIGH
D11	D31	LOW	LOW
D12	VDDC		
D13	nSCS1	HIGH	HIGH
D14	D21	LOW	LOW
D15	A20	LOW	LOW
D16	D19	LOW	LOW
E1	VDDC		
E2	UARTCTS2	Input	Input
E3	UARTDCD2	Input	Input
E4	nPWRFL	Input	Input
E5	UARTDSR2	Input	Input
E6	PF6/INT6/PCRDY1	Input: PF6	No Change
E7	nPWME0	Input	Input
E8	VSS		
E9	DQM3	HIGH	LOW
E10	VDD		
E11	nSCS2	HIGH	HIGH
E12	D27	LOW	LOW
E13	A18	LOW	LOW
E14	D18	LOW	LOW
E15	VDDC		
E16	A17/SB1	LOW: SBANK1	LOW
F1	VDD		
F2	UARTIRTX1	LOW	LOW
F3	UARTIRRX1	Input	Input
F4	UARTTX2	HIGH	HIGH
F5	COL1	HIGH	HIGH
F6	COL0	HIGH	HIGH
F7	VSS		
F8	A26/SCCLK	LOW: A26	LOW
F9	nRAS	HIGH	HIGH
F10	D22	LOW	LOW

Table 4. 256-Ball PBGA Package Numerical Pin List (Cont'd)

BGA PIN	SIGNAL	RESET STATE	STANDBY STATE
F11	A19	LOW	LOW
F12	D17	LOW	LOW
F13	VDD		
F14	A16/SB0	LOW: SBANK0	LOW
F15	D16	LOW	LOW
F16	A15/SA13	LOW: SA13	LOW
G1	COL2	HIGH	HIGH
G2	COL3	HIGH	HIGH
G3	VSS		
G4	COL4	HIGH	HIGH
G5	COL5	HIGH	HIGH
G6	VSSC		
G7	VDD		
G8	A25/SCIO	LOW: A25	LOW
G9	SCKE3	LOW	LOW
G10	D28	LOW	LOW
G11	D14	LOW	LOW
G12	D15	LOW	LOW
G13	A14/SA12	LOW: SA12	LOW
G14	A13/SA11	LOW: SA11	LOW
G15	D13	LOW	LOW
G16	A12/SA10	LOW: SA10	LOW
H1	COL6	HIGH	HIGH
H2	COL7	HIGH	HIGH
H3	TBUZ	LOW	LOW
H4	SSPCLK	LOW	LOW
H5	VSSC		
H6	nURESET	Input	Input
H7	VSS		
H8	PF3/INT3	Input: PF3	No Change
H9	VSS		
H10	D20	LOW	LOW
H11	D6	LOW	LOW
H12	VSSC		
H13	D12	LOW	LOW
H14	A11/SA9	LOW: SA9	LOW
H15	D11	LOW	LOW
H16	A10/SA8	LOW: SA8	LOW
J1	SSPRX	Input	Input
J2	SSPTX	LOW	LOW
J3	SSPFRM/nSSPFRM	Input: nSSPFRM	Input
J4	VDDC		
J5	PA0/LCDVD16	Input: PA0	No Change
J6	PGMCLK	LOW	LOW
J7	UARTRX2	Input	Input

Table 4. 256-Ball PBGA Package Numerical Pin List (Cont'd)

BGA PIN	SIGNAL	RESET STATE	STANDBY STATE
J8	A6/SA4	LOW: SA4	LOW
J9	A9/SA7	LOW: SA7	LOW
J10	D10	LOW	LOW
J11	VDD		
J12	VDD		
J13	D9	LOW	LOW
J14	A8/SA6	LOW: SA6	LOW
J15	D8	LOW	LOW
J16	A7/SA5	LOW: SA5	LOW
K1	PA1/LCDVD17	Input: PA1	No Change
K2	PA2	Input	No Change
K3	PA3	Input	No Change
K4	VSS		
K5	PA4	Input	No Change
K6	PC3/LCDREV	LOW: PC3	No Change
K7	VDD		
K8	PD2/LCDVD10	LOW: PD2	LOW if Dual-Panel LCD is Enabled; otherwise, No Change
K9	VDDC		
K10	nCS1	HIGH	HIGH
K11	nCS0	HIGH	HIGH
K12	D7	LOW	LOW
K13	VSS		
K14	A5/SA3	LOW: SA3	LOW
K15	A4/SA2	LOW: SA2	LOW
K16	A3/SA1	LOW: SA1	LOW
L1	PA5	Input	No Change
L2	PA6	Input	No Change
L3	PA7	Input	No Change
L4	PB0/UARTX1	Input: PB0	No Change
L5	PB1/UARTX3	Input: PB1	LOW if UART3 is Enabled, otherwise No Change
L6	PG2/nPCIOR	LOW: PG2	No Change
L7	PB2/UARTX3	Input: PB2	No Change
L8	PC4/LCDSPS	LOW: PC4	No Change
L9	VSSC		
L10	PE0/LCDVD4	Input: PE0	LOW if 8-bit LCD is Enabled, otherwise No Change
L11	PD1/LCDVD9	LOW: PD1	LOW if Dual-Panel LCD is Enabled; otherwise, No Change
L12	D0	LOW	LOW
L13	VDDC		
L14	D5	LOW	LOW
L15	D4	LOW	LOW
L16	D3	LOW	LOW
M1	VDD		
M2	PB3/UARTCTS3	Input: PB3	No Change
M3	VSSC		

Table 4. 256-Ball PBGA Package Numerical Pin List (Cont'd)

BGA PIN	SIGNAL	RESET STATE	STANDBY STATE
M4	PB4/UARTDCD3	Input: PB4	No Change
M5	VDD		
M6	PG3/nPCIOW	LOW: PG3	No Change
M7	PG5/nPCCE1	LOW: PG5	No Change
M8	PG6/nPCCE2	LOW: PG6	No Change
M9	PE2/LCDVD6	Input: PE2	LOW if 8-bit LCD is Enabled; otherwise No Change
M10	PE3/LCDVD7	Input: PE3	LOW if 8-bit LCD is Enabled; otherwise No Change
M11	PD0/LCDVD8	LOW: PD0	LOW if Dual-Panel LCD is Enabled; otherwise, No Change
M12	nCS3/nMMSPICS	HIGH: nCS3	HIGH
M13	A2/SA0	LOW: SA0	LOW
M14	VDD		
M15	D1	LOW	LOW
M16	A0/nWE1	HIGH: nWE1	HIGH
N1	PB5/UARTDSR3	Input: PB5	No Change
N2	PB6/SWID/SMBD	Input: PB6	Input if SMB is Enabled; otherwise No Change
N3	PB7/SMBCLK	Input: PB7	Input if SMB is Enabled; otherwise No Change
N4	PG7/PCDIR	LOW: PG7	No Change
N5	VSS		
N6	PG4/nPCREG	LOW: PG4	No Change
N7	PH3/CFA9/PCMCIAA25/nPCSLOTE2	Input: PH3	No Change
N8	LCDVD3	LOW	LOW
N9	LCDDCLK	LOW	LOW
N10	PE1/LCDVD5	Input: PE1	LOW if 8-bit LCD is Enabled; otherwise No Change
N11	PD3/LCDVD11	LOW: PD3	LOW if Dual-Panel LCD is Enabled; otherwise, No Change
N12	VDDA		
N13	D2	LOW	LOW
N14	A1/nWE2	HIGH: nWE2	HIGH
N15	VSSC		
N16	VSS		
P1	PC0/UARTTX1	LOW: PC0	No Change
P2	PC1/LCDPS	LOW: PC1	No Change
P3	VDDC		
P4	PH0/PCRESET1	Input: PH0	No Change
P5	PH5/CFA10/PCMCIAA24/nPCWAIT2	Input: PH5	No Change
P6	VSS		
P7	LCDVD0	LOW	LOW
P8	PH4/nPCWAIT1	Input: PH4	No Change
P9	LCDENAB/LCDM	LOW: LCDENAB	LOW
P10	PD6/LCDVD14	LOW: PD6	LOW if Dual-Panel LCD is Enabled; otherwise, No Change
P11	WIDTH0	Input	Input
P12	VSSA		
P13	nCS2	HIGH	HIGH
P14	CLKEN	LOW	LOW

Table 4. 256-Ball PBGA Package Numerical Pin List (Cont'd)

BGA PIN	SIGNAL	RESET STATE	STANDBY STATE
P15	XTAL32OUT	Output	Output
P16	XTAL32IN	Input	Input
R1	PC2/LCDVDDEN	LOW: PC2	No Change
R2	PC7/LCDSPL	LOW: PC7	No Change
R3	PG0/nPCOE	LOW: PG0	No Change
R4	PH1/CFA8/PCRESET2	Input: PH1	No Change
R5	PH6/nAC97/RESET	Input: PH6	No Change
R6	LCDFP	LOW	LOW
R7	LCDVD1	LOW	LOW
R8	LCDLP	LOW	LOW
R9	PD4/LCDVD12	LOW: PD4	LOW if Dual-Panel LCD is Enabled; otherwise, No Change
R10	PD7/LCDVD15	LOW: PD7	LOW if Dual-Panel LCD is Enabled; otherwise, No Change
R11	VDDA		
R12	WIDTH1	Input	Input
R13	XTALIN	Input	Input
R14	VDD		
R15	nTEST1	Input with Pull-up	Input with Pull-up
R16	VSS		
T1	PC5/LCDCLS	LOW: PC5	No Change
T2	PC6/LCDHRLP	LOW: PC6	No Change
T3	PG1/nPCWE	LOW: PG1	No Change
T4	PH2/nPCSLOTE1	Input: PH2	No Change
T5	PH7/nPCSTATRE	Input: PH7	No Change
T6	VDD		
T7	LCDVD2	LOW	LOW
T8	VDDC		
T9	PD5/LCDVD13	LOW: PD5	LOW if Dual-Panel LCD is Enabled; otherwise, No Change
T10	VSSC		
T11	VSSA		
T12	nTEST0	Input with Pull-up	Input with Pull-up
T13	XTALOUT	LOW	LOW
T14	VSS		
T15	USBDP	HIGH	HIGH
T16	USBDN	LOW	LOW

NOTE: 'No Change' means the pin remains as it was programmed prior to entering the Standby state.

Table 5. 256-Ball CABGA Package Numerical Pin List

CABGA PIN	SIGNAL	RESET STATE	STANDBY STATE
A1	ACOUT	LOW	LOW
A2	ACBITCLK	Input	Input
A3	PF7/INT7/PCRDY2	Input: PF7 (Schmitt)	No Change
A4	PF6/INT6/PCRDY1	Input: PF6 (Schmitt)	No Change
A5	PF0/INT0	Input: PF0 (Schmitt)	No Change
A6	nPWME1	Input	Input
A7	A27/SCRST	LOW: A27	LOW
A8	DQM3	HIGH	HIGH
A9	DQM1	HIGH	HIGH
A10	CS7/SCKE0	LOW: CS7	LOW
A11	SCKE3	LOW	LOW
A12	D31	LOW	LOW
A13	nSWE	HIGH	HIGH
A14	D29	LOW	LOW
A15	nSCS1	HIGH	HIGH
A16	D25	LOW	LOW
B1	MMCCMD/MMSPIDIN	Input: MMCCMD	Input
B2	ACSYNC	LOW	LOW
B3	PF3/INT3	Input: PF3 (Schmitt)	No Change
B4	PF1/INT1	Input: PF1 (Schmitt)	No Change
B5	PWM1	Input	Input
B6	PWM0	Input	Input
B7	A26/SCCLK	LOW: A26	LOW
B8	VSS		
B9	DQM2	HIGH	HIGH
B10	SCLK	LOW	LOW
B11	nCAS	HIGH	HIGH
B12	D30	LOW	LOW
B13	D26	LOW	LOW
B14	D27	LOW	LOW
B15	A23	LOW	LOW
B16	D23	LOW	LOW
C1	TMS	Input with Pull-up	Input with Pull-up
C2	TCK	Input	Input
C3	MMCCLK/MMSPICLK	LOW: MMCCLK	LOW
C4	VDDC		
C5	PF4/INT4/SCVCCEN	Input: PF4 (Schmitt)	LOW if SCI is Enabled; otherwise, No Change
C6	VSS		
C7	nPWME0	Input	Input
C8	nOE	HIGH	HIGH
C9	DQM0	HIGH	HIGH
C10	VDD		
C11	nRAS	HIGH	HIGH

Table 5. 256-Ball CABGA Package Numerical Pin List

CABGA PIN	SIGNAL	RESET STATE	STANDBY STATE
C12	D28	LOW	LOW
C13	nSCS0	HIGH	HIGH
C14	A22	LOW	LOW
C15	A21	LOW	LOW
C16	A20	LOW	LOW
D1	nURESET	Input (Schmitt)	Input
D2	nEXTPWR	Input (Schmitt)	Input
D3	TDO	Input	No Change
D4	MMCDATA/MMSPIDOUT	Input: MMCDATA	Input
D5	VSS		
D6	PF5/INT5/SCDETECT	Input: PF5 (Schmitt)	No Change
D7	VDDC		
D8	A25/SCIO	LOW: A25	LOW
D9	nWE3	HIGH	HIGH
D10	VDDC		
D11	nSCS2	HIGH	HIGH
D12	D24	LOW	LOW
D13	VSS		
D14	D21	LOW	LOW
D15	A19	LOW	LOW
D16	D18	LOW	LOW
E1	UARTCTS2	Input	Input
E2	WAKEUP	Input (Schmitt)	Input
E3	BATOK	Input (Schmitt)	Input
E4	nPOR	Input	Input
E5	TDI	Input with Pull-up	Input with Pull-up
E6	ACIN	Input	Input
E7	PF2/INT2	Input: PF2 (Schmitt)	No Change
E8	VSS		
E9	CS6/SCKE1_2	LOW: CS6	LOW
E10	nSCS3	HIGH	HIGH
E11	A24	LOW	LOW
E12	D22	LOW	LOW
E13	D20	LOW	LOW
E14	A18	LOW	LOW
E15	D17	LOW	LOW
E16	A16/SB0	LOW	LOW
F1	UARTTX2	HIGH	HIGH
F2	nPWRFL	Input (Schmitt)	Input
F3	UARTDCD2	Input	Input
F4	VDDC		
F5	MEDCHG	Input (Schmitt)	Input
F6	nBATCHG	Input (Schmitt)	Input

Table 5. 256-Ball CABGA Package Numerical Pin List

CABGA PIN	SIGNAL	RESET STATE	STANDBY STATE
F7	VSS		
F8	nWE0	HIGH	HIGH
F9	VDD		
F10	VDDC		
F11	VDD		
F12	D19	LOW	LOW
F13	A17/SB1	LOW	LOW
F14	VDD		
F15	D16	LOW	LOW
F16	A15/SA13	LOW	LOW
G1	COL1	HIGH	HIGH
G2	COL0	HIGH	HIGH
G3	UARTRX2	Input	Input
G4	UARTDSR2	Input	Input
G5	UARTIRTX1	LOW	LOW
G6	UARTIRRX1	Input	Input
G7	VSSC		
G8	VDD		
G9	D13	LOW	LOW
G10	A13/SA11	LOW	LOW
G11	A14/SA12	LOW	LOW
G12	D15	LOW	LOW
G13	VSS		
G14	D14	LOW	LOW
G15	A12/SA10	LOW	LOW
G16	D12	LOW	LOW
H1	COL7	HIGH	HIGH
H2	COL6	HIGH	HIGH
H3	COL2	HIGH	HIGH
H4	VSSC		
H5	COL3	HIGH	HIGH
H6	COL4	HIGH	HIGH
H7	COL5	HIGH	HIGH
H8	VSSC		
H9	VSS		
H10	A10/SA8	LOW	LOW
H11	D11	LOW	LOW
H12	A11/SA9	LOW	LOW
H13	VDD		
H14	D10	LOW	LOW
H15	A9/SA7	LOW	LOW
H16	D9	LOW	LOW
J1	TBUZ	LOW	LOW

Table 5. 256-Ball CABGA Package Numerical Pin List

CABGA PIN	SIGNAL	RESET STATE	STANDBY STATE
J2	SSPFRM/nSSPFRM	Input: nSSPFRM	Input
J3	SSPCLK	LOW	LOW
J4	VDDC		
J5	PGMCLK	LOW	LOW
J6	SSPRX	Input	Input
J7	SSPTX	LOW	LOW
J8	VDDC		
J9	VDD		
J10	D8	LOW	LOW
J11	A7/SA5	LOW	LOW
J12	D7	LOW	LOW
J13	A6/SA4	LOW	LOW
J14	VSS		
J15	D6	LOW	LOW
J16	A8/SA6	LOW	LOW
K1	PA0/LCDVD16	Input: PA0	No Change
K2	PA1/LCDVD17	Input: PA1	No Change
K3	PA2	Input	No Change
K4	PA3	Input	No Change
K5	PA5	Input	No Change
K6	PA4	Input	No Change
K7	VSS		
K8	VDDC		
K9	PE1/LCDVD5	Input: PE1	
K10	PD1/LCDVD9	LOW: PD1	
K11	D3	LOW	LOW
K12	A3/SA1	LOW	LOW
K13	A4/SA2	LOW	LOW
K14	D5	LOW	LOW
K15	VDD		
K16	A5/SA3	LOW	LOW
L1	PA6	Input	No Change
L2	PA7	Input	No Change
L3	PB0/UARTRX1	Input: PB0	No Change
L4	VSSC		
L5	PB4/UARTDCD3	Input: PB4	No Change
L6	VDDC		
L7	VDD		
L8	VSS		
L9	VSSC		
L10	VSS		
L11	D0	LOW	LOW
L12	VSS		

Table 5. 256-Ball CABGA Package Numerical Pin List

CABGA PIN	SIGNAL	RESET STATE	STANDBY STATE
L13	D1	LOW	LOW
L14	D2	LOW	LOW
L15	A2/SA0	LOW	LOW
L16	D4	LOW	LOW
M1	PB1/UARTTX3	Input: PB1	LOW if UART3 is Enabled, otherwise No Change
M2	PB2/UARTRX3	Input: PB2	No Change
M3	PB3/UARTCTS3	Input: PB3	No Change
M4	PB7/SMBCLK	Input: PB7	Input if SMB is Enabled, otherwise No Change
M5	PC3/LCDREV	LOW: PC3	No Change
M6	PG0/nPCOE	LOW: PG0	No Change
M7	PH2/nPCSLOTE1	Input: PH2	No Change
M8	LCDVD0	LOW	LOW
M9	PD0/LCDVD8	LOW: PD0	LOW if Dual-Panel LCD is Enabled; otherwise, No Change
M10	VDDA		
M11	VSS		
M12	CLKEN	LOW	LOW
M13	XTAL32OUT	Output	Output
M14	VSS		
M15	A0/nWE1	HIGH: nWE1	HIGH
M16	A1/nWE2	HIGH: nWE2	HIGH
N1	PB5/UARTDSR3	Input: PB5	No Change
N2	PB6/SWID/SMBD	Input: PB6	Input if SMB is Enabled, otherwise No Change
N3	VSSC		
N4	PC5/LCDCLS	LOW: PC5	No Change
N5	PC7/LCDSPL	LOW: PC7	No Change
N6	VDD		
N7	VSSC		
N8	VDD		
N9	LCDDCLK	LOW	LOW
N10	VSSC		
N11	VSSA		
N12	VDD		
N13	VDD		
N14	XTAL32IN	Input	Input
N15	nCS2	HIGH	HIGH
N16	nCS3/nMMSPICS	HIGH: nCS3	HIGH
P1	PC0/UARTTX1	LOW: PC0	No Change
P2	PC1/LCDPS	LOW: PC1	No Change
P3	PC4/LCDSPS	LOW: PC4	No Change
P4	PG2/nPCIOR	LOW: PG2	No Change
P5	PG5/nPCCE1	LOW: PG5	No Change
P6	PH0/PCRESET1	Input: PH0	No Change

Table 5. 256-Ball CABGA Package Numerical Pin List

CABGA PIN	SIGNAL	RESET STATE	STANDBY STATE
P7	PH6/AC97RESET	Input: PH6	No Change
P8	LCDVD1	LOW	LOW
P9	LCDENAB/LCDM	LOW: LCDENAB	LOW
P10	PD2/LCDVD10	LOW: PD2	No Change
P11	VDD		No Change
P12	VDDA		
P13	nTEST1	Input with Pull-up	Input with Pull-up
P14	nCS0	HIGH	HIGH
P15	nTEST0	Input with Pull-up	Input with Pull-up
P16	nCS1	HIGH	HIGH
R1	PC2/LCDVDDEN	LOW: PC2	No Change
R2	PC6/LCDHRLP	LOW: PC6	No Change
R3	PG3/nPCIOW	LOW: PG3	No Change
R4	PG6/nPCCE2	LOW: PG6	No Change
R5	VSSC		
R6	PH4/nPCWAIT1	Input: PH4	No Change
R7	PH5/CFA10/PCMCIAA24/nPCWAIT2	Input: PH5	No Change
R8	LCDVD2	LOW	LOW
R9	LCDLP	LOW	LOW
R10	PE3/LCDVD7	Input: PE3	No Change
R11	PD5/LCDVD13	LOW: PD5	No Change
R12	PD6/LCDVD14	LOW: PD6	No Change
R13	VSSA		
R14	XTALIN	Input	Input
R15	XTALOUT	LOW	LOW
R16	USBDN	Input	Input
T1	PG1/nPCWE	LOW: PG1	No Change
T2	PG4/nPCREG	LOW: PG4	No Change
T3	PG7/PCDIR	LOW: PG7	No Change
T4	PH1/CFA8/PCRESET2	Input: PH1	No Change
T5	PH3/CFA9/PCMCIAA25/nPCSLOTE2	Input: PH3	No Change
T6	PH7/nPCSTATRE	Input: PH7	No Change
T7	LCDFP	LOW	LOW
T8	LCDVD3	LOW	LOW
T9	PE0/LCDVD4	Input: PE0	LOW if 8-bit LCD is Enabled, otherwise No Change
T10	PE2/LCDVD6	Input: PE2	No Change
T11	PD3/LCDVD11	LOW: PD3	No Change
T12	PD4/LCDVD12	LOW: PD4	No Change
T13	PD7/LCDVD15	LOW: PD7	No Change
T14	WIDTH0	Input (Schmitt)	Input
T15	WIDTH1	Input (Schmitt)	Input
T16	USBDP	Input	Input

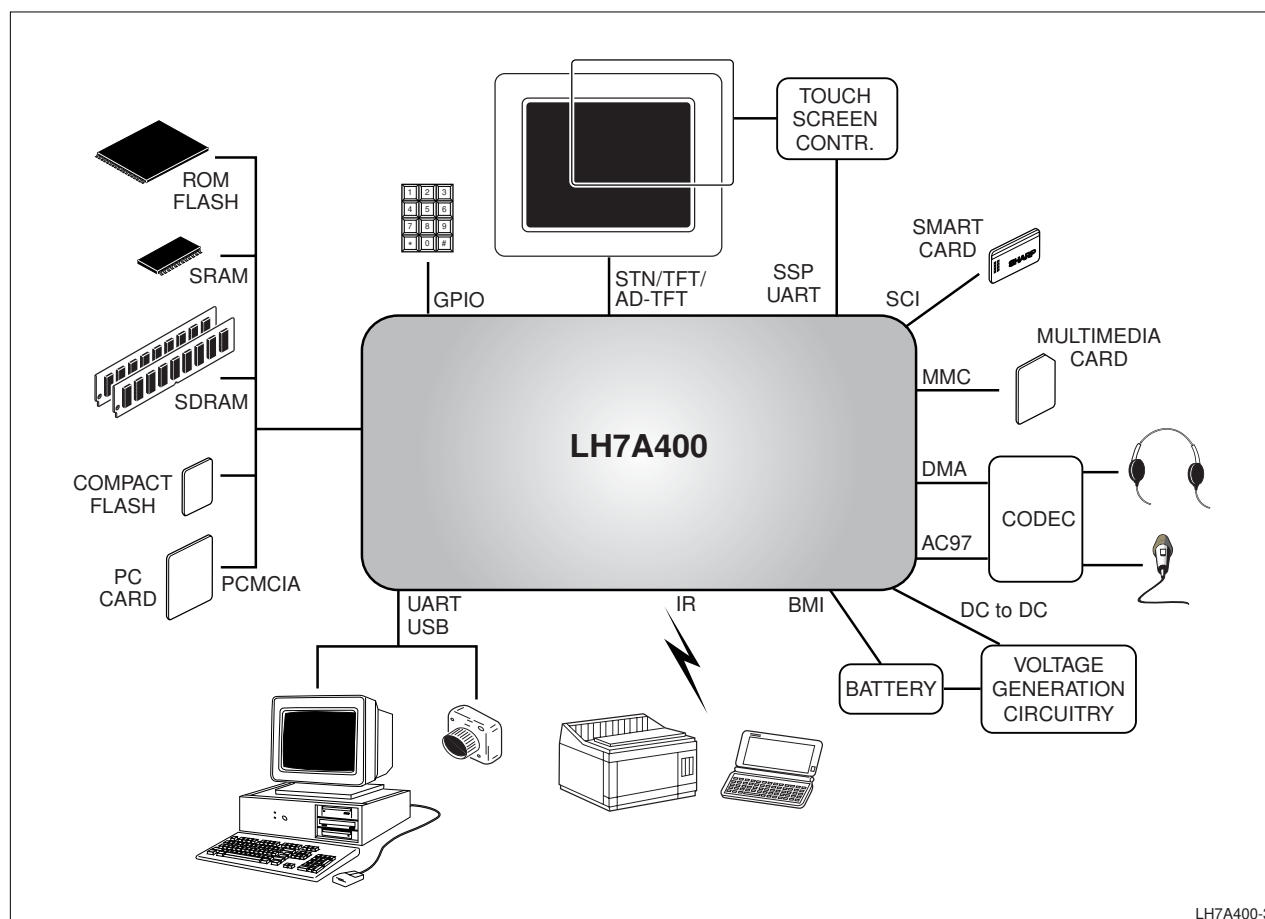


Figure 2. Application Diagram

SYSTEM DESCRIPTIONS

ARM922T Processor

The LH7A400 microcontroller features the ARM922T cached core with an Advanced High Performance Bus (AHB) interface. The processor is a member of the ARM9T family of processors. For more information, see the ARM document, 'ARM922T Technical Reference Manual', available on ARM's website at www.arm.com.

Clock and State Controller

The clocking scheme in the LH7A400 is based around two primary oscillator inputs. These are the 14.7456 MHz input crystal and the 32.768 kHz real time clock oscillator. See Figure 3. The 14.7456 MHz oscillator is used to generate the main system clock domains for the LH7A400, whereas the 32.768 kHz is used for controlling the power down operations and real time clock peripheral. The clock and state controller provides the clock gating and frequency division necessary, and then supplies the clocks to the processor and to the rest of the system. The amount of clock gating that actually takes place is dependent on the current power saving mode selected.

The 32.768 kHz clock provides the source for the Real Time Clock tree and power-down logic. This clock is used for the power state control in the design and is the only clock in the LH7A400 that runs permanently. The 32.768 kHz clock is divided down to 1 Hz using a ripple divider to save power. This generated 1 Hz clock is used in the Real Time Clock counter.

The 14.7456 MHz source is used to generate the main system clocks for the LH7A400. It is the source for PLL1 and PLL2, it acts as the primary clock to the peripherals and is the source clock to the Programmable clock (PGM) divider.

PLL1 provides the main clock tree for the chip, it generates the following clocks: FCLK, HCLK and PCLK. FCLK is the clock that drives the ARM922T core. HCLK is the main bus (AHB) clock, as such it clocks all memory interfaces, bus arbitrators and the AHB peripherals. HCLK is generated by dividing FCLK by 1, 2, 3, or 4. HCLK can be gated by the system to enable low power operation. PCLK is the peripheral bus (APB) clock. It is generated by dividing HCLK by either 2, 4, or 8.

PLL2 is used to generate a fixed frequency of 48 MHz for the USB peripheral.