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SHARP

Data Sheet

LH7A404
32-Bit System-on-Chip

FEATURES

- ARM922T™ Core:
  - 32-bit ARM9TDMI™ RISC Core (200 MHz)
  - 16KB Cache: 8KB Instruction Cache and 8KB Data Cache
  - MMU (Windows CE™ Enabled)
- 80KB On-Chip Memory
- Vectored Interrupt Controller
- External Bus Interface
  - 100 MHz
  - Asynchronous SRAM/ROM/Flash
  - Synchronous DRAM/Flash
  - PCMCIA
  - CompactFlash
- Clock and Power Management
  - 32.768 kHz and 14.7456 MHz Oscillators
  - Programmable PLL
- Low Power Modes (Typical)
  - Run (147 mA), Halt (41 mA), Standby (70 μA)
- Programmable LCD Controller
  - Up to 1,024 × 768 Resolution
  - Supports STN, Color STN, AD-TFT, HR-TFT, TFT
  - Up to 64 K-Colors and 15 Gray Shades
- 9 Channel, 10-bit A/D Converter
  - Touch Screen Controller
  - Brownout Detector
- DMA (12 Channels)
  - External DMA Channels
  - AC97
  - MMC
  - USB
- USB 2.0 Full Speed Host (two downstream ports)
- USB 2.0 Full Speed Device
- Synchronous Serial Port (SSP)
  - Motorola SPI™
  - Texas Instruments SSI
  - National MICROWIRE™
- On-board Boot ROM
  - Supports booting from NAND Flash, I^2C, EEPROM, or XMODEM
- PS/2 Keyboard/Mouse Interface (KMI)
- Three Programmable Timers
- Three UARTs
  - Classic IrDA (115 kbit/s)
- Smart Card Interface (ISO7816)
- Four Pulse Width Modulators (PWMs)
- MultiMediaCard Interface with Secure Digital (MMC 2.11/SD 1.0)
- AC97 Codec Interface
- Smart Battery Monitor Interface
- Real Time Clock (RTC)
- Up to 64 General Purpose I/O Channels
- Watchdog Timer
- JTAG Debug Interface and Boundary Scan
- Operating Voltage
  - 1.8 V Core
  - 3.3 V Input/Output
- 5 V Tolerant Digital Inputs (excludes oscillator pins)
  - The oscillator pins T19, T20, Y18, and Y19 are 1.8 V ± 10%
- Operating Temperature
  - 0°C to +70°C Commercial
  - -40°C to +85°C Industrial with Clock Frequency Reduction (See Recommended Operating Conditions)
- 324-Ball CABGA Package

DESCRIPTION

The advent of 3G technology opens the door for a wide range of multimedia applications in mobile information appliances. These appliances require high processing performance and low power consumption. The LH7A404 is designed from the ground up to provide high processing performance, low power consumption, and a high level of integration.

The LH7A404 contains a high performance 32-bit ARM922T Core. Power consumption is reduced by the high level of integration, 80KB on-chip SRAM, fully static design, power management unit, low voltage operation (1.8 V Core, 3.3 V I/O) and on-chip PLL.

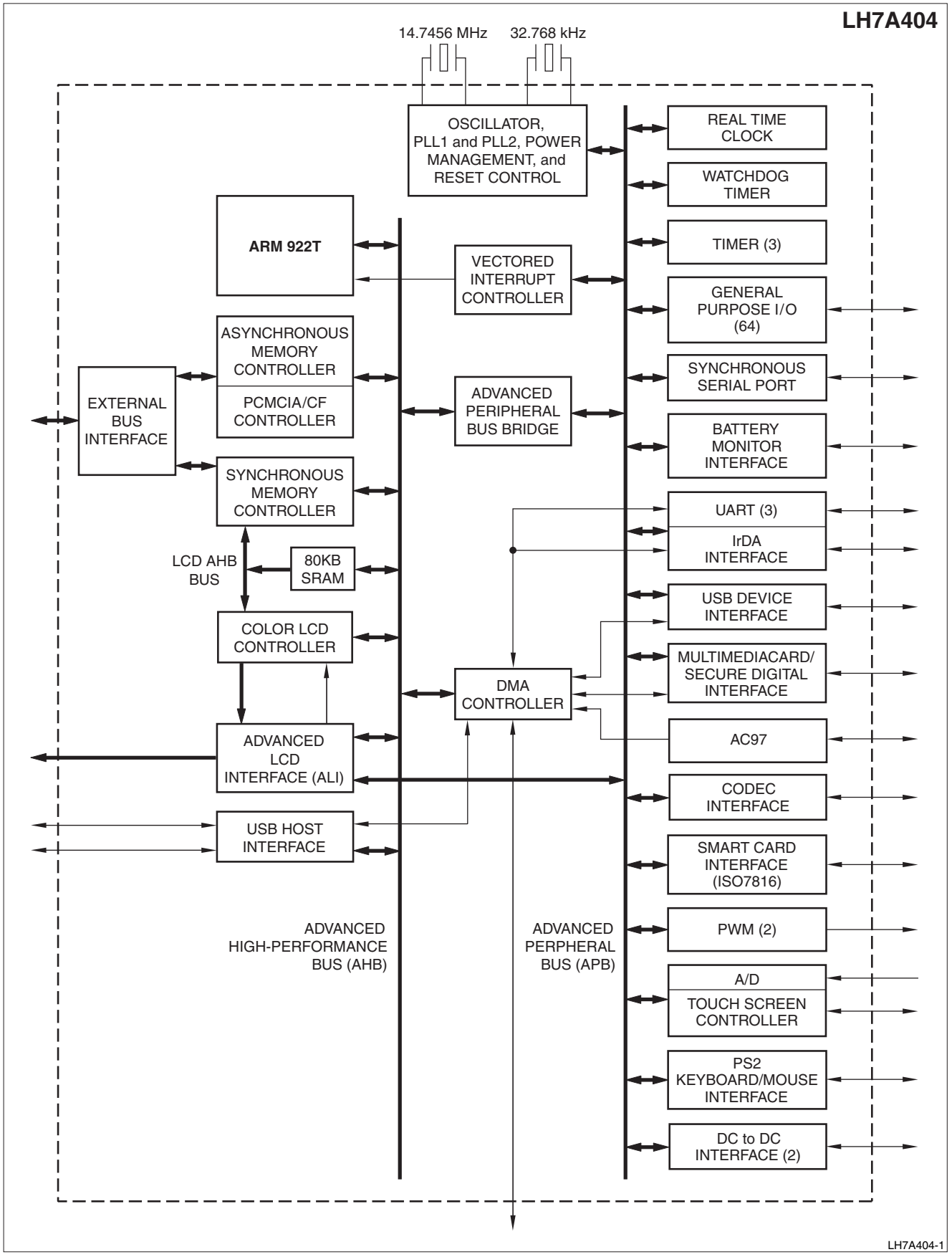

Figure 1. LH7A404 Block Diagram

Table 1. LH7A404 Functional Pin List

CABGA	SIGNAL	DESCRIPTION	RESET STATE	STANDBY STATE	OUTPUT DRIVE	I/O	NOTES
E10	VDD	I/O Ring Power					
E11							
H10							
H11							
K5							
K8							
K13							
K16							
L5							
L8							
L13							
L16							
N10							
N11							
T10							
T11							
U18							
J9	VSS	I/O Ring Ground					
J10							
J11							
J12							
K9							
K10							
K11							
K12							
L9							
L10							
L11							
L12							
M9							
M10							
M11							
M12							
T18							
E7	VDDC	Core Power					
E9							
E14							
G5							
G16							
P5							
P16							
T7							
T12							
T14							

Table 1. LH7A404 Functional Pin List (Cont'd)

CABGA	SIGNAL	DESCRIPTION	RESET STATE	STANDBY STATE	OUTPUT DRIVE	I/O	NOTES
E6	VSSC	Core Ground					
E15							
F5							
F16							
J16							
M5							
R5							
R16							
T6							
T15							
Y17	VDDA	Analog Power for PLL1 and PLL2					
W17							
V16	VSSA	Analog Ground for PLL1 and PLL2					
U15							
W16	VDDAD	Analog Power for A/D, Touch Screen Controller					
V13	VSSAD	Analog Ground for A/D, Touch Screen Controller					
D2	nPOR	Power on Reset	Input	Input		I	3
E1	nURESET	User Reset	Input	Input		I	3
F3	WAKEUP	Wake Up	Input	Input		I	3
F4	nPWRFL	Power Fail Signal	Input	Input		I	3
C1	nEXTPWR	External Power	Input	Input		I	3
C5	nRESETOUT	Reset Output to external devices. This pin carries the same state as the internal SoC reset signal.			12 mA		
Y18	XTALIN	14.7456 MHz Crystal Oscillator pins. To drive the device from an external clock source, XTALIN can be used while XTALOUT is left unconnected.					
Y19	XTALOUT						
T19	XTAL32IN	32.768 kHz Real Time Clock, Crystal Oscillator pins. To drive the device from an external clock source, XTAL32IN can be used while XTAL32OUT is left unconnected.					
T20	XTAL32OUT						
L2	PGMCLK	Programmable Clock (14.7456 MHz MAX.)	LOW	LOW	8 mA	O	
T16	CLKEN	External Oscillator Enable Output	LOW	LOW	8 mA	I/O	4
Y13	WIDTH0	Boot Width Pins. Used with the MEDCHG and INTBOOT bits for internal Boot ROM. On power up, the values on these pins are latched to determine the width and type of Boot device. Boot width can be 8-, 16-, or 32-bit. These pins have a weak internal pull-up resistor	Input with pull-up	Input with pull-up		I	3
W13	WIDTH1						
E4	MEDCHG	Media Change bit; used at power on with INTBOOT and WIDTHx pins to determine boot device.	Input	No Change		I	3
Y20	INTBOOT	When LOW, boot device is selected according to the MEDCHG bit. When HIGH, the lower 64KB addresses are mapped to the internal Boot ROM.	Input	No Change		I	

Table 1. LH7A404 Functional Pin List (Cont'd)

CABGA	SIGNAL	DESCRIPTION	RESET STATE	STANDBY STATE	OUTPUT DRIVE	I/O	NOTES
N19	D0	Data Bus	LOW	LOW	12 mA	I/O	6
P20	D1						
N18	D2						
N20	D3						
M16	D4						
M18	D5						
L18	D6						
L17	D7						
L19	D8						
J19	D9						
K17	D10						
J18	D11						
H19	D12						
G20	D13						
G19	D14						
H17	D15						
F19	D16						
E20	D17						
E19	D18						
D20	D19						
E18	D20						
C20	D21						
D18	D22						
B20	D23						
C18	D24						
A20	D25						
B18	D26						
C16	D27						
B17	D28						
A18	D29						
A17	D30						
B15	D31						
P17	A0	Asynchronous Address Bus	HIGH	LOW	12 mA	O	
N16	A1						

Table 1. LH7A404 Functional Pin List (Cont'd)

CABGA	SIGNAL	DESCRIPTION	RESET STATE	STANDBY STATE	OUTPUT DRIVE	I/O	NOTES
N17	A2/SA0	Asynchronous Address Bus and Synchronous Address Bus	LOW	LOW	12 mA	O	
M19	A3/SA1						
M20	A4/SA2						
L20	A5/SA3						
M17	A6/SA4						
K18	A7/SA5						
K20	A8/SA6						
K19	A9/SA7						
J20	A10/SA8						
H20	A11/SA9						
J17	A12/SA10						
H18	A13/SA11						
F20	A14/SA12						
G18	A15/SA13						
H16	A16/SB0	• Asynchronous Address Bus • Synchronous Device Bank Address 0	LOW	LOW	12 mA	O	
F18	A17/SB1	• Asynchronous Address Bus • Synchronous Device Bank Address 1	LOW	LOW	12 mA	O	
G17	A18	Asynchronous Address Bus	LOW	LOW	12 mA	O	
F17	A19						
D19	A20	Asynchronous Address Bus	LOW	LOW	12 mA	O	6
E17	A21						
C19	A22	Asynchronous Address Bus	LOW	LOW	12 mA	O	
D17	A23						
B19	A24						
A16	A25						
D15	A26						
B14	A27						
V18	nCS0	Asynchronous Memory Chip Select 0	HIGH	HIGH	12 mA	O	
R19	nCS1	Asynchronous Memory Chip Select 1	HIGH	HIGH	12 mA	O	
R18	nCS2	Asynchronous Memory Chip Select 2	HIGH	HIGH	12 mA	O	
P19	nCS3	Asynchronous Memory Chip Select 3	HIGH	HIGH	12 mA	O	
R20	nCS6	Asynchronous Memory Chip Select 6	HIGH	No Change	12 mA	O	
R17	nCS7	Asynchronous Memory Chip Select 7	HIGH	No Change	12 mA	O	
C12	nOE	Asynchronous Memory Output Enable	HIGH	HIGH	12 mA	O	6
D12	nWE	Asynchronous Memory Write Enable	HIGH	HIGH	12 mA	O	6
P18	nWAIT	Asynchronous Memory Controller Wait	Input	No Change		I	
C17	nSCS0	Synchronous Memory Chip Select 0	HIGH	HIGH	12 mA	I/O	4
A19	nSCS1	Synchronous Memory Chip Select 1	HIGH	HIGH	12 mA	I/O	4
D16	nSCS2	Synchronous Memory Chip Select 2	HIGH	HIGH	12 mA	I/O	4
E16	nSCS3	Synchronous Memory Chip Select 3	HIGH	HIGH	12 mA	I/O	4
B16	nSWE	Synchronous Memory Write Enable	HIGH	HIGH	12 mA	O	
A14	SCKE0	Clock Enable 0 for Synchronous Memory	HIGH	No Change	12 mA	O	
B13	SCKE1_2	Clock Enable 1 OR 2 for Synchronous Memory	HIGH	No Change	12 mA	O	

Table 1. LH7A404 Functional Pin List (Cont'd)

CABGA	SIGNAL	DESCRIPTION	RESET STATE	STANDBY STATE	OUTPUT DRIVE	I/O	NOTES
C14	SCKE3	Clock Enable 3 for Synchronous Memory	Depends on MEDCHG	LOW	12 mA	I/O	4
D14	SCLK	Synchronous Memory Clock	LOW	No Change	24 mA	I/O	2, 4
A13	nBLE0	Byte Lane Enable 0	HIGH	HIGH	12 mA	I/O	4
U9	nBLE1	Byte Lane Enable 1	HIGH	HIGH	12 mA	O	
Y7	nBLE2	Byte Lane Enable 2	HIGH	HIGH	12 mA	O	
C13	nBLE3	Byte Lane Enable 3	HIGH	HIGH	8 mA	O	
C15	nCAS	Synchronous Memory Column Address Strobe	HIGH	HIGH	12 mA	I/O	4
A15	nRAS	Synchronous Memory Row Address Strobe	HIGH	HIGH	12 mA	I/O	4
D13	DQM0	Data Mask for Synchronous Memories	HIGH	No Change	12 mA	O	
E13	DQM1						
B12	DQM2						
A12	DQM3						
M2	PA0/ LCDVD16	• GPIO Port A0 • LCD Data pin 16	PA0: Input	No Change	8 mA	I/O	
L4	PA1/ LCDVD17	• GPIO Port A1 • LCD Data pin 17	PA1: Input	No Change	8 mA	I/O	
M3	PA2	GPIO Port A[6:2]	PAx: Input	No Change	8 mA	I/O	
M4	PA3						
M1	PA4						
N3	PA5						
N2	PA6						
N1	PA7	• GPIO Port A7 • Boot Width Selection (See Table 5)	PA7: Input	No Change	8 mA	I/O	6
N4	PB0/ UARTRX1	• GPIO Port B0 • UART1 Receive Data Input	PB0: Input	No Change	8 mA	I/O	
P3	PB1/ UARTTX3	• GPIO Port B1 • UART3 Transmit Data Out	PB1: Input	No Change	8 mA	I/O	
P2	PB2/ UARTRX3	• GPIO Port B2 • UART3 Receive Data In	PB2: Input	No Change	8 mA	I/O	
P1	PB3/ UARTCTS3	• GPIO Port B3 • UART3 Clear to Send	PB3: Input	No Change	8 mA	I/O	
R3	PB4/ UARTDCD3	• GPIO Port B4 • UART3 Data Carrier Detect	PB4: Input	No Change	8 mA	I/O	
N5	PB5/ UARTDSR3	• GPIO Port B5 • UART3 Data Set Ready	PB5: Input	No Change	8 mA	I/O	
R2	PB6/ SWID/ SMBD	• GPIO Port B6 • Single Wire Data • Smart Battery Data	PB6: Input	No Change	8 mA	I/O	
R1	PB7/ SMBCLK	• GPIO Port B7 • Smart Battery Clock	PB7: Input	No Change	8 mA	I/O	
P4	PC0/ UARTTX1	• GPIO Port C0 • UART1 Transmit Data Output	PC0: LOW	No Change	12 mA	I/O	
T1	PC1	GPIO Port C[5:1]	PCx: LOW	No Change	12 mA	I/O	
T2	PC2						
T3	PC3						
R4	PC4						
U1	PC5						
U2	PC6	GPIO Port C6	PC6: LOW	No Change	12 mA	I/O	6

Table 1. LH7A404 Functional Pin List (Cont'd)

CABGA	SIGNAL	DESCRIPTION	RESET STATE	STANDBY STATE	OUTPUT DRIVE	I/O	NOTES
V1	PC7	GPIO Port C7	PC7: LOW	No Change	12 mA	I/O	
Y11	PD0/LCDVD8	• GPIO Port D[7:0] • LCD Video Data Interface	PDx: LOW	LOW if 8-bit LCD enabled; else No Change	12 mA	I/O	
U10	PD1/LCDVD9						
W12	PD2/LCDVD10						
V11	PD3/LCDVD11						
W11	PD4/LCDVD12						
U11	PD5/LCDVD13						
V12	PD6/LCDVD14						
Y12	PD7/LCDVD15						
Y9	PE0/LCDVD4	• GPIO Port E[3:0] • LCD Video Data Interface	PEx: Input	LOW if 8-bit LCD enabled; else No Change	12 mA	I/O	
W10	PE1/LCDVD5						
V10	PE2/LCDVD6						
T9	PE3/LCDVD7						
D4	PE4/ SCCLKIN	• GPIO Port E4 • Smart Card Push-Pull Mode Clock Input	PE4: Input	No Change	12 mA	I/O	
C3	PE5/ SCCLKEN	• GPIO Port E5 • Smart Card Push-Pull Mode External Clock Buffer Enable	PE5: Input	No Change	12 mA	I/O	
B2	PE6/ SCIN	• GPIO Port E6 • Smart Card Push-Pull Mode Data Input	PE6: Input	No Change	12 mA	I/O	
A1	PE7/ SCDATEN	• GPIO Port E7 • Smart Card Push-Pull Mode Data Out External Buffer Enable	PE7: Input	No Change	12 mA	I/O	
A9	PF0/ INT0	• GPIO Port F0 • Interrupt 0	PF0: Input	No Change	8 mA	I/O	3
D9	PF1/ INT1	• GPIO Port F1 • Interrupt 1	PF1: Input	No Change	8 mA	I/O	3
A8	PF2/ INT2	• GPIO Port F2 • Interrupt 2	PF2: Input	No Change	8 mA	I/O	3
C8	PF3/ INT3	• GPIO Port F3 • Interrupt 3	PF3: Input	No Change	8 mA	I/O	3
B8	PF4/ INT4	• GPIO Port F4 • Interrupt 4	PF4: Input	No Change	8 mA	I/O	3
D8	PF5/ INT5/ SCDETECT	• GPIO Port F5 • Interrupt 5 • Smart Card Interface Card Detect Signal	PF5: Input	No Change	8 mA	I/O	3
A7	PF6/ INT6/ PCRDY1	• GPIO Port F6 • Interrupt 6 • Ready for Card 1 for PC Card (PCMCIA or CompactFlash) in Single or Dual Card mode	PF6: Input	No Change	8 mA	I/O	3
E8	PF7/ INT7/ PCRDY2	• GPIO Port F7 • Interrupt 7 • Ready for Card 2 for PC Card (PCMCIA or CompactFlash) in Single or Dual Card mode	PF7: Input	No Change	8 mA	I/O	3
Y2	PG0/ nPCOE	• GPIO Port G0 • Output Enable for PC Card (PCMCIA or CompactFlash) in Single or Dual Card mode	LOW	No Change	8 mA	I/O	
W4	PG1/ nPCWE	• GPIO Port G1 • Write Enable for PC Card (PCMCIA or CompactFlash) in Single or Dual Card mode	LOW	No Change	8 mA	I/O	

Table 1. LH7A404 Functional Pin List (Cont'd)

CABGA	SIGNAL	DESCRIPTION	RESET STATE	STANDBY STATE	OUTPUT DRIVE	I/O	NOTES
Y3	PG2/ nPCIOR	• GPIO Port G2 • I/O Read Strobe for PC Card (PCMCIA or CompactFlash) in Single or Dual Card mode	LOW	No Change	8 mA	I/O	
U5	PG3/ nPCIOW	• GPIO Port G3 • I/O Write Strobe for PC Card (PCMCIA or CompactFlash) in Single or Dual Card mode	LOW	No Change	8 mA	I/O	
T5	PG4/ nPCREG	• GPIO Port G4 • Register Memory Access for PC Card (PCMCIA or CompactFlash) in Single or Dual Card mode	LOW	No Change	8 mA	I/O	
W5	PG5/ nPCCE1	• GPIO Port G5 • Card Enable 1 for PC Card (PCMCIA or CompactFlash) in Single or Dual Card mode. This signal and nPCCE2 are used by the PC Card for decoding low and high byte accesses.	LOW	No Change	8 mA	I/O	
Y4	PG6/ nPCCE2	• GPIO Port G6 • Card Enable 2 for PC Card (PCMCIA or CompactFlash) in Single or Dual Card mode. This signal and nPCCE1 are used by the PC Card for decoding low and high byte accesses.	LOW	No Change	8 mA	I/O	
W6	PG7/ PCDIR	• GPIO Port G7 • Direction for PC Card (PCMCIA or CompactFlash) in Single or Dual Card mode	LOW	No Change	8 mA	I/O	
V6	PH0/ PCRESET1	• GPIO Port H0 • Reset Card 1 for PC Card (PCMCIA or CompactFlash) in Single or Dual Card mode	PHx: Input	No Change	8 mA	I/O	
Y5	PH1/ CFA8/ PCRESET2	• GPIO Port H1 • Address Bit 8 for PC Card (CompactFlash) in Single Card mode • Reset Card 2 for PC Card (PCMCIA or CompactFlash) in Dual Card mode	PHx: Input	No Change	8 mA	I/O	
W7	PH2/ nPCSLOTE1	• GPIO Port H2 • Enable Card 1 for PC Card (PCMCIA or CompactFlash) in Single or Dual Card mode. This signal is used for gating other control signals to the appropriate PC Card.	PHx: Input	No Change	8 mA	I/O	
U6	PH3/CFA9/ PCMCIAA25/ nPCSLOTE2	• GPIO Port H3 • Address Bit 9 for PC Card (CompactFlash) in Single Card mode • Address Bit 25 for PC Card (PCMCIA) in Single Card mode • Enable Card 2 for PC Card (PCMCIA or CompactFlash) in Dual Card mode. Used for gating other control signals to the appropriate PC Card.	PHx: Input	No Change	8 mA	I/O	
W8	PH4/ nPCWAIT1	• GPIO Port H4 • WAIT Signal for Card 1 for PC Card (PCMCIA or CompactFlash) in Single or Dual Card mode	PHx: Input	No Change	8 mA	I/O	
Y6	PH5/CFA10/ PCMCIAA24/ nPCWAIT2	• GPIO Port H5 • Address Bit 10 for PC Card (CompactFlash) in Single Card mode • Address Bit 24 for PC Card (PCMCIA) in Single Card mode • WAIT Signal for Card 2 for PC Card (PCMCIA or CompactFlash) in Dual Card mode	PHx: Input	No Change	8 mA	I/O	
V7	PH6/ nAC97RESET	• GPIO Port H6 • AC97 Reset	PHx: Input	No Change	8 mA	I/O	

Table 1. LH7A404 Functional Pin List (Cont'd)

CABGA	SIGNAL	DESCRIPTION	RESET STATE	STANDBY STATE	OUTPUT DRIVE	I/O	NOTES
U7	PH7/ nPCSTATRE	• GPIO Port H7 • Status Read Enable for PC Card (PCMCIA or CompactFlash) in Single or Dual Card mode	PHx: Input	No Change	8 mA	I/O	
T4	LCDFP/ LCDSPS	• LCD Frame Pulse • ALI Reset Row Driver Counter	LOW	LOW if not in ALI mode	12 mA	O	
V2	LCDLP/ LCDHRLP	• LCD Linepulse • ALI Latch Pulse	LOW	LOW if not in ALI mode	12 mA	O	
U3	LCDCLS	ALI Clock for Row Drivers	Input	No Change	12 mA	O	
V3	LCDSPL	ALI Start Pulse Left for reverse scanning	LOW	No Change	12 mA	O	
U4	LCDUBL	ALI Up, Down signal for reverse scanning	Input	No Change	12 mA	O	
W1	LCDSPR	ALI Start Pulse Right for normal scanning	Input	No Change	12 mA	O	
V4	LCDLBR	ALI Output for reverse scanning	HIGH	No Change	12 mA	O	
W2	LCDMOD	ALI MOD Signal used by the row driver	LOW	No Change	12 mA	O	
V5	LCDPS	ALI Power Save	HIGH	No Change	12 mA	O	
Y1	LCDVDDEN	ALI Power Sequence Control	LOW	No Change	12 mA	O	
W3	LCDREV	ALI Reverse	HIGH	No Change	12 mA	O	
U8	LCDCLKIN	External Clock Input for LCD controller	Input	No Change		I	
V8	LCDVD0	LCD Video Data Interface	LOW	LOW	12 mA	O	
T8	LCDVD1						
W9	LCDVD2						
Y8	LCDVD3						
V9	LCDENAB/ LCDM	• LCD TFT Data Enable • LCD STN AC Bias	LOW	LOW	12 mA	O	
Y10	LCDDCLK	LCD Pixel Clock	LOW	LOW	12 mA	O	
U17	USBDCP	USB Device Full Speed Pull-up Resistor Control	Input	Input	12 mA	I	
U20	USBDP	USB Device Data Positive (Differential Pair)	Input	Input	12 mA	I/O	
U19	USBDN	USB Device Data Negative (Differential Pair)	Input	Input	12 mA	I/O	
W19	USBHDP0	USB Data Host Positive 0 (Differential Pair)	Input	HIGH	12 mA	I/O	
W20	USBHDN0	USB Data Host Negative 0 (Differential Pair)	Input	LOW	12 mA	I/O	
V19	USBHDP1	USB Data Host Positive 1 (Differential Pair)	Input	Input	12 mA	I/O	
V20	USBHDN1	USB Data Host Negative 1 (Differential Pair)	Input	Input	12 mA	I/O	
T17	USBHPWR	USB Host Power	LOW	Input	12 mA	O	
V17	USBHOVRCURR	USB Host Overcurrent	Input	Input	12 mA	I	
D11	nPWME0	DC-DC Converter 0 PWM 0 Enable	Input	Input	8 mA	I/O	5
A10	nPWME1	DC-DC Converter 1 PWM 1 Enable	Input	Input	8 mA	I/O	5
C11	PWM0	DC-DC Converter 0 Output (Pulse Width Modulated)	Input	Input	8 mA	I/O	4
C10	PWM1	DC-DC Converter 1 Output (Pulse Width Modulated)	Input	Input	8 mA	I/O	4
B9	PWM2	PWM Output 2	Input	No Change	8 mA	O	
D10	PWM3	PWM Output 3	Input	No Change		O	
C9	PWMSYNC	PWM Synchronizing Input for PWM2	Input	No Change	8 mA	I	
C7	ACBITCLK	• Audio Codec (AC97) Clock • Audio Codec (ACI) Clock	Input	No Change	8 mA	I/O	
B7	ACOUT	• Audio Codec (AC97) Output • Audio Codec (ACI) Output	LOW	LOW	8 mA	O	
A6	ACSYNC	• Audio Codec (AC97) Synchronization • Audio Codec (ACI) Synchronization	LOW	LOW	8 mA	O	

Table 1. LH7A404 Functional Pin List (Cont'd)

CABGA	SIGNAL	DESCRIPTION	RESET STATE	STANDBY STATE	OUTPUT DRIVE	I/O	NOTES
B6	ACIN	• Audio Codec (AC97) Input • Audio Codec (ACI) Input	Input	No Change	8 mA	I/O	5
A5	MMCCLK	MultiMediaCard Clock (20 MHz MAX.)	LOW	LOW	8 mA	I/O	4
D7	MMCCMD	MultiMediaCard Command	Input	Input	8 mA	I/O	
C6	MMCDATA0	MultiMediaCard Data 0	Input	Input	8 mA	I/O	
B5	MMCDATA1	MultiMediaCard Data 1	Input	Input	8 mA	I/O	
A4	MMCDATA2	MultiMediaCard Data 2	Input	Input	8 mA	I/O	
B4	MMCDATA3	MultiMediaCard Data 3	Input	Input	8 mA	I/O	
F2	UARTCTS2	UART2 Clear to Send Signal	Input	Input	8 mA	I/O	5
F1	UARTDCD2	UART2 Data Carrier Detect Signal	Input	Input	8 mA	I/O	5
G2	UARTDSR2	UART2 Data Set Ready Signal	Input	Input	8 mA	I/O	5
G3	UARTIRTX1	IrDA Transmit	LOW	No Change	8 mA	I/O	4
G1	UARTIRRX1	IrDA Receive	Input	Input	8 mA	I/O	5
H2	UARTTX2	UART2 Transmit Data Output	HIGH	No Change	8 mA	I/O	4
G4	UARTRX2	UART2 Receive Data Input	Input	Input	8 mA	I/O	5
K3	SSPCLK	Synchronous Serial Port Clock	LOW	LOW	8 mA	O	
L1	SSPRX	Synchronous Serial Port Receive	Input	Input	8 mA	I/O	5
L3	SSPTX	Synchronous Serial Port Transmit	Input	INput	8 mA	O	
K4	SSPFRM	Synchronous Serial Port Frame Sync	HIGH	HIGH	8 mA	O	
J2	COL0	Keyboard Interface	HIGH	HIGH	8 mA	I/O	4
H4	COL1						
H5	COL2						
J1	COL3						
J3	COL4						
J4	COL5						
J5	COL6						
K2	COL7						
E2	BATOK	Battery OK	Input	Input		I	3
D1	nBATCHG	Battery Change	Input	Input		I	3
U12	BATCNTL	Battery Control for A/D controller battery monitor.	LOW	No Change	12 mA	O	
H1	KMIDAT	Keyboard/Mouse Data	Input	No Change	12 mA	I/O	
H3	KMICLK	Keyboard/Mouse Clock	Input	No Change	12 mA	I/O	
K1	TBUZ	Timer Buzzer Output (254 kHz MAX.)	LOW	LOW	8 mA	I/O	4
Y16	AN0/UL/X+	• ADC channel 0 • Touch Screen Controller Upper Left • Touch Screen Controller X-plus	Input	Input		I	
Y15	AN1/UR/X-	• ADC channel 1 • Touch Screen Controller Upper Right • Touch Screen Controller X-minus	Input	Input		I	
W14	AN2/LL/Y+	• ADC channel 2 • Touch Screen Controller Lower Left • Touch Screen Controller Y-plus	Input	Input		I	
U13	AN3/LR/Y-	• ADC channel 3 • Touch Screen Controller Lower Right • Touch Screen Controller Y-minus	Input	Input		I	
V14	AN4/WIPER	• ADC channel 4 • Wiper input from 5-wire Touch Screen	Input	Input		I	
U14	VSS or VSSA	Connect pin to either VSS or VSSA	Input	Input		I	

Table 1. LH7A404 Functional Pin List (Cont'd)

CABGA	SIGNAL	DESCRIPTION	RESET STATE	STANDBY STATE	OUTPUT DRIVE	I/O	NOTES
V15	AN6	ADC channel 6	Input	Input		I	
W15	AN7	ADC channel 7	Input	Input		I	
T13	AN8	ADC channel 8	Input	Input		I	
Y14	AN9	ADC channel 9	Input	Input		I	
E12	SCIO	Smart Card Interface I/O	LOW	LOW	12 mA	I/O	
A11	SCCLK	Smart Card Interface Clock	LOW	LOW	12 mA	I/O	
B11	nSCRESET	Smart Card Interface Reset	LOW	LOW	12 mA	O	
B10	SCVCCEN	Smart Card Interface VCC Enable	LOW	No Change	12 mA	O	
D6	CTCLKIN	Counter Timer Clock Input	Input	No Change		I	
A3	DREQ0	DMA Request 0	Input	No Change		I	
D5	DACK0	DMA Acknowledge 0	Input	No Change	12 mA	O	
C4	DEOT0	DMA End of Transfer 0	Input	No Change	12 mA	I/O	
B3	DREQ1	DMA Request 1	Input	No Change		I	
A2	DACK1	DMA Acknowledge 1	Input	No Change	12 mA	O	
E5	DEOT1	DMA End of Transfer 1	Input	No Change	12 mA	I/O	
U16	nTEST0	Test Pin 0. Internal weak pull up to VDD. Status latched at nPOR going HIGH. Pull LOW for JTAG mode. Pull HIGH (or leave open) for Normal mode. See Table 2.	Input with pull-up	Input with pull-up		I	
W18	nTEST1	Test Pin 1. Internal weak pull up to VDD. Status latched at nPOR going HIGH. Pull HIGH (or leave open) for both JTAG and Normal mode. See Table 2.	Input with pull-up	Input with pull-up		I	
D3	TDI	JTAG Data In. Internal weak pull up to VDD.	Input	No Change		I	
C2	TCK	JTAG Clock. Internal weak pull up to VDD.	Input	No Change		I	3
B1	TDO	JTAG Data Out	High Z	No Change	4 mA	O	5
E3	TMS	JTAG Test Mode Select. Internal weak pull up to VDD.	Input	No Change		I	

NOTES:
1. Signals beginning with 'n' are Active LOW.
2. The SCLK pin can source up to 12 mA and sink up to 20 mA. See 'DC Characteristics'.
3. Schmitt trigger input
4. Input only for JTAG boundary scan mode.
5. Output only for JTAG boundary scan mode.
6. These pins have alternate NAND Flash functions during boot-up when using the internal Boot ROM. Consult the Boot ROM Chapter of the User's Guide for more information.

Table 2. nTEST Pin Function

MODE	nTEST0	nTEST1	nURESET
JTAG	0	1	1
Normal	1	1	x

Table 3. LCD Controller Pins

CABGA PIN	RESET STATE	LCD SIGNAL	STN						TFT	AD-TFT/ HR-TFT
			MONO 4-BIT		MONO 8-BIT		COLOR			
			SINGLE PANEL	DUAL PANEL	SINGLE PANEL	DUAL PANEL	SINGLE PANEL	DUAL PANEL		
L4	PA1	LCDVD17								LOW
M2	PA0	LCDVD16								LOW
Y12	PD7	LCDVD15				MLSTN7		CLSTN7	Intensity	Intensity
V12	PD6	LCDVD14				MLSTN6		CLSTN6	BLUE4	BLUE4
U11	PD5	LCDVD13				MLSTN5		CLSTN5	BLUE3	BLUE3
W11	PD4	LCDVD12				MLSTN4		CLSTN4	BLUE2	BLUE2
V11	PD3	LCDVD11				MLSTN3		CLSTN3	BLUE1	BLUE1
W12	PD2	LCDVD10				MLSTN2		CLSTN2	BLUE0	BLUE0
U10	PD1	LCDVD9				MLSTN1		CLSTN1	GREEN4	GREEN4
Y11	PD0	LCDVD8				MLSTN0		CLSTN0	GREEN3	GREEN3
T9	PE3	LCDVD7		MLSTN3	MUSTN7	MUSTN7	CUSTN7	CUSTN7	GREEN2	GREEN2
V10	PE2	LCDVD6		MLSTN2	MUSTN6	MUSTN6	CUSTN6	CUSTN6	GREEN1	GREEN1
W10	PE1	LCDVD5		MLSTN1	MUSTN5	MUSTN5	CUSTN5	CUSTN5	GREEN0	GREEN0
Y9	PE0	LCDVD4		MLSTN0	MUSTN4	MUSTN4	CUSTN4	CUSTN4	RED4	RED4
Y8	LCDVD3	LCDVD3	MUSTN3	MUSTN3	MUSTN3	MUSTN3	CUSTN3	CUSTN3	RED3	RED3
W9	LCDVD2	LCDVD2	MUSTN2	MUSTN2	MUSTN2	MUSTN2	CUSTN2	CUSTN2	RED2	RED2
T8	LCDVD1	LCDVD1	MUSTN1	MUSTN1	MUSTN1	MUSTN1	CUSTN1	CUSTN1	RED1	RED1
V8	LCDVD0	LCDVD0	MUSTN0	MUSTN0	MUSTN0	MUSTN0	CUSTN0	CUSTN0	RED0	RED0
U3	LCDCLS	LCDCLS								LCDCLS
Y10	LCDDCLK	LCDDCLK	LCDDCLK	LCDDCLK	LCDDCLK	LCDDCLK	LCDDCLK	LCDDCLK	LCDDCLK	LCDDCLK
T4	LCDFP	LCDFP/ LCDSPS	LCDFP	LCDFP	LCDFP	LCDFP	LCDFP	LCDFP	LCDFP	LCDSPS
V2	LCDLP	LCDLP/ LCDHRLP	LCDLP	LCDLP	LCDLP	LCDLP	LCDLP	LCDLP	LCDLP	LCDHRLP
W2	LCDMOD	LCDMOD								LCDMOD
V5	LCDPS	LCDPS								LCDPS
W3	LCDREV	LCDREV								LCDREV
V3	LCDSPL	LCDSPL								LCDSPL
V4	LCDLBR	LCDLBR								LCDLBR
W1	LCDSPR	LCDSPR								LCDSPR
U4	LCDUBL	LCDUBL								LCDUBL
Y1	LCDVDDEN	LCDVDDEN								LCDVDDEN
U8	LCDCLKIN	LCDCLKIN	LCDCLKIN	LCDCLKIN	LCDCLKIN	LCDCLKIN	LCDCLKIN	LCDCLKIN	LCDCLKIN	LCDCLKIN
V9	LCDENAB	LCDENAB/ LCDM	LCDM	LCDM	LCDM	LCDM	LCDM	LCDM	LCDENAB	

NOTES:
1. The Intensity bit is identically generated for all three colors.
2. MU = Monochrome Upper Panel
   CU = Color Upper Panel
   CL = Color Lower Panel

Table 4. CABGA Numerical Pin List

CABGA	SIGNAL	SLEW RATE	OUTPUT DRIVE
A1	PE7/SCDATEN	95 mV/ns	12 mA
A2	DACK1	95 mV/ns	12 mA
A3	DREQ0		
A4	MMCDATA2	110 mV/ns	8 mA
A5	MMCCLK	110 mV/ns	8 mA
A6	ACSYNC	110 mV/ns	8 mA
A7	PF6/INT6/PCRDY1	110 mV/ns	8 mA
A8	PF2/INT2	110 mV/ns	8 mA
A9	PF0/INT0	110 mV/ns	8 mA
A10	nPWME1	95 mV/ns	12 mA
A11	SCCLK	95 mV/ns	12 mA
A12	DQM3	110 mV/ns	8 mA
A13	nBLE0	95 mV/ns	12 mA
A14	SCKE0	95 mV/ns	12 mA
A15	nRAS	95 mV/ns	12 mA
A16	A25	95 mV/ns	12 mA
A17	D30	95 mV/ns	12 mA
A18	D29	95 mV/ns	12 mA
A19	nSCS1	95 mV/ns	12 mA
A20	D25	95 mV/ns	12 mA
B1	TDO	100 mV/ns	4 mA
B2	PE6/SCIN	95 mV/ns	12 mA
B3	DREQ1		
B4	MMCDATA3	110 mV/ns	8 mA
B5	MMCDATA1	110 mV/ns	8 mA
B6	ACIN	110 mV/ns	8 mA
B7	ACOUT	110 mV/ns	8 mA
B8	PF4/INT4	110 mV/ns	8 mA
B9	PWM2	110 mV/ns	8 mA
B10	SCVCCEN	95 mV/ns	12 mA
B11	nSCRESET	95 mV/ns	12 mA
B12	DQM2	95 mV/ns	12 mA
B13	SCKE1_2	95 mV/ns	12 mA
B14	A27	95 mV/ns	12 mA
B15	D31	95 mV/ns	12 mA
B16	nSWE	95 mV/ns	12 mA
B17	D28	95 mV/ns	12 mA
B18	D26	95 mV/ns	12 mA
B19	A24	95 mV/ns	12 mA
B20	D23	95 mV/ns	12 mA
C1	nEXTPWR		
C2	TCK		
C3	PE5/SCCLKEN	95 mV/ns	12 mA
C4	DEOT0	95 mV/ns	12 mA
C5	nRESETOUT		

Table 4. CABGA Numerical Pin List (Cont'd)

CABGA	SIGNAL	SLEW RATE	OUTPUT DRIVE
C6	MMCDATA	110 mV/ns	8 mA
C7	ACBITCLK	110 mV/ns	8 mA
C8	PF3/INT3	110 mV/ns	8 mA
C9	PWMSYNC		
C10	PWM1	110 mV/ns	8 mA
C11	PWM0	110 mV/ns	8 mA
C12	nOE	95 mV/ns	12 mA
C13	nBLE3	110 mV/ns	8 mA
C14	SCKE3	95 mV/ns	12 mA
C15	nCAS	95 mV/ns	12 mA
C16	D27	95 mV/ns	12 mA
C17	nSCS0	95 mV/ns	12 mA
C18	D24	95 mV/ns	12 mA
C19	A22	95 mV/ns	12 mA
C20	D21	95 mV/ns	12 mA
D1	nBATCHG		
D2	nPOR		
D3	TDI		
D4	PE4/SCCLKIN	95 mV/ns	12 mA
D5	DACK0	95 mV/ns	12 mA
D6	CTCLKIN		
D7	MMCCMD	110 mV/ns	8 mA
D8	PF5/INT5/SCDETECT	110 mV/ns	8 mA
D9	PF1/INT1	110 mV/ns	8 mA
D10	PWM3	110 mV/ns	8 mA
D11	nPWME0	110 mV/ns	8 mA
D12	nWE	95 mV/ns	12 mA
D13	DQM0	95 mV/ns	12 mA
D14	SCLK	190 mV/ns	24 mA
D15	A26	95 mV/ns	12 mA
D16	nSCS2	95 mV/ns	12 mA
D17	A23	95 mV/ns	12 mA
D18	D22	95 mV/ns	12 mA
D19	A20	95 mV/ns	12 mA
D20	D19	95 mV/ns	12 mA
E1	nURESET		
E2	BATOK		
E3	TMS		
E4	MEDCHG		
E5	DEOT1	95 mV/ns	12 mA
E6	VSSC		
E7	VDDC		
E8	PF7/INT7/PCRDY2	110 mV/ns	8 mA
E9	VDDC		
E10	VDD		

Table 4. CABGA Numerical Pin List (Cont'd)

CABGA	SIGNAL	SLEW RATE	OUTPUT DRIVE
E11	VDD		
E12	SCIO	95 mV/ns	12 mA
E13	DQM1	95 mV/ns	12 mA
E14	VDDC		
E15	VSSC		
E16	nSCS3	95 mV/ns	12 mA
E17	A21	95 mV/ns	12 mA
E18	D20	95 mV/ns	12 mA
E19	D18	95 mV/ns	12 mA
E20	D17	95 mV/ns	12 mA
F1	UARTDCD2	110 mV/ns	8 mA
F2	UARTCTS2	110 mV/ns	8 mA
F3	WAKEUP		
F4	nPWRFL		
F5	VSSC		
F16	VSSC		
F17	A19	95 mV/ns	12 mA
F18	A17/SBANK1	95 mV/ns	12 mA
F19	D16	95 mV/ns	12 mA
F20	A14/SA12	95 mV/ns	12 mA
G1	UARTIRRX1	110 mV/ns	8 mA
G2	UARTDSR2	110 mV/ns	8 mA
G3	UARTIRTX1	110 mV/ns	8 mA
G4	UARTRX2	110 mV/ns	8 mA
G5	VDDC		
G16	VDDC		
G17	A18	95 mV/ns	12 mA
G18	A15/SA13	95 mV/ns	12 mA
G19	D14	95 mV/ns	12 mA
G20	D13	95 mV/ns	12 mA
H1	KMIDAT	95 mV/ns	12 mA
H2	UARTTX2	110 mV/ns	8 mA
H3	KMICLK	95 mV/ns	12 mA
H4	COL1	100 mV/ns	8 mA
H5	COL2	100 mV/ns	8 mA
H10	VDD		
H11	VDD		
H16	A16/SBANK0	95 mV/ns	12 mA
H17	D15	95 mV/ns	12 mA
H18	A13/SA11	95 mV/ns	12 mA
H19	D12	95 mV/ns	12 mA
H20	A11/SA9	95 mV/ns	12 mA
J1	COL3	100 mV/ns	8 mA
J2	COL0	100 mV/ns	8 mA
J3	COL4	100 mV/ns	8 mA

Table 4. CABGA Numerical Pin List (Cont'd)

CABGA	SIGNAL	SLEW RATE	OUTPUT DRIVE
J4	COL5	100 mV/ns	8 mA
J5	COL6	100 mV/ns	8 mA
J9	VSS		
J10	VSS		
J11	VSS		
J12	VSS		
J16	VSSC		
J17	A12/SA10	95 mV/ns	12 mA
J18	D11	95 mV/ns	12 mA
J19	D9	95 mV/ns	12 mA
J20	A10/SA8	95 mV/ns	12 mA
K1	TBUZ	110 mV/ns	8 mA
K2	COL7	100 mV/ns	8 mA
K3	SSPCLK	110 mV/ns	8 mA
K4	SSPFRM	110 mV/ns	8 mA
K5	VDD		
K8	VDD		
K9	VSS		
K10	VSS		
K11	VSS		
K12	VSS		
K13	VDD		
K16	VDD		
K17	D10	95 mV/ns	12 mA
K18	A7/SA5	95 mV/ns	12 mA
K19	A9/SA7	95 mV/ns	12 mA
K20	A8/SA6	95 mV/ns	12 mA
L1	SSPRX	110 mV/ns	8 mA
L2	PGMCLK	110 mV/ns	8 mA
L3	SSPTX	110 mV/ns	8 mA
L4	PA1/LCDVD17	110 mV/ns	8 mA
L5	VDD		
L8	VDD		
L9	VSS		
L10	VSS		
L11	VSS		
L12	VSS		
L13	VDD		
L16	VDD		
L17	D7	95 mV/ns	12 mA
L18	D6	95 mV/ns	12 mA
L19	D8	95 mV/ns	12 mA
L20	A5/SA3	95 mV/ns	12 mA
M1	PA4	110 mV/ns	8 mA
M2	PA0/LCDVD16	110 mV/ns	8 mA

Table 4. CABGA Numerical Pin List (Cont'd)

CABGA	SIGNAL	SLEW RATE	OUTPUT DRIVE
M3	PA2	110 mV/ns	8 mA
M4	PA3	110 mV/ns	8 mA
M5	VSSC		
M9	VSS		
M10	VSS		
M11	VSS		
M12	VSS		
M16	D4	95 mV/ns	12 mA
M17	A6/SA4	95 mV/ns	12 mA
M18	D5	95 mV/ns	12 mA
M19	A3/SA1	95 mV/ns	12 mA
M20	A4/SA2	95 mV/ns	12 mA
N1	PA7	110 mV/ns	8 mA
N2	PA6	110 mV/ns	8 mA
N3	PA5	110 mV/ns	8 mA
N4	PB0/UARTRX1	110 mV/ns	8 mA
N5	PB5/UARTDSR3	110 mV/ns	8 mA
N10	VDD		
N11	VDD		
N16	A1	95 mV/ns	12 mA
N17	A2/SA0	95 mV/ns	12 mA
N18	D2	95 mV/ns	12 mA
N19	D0	95 mV/ns	12 mA
N20	D3	95 mV/ns	12 mA
P1	PB3/UARTCTS3	110 mV/ns	8 mA
P2	PB2/UARTRX3	110 mV/ns	8 mA
P3	PB1/UARTTX3	110 mV/ns	8 mA
P4	PC0/UARTTX1	95 mV/ns	12 mA
P5	VDDC		
P16	VDDC		
P17	A0	95 mV/ns	12 mA
P18	nWAIT		
P19	nCS3	95 mV/ns	12 mA
P20	D1	95 mV/ns	12 mA
R1	PB7/SMBCLK	110 mV/ns	8 mA
R2	PB6/SWID/SMBD	110 mV/ns	8 mA
R3	PB4/UARTDCD3	110 mV/ns	8 mA
R4	PC4	95 mV/ns	12 mA
R5	VSSC		
R16	VSSC		
R17	nCS7	95 mV/ns	12 mA
R18	nCS2	95 mV/ns	12 mA
R19	nCS1	95 mV/ns	12 mA
R20	nCS6	95 mV/ns	12 mA
T1	PC1	95 mV/ns	12 mA

Table 4. CABGA Numerical Pin List (Cont'd)

CABGA	SIGNAL	SLEW RATE	OUTPUT DRIVE
T2	PC2	95 mV/ns	12 mA
T3	PC3	95 mV/ns	12 mA
T4	LCDFP/LCDSPS	95 mV/ns	12 mA
T5	PG4/nPCREG	110 mV/ns	8 mA
T6	VSSC		
T7	VDDC		
T8	LCDVD1	95 mV/ns	12 mA
T9	PE3/LCDVD7	95 mV/ns	12 mA
T10	VDD		
T11	VDD		
T12	VDDC		
T13	AN8		
T14	VDDC		
T15	VSSC		
T16	CLKEN	110 mV/ns	8 mA
T17	USBHPWR	95 mV/ns	12 mA
T18	VSS		
T19	XTAL32IN		
T20	XTAL32OUT		
U1	PC5	95 mV/ns	12 mA
U2	PC6	95 mV/ns	12 mA
U3	LCDCLS	95 mV/ns	12 mA
U4	LCDUBL	95 mV/ns	12 mA
U5	PG3/nPCIOW	110 mV/ns	8 mA
U6	PH3/CFA9/PCMCIAA25/ nPCSLOTE2	110 mV/ns	8 mA
U7	PH7/nPCSTATRE	110 mV/ns	8 mA
U8	LCDCLKIN		
U9	nBLE1	95 mV/ns	12 mA
U10	PD1/LCDVD9	95 mV/ns	12 mA
U11	PD5/LCDVD13	95 mV/ns	12 mA
U12	BATCTL	95 mV/ns	12 mA
U13	AN3/LR/Y-		
U14	VSS or VSSA		
U15	VSSA		
U16	nTEST0		
U17	USBDCP		
U18	VDD		
U19	USBDN		
U20	USBDP		
V1	PC7	95 mV/ns	12 mA
V2	LCDLP/LCDHRLP	95 mV/ns	12 mA
V3	LCDSPL	95 mV/ns	12 mA
V4	LCDLBR	95 mV/ns	12 mA
V5	LCDPS	95 mV/ns	12 mA

Table 4. CABGA Numerical Pin List (Cont'd)

CABGA	SIGNAL	SLEW RATE	OUTPUT DRIVE
V6	PH0/PCRESET1	110 mV/ns	8 mA
V7	PH6/nAC97RESET	110 mV/ns	8 mA
V8	LCDVD0	95 mV/ns	12 mA
V9	LCDENAB/LCDM	95 mV/ns	12 mA
V10	PE2/LCDVD6	95 mV/ns	12 mA
V11	PD3/LCDVD11	95 mV/ns	12 mA
V12	PD6/LCDVD14	95 mV/ns	12 mA
V13	VSSAD		
V14	AN4/WIPER		
V15	AN6		
V16	VSSA		
V17	USBHOVRCURR		
V18	nCS0	95 mV/ns	12 mA
V19	USBHDP1		
V20	USBHDN1		
W1	LCDSPR	95 mV/ns	12 mA
W2	LCDMOD	95 mV/ns	12 mA
W3	LCDREV	95 mV/ns	12 mA
W4	PG1/nPCWE	110 mV/ns	8 mA
W5	PG5/nPCCE1	110 mV/ns	8 mA
W6	PG7/PCDIR	110 mV/ns	8 mA
W7	PH2/nPCSLOTE1	110 mV/ns	8 mA
W8	PH4/nPCWAIT1	110 mV/ns	8 mA
W9	LCDVD2	95 mV/ns	12 mA
W10	PE1/LCDVD5	95 mV/ns	12 mA
W11	PD4/LCDVD12	95 mV/ns	12 mA
W12	PD2/LCDVD10	95 mV/ns	12 mA

Table 4. CABGA Numerical Pin List (Cont'd)

CABGA	SIGNAL	SLEW RATE	OUTPUT DRIVE
W13	WIDTH1		
W14	AN2/LL/Y+		
W15	AN7		
W16	VDDAD		
W17	VDDA		
W18	nTEST1		
W19	USBHDP0		
W20	USBHDN0		
Y1	LCDVDDEN	95 mV/ns	12 mA
Y2	PG0/nPCOE	110 mV/ns	8 mA
Y3	PG2/nPCIOR	110 mV/ns	8 mA
Y4	PG6/nPCCE2	110 mV/ns	8 mA
Y5	PH1/CFA8/PCRESET2	110 mV/ns	8 mA
Y6	PH5/CFA10/PCMCIAA24/ nPCWAIT2	110 mV/ns	8 mA
Y7	nBLE2	95 mV/ns	12 mA
Y8	LCDVD3	95 mV/ns	12 mA
Y9	PE0/LCDVD4	95 mV/ns	12 mA
Y10	LCDDCLK	95 mV/ns	12 mA
Y11	PD0/LCDVD8	95 mV/ns	12 mA
Y12	PD7/LCDVD15	95 mV/ns	12 mA
Y13	WIDTH0		
Y14	AN9		
Y15	AN1/UR/X-		
Y16	AN0/UL/X+		
Y17	VDDA		
Y18	XTALIN		
Y19	XTALOUT		
Y20	INTBOOT		

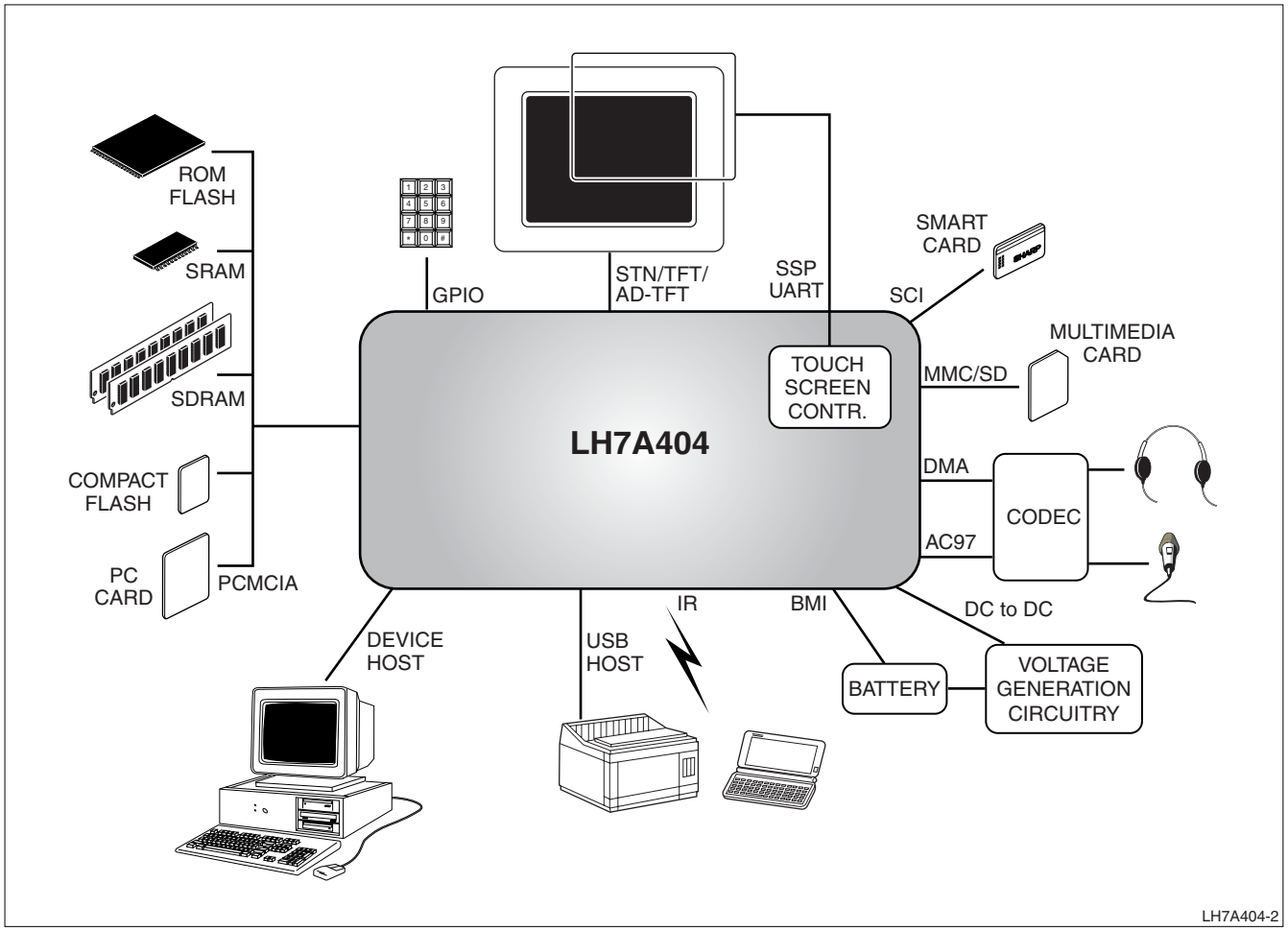

Figure 2. Application Diagram

SYSTEM DESCRIPTIONS

ARM922T Processor

The LH7A404 microcontroller features the ARM922T cached core with an Advanced High-performance Bus (AHB) interface. The processor is a member of the ARM9T family of processors. For more information, see the ARM document, 'ARM922T Technical Reference Manual', available on ARM's website at www.arm.com.

Clock and State Controller

The clocking scheme in the LH7A404 is based around two primary oscillator inputs. These are the 14.7456 MHz input crystal and the 32.768 kHz real time clock oscillator; see Figure 3. The 14.7456 MHz oscillator supplies the main system clock domains for the LH7A404. The 32.768 kHz oscillator controls the power-down operations and real time clock peripheral. The clock and state controller provides the clock gating and frequency division necessary, and then supplies the clocks to the processor and rest of the system. The amount of clock gating that actually takes place depends on the power saving mode selected.

The 32.768 kHz clock provides the source for the Real Time Clock tree and power-down logic. This clock is used for the power state control and is the only clock in the LH7A404 that runs continuously. The 32.768 kHz clock is divided down to 1 Hz for the Real Time Clock counter using a ripple divider to save power.

The 14.7456 MHz source is used to generate the main system clocks for the LH7A404. It is the source for PLL1 and PLL2, the primary clock for the peripherals, and the source clock to the programmable clock (PGM) divider.

PLL1 provides the main clock tree for the chip. It generates the following clocks: FCLK, HCLK, and PCLK. FCLK is the clock that drives the ARM922T core.

HCLK is the main bus (AHB) clock, as such it clocks all memory interfaces, bus arbitrators and the AHB peripherals. HCLK is generated by dividing FCLK by 1, 2, 3, or 4. HCLK can be gated by the system to enable low power operation.

PCLK is the peripheral bus (APB) clock. It is generated by dividing HCLK by either 2, 4, or 8.

PLL2 generates a fixed 48 MHz clock signal for the USB peripheral.

Power Modes

The LH7A404 has three operational states: Run, Halt, and Standby. During Run all clocks are hardware enabled and the processor is clocked. In the Halt mode the device is functioning, but the processor clock is halted while it waits for an event such as a key press. Standby equates to the computer being switched 'off', i.e. no display (LCD disabled) and the main oscillator is shut down.

Reset Modes

Three external signals can generate resets to the LH7A404: nPOR (power on reset), nPWRFL (power failure) and nURESET (user reset). If any of these are active, a system reset is internally generated. An nPOR reset performs a full system reset. The nPWRFL and nURESET resets perform a full system reset except for the SDRAM refresh control, SDRAM Global Configuration, SDRAM Device Configuration, and the RTC peripheral registers. The SDRAM controller issues a self-refresh command to external SDRAM before the system enters an nPWRFL and nURESET reset. This allows the system to maintain its Real Time Clock and SDRAM contents. Upon release of Reset, the chip enters Standby mode. Once in the Run mode the PWRSR register can be interrogated to determine the nature of the reset and the trigger source, after which software can then take appropriate actions.

Data Paths

The data paths in the LH7A404 are:

- The AMBA AHB bus
- The AMBA APB bus
- The External Bus Interface
- The LCD AHB bus
- The DMA busses.

AMBA AHB BUS

The Advanced Microprocessor Bus Architecture AHB (AMBA AHB) is a high speed 32-bit-wide data bus. The AMBA AHB is for high-performance, high-clock-frequency system modules.

LH7A404 peripherals and memory with high bandwidth requirements are connected to the ARM922T processor and other bus masters using a multi-master AHB bus. These peripherals include the external memory interfaces, on-chip SRAM, LCD Controller (bus master), DMA Controller (bus master), and USB Host (bus master). Remaining peripherals reside on the lower bandwidth Advanced Peripheral Bus (APB), which is accessed from the AHB via the APB Bridge. The APB Bridge is the only master on the APB, and its operation is transparent to the user as it converts AHB accesses into slower APB accesses automatically.

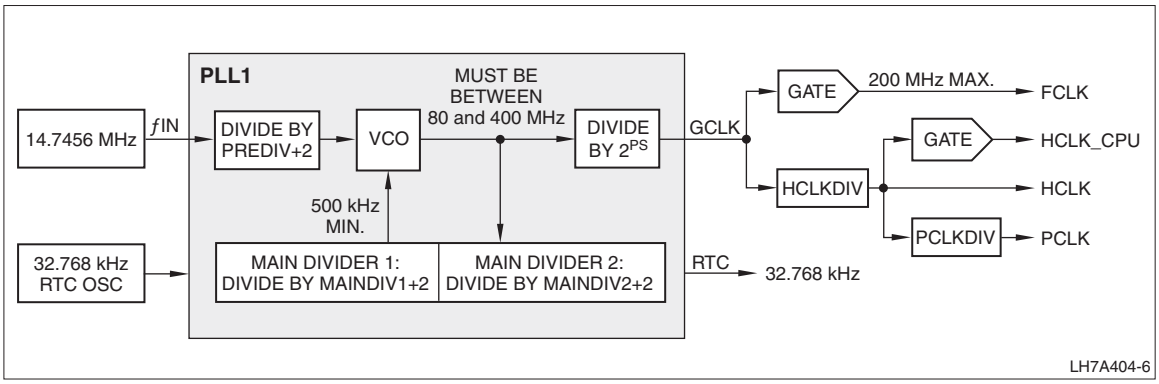

Figure 3. Clock and State Controller Block Diagram

AMBA APB BUS

The AMBA APB provides a lower-bandwidth bus for peripherals accessed less frequently. This reduces the loading on the AHB, allowing it to run faster to maximize system performance, while the APB can operate at a lower clock rate to conserve power. The APB Bridge is the only master on the APB. All AHB masters can access APB peripherals via the ABP Bridge. The APB clock frequency can be selected by software to divide the clock speed of the AHB bus by 2, 4, or 8.

EXTERNAL BUS INTERFACE (EBI)

The External Bus Interface (EBI) provides a 32-bit-wide, high speed gateway to external memory devices. The supported memory devices include:

- Asynchronous RAM/ROM/Flash
- Synchronous DRAM/Flash
- PCMCIA interfaces
- CompactFlash interfaces.

The EBI can be controlled by either the Asynchronous Memory Controller or Synchronous Memory Controller. There is an arbiter on the EBI input, with priority given to the Synchronous Memory Controller interface.

LCD BUS

The LCD controller has its own local memory bus that connects it to the system's embedded memory and external SDRAM. The function of this local data bus is to allow the LCD controller to perform its video refresh function without congesting the main AHB bus. This leads to better system performance and lower power consumption. There is an arbiter on both the embedded memory and the synchronous memory controller. In both cases the LCD bus is given priority.

DMA BUSES

The LH7A404 has a DMA system that connects the higher speed/higher data volume APB peripherals (MMC, USB Device and AC97) to the AHB bus. This enables the efficient transfer of data between these peripherals and external memory without the intervention of the ARM922T core.

USB HOST CONTROLLER DMA BUS

The USB Host Controller has its own DMA controller. It acts as another bus master on the AHB bus. It does not interact with the non-USB DMA controller except in bus arbitration.

Memory Map

The LH7A404 system has a 32-bit-wide address bus, allowing addressing up to 4GB of memory. This memory space is subdivided into a number of memory banks, shown in Figure 4. Four of these banks (each 256MB) are allocated to the Synchronous Memory Controller. Eight banks (each 256MB) are allocated to the Asynchronous Memory Controller. Two of these eight banks are designed for PCMCIA systems. Part of the remaining memory space is allocated to the embedded SRAM, and to the control registers of the AHB and APB. The rest of the memory space is not used.

The LH7A404 can boot from both internal and external devices. The selection is determined by the value of five pins at power-on reset as shown in Table 5. If booting is from an external device (with INTBOOT = 0), refer to Table 6. When booting from external synchronous memory, bank 4 (nSCS3) is mapped into memory location zero. When booting from external asynchronous memory, memory bank 0 (nSCS0) is mapped into memory location zero.

Figure 4 shows the memory map of the LH7A404 system for the two boot modes.

Once the LH7A404 has booted, the boot code can configure the ARM922T MMU to remap the low memory space to a location in RAM. This allows the user to set the interrupt vector table.

Table 5. Internal Boot Modes

BOOT DEVICE	GPIO PA7	LATCHED MEDCHG	LATCHED WIDTH1	LATCHED WIDTH0	LATCHED INTBOOT
External device	See Table 6				0
8-bit interface, 3-byte address NAND Flash	0	0	0	0	1
8-bit interface, 4-byte address NAND Flash	0	0	0	1	1
8-bit interface, 5-byte address NAND Flash	0	0	1	0	1
16-bit interface, 3-byte address NAND Flash	1	0	0	0	1
16-bit interface, 4-byte address NAND Flash	1	0	0	1	1
16-bit interface, 5-byte address NAND Flash	1	0	1	0	1
XMODEM using UART2	0	1	0	0	1
I^2C EEPROM	0	1	0	1	1
Undefined	0	0	1	1	1
	0	1	1	1	1
	1	0	1	1	1
	1	1	x	x	1

Table 6. External Boot Modes

BOOT MODE	WIDTH1	WIDTH0	MEDCHG	INTBOOT
8-bit ROM	0	0	0	0
16-bit ROM	0	1	0	0
32-bit ROM	1	0	0	0
Invalid: Do not allow this condition.	1	1	0	0
16-bit SynchFlash (Initializes device MODE Register)	0	0	1	0
16-bit SROM (Initializes device MODE Register)	0	1	1	0
32-bit SynchFlash (Initializes device MODE Register)	1	0	1	0
32-bit SROM (Initializes device MODE Register)	1	1	1	0
Boot from internal Boot ROM; see Table 5	x	x	x	1

Vectored Interrupt Controller (VIC)

The LH7A404 has two VICs working together to manage interrupt requests from on-chip and off-chip sources. Each VIC performs these primary functions:

- Determine if an interrupt source is disabled or can generate an FIQ or IRQ to the ARM core
- Prioritize up to 16 separate interrupt sources for simultaneous and nested processing
- Obtain the address of the interrupt handler (vector) for up to 16 interrupt sources
- Provide a default vector and a set of status registers for up to 16 non-vectored sources. Software determines the priority of these interrupts.

Two VICs are daisy-chained together to support up to 64 different interrupts, 32 of which are vectored. The VIC supports both FIQ and IRQ interrupts. FIQ interrupts have a higher priority than IRQ interrupts. If two interrupts with the same priority become active at the same time, the priority must be resolved in software. When an interrupt becomes active, the VIC generates an FIQ or IRQ if the corresponding mask bit is set. Interrupts are not latched in the VIC, but may latch on a particular peripheral when applicable.

After a power-on reset, all mask register bits are cleared, masking all interrupts. They must be set by software after power-on reset to enable interrupts.

A vectored interrupt has improved latency as it provides direct information about where its service routine is located and eliminates software arbitration needed with a simple interrupt controller.

The VICs continue to operate in Halt and Standby modes, so external interrupts may bring the chip out of these low power modes.

External Bus Interface

The ARM922T, LCD controller, and DMA engine have access to an external memory system. The LCD controller has access to an internal frame buffer in embedded SRAM and an extension buffer in Synchronous Memory for large displays. The processor and DMA engine share the main system bus, providing access to all external memory devices and the embedded SRAM frame buffer.

An arbitration unit ensures that control over the External Bus Interface (EBI) is only granted when an existing access has been completed. See Figure 4.

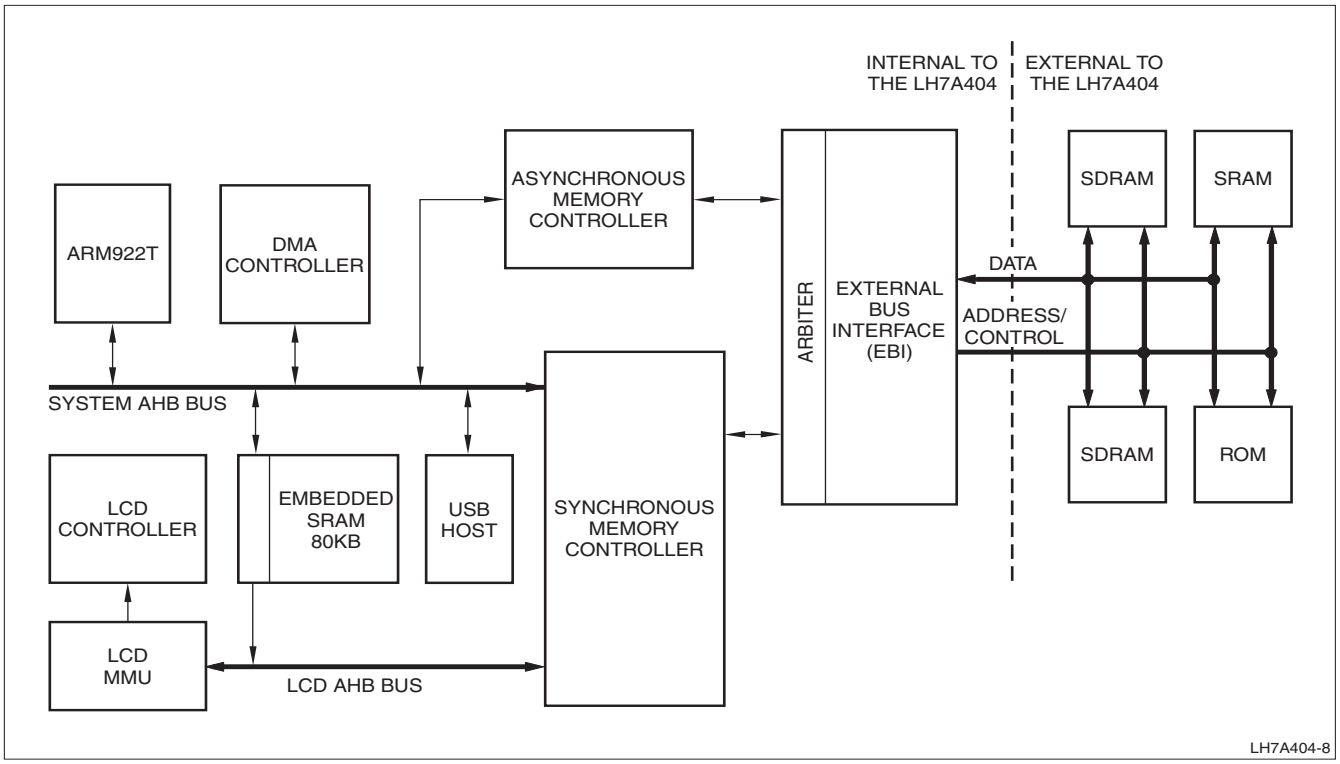

Figure 4. External Bus Interface Block Diagram

Embedded SRAM

The LH7A404 incorporates 80KB of embedded SRAM. This embedded memory is used for storing code, data, or LCD frame data and is contiguous with external SDRAM. The 80KB is large enough to store a QVGA frame (320 × 240) at 8 bits per pixel, equivalent to 70KB of information.

Locating the frame buffer on chip reduces the overall power consumed by LH7A404 applications. Normally, the system performs external accesses to acquire this data. The LCD controller automatically uses an overflow frame buffer in SDRAM if a larger screen size is required. This overflow buffer can be located on any 4KB page boundary in SDRAM, allowing software to set the MMU (in the LCD controller) page tables so the two memory areas appear contiguous, allowing byte, half-word, and word accesses.

Static Memory Controller (SMC)

The asynchronous Static Memory Controller (SMC) provides an interface between the AMBA AHB system bus and external (off-chip) memory devices.

The SMC simultaneously supports up to eight independently configurable memory banks. Each memory bank can support:

- SRAM
- ROM
- Flash EPROM
- Burst ROM memory.

Each memory bank may use devices with either 8-, 16-, or 32-bit external memory data paths. The memory controller can be configured to support either little-endian or big-endian operation.

The memory banks can be configured to support:

- Non-burst read and write accesses only to high-speed CMOS static RAM
- Non-burst write accesses, nonburst read accesses and asynchronous page mode read accesses to fast-boot block flash memory.

The SMC has six main functions:

- Memory bank select
- Access sequencing
- Wait state generation
- Byte lane write control
- External bus interface
- CompactFlash or PCMCIA interfacing.

SDRAM (Synchronous) Memory Controller

The SDRAM (Synchronous) Memory Controller provides a high speed memory interface to a wide variety of synchronous memory devices, including Synchronous DRAM, Synchronous Flash and Synchronous ROMs.

The key features of the controller are:

- LCD DMA port for high bandwidth
- Up to four Synchronous Memory banks can be independently set up
- Includes special configuration bits for Synchronous ROM operation
- Includes ability to program Synchronous Flash devices using write and erase commands
- On booting from Synchronous ROM, (and optionally with Synchronous Flash), a configuration sequence is performed before releasing the processor from reset
- Data is transferred between the controller and the Synchronous DRAM in four-word bursts. Longer transfers within the same page are concatenated, forming a seamless burst
- Programmable for 16- or 32-bit data bus size
- Two reset domains enable Synchronous DRAM contents to be preserved over a ‘soft’ reset
- Power saving Synchronous Memory SCKE and external clock modes provided.

Secure Digital/MultiMediaCard (MMC)

The SD Memory Card is a flash-based memory card that meets the security, capacity, performance, and environment requirements inherent in electronic devices. The SD Memory Card host supports MultiMediaCard (MMC) operation as well, and is compatible with MMC Cards.

The SD/MMC controller can be used as an MMC card controller or as an SD Card controller, and supports the full SD/MMC bus protocol as defined in the MMC system specification 2.11 provided by the MMC Association and the SD Memory Card Spec v1.0 from the SD Association.

SD/MMC INTERFACE DESCRIPTION

The SD/MMC controller uses the three-wire signal bus (clock, command, and data) to input and output data to and from the MMC, and to configure and acquire status information from the card. The SD controller differs in that it has four data lines instead of one.

The SD/MMC bus lines can be divided into three groups:

- Power supply: VSS1, VSS2, and VDD
- Data transfer group: MMCCMD, MMCDATA0, MMCDATA1, MMCDATA2, MMCDATA3 (for MMC, do not use MMCDATA1, MMCDATA2, MMCDATA3)
- Clock: MMCCLK

MMC CONTROLLER

The MMC controller implements MMC-specific functions, serves as the bus master for the MMC Bus and implements the standard interface to the MMC (card initialization, CRC generation and validation, command/response transactions, etc.).

Smart Card Interface (SCI)

The SCI (ISO7816) connects to an external Smart Card reader. The SCI can autonomously control data transfer to and from the Smart Card. Transmit and receive data FIFOs are provided to reduce the required interaction between the CPU core and the peripheral.

SCI FEATURES

- Supports asynchronous T0 and T1 transmission protocols
- Supports clock rate conversion factor F = 372, with bit rate adjustment factors of D = 1, 2, or 4
- Eight-character-deep buffered Tx and Rx paths
- Direct interrupts for Tx and Rx FIFO level monitoring
- Interrupt status register
- Hardware-initiated card deactivation sequence on detection of card removal
- Software-initiated card deactivation sequence on transaction complete
- Limited support for synchronous smart cards via registered input/output.

PROGRAMMABLE PARAMETERS

- Smart Card clock frequency
- Communication baud rate
- Protocol convention
- Card activation/deactivation time
- Maximum time for first character of Answer to Reset (ATR) reception checking
- Maximum ATR character stream duration checking
- Maximum time of receipt of first character of data stream checking
- Maximum time allowed between characters checking
- Character guard time
- Block guard time
- Transmit/receive character retry.

Direct Memory Access Controller (DMA)

The DMA Controller can be used to interface streams from 20 internal peripherals to the system memory using 10 fully-independent programmable channels which consist of five M2P (transmit) channels and five P2M (receive) channels.

The following peripherals may be allocated to the 10 channels:

- USB Device
- USB Host
- SD/MMC
- AC97
- UART1
- UART2
- UART3

Each of the above peripherals contain one Tx and one Rx channel, except the AC97, which contains three Tx and Rx channels. These peripherals also have their own bi-directional DMA bus, capable of simultaneously transferring data in both directions. All memory transfers take place via the main system AHB bus.

The DMA Controller can also be used to interface streams from memory-to-memory (M2M) or memory-to-external peripheral (M2P) using two dedicated M2M channels. External handshake signals are available to support memory-to-/from-external peripheral (M2P/P2M) transfers. A software trigger is available for M2M transfers only.

The DMA Controller features:

- Two dedicated channels for M2M and external M2P/P2M
- Ten fully independent, programmable DMA controller internal M2P/P2M channels (5 Tx and 5 Rx)
- Channels assignable to one of a number of different peripherals
- Independent source and destination address registers. Source and destination can be programmed to auto-increment or not auto-increment for M2M channels
- Two buffer descriptors per M2P and M2M channel to avoid potential data under/over-flow due to software introduced latency. A buffer refers to the area in system memory that is characterized by a buffer descriptor, i.e., a start address and the length of the buffer in bytes
- No AMBA wrapping bursts for DMA channels; only incrementing bursts are supported
- Buffer size independent of the peripheral's packet size for the internal M2P channels. Transfers can automatically switch between buffers
- Maskable interrupt generation
- Internal arbitration between DMA channels, plus support for an AHB bus arbiter
- DMA data transfer sizes, byte, word and quad-word data transfers are supported using a 16-byte data. Maximum data transfer size per M2M channel is programmable
- Per-channel clock gating reducing power in channels that have not been enabled by software. See the 'Clock and State Controller' section.

A set of control and status registers are available to the system processor for setting up DMA operations and monitoring their status. System interrupts are generated when any/all of the DMA channels wish to inform the processor to update the buffer descriptor. The DMA controller can service 10 out of 20 possible peripherals using the ten DMA channels, each with its own peripheral DMA bus capable of simultaneously transferring data in both directions.

The SD/MMC, UART[3:1], USB Device, and USB Host peripherals can each use two DMA channels, one for transmit and one for receive. The AC97 peripheral can use six DMA channels (three transmit and three receive) to allow different sample frequency data queues to be handled with low software overhead.

The DMA controller includes an M2M transfer feature allowing block moves of data from one memory address space to another with minimum of program effort and time. An M2M software trigger capability is provided. The DMA controller can also fill a block of memory with data from a single location.

The DMA controller's M2M channels can also be used in M2P/P2M mode. A set of external handshake signals, DREQ, DACK and TC/DEOT are provided for each of two M2M channels.

DREQ (input) can be programmed edge or level active, and active HIGH or LOW. The peripheral may hold DREQ active for the duration of the block transfers or may assert/deassert on each transfer.

DACK (output) can be programmed active HIGH or LOW. DACK will assert and return to de-asserted with each Read or Write, the timing coinciding with nOE or nWE from the EBI.

TC/DEOT is a bidirectional signal with programmable direction and active polarity. When configured as an Output, the DMA will assert Terminal Count (TC) on the final transfer to coincide with the DACK, typically when the byte count has expired. When configured as an Input, the peripheral must assert DEOT concurrent with DREQ for the final transfer in the block.

Transfer is terminated when DEOT is asserted by the external peripheral or when the byte count expires, whichever occurs first. Status bits indicate if the actual byte count is equal to the programmed limit, and if the count was terminated by peripheral asserting DEOT. Terminating the transfer causes a DMA interrupt on that channel and rollover to the 'other' buffer if so configured.

USB Device

The features of the USB are:

- Compliant with USB 2.0 Full Speed specification
- Provides a high-level interface that removes the USB protocol details from firmware
- Compatible with both OpenHCI and Intel UHCI standards
- Supports full-speed (12 Mbit/s) functions
- Supports Suspend and Resume signalling.

USB Host Controller

The features of the USB Host Controller are:

- Open Host Controller Interface Specification (OpenHCI) Rev. 1.0 Compliant
- Universal Serial Bus Specification 2.0 Full Speed compatible
- Supports Low Speed and High Speed USB devices
- Root Hub has two Downstream Ports
- DMA functionality.