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CrossLink LIF-MD6000 Master Link Board

Evaluation Board User Guide

EB105 Version 1.1

April 2017

Contents

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Acronyms in This Document

A list of acronyms used in this document.

Acronym	Definition
CMOS	Complementary Metal-Oxide Semiconductor
CSI-2	Camera Serial Interface
DSI	Display Serial Interface
FTDI	Future Technology Devices International
I^2C	Inter-Integrated Circuit
IO	Input/Output
LVDS	Low-Voltage Differential Signaling
MIPI	Mobile Industry Processor Interface
SPI	Serial Peripheral Interface

1. Introduction

This document describes the Lattice Semiconductor CrossLink™ LIF-MD6000 Master Link board that supports a variety of demos, encompassing different signaling logic standards bridging with MIPI® CSI-2/DSI interface. The board's key component is the CrossLink Family device that features built in MIPI D-PHY hard blocks to support different bridging solutions.

For the latest information about this board, including optional Tx/Rx Link boards, demo files, further documentation and more, see the Lattice website at: www.latticesemi.com/masterlink

For details about the CrossLink device, refer to FPGA-DS-02007, CrossLink Family Data Sheet.

The content of this user guide includes descriptions of on-board jumper settings, programming circuit, a complete set of schematics, and bill of materials for LIF-MD6000 Master Link board.

Refer to Appendix A, B, C, D, E, F for the schematics and BOM of the CrossLink LIF-MD6000 Master Link board and the schematics and BOMs of the Breakout IO Link and SMA IO Link boards that are included in the demo kit.

Circuits on the development kit board:

- Programming Circuit
  - Mini USB Type-B connector to FTDI
  - FTDI to CrossLink using SPI
  - FTDI to XO3LF device using JTAG
- CrossLink
  - MIPI CSI-2/DSI hard block
  - Bridging of multiple signaling standards
  - SPI flash configuration
  - General Purpose Input/Output
  - LED display
- LCMXO3LF-1300E
  - I^2C muxing

Figure 1.1 shows the top view of the LIF-MD6000 Master Link board and its key components. Figure 1.2 on the next page shows the bottom view of the board.

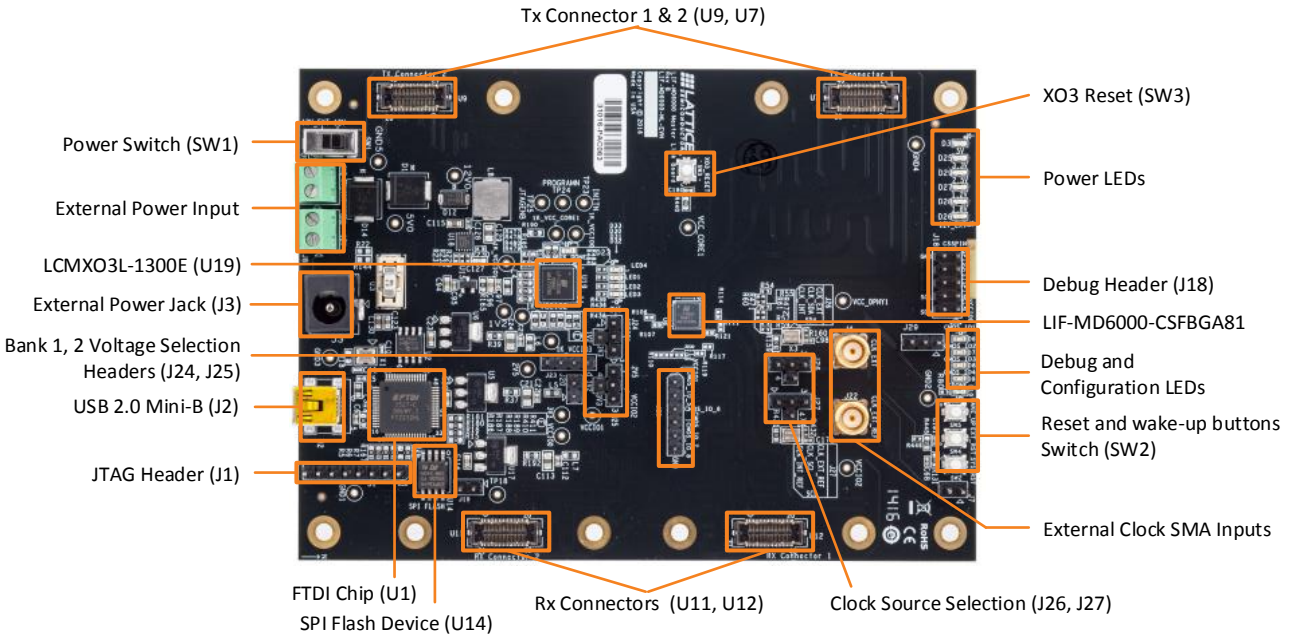


Figure 1.1. Top View of Master Link Board and its Key Components

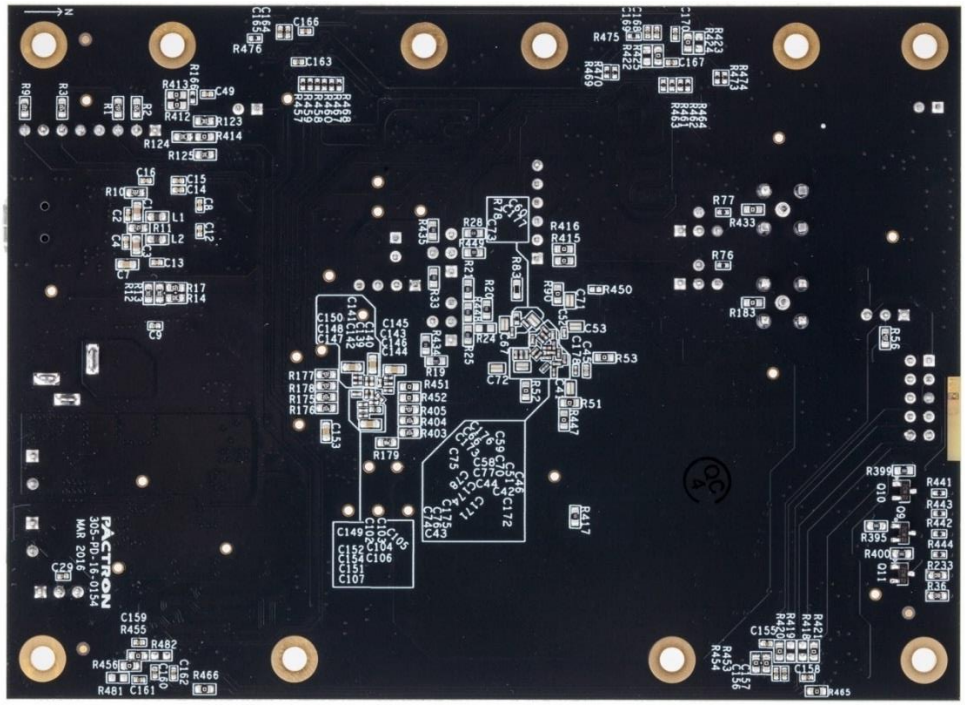


Figure 1.2. Bottom View of Master Link Board

2. Headers and Test Connections

Figure 1.1 shows the top view of the Master Link board. The headers and test connections on the board provide access to LIF-MD6000 Master Link demo board circuits. Table 2.1 lists the headers and test connectors.

Table 2.1. Headers and Test Connectors

Part	Description	Setting
J1	External JTAG interface - For LCMX03 only	—
J8	External 12 V terminal block	Open
J9	External 5 V terminal block	Open
SW1	External adaptor power ON/OFF	—
J22	External reference clock input for MIPI D-PHY reference clock	—
J21	External or internal reference clock selection	1–2 (External), 2–3 (Internal)
J5	Debug I/O	—
J20	LIF-MD6000 chip select	OPEN-OFF, SHORT-ON
J19	SPI Flash chip select	OPEN-OFF, SHORT-ON
J4	External clock input for MIPI D-PHY reference clock	—
J6	External or internal clock selection	1–2 (External), 2–3 (Internal)
J18	External SP/I²C access	—
SW2	Configuration reset for LIF-MD6000	—
J29	Reset signal voltage selector	1-2 (VCCIO2), 2-3 (VCCIO0)
J28	Reveal analyzer signal connector	—
J26	Internal/External clock and I2C SDA Mux	1-2 (CLK_INT), 2-3 (CLK_EXT), 2-4 (SDA)
J27	Internal/External reference clock and I2C SCL Mux	1-2 (CLK_INT_REF), 2-3 (CLK_EXT_REF), 2-4 (SCL)
J24	VCCIO1 Bank voltage selector	1-2 (2.5 V), 2-3 (3.3 V), 2-4 (1.2 V)
J25	VCCIO1 Bank voltage selector	1-2 (2.5 V), 2-3 (3.3 V), 2-4 (1.2 V)
J3	External power jack	—
U7, U9	Tx Connectors for external interface	—
U11, U12	Rx Connectors for external interface	—
SW4	External reset for LIF-MD6000 device	—
SW3	External reset for LCMXO3L device	—
SW5	PMU WAKEUP Switch	—
J23	Debug Header for LCMXO3L device	—

3. Programming Circuit

The Mini-B USB connector is used for programming the board by using Lattice Diamond® Programmer software. Figure 3.1 shows the programming block of LIF-MD6000 Master Link board.

The Mini-B USB connector interfaces to the FTDI FT2232H IC. The FTDI IC works with Diamond programmer software to provide interfaces for:

- JTAG – to program MachXO2-1300E
- SPI – to program both CrossLink, and SPI Flash Memory

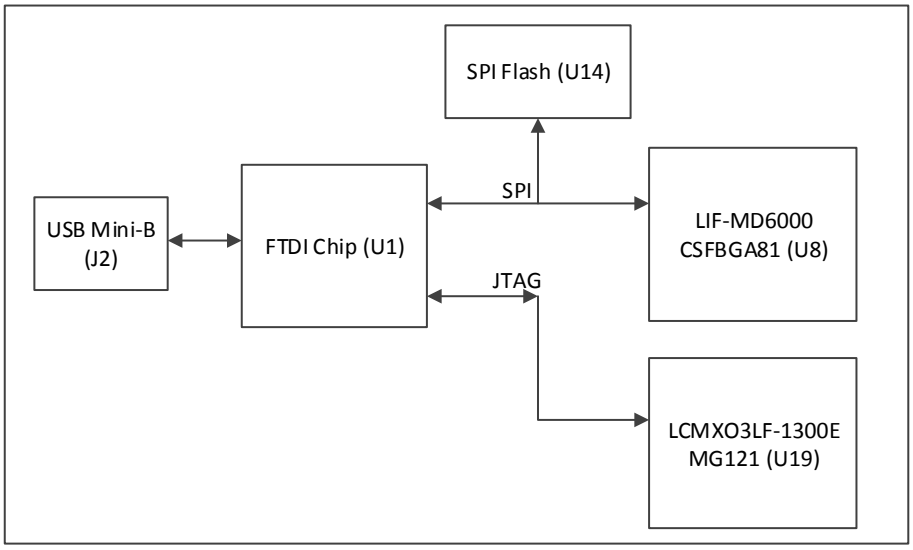


Figure 3.1. Programming Block

3.1. Bridging Circuit

Figure 3.2 shows the block diagram of bridging of different standard interfaces. The CrossLink device is used as a bridging device that supports a variety of I/O standards. This demo board supports development of the following interface bridges:

- 1:1 MIPI DSI Display Interface Bridge
- 1:2 MIPI DSI Display Interface Bridge
- 2:1 MIPI CSI-2 Image Sensor Aggregator Bridge
- CMOS to MIPI CSI-2 Image Sensor Interface Bridge
- MIPI CSI-2 to CMOS Image Sensor Interface Bridge
- MIPI DSI to CMOS Display Interface Bridge
- OpenLDI LVDS to MIPI DSI Display Interface Bridge
- CMOS to MIPI DSI Display Interface Bridge

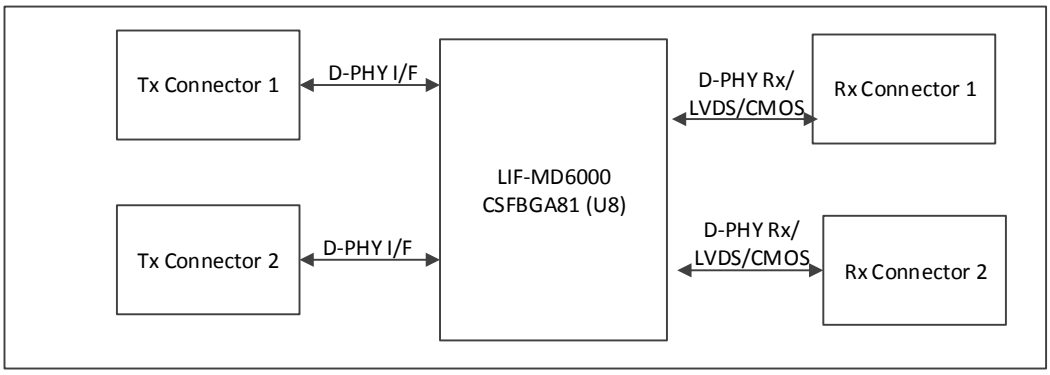


Figure 3.2. Bridging Block

3.2. I²C Expander

Figure 3.3 shows the block diagram of the I²C expander. The LCMXO3LF-1200E device is used as an I²C expander and it supports a single master and multiple slave devices connected to the board. The master I²C interface is connected to the Tx header and the slave device I²C interface is connected to the Rx connectors supporting any slave device access from the master based on the slave address.

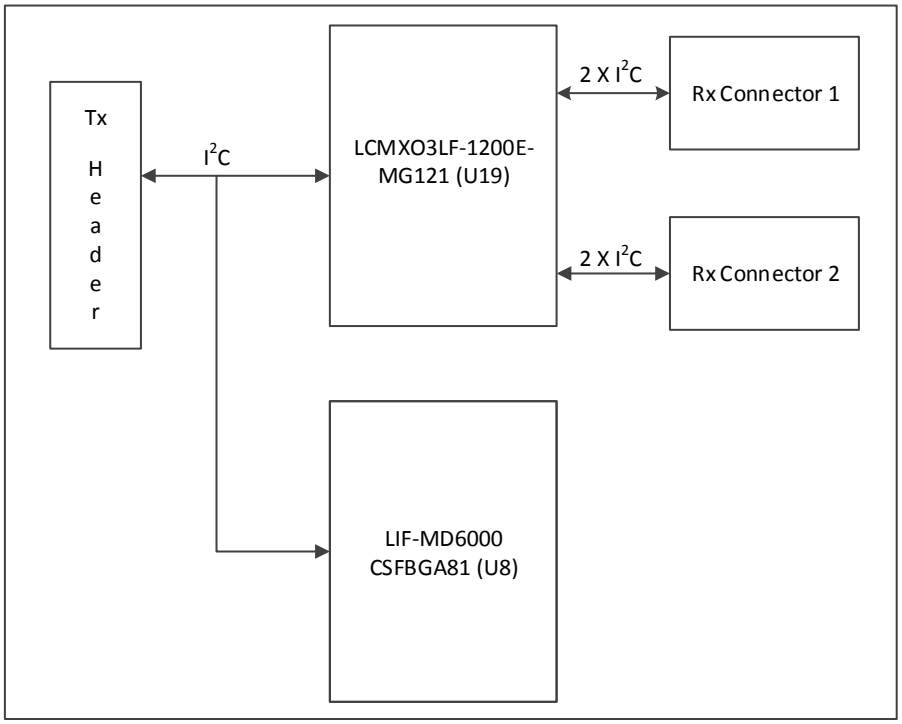


Figure 3.3. I²C Expander Block

4. Power Supply

The power supply to the development kit is provided by the Mini-B USB connector or from an external adaptor.

Figure 4.1 shows the power supply block of the CrossLink LIF-MD6000 Master Link board. The Mini-B USB connector is used only for programming and the onboard power regulator for the successful programming. The external adaptor provides 12 V power source through voltage regulators on the board to CrossLink and LCMXO3LF-1300E, as well as to the external boards connected to Tx and Rx Headers. Each I/O and core voltage rail on the board is accessible by a test point on the board. The current flowing to each rail can be measured using a 1 Ω resistor placed in the path of each voltage rail.

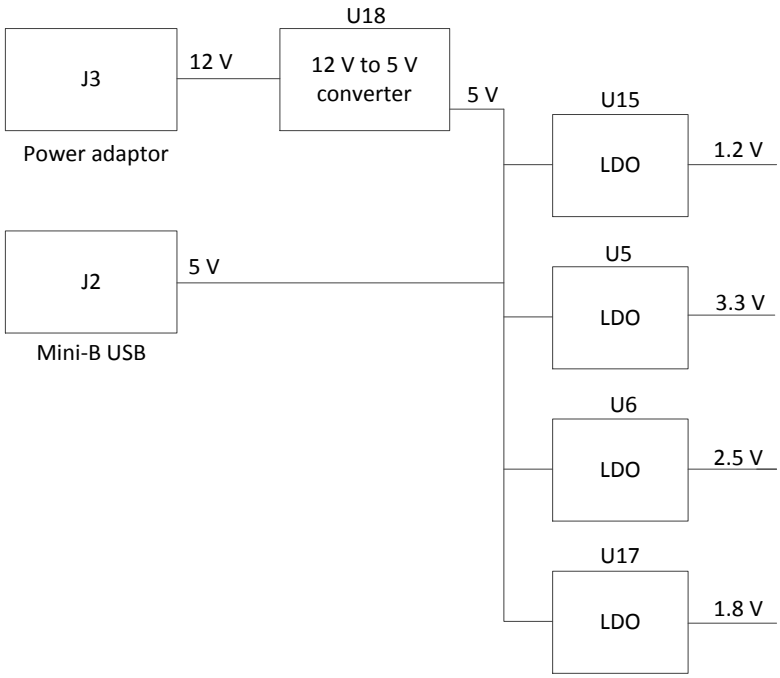


Figure 4.1. Power Supply Block

Table 4.1 lists the device power rails. There are five voltage regulators on the board used to supply the 5 V, 3.3 V, 2.5V 1.8 V, and 1.2 V rails. The input to these regulators is either from the Mini-B USB connector or the external 12 V adaptor that is connected to the board. Switch SW2 is used to connect or disconnect the external adaptor power to the board.

Table 4.1. Power LEDs

Voltage Rail	LEDs	Color
12	D26	Green
5	D3	Green
3.3	D25	Green
2.5	D29	Green
1.8	D28	Green
1.2	D27	Green

Table 4.2 on the next page lists the board voltage rails, including the rail source voltage, test point number, and current sense resistor number.

Table 4.2. Device Power Rail Summary and Test Points

Voltage Rail	Source Rail	Current Sense Resistor	Test Points
12 V	12_Ext	—	12V
5 V	12 V	—	5V
+3.3 V	5 V	—	3V3
+2.5 V	5 V	—	2V5
+1.8 V	5 V	—	1V8
+1.2 V	5 V	—	1V2
VCCCORE	+1.2 V	R19	VCC_CORE
VCCIO0	+3.3 V	R20	VCCIO0
VCCIO1	+3.3 V	R21	VCCIO1
VCCIO2	+3.3 V	R28	VCCIO2
VCC_DPHY	+1.2 V	R417	VCC_DPHY
1K_VCC_CORE	1.2 V	R190	1K_VCC_CORE
1K_VCCIO0	+3.3 V	R410	1K_VCCIO0
1K_VCCIO1	+3.3 V	R184	1K_VCCIO1
1K_VCCIO2	+3.3 V	R186	1K_VCCIO2
1K_VCCIO3	+3.3 V	R188	1K_VCCIO3

5. Status Indicators

The LED status indicators on the board show power, configuration, and application status. Table 5.1 lists the status LED I/O map.

Table 5.1. Status LED I/O Map

Device	LED	Net Name	Color
CrossLink	D6	CMOS_IO_1	Blue
CrossLink	D7	CMOS_IO_2	Blue
CrossLink	D8	CMOS_IO_3	Blue
CrossLink	D9	CMOS_IO_4	Blue
CrossLink	D10	CDONE	Green
LCMX03LF-1300E	D23	DONE	Red

6. SMA IO Link Board

The SMA IO Link board connects to the CrossLink LIF-MD6000 Master Link board's Tx or Rx connectors (U7, U9, U11 or U12) and transfers signals to the respective SMA connectors.

Table 6.1. Headers and Test Connectors

Part	Description	Mapping to U1
J1	SMA connector for DCK_TX_P	Pin 1
J2	SMA connector for DCK_TX_N	Pin 2
J3	SMA connector for DATA0_TX_P	Pin 4
J4	SMA connector for DATA0_TX_N	Pin 5
J5	SMA connector for DATA1_TX_P	Pin 7
J6	SMA connector for DATA1_TX_N	Pin 8
J7	SMA connector for DATA2_TX_P	Pin 13
J8	SMA connector for DATA2_TX_N	Pin 14
J9	SMA connector for DATA3_TX_P	Pin 16
J10	SMA connector for DATA3_TX_N	Pin 17
J11	SMA connector for DATA4_TX_P	Pin 24
J12	SMA connector for DATA4_TX_N	Pin 25
J13	SMA connector for DATA5_TX_P	Pin 27
J14	SMA connector for DATA5_TX_N	Pin 28
U1	Connector to interface to CrossLink Master Link board	N/A

Table 6.2. U1 Connector Description

Pin	Name
1	CH4_DCK_P
2	CH4_DCK_N
3	GND
4	CH4_DATA0_P
5	CH4_DATA0_N
6	GND
7	CH4_DATA1_P
8	CH4_DATA1_N
9	GND
10	SN
11	SCLK
12	GND
13	CH4_DATA2_P
14	CH4_DATA2_N
15	GND
16	CH4_DATA3_P
17	CH4_DATA3_N
18	GND
19	12V
20	12V

Pin	Name
21	TBD
22	RESETN
23	PWR_5-0V
24	GND
25	GND
26	PWR_3-3V
27	GND
28	GND
29	PWR_1-8V
30	MOSI
31	MISO
32	PWR_1-8V
33	GND
34	GND
35	PWR_3-3V
36	GND
37	GND
38	PWR_5-0V
39	SDA
40	SCL

Note: U1 connector pin names may be different than the actual signal depending on which CrossLink LIF-MD6000 Master Link board connector this daughter board is connected to.

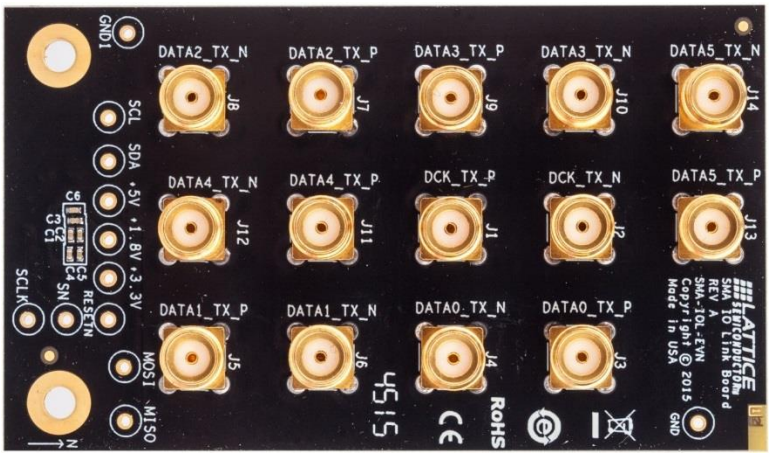


Figure 6.1. Top View of SMA IO Link Board

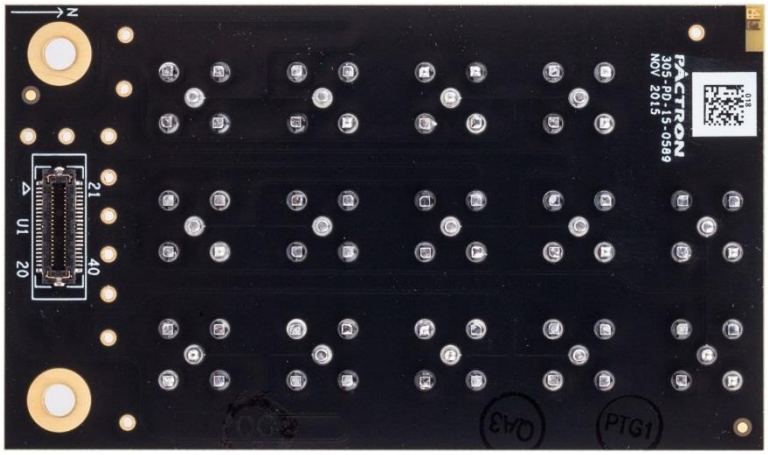


Figure 6.2. Bottom View of SMA IO Link Board

7. Breakout IO Link Board

The Breakout IO Link board connects to the CrossLink LIF-MD6000 Master Link board's Tx or Rx connectors (U7, U9, U11 or U12) and transfers signals to the 26-pin header (J2).

Table 7.1. Headers and Test Connectors

Part	Description	Setting
J2	13x2 Header	—
U1	Connector to interface to CrossLink Master Link board	—

Table 7.2. U1 Connector Description

Pin	Name
1	CH4_DCK_P
2	CH4_DCK_N
3	GND
4	CH4_DATA0_P
5	CH4_DATA0_N
6	GND
7	CH4_DATA1_P
8	CH4_DATA1_N
9	GND
10	SN
11	SCLK
12	GND
13	CH4_DATA2_P
14	CH4_DATA2_N
15	GND
16	CH4_DATA3_P
17	CH4_DATA3_N
18	GND
19	12V
20	12V

Pin	Name
21	TBD
22	RESETN
23	PWR_5-0V
24	GND
25	GND
26	PWR_3-3V
27	GND
28	GND
29	PWR_1-8V
30	MOSI
31	MISO
32	PWR_1-8V
33	GND
34	GND
35	PWR_3-3V
36	GND
37	GND
38	PWR_5-0V
39	SDA
40	SCL

Note: U1 connector pin names may be different than the actual signal depending on which CrossLink LIF-MD6000 Master Link board connector this daughter board is connected to.

Table 7.3. J2 Header Description

Pin	Name	Mapping to U1
1	+3.3V	N/A
2	+1.8V	N/A
3	RESETN	Pin 22
4	CH4_DCK_TX_P	Pin 1
5	SDA	Pin 39
6	CH4_DCK_TX_N	Pin 2
7	SCL	Pin 40
8	GND	N/A
9	GND	N/A
10	CH4_DATA0_TX_P	Pin 4
11	CH4_DATA3_TX_P	Pin 16
12	CH4_DATA0_TX_N	Pin 5
13	CH4_DATA3_TX_N	Pin 17
14	GND	N/A
15	GND	N/A
16	CH4_DATA1_TX_P	Pin 7
17	CH4_DATA4_TX_P	Pin 24
18	CH4_DATA1_TX_N	Pin 8
19	CH4_DATA4_TX_N	Pin 25
20	GND	N/A
21	GND	N/A
22	CH4_DATA2_TX_P	Pin 13
23	CH4_DATA5_TX_P	Pin 27
24	CH4_DATA2_TX_N	Pin 14
25	CH4_DATA5_TX_N	Pin 28
26	GND	N/A

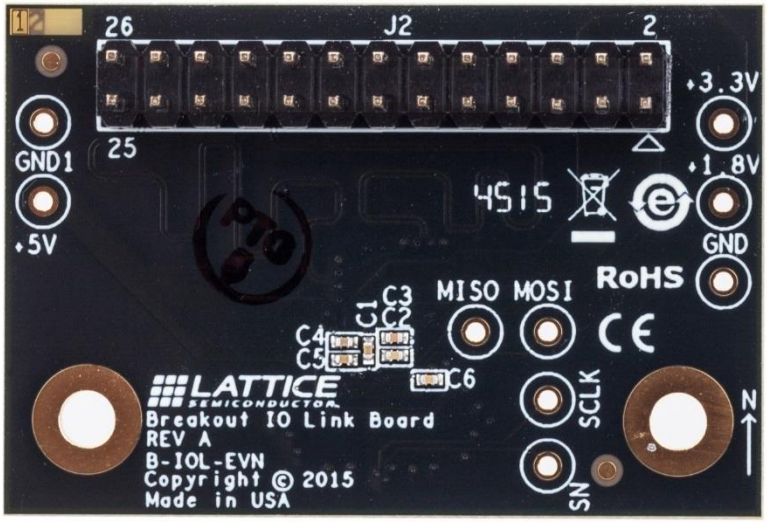


Figure 7.1. Top View of Breakout IO Link Board

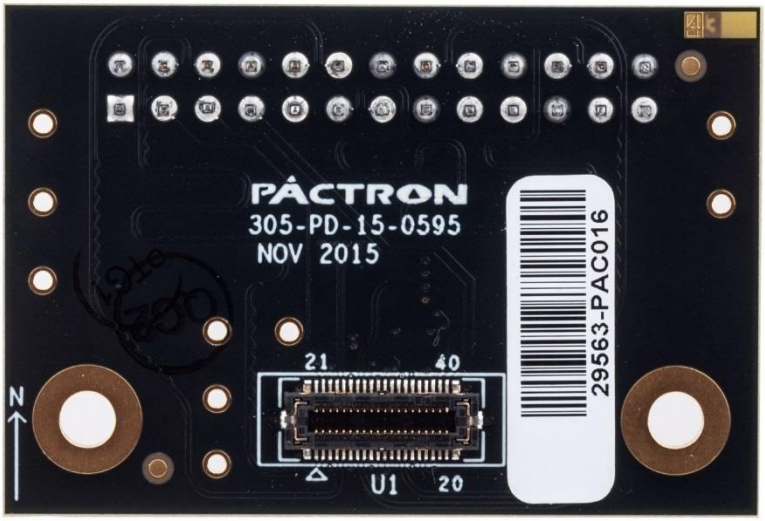


Figure 7.2. Bottom View of Breakout IO Link Board

8. Ordering Information

Table 8.1. Ordering Information

Description	Ordering Part Number	China RoHS Environment-Friendly Use Period (EFUP)
CrossLink: LIF-MD6000 Master Link Board (Includes 1 SMA IO Link Board and 1 Breakout IO Link Board)	LIF-MD6000-ML-EVN	
CrossLink: LIF-MD6000 IO Link Boards (Includes 1 SMA IO Link Board and 1 Breakout IO Link Board)	LIFMD-IOL-EVN	

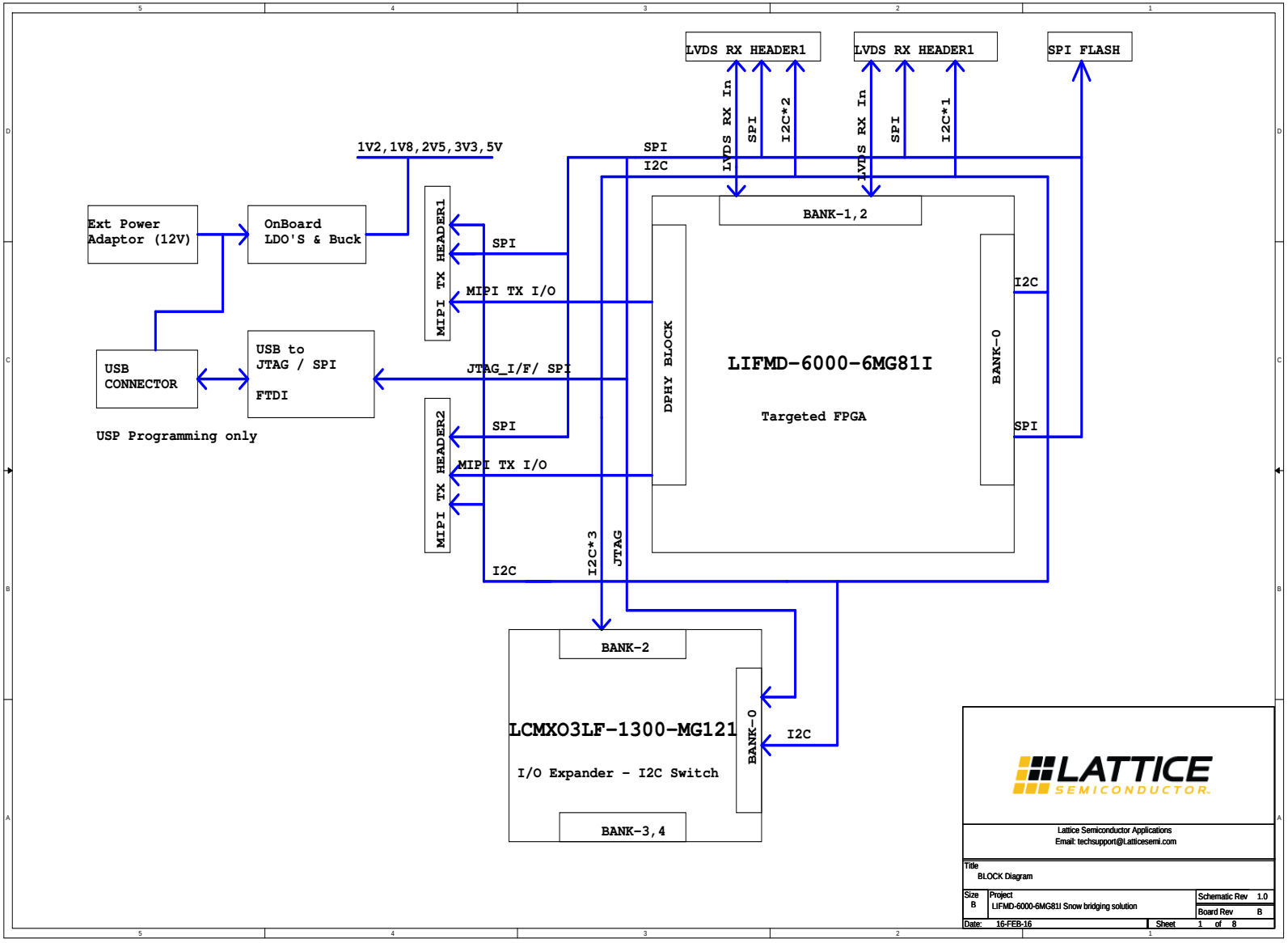
References

For more information, refer to FPGA-DS-02007 (previously DS1055), CrossLink Family Data Sheet

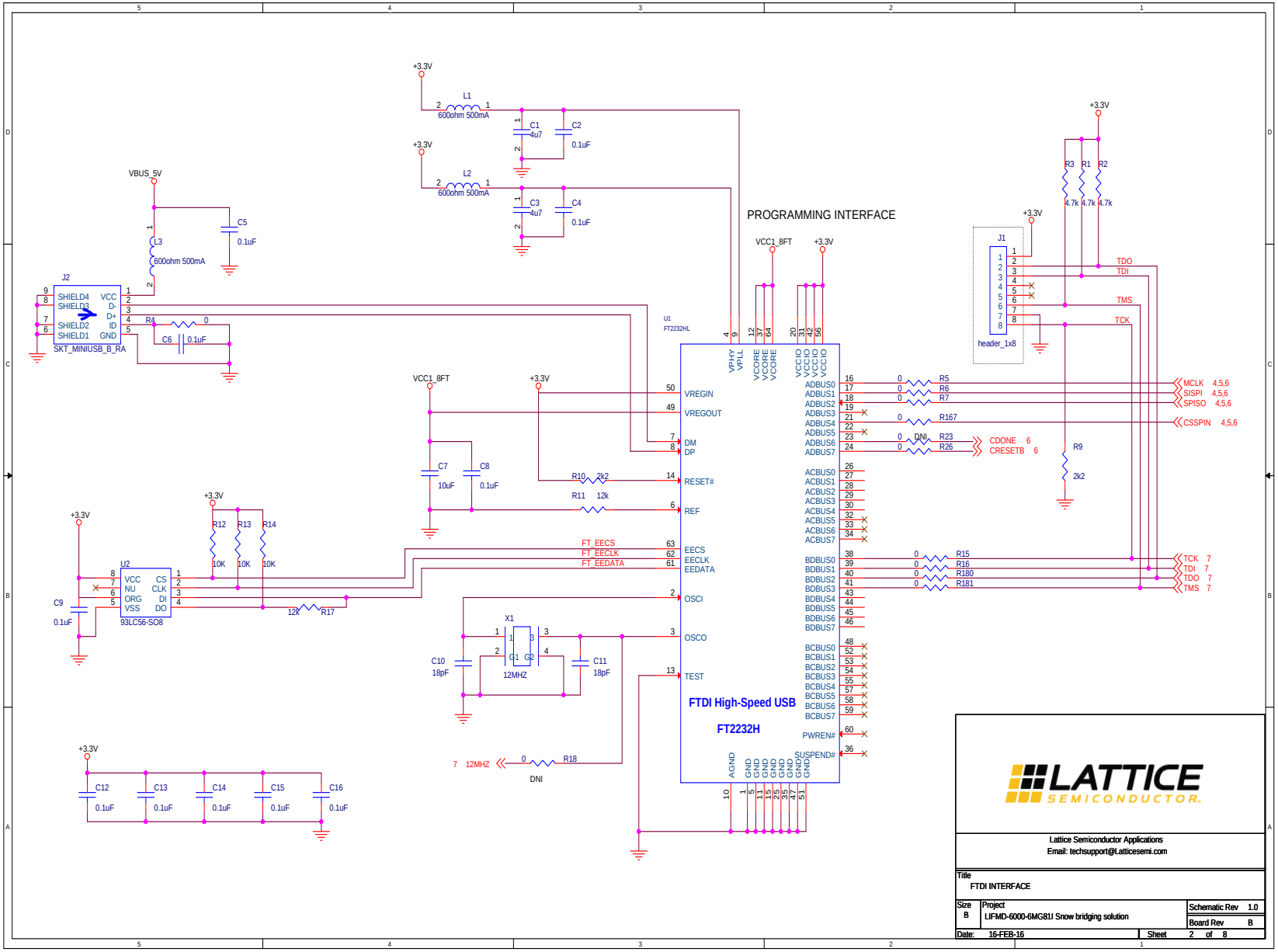
Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

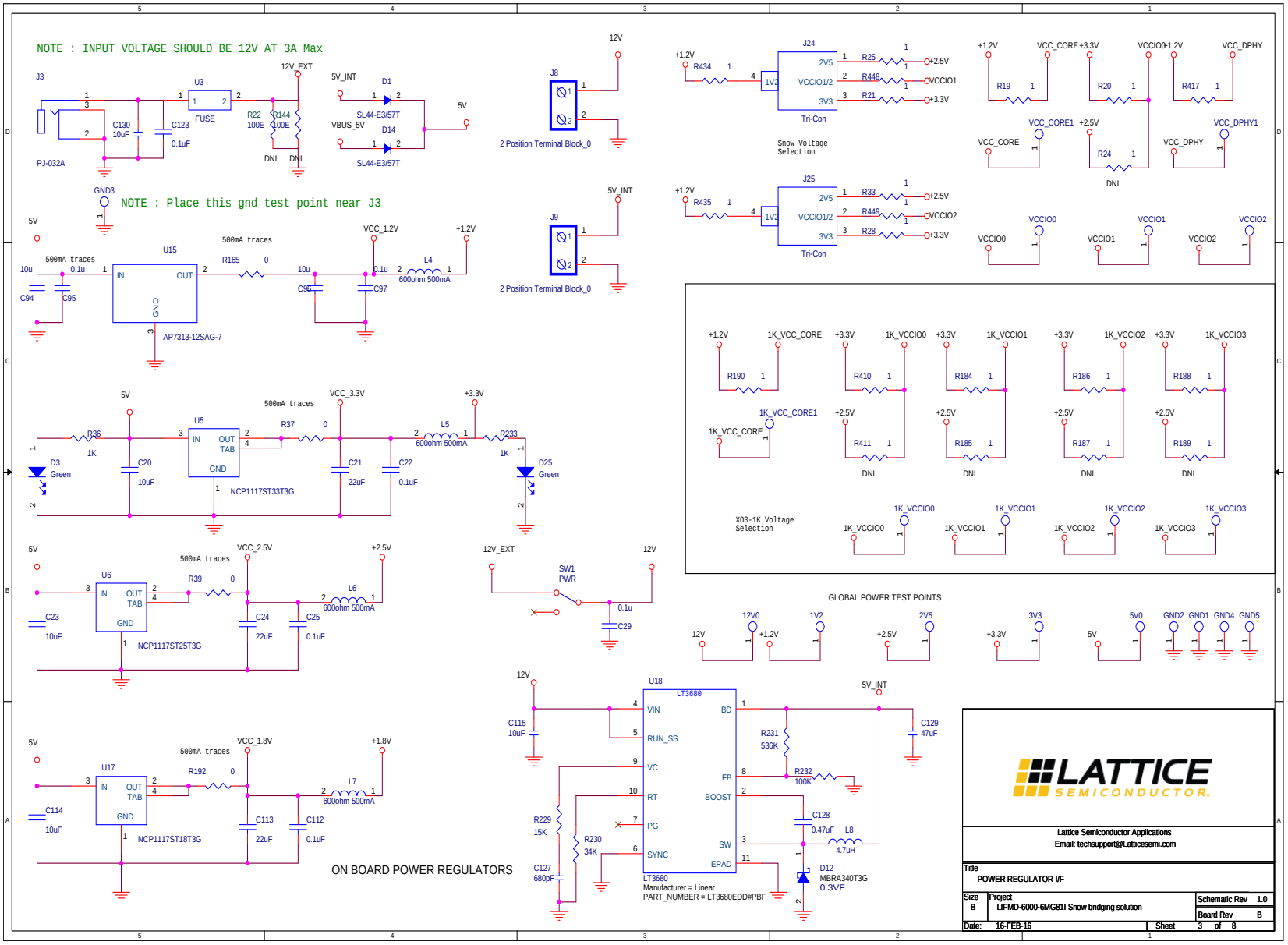
Appendix A. LIF-MD6000-ML-EVN-BRD Schematics



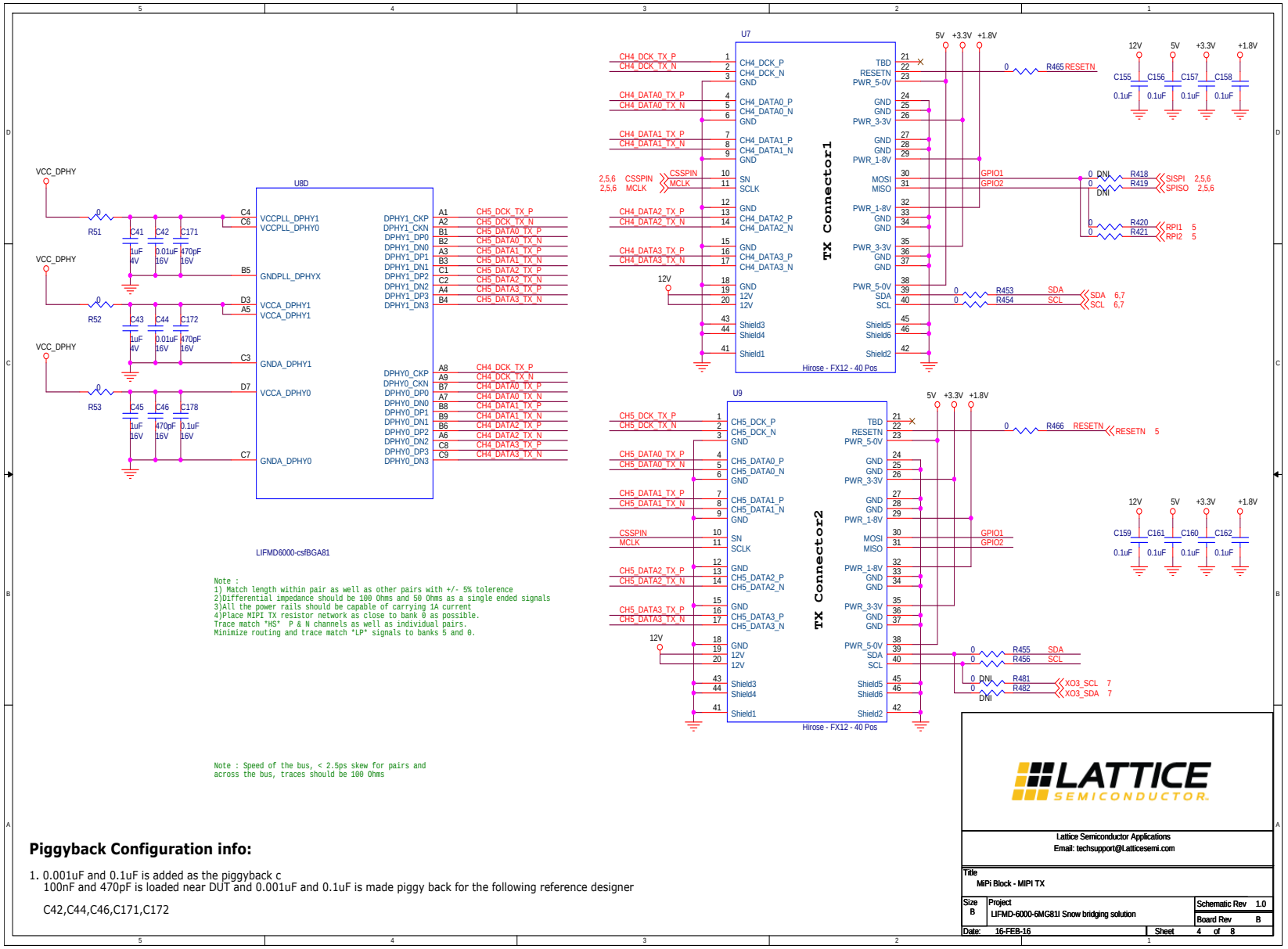
LIF-MD6000 Master Link Board Block Diagram



FTDI Interface



Power Regulator Interface

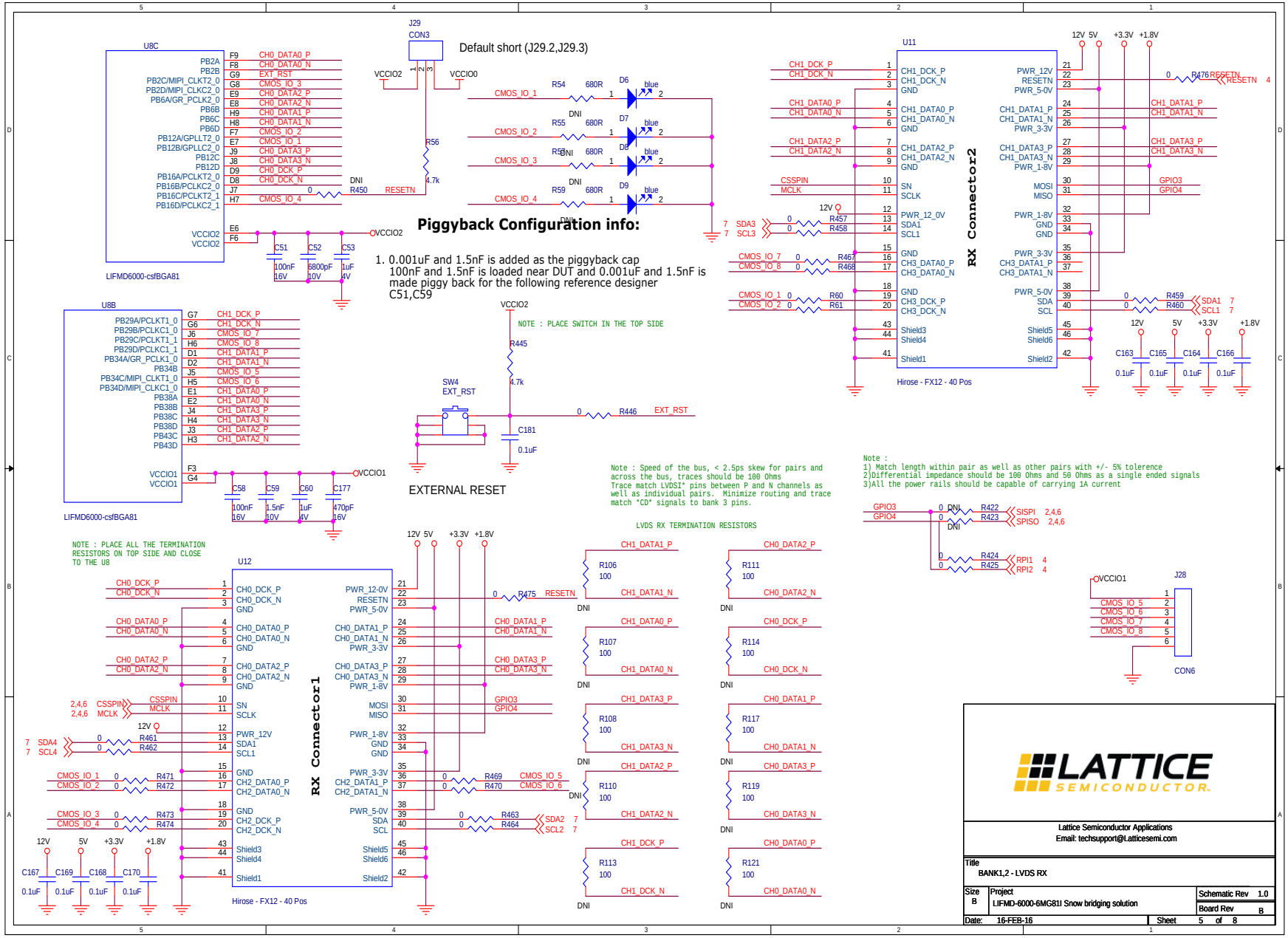


Piggyback Configuration info:

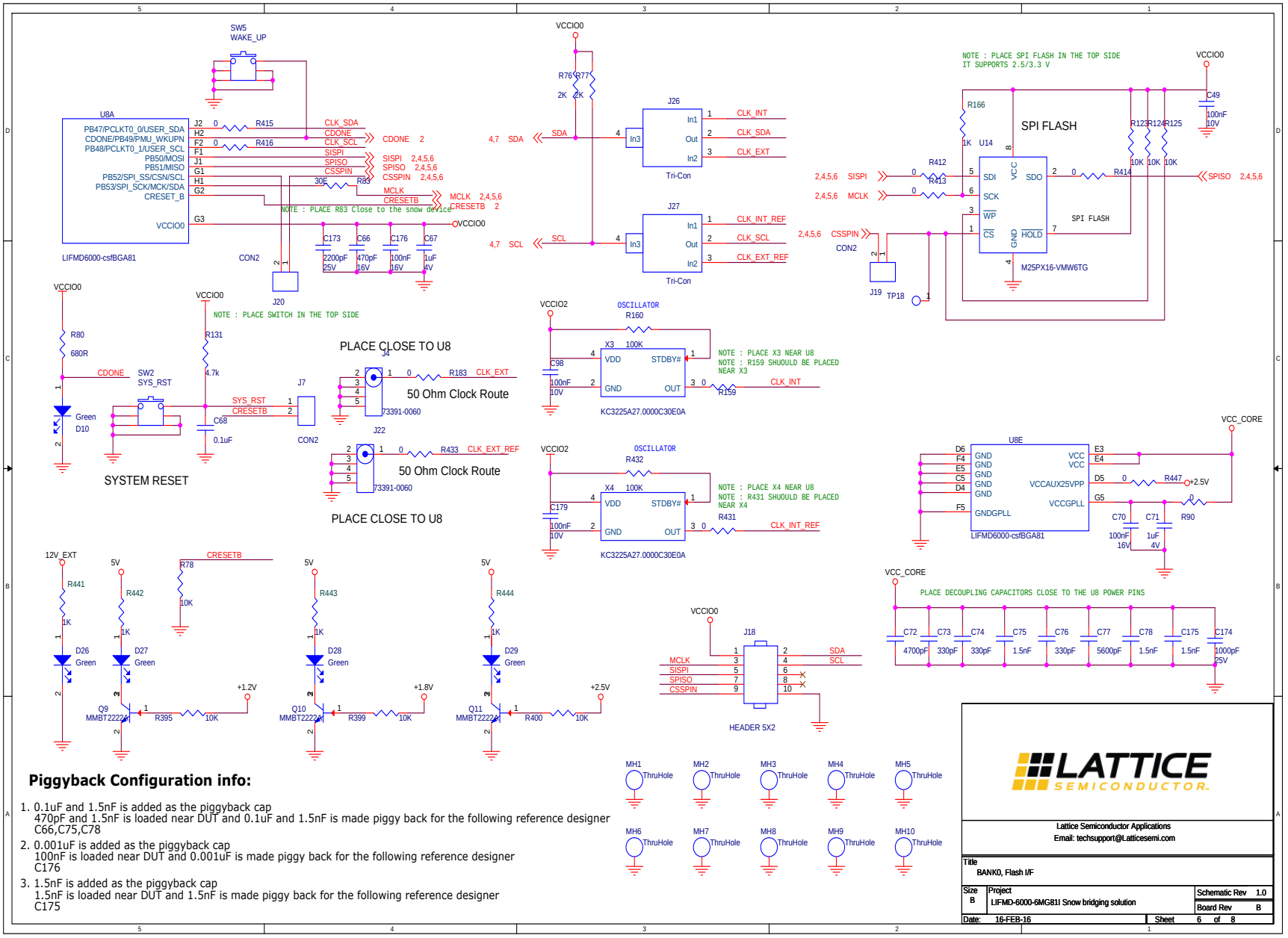
1. 0.001uF and 0.1uF is added as the piggyback c
   100nF and 470pF is loaded near DUT and 0.001uF and 0.1uF is made piggy back for the following reference designer

   C42,C44,C46,C171,C172

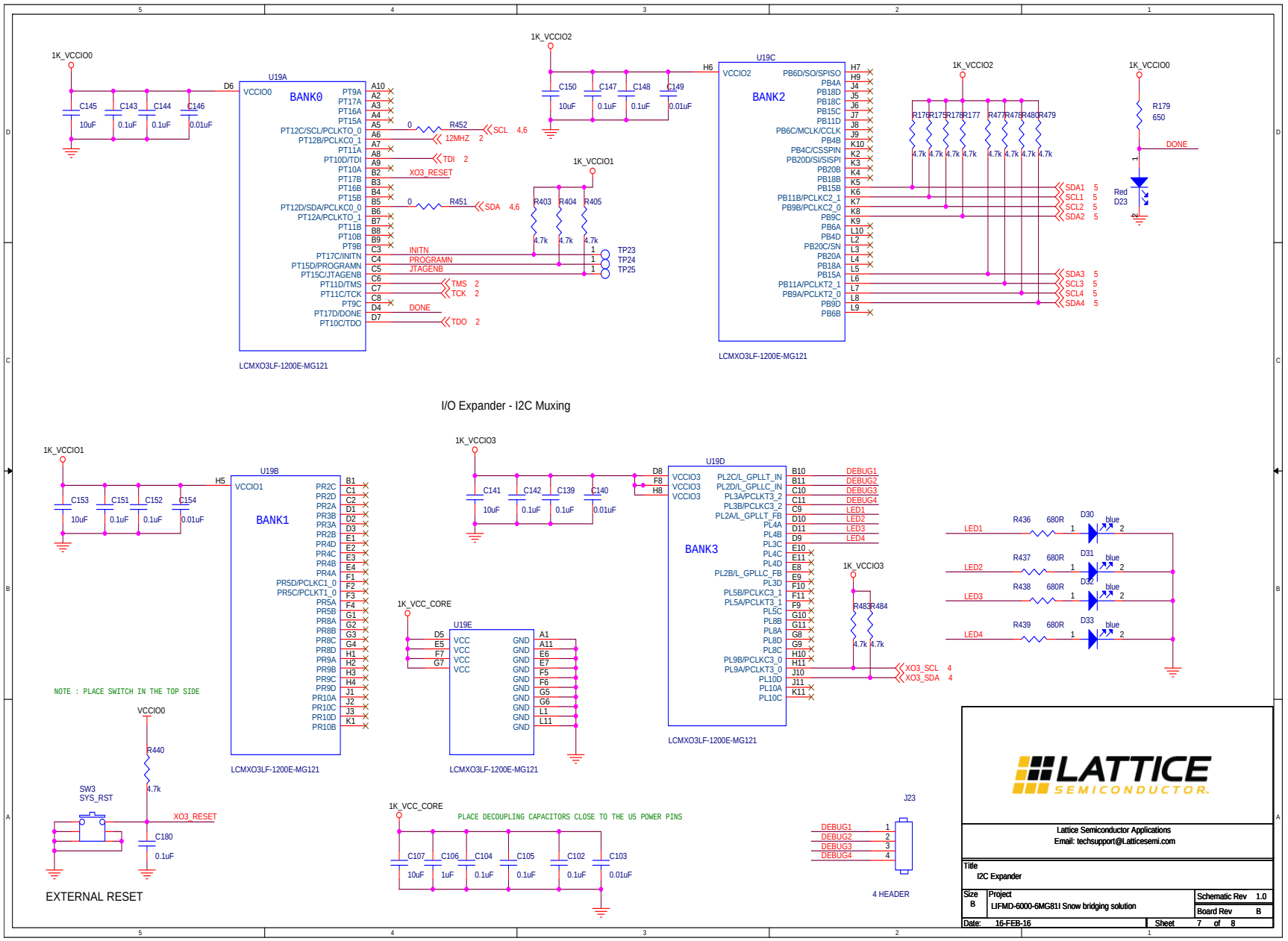
MIPI Block – MIPI Tx



Bank 1, 2 – LVDS Rx



Bank0, Flash Interface



I²C Expander