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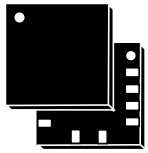
LIS2DS12

MEMS digital output motion sensor: ultra-low-power high-performance 3-axis "pico" accelerometer

Datasheet - production data



LGA-12 (2.0x2.0x0.86 mm)

Features

- Supply voltage, 1.62 V to 1.98 V
- Independent IOs supply (1.8 V) and supply voltage compatible
- Ultra-low power consumption
- ±2g/±4g/±8*g*/±16*g* full scale
- High-speed I^2C/SPI digital output interface
- Low noise
- 16-bit data output
- Embedded temperature sensor
- Self-test
- 256-level FIFO
- 10000 *g* high shock survivability
- ECOPACK®, RoHS and “Green” compliant

Applications

- Motion-activated functions and user interfaces
- Gesture recognition and gaming
- Pedometer, step detector and step counters
- Display orientation
- Sensor hub function
- Tilt function
- Tap/double-tap recognition
- 6D/4D orientation
- Free-fall detection
- Smartpower saving for handheld devices
- Impact recognition and logging

Description

The LIS2DS12 is an ultra-low-power high-performance three-axis linear accelerometer belonging to the “pico” family which leverages on the robust and mature manufacturing processes already used for the production of micromachined accelerometers.

The LIS2DS12 has user-selectable full scales of ±2g/±4g/±8g/±16*g* and is capable of measuring accelerations with output data rates from 1 Hz to 6400 Hz.

The LIS2DS12 has an integrated 256-level first-in, first-out (FIFO) buffer allowing the user to store data in order to limit intervention by the host processor.

The embedded self-test capability allows the user to check the functioning of the sensor in the final application.

The LIS2DS12 has a dedicated internal engine architecture in order to process internally motion and acceleration detection including free-fall, wakeup, single and double-tap detection, activity-inactivity, portrait and landscape detection, step counter and step detection along with significant motion detection.

The LIS2DS12 is available in a small thin plastic land grid array package (LGA) and it is guaranteed to operate over an extended temperature range from -40 °C to +85 °C.

Table 1. Device summary

Order codes	Temperature range [°C]	Package	Packaging
LIS2DS12	-40 to +85	LGA-12	Tray
LIS2DS12TR	-40 to +85	LGA-12	Tape and reel

Contents

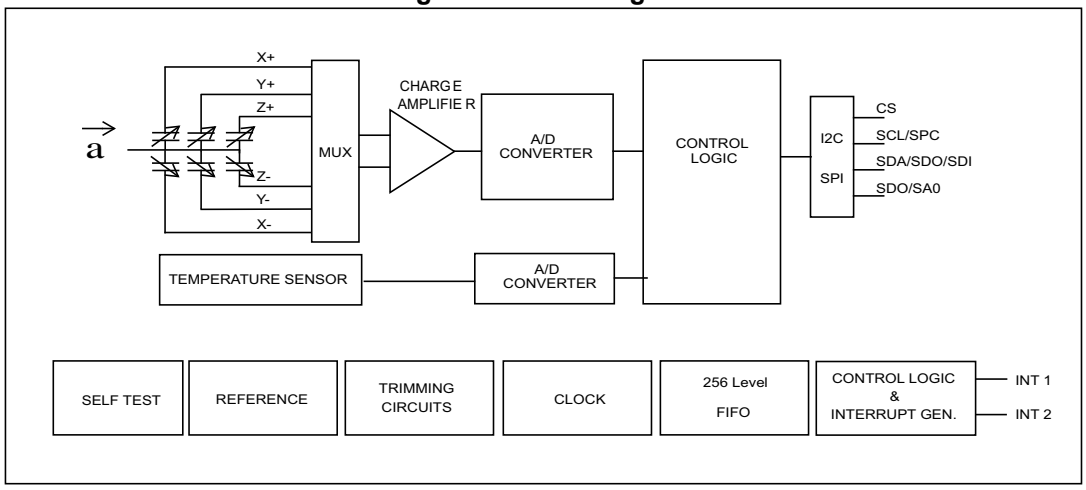
List of tables

List of figures

1 Block diagram and pin description

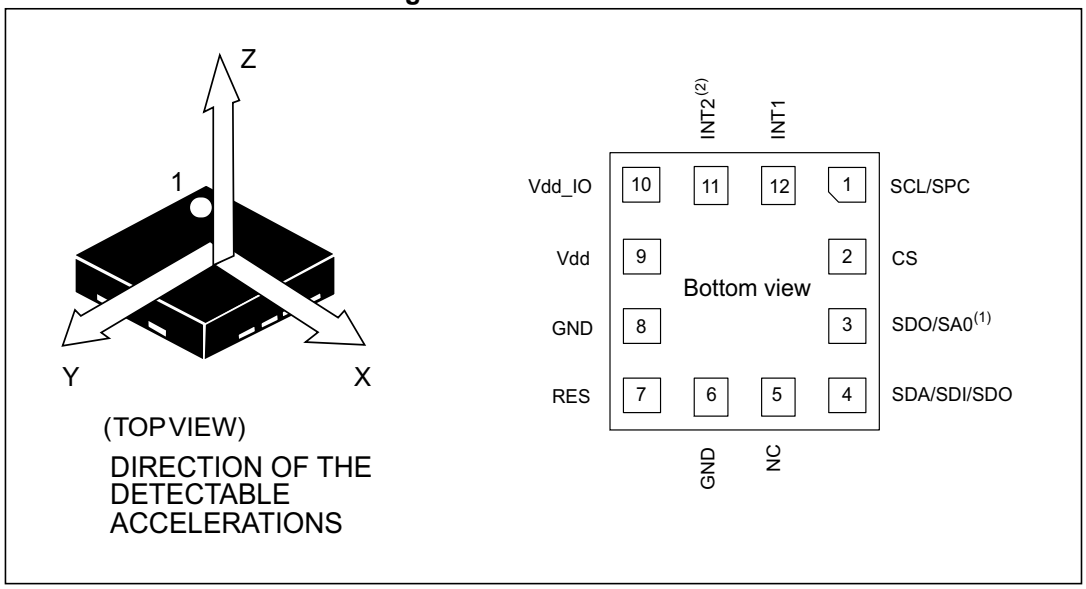
1.1 Block diagram

Figure 1. Block diagram



1.2 Pin description

Figure 2. Pin connections



1. When the sensor hub is used, this pin is the I^2C data master line (MSDA).
2. When sensor hub is used, this pin is the I^2C clock master line (MSCL).

Table 2. Pin description

Pin#	Name	Function
1	SCL SPC	I^2C serial clock (SCL) SPI serial port clock (SPC)
2(1)	CS	SPI enable I^2C/SPI mode selection (1: SPI idle mode / I^2C communication enabled; 0: SPI communication mode / I^2C disabled)
3(2)	SDO SA0	SPI serial data output (SDO) I^2C less significant bit of the device address (SA0)
4	SDA SDI SDO	I^2C serial data (SDA) SPI serial data input (SDI) 3-wire interface serial data output (SDO)
5	NC	Internally not connected. Can be tied to VDD, VDDIO or GND.
6	GND	0 V supply
7	RES	Connect to GND
8	GND	0 V supply
9	Vdd	Power supply
10	Vdd_IO	Power supply for I/O pins
11(3)	INT2	Interrupt pin 2
12	INT1	Interrupt pin 1

1. CS has an active pull-up and can be left unconnected
2. When the sensor hub is used, this pin is the I^2C data master line (MSDA), is internally set to 0 and can be internally pulled up through the TUD_EN bit of *FUNC_CTRL (3Fh)*.
3. When sensor hub is used, this pin is the I^2C clock master line (MSCL) and can be internally pulled up through the TUD_EN bit of *FUNC_CTRL (3Fh)*.

2 Mechanical and electrical specifications

2.1 Mechanical characteristics

Table 3. Mechanical characteristics @ Vdd = 1.8 V, T = 25 °C unless otherwise noted (1)

Symbol	Parameter	Test conditions	Min.	Typ.(2)	Max.	Unit
FS	Measurement range			±2		*g*
				±4		
				±8		
				±16		
So	Sensitivity 16-bit(3)	@ FS ±2 *g*		0.061		mg/digit
		@ FS ±4 *g*		0.122		
		@ FS ±8 *g*		0.244		
		@ FS ±16 *g*		0.488		
An	Noise density - high-performance mode (HR or HF mode)(4)	@ FS ±2 *g*		120		µg/√Hz
		@ FS ±4 *g*		150		
		@ FS ±8 *g*		200		
		@ FS ±16 *g*		300		
RMS	RMS noise - low-power mode(5)	@ FS ±2 *g*		6.3		mg(RMS)
		@ FS ±4 *g*		8.2		
		@ FS ±8 *g*		11		
		@ FS ±16 *g*		17		
Off, board	Zero-*g* offset on soldered board(6)			±30		mg
TCO	Zero-*g* offset change vs. temperature			±0.2		mg/°C
TCS	Sensitivity change vs. temperature			0.01		%/°C
ST	Self-test positive difference(7)		70		1500	mg

1. The product is factory calibrated at 1.8 V. The operational power supply range is from 1.62 V to 1.98 V.
2. Typical specifications are not guaranteed.
3. Sensitivity calculated at 16-bit.
4. Noise density is the same for all ODR.
5. RMS noise is the same for all ODR.
6. Offset can be eliminated by enabling the slope filter.
7. “Self-test positive difference” is defined as: OUTPUT[mg]$_{(CTRL3\ ST2,\ ST1\ bits=01)}$ - OUTPUT[mg]$_{(CTRL3\ ST2,\ ST1\ bits=00)}$ in steady state.

2.2 Electrical characteristics

Table 4. Electrical characteristics @ Vdd = 1.8 V, T = 25 °C unless otherwise noted (1)

Symbol	Parameter	Test conditions	Min.	Typ.(2)	Max.	Unit
Vdd	Supply voltage		1.62	1.8	1.98	V
Vdd_IO	I/O pins supply voltage(3)		1.62		Vdd+0.1	V
IddHR	Current consumption in high-resolution mode	@ ODR range 12.5 Hz - 6400 Hz, 12-14 bit		150		µA
IddLP	Current consumption in low-power mode	ODR 100 Hz		12.5		µA
		ODR 50 Hz		8		
		ODR 12.5 Hz		4		
		ODR 1 Hz		2.5		
Idd_PD	Current consumption in power-down			0.7		µA
V_{IH}	Digital high-level input voltage		0.8*Vdd_IO			V
V_{IL}	Digital low-level input voltage				0.2*Vdd_IO	V
V_{OH}	Digital high-level output voltage	I_{OH} = 4 mA(4)	VDD_IO - 0.2 V			
V_{OL}	Digital low-level output voltage	I_{OL} = 4 mA(4)			0.2 V	

1. The product is factory calibrated at 1.8 V. The operational power supply range is from 1.62 V to 1.98 V.
2. Typical specifications are not guaranteed.
3. It is possible to remove Vdd maintaining Vdd_IO without blocking the communication busses. In this condition the measurement chain is powered off.
4. 4 mA is the maximum driving capability, ie. the maximum DC current that can be sourced/sunk by the digital pad in order to guarantee the correct digital output voltage levels V_{OH} and V_{OL}.

2.3 Temperature sensor characteristics

@ Vdd =1.8 V, T=25 °C unless otherwise noted

Table 5. Temperature sensor characteristics

Symbol	Parameter	Min.	Typ.(1)	Max.	Unit
Top	Operating temperature range	-40		+85	°C
Toff	Temperature offset(2)	-15		+15	°C
TSDr	Temperature sensor output change vs. temperature		1		LSB/°C(3)
TODR	Temperature refresh rate		12.5		Hz

1. Typical specifications are not guaranteed.
2. The output of the temperature sensor is 0 LSB (typ.) at 25 °C.
3. 8-bit resolution.

2.4 Communication interface characteristics

2.4.1 SPI - serial peripheral interface

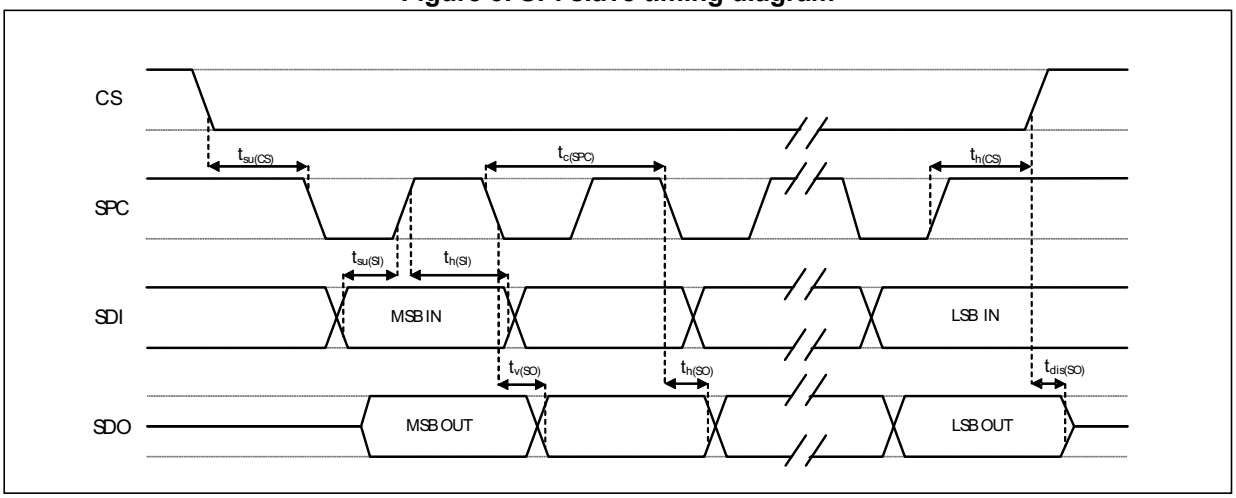
Subject to general operating conditions for Vdd and Top.

Table 6. SPI slave timing values

Symbol	Parameter	Value(1)		Unit
		Min	Max	
$t_{c(SPC)}$	SPI clock cycle	100		ns
$f_{c(SPC)}$	SPI clock frequency		10	MHz
$t_{su(CS)}$	CS setup time	6		ns
$t_{h(CS)}$	CS hold time	8		
$t_{su(SI)}$	SDI input setup time	5		
$t_{h(SI)}$	SDI input hold time	15		
$t_{v(SO)}$	SDO valid output time		50	
$t_{h(SO)}$	SDO output hold time	9		
$t_{dis(SO)}$	SDO output disable time		50	

1. 10 MHz clock frequency for SPI with both 4 and 3 wires, based on characterization results, not tested in production.

Figure 3. SPI slave timing diagram



Note: Measurement points are done at 0.2·Vdd_IO and 0.8·Vdd_IO, for both input and output ports.

2.4.2 I²C - inter-IC control interface

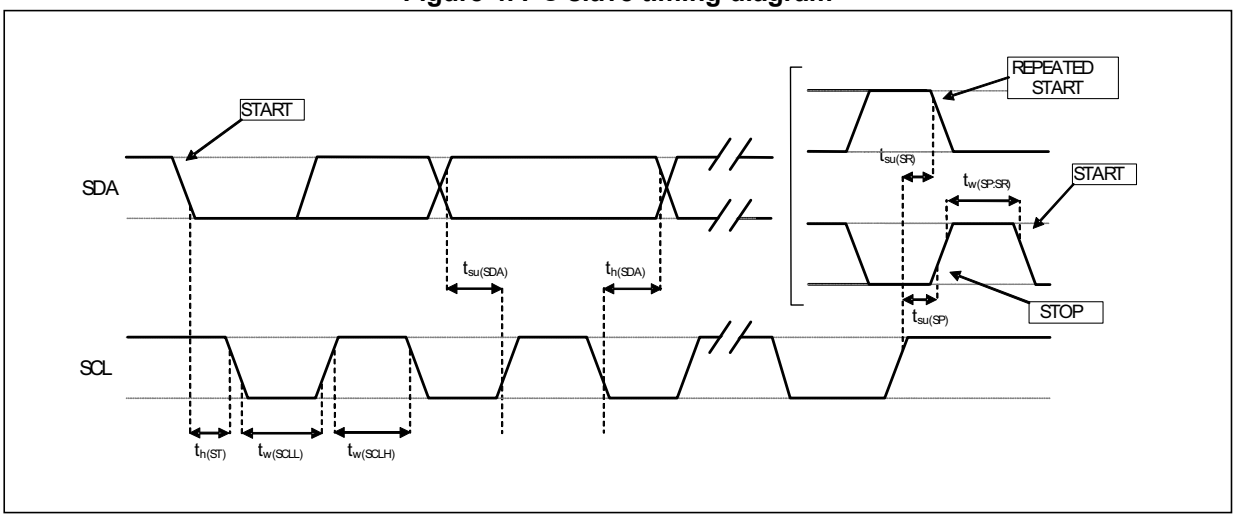
Subject to general operating conditions for Vdd and Top.

Table 7. I²C slave timing values

Symbol	Parameter	I²C standard mode (1)		I²C fast mode (1)		Unit
		Min	Max	Min	Max	
$f_{(SCL)}$	SCL clock frequency	0	100	0	400	kHz
$t_{w(SCLL)}$	SCL clock low time	4.7		1.3		µs
$t_{w(SCLH)}$	SCL clock high time	4.0		0.6		
$t_{su(SDA)}$	SDA setup time	250		100		ns
$t_{h(SDA)}$	SDA data hold time	0.01	3.45	0.01	0.9	µs
$t_{h(ST)}$	START condition hold time	4		0.6		µs
$t_{su(SR)}$	Repeated START condition setup time	4.7		0.6		
$t_{su(SP)}$	STOP condition setup time	4		0.6		
$t_{w(SP:SR)}$	Bus free time between STOP and START condition	4.7		1.3		

1. Data based on standard I²C protocol requirement, not tested in production

Figure 4. I²C slave timing diagram



Note: Measurement points are done at 0.2·Vdd_IO and 0.8·Vdd_IO, for both ports.

Table 8. I^2C high-speed mode specifications at 1 MHz and 3.4 MHz

	Symbol	Parameter	Min	Max	Unit
Fast mode plus(1)	f_{SCL}	SCL clock frequency	0	1	MHz
	$t_{HD;STA}$	Hold time (repeated) START condition	260	-	ns
	t_{LOW}	Low period of the SCL clock	500	-	
	t_{HIGH}	High period of the SCL clock	260	-	
	$t_{SU;STA}$	Setup time for a repeated START condition	260	-	
	$t_{HD;DAT}$	Data hold time	0	-	
	$t_{SU;DAT}$	Data setup time	50	-	
	t_{rDA}	Rise time of SDA signal	-	120	
	t_{fDA}	Fall time of SDA signal	-	120	
	t_{rCL}	Rise time of SCL signal	20*Vdd/5.5	120	
	t_{fCL}	Fall time of SCL signal	20*Vdd/5.5	120	
	$t_{SU;STO}$	Setup time for STOP condition	260	-	
	C_b	Capacitive load for each bus line	-	550	pF
	$t_{VD;DAT}$	Data valid time	-	450	ns
	$t_{VD;ACK}$	Data valid acknowledge time	-	450	
	V_{nL}	Noise margin at low level	0.1Vdd	-	V
	V_{nH}	Noise margin at high level	0.2Vdd	-	
	t_{SP}	Pulse width of spikes that must be suppressed by the input filter	0	50	ns
High-speed mode(1)	f_{SCLH}	SCLH clock frequency	0	3.4	MHz
	$t_{SU;STA}$	Setup time for a repeated START condition	160	-	ns
	$t_{HD;STA}$	Hold time (repeated) START condition	160	-	
	t_{LOW}	Low period of the SCLH clock	160	-	
	t_{HIGH}	High period of the SCLH clock	60	-	
	$t_{SU;DAT}$	Data setup time	10	-	
	$t_{HD;DAT}$	Data hold time	0	70	
	t_{rCL}	Rise time of SCLH signal	10	40	
	t_{rCL1}	Rise time of SCLH signal after a repeated START condition and after an acknowledge bit	10	80	
	t_{fCL}	Fall time of SCLH signal	10	40	
	t_{rDA}	Rise time of SDAH signal	10	80	
	t_{fDA}	Fall time of SDAH signal	10	80	
	$t_{SU;STO}$	Setup time for STOP condition	160	-	
	C_b	Capacitive load for each bus line	-	100	pF
	V_{nH}	Noise margin at high level	0.2Vdd	-	V
	t_{SP}	Pulse width of spikes that must be suppressed by the input filter	0	10	ns

1. Data based on characterization, not tested in production

2.5 Absolute maximum ratings

Stresses above those listed as “absolute maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 9. Absolute maximum ratings

Symbol	Ratings	Maximum value	Unit
Vdd	Supply voltage	-0.3 to 2.2	V
Vdd_IO	I/O pins supply voltage	-0.3 to 2.2	V
Vin	Input voltage on any control pin (CS, SCL/SPC, SDA/SDI/SDO, SDO/SA0)	-0.3 to Vdd_IO +0.3	V
A_{POW}	Acceleration (any axis, powered, Vdd = 1.8 V)	3000 for 0.5 ms	*g*
		10000 for 0.2 ms	*g*
A_{UNP}	Acceleration (any axis, unpowered)	3000 for 0.5 ms	*g*
		10000 for 0.2 ms	*g*
T_{OP}	Operating temperature range	-40 to +85	°C
T_{STG}	Storage temperature range	-40 to +125	°C
ESD	Electrostatic discharge protection	2 (HBM)	kV

Note: Supply voltage on any pin should never exceed 2.2 V.

This device is sensitive to mechanical shock, improper handling can cause permanent damage to the part.

This device is sensitive to electrostatic discharge (ESD), improper handling can cause permanent damage to the part.

2.6 Terminology

2.6.1 Zero-*g* offset

Zero-*g* offset describes the deviation of an actual output signal from the ideal output signal if no acceleration is present. A sensor in a steady state on a horizontal surface will measure 0 *g* on the X-axis and 0 *g* on the Y-axis whereas the Z-axis will measure 1 *g*. The output is ideally in the middle of the dynamic range of the sensor (content of OUT registers 00h, data expressed as two's complement number). A deviation from ideal value in this case is called Zero-*g* offset. Offset is to some extent a result of stress to the MEMS sensor and therefore the offset can slightly change after mounting the sensor onto a printed circuit board or exposing it to extensive mechanical stress. Offset changes little over temperature, see "Zero-*g* offset change vs. temperature".

2.6.2 Sensitivity

Sensitivity describes the gain of the sensor and can be determined by applying 1 *g* acceleration to it. As the sensor can measure DC accelerations this can be done easily by pointing the axis of interest towards the center of the Earth, noting the output value, rotating the sensor by 180 degrees (pointing to the sky) and noting the output value again. By doing so, ±1 *g* acceleration is applied to the sensor. Subtracting the larger output value from the smaller one, and dividing the result by 2, leads to the actual sensitivity of the sensor. This value changes very little over temperature and time. The sensitivity tolerance describes the range of sensitivities of a large population of sensors.

2.6.3 Self-test

The self-test allows checking the sensor functionality without moving it. The self-test function is off when the self-test bits (ST) are programmed to '00'. When the self-test bits are changed, an actuation force is applied to the sensor, simulating a definite input acceleration. In this case the sensor outputs will exhibit a change in their DC levels which are related to the selected full scale through the device sensitivity. When the self-test is activated, the device output level is given by the algebraic sum of the signals produced by the acceleration acting on the sensor and by the electrostatic test-force. If the output signals change within the amplitude specified in *Table 3*, then the sensor is working properly and the parameters of the interface chip are within the defined specifications.

2.7 Sensing element

A proprietary process is used to create a surface micromachined accelerometer. The technology allows processing suspended silicon structures which are attached to the substrate in a few points called anchors and are free to move in the direction of the sensed acceleration. In order to be compatible with the traditional packaging techniques, a cap is placed on top of the sensing element to avoid blocking the moving parts during the molding phase of the plastic encapsulation. When an acceleration is applied to the sensor the proof mass displaces from its nominal position, causing an imbalance in the capacitive half-bridge. This imbalance is measured using charge integration in response to a voltage pulse applied to the capacitor.

At steady-state the nominal value of the capacitors are a few pF and when an acceleration is applied, the maximum variation of the capacitive load is in the fF range.

2.8 IC interface

The complete measurement chain is composed of a low-noise capacitive amplifier which converts the capacitive unbalancing of the MEMS sensor into an analog voltage using an analog-to-digital converter.

The acceleration data may be accessed through an I^2C/SPI interface thus making the device particularly suitable for direct interfacing with a microcontroller.

The LIS2DS12 features a data-ready signal which indicates when a new set of measured acceleration data is available, thus simplifying data synchronization in the digital system that uses the device.

3 Factory calibration

The IC interface is factory-calibrated for sensitivity (So) and Zero-*g* offset.

The trim values are stored inside the device in nonvolatile memory. Any time the device is turned on, the trimming parameters are downloaded into the registers to be used during active operation. This allows using the device without further calibration.

4 Application hints

Figure 5. LIS2DS12 electrical connections in standard configuration (top view)

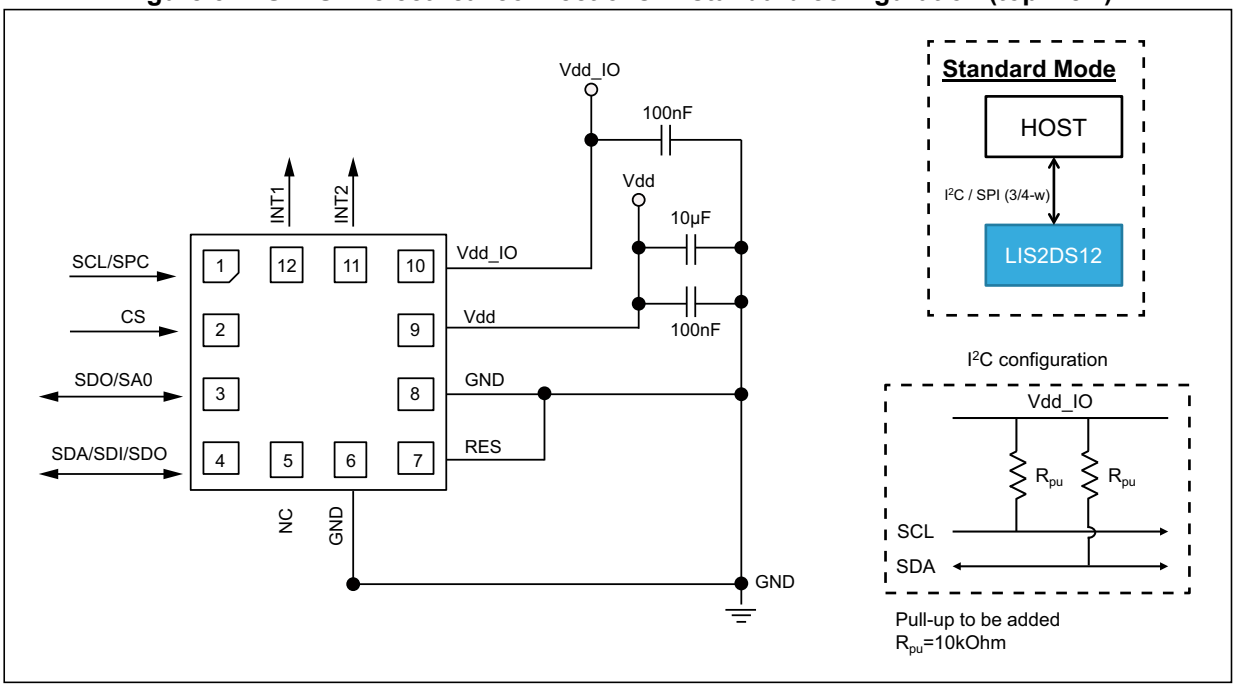
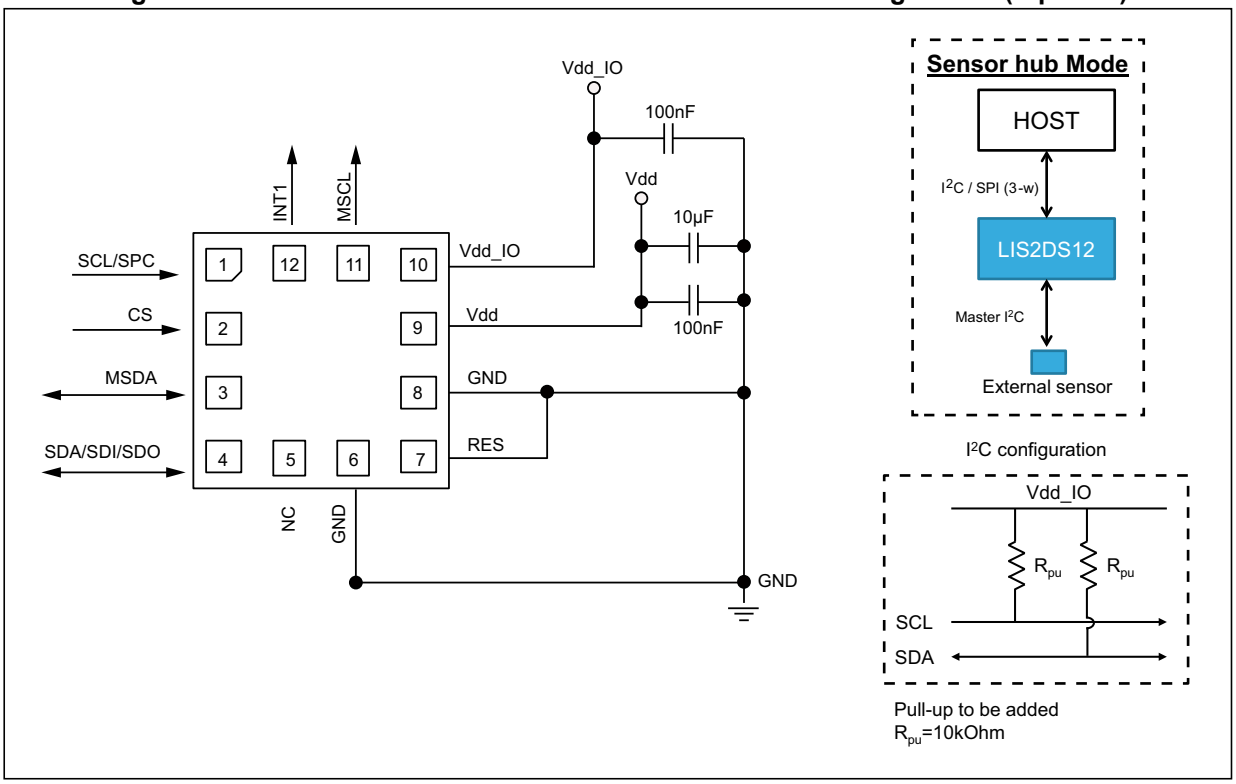


Figure 6. LIS2DS12 electrical connections in sensor hub configuration (top view)



The device core is supplied through the Vdd line while the I/O pads are supplied through the Vdd_IO line. Power supply decoupling capacitors (100 nF ceramic, 10 µF aluminum) should be placed as near as possible to pin 9 of the device (common design practice).

All the voltage and ground supplies must be present at the same time to have proper behavior of the IC (refer to *Figure 5* and *Figure 6*). It is possible to remove Vdd while maintaining Vdd_IO without blocking the communication bus, in this condition the measurement chain is powered off.

The functionality of the device and the measured acceleration data are selectable and accessible through the I^2C or SPI interfaces. When using the I^2C, CS must be tied high (i.e. connected to Vdd_IO).

The functions, the threshold and the timing of the two interrupt pins (INT1 and INT2) can be completely programmed by the user through the I^2C/SPI interface.

5 Digital main blocks

5.1 Power modes

The LIS2DS12 provides two different power modes: high-resolution (including high-frequency mode) and low-power modes.

The tables below summarize the selection of the different operating modes as well as the low-pass filter and current consumption.

Table 10. Operating modes

CTRL1(ODR[3:1])	CTRL1(HF_ODR)	ODR selection [Hz]	Mode
Low-power mode			
0000	-	-	PD
1000	-	1	LP
1001	-	12.5	
1010	-	25	
1011	-	50	
1100	-	100	
1101	-	200	
1110	-	400	
1111	-	800	
High-resolution mode			
0001	-	12.5	HR
0010	-	25	
0011	-	50	
0100	-	100	
0101	0	200	
0110	0	400	
0111	0	800	
0101	1	1600	HF
0110	1	3200	
0111	1	6400	

Table 11. Low-pass filter in low-power, high-resolution and high-frequency modes

ODR [Hz]	LPF cutoff [Hz]
Low-power mode	
800	3200
400	
200	
100	
50	
25	
12.5	
1	
High-resolution mode	
800	355
400	177
200	88
100	44
50	22
25	11
12.5	5.5
High-frequency mode	
6400	2840
3200	1420
1600	710

Table 12. Current consumption of operating modes

ODR (Hz)	Typical current consumption in high-resolution/high-frequency mode [µA]	Typical current consumption in low-power mode [µA]
1	-	2.5
12.5	150	4
25		5.5
50		8
100		12.5
200		22
400		41
800		80
1600		-
3200		-
6400		-

5.2 Activity/Inactivity function

The Activity/Inactivity recognition function allows reducing the power consumption of the system in order to develop new smart applications.

When the Activity/Inactivity recognition function is activated, the LIS2DS12 is able to automatically go to 12.5 Hz sampling rate and to wake up as soon as the interrupt event has been detected, increasing the output data rate and bandwidth.

With this feature the system may be efficiently switched from low-power mode to full performance depending on user-selectable positioning and acceleration events, thus ensuring power saving and flexibility.

The Activity/Inactivity recognition function is activated by writing the desired threshold in the *WAKE_UP_THS (33h)* register. The high-pass filter is automatically enabled.

If the device is in Sleep (Inactivity) mode, when at least one of the axes exceeds the threshold in the *WAKE_UP_THS (33h)* the device goes into Sleep-to-Wake (as Wake-Up).

Activity/Inactivity threshold and duration can be configured in the control registers:

WAKE_UP_THS (33h)

WAKE_UP_DUR (34h)

5.3 Data stabilization time vs. ODR setting

The data stabilization time required when an ODR change is applied in order to have valid usable data depends on the ODR selected and device setting.

The table below provides the number of samples to be discarded in order to obtain valid usable data.

Table 13. Number of samples to be discarded

ODR [Hz]	HF	HR	LP
6400	6	-	-
3200	2	-	-
1600	1	-	-
800	-	1	0
400	-	1	0
200	-	1	0
100	-	1	0
50	-	0	0
25	-	0	0
12.5	-	0	0
1	-	-	0

5.4 FIFO

The LIS2DS12 embeds 256 slots of 14-bit data FIFO for each of the three output channels, X, Y and Z of the acceleration module. This allows consistent power saving for the system, since the host processor does not need to continuously poll data from the sensor, but it can wake up only when needed and burst the significant data out from the FIFO.

The internal FIFO allows collecting 256 samples (14-bit size data) for each axis or storing the output of the module computation up to 768 samples (14-bit size data).

When the FIFO mode is other than Bypass, reading the output registers (28h to 2Dh) returns the oldest FIFO sample set. In order to minimize communication between the master and slave, the address read may be automatically incremented by the device by setting the IF_ADD_INC bit of *CTRL2 (21h)* to '1'; the device rolls back to 0x28 when register 0x2D is reached.

This buffer can work according to the following 5 different modes:

- Bypass mode
- FIFO mode
- Continuous-to-FIFO
- Bypass-to-Continuous
- Continuous

Each mode is selected by the FIFO_MODE bits in the *FIFO_CTRL (25h)* register.