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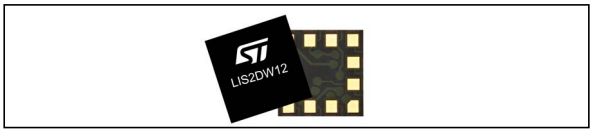
LIS2DW12

MEMS digital output motion sensor: high-performance ultra-low-power 3-axis "femto" accelerometer

Datasheet - production data



Features

- Ultra-low power consumption: 50 nA in power-down mode, below 1 µA in active low-power mode
- Very low noise: down to 1.3 m*g* RMS in low-power mode
- Multiple operating modes with multiple bandwidths
- Android stationary detection, motion detection
- Supply voltage, 1.62 V to 3.6 V
- Independent IO supply
- ±2g/±4g/±8*g*/±16*g* full scale
- High-speed I^2C/SPI digital output interface
- Single data conversion on demand
- 16-bit data output
- Embedded temperature sensor
- Self-test
- 32-level FIFO
- 10000 *g* high shock survivability
- ECOPACK®, RoHS and “Green” compliant

Applications

- Motion detection for wearables
- Gesture recognition and gaming
- Motion-activated functions and user interfaces
- Display orientation
- Tap/double-tap recognition
- Free-fall detection
- Smart power saving for handheld devices
- Hearing aids
- Portable healthcare devices
- Wireless sensor nodes
- Motion-enabled metering devices

Description

The LIS2DW12 is an ultra-low-power high-performance three-axis linear accelerometer belonging to the “femto” family which leverages on the robust and mature manufacturing processes already used for the production of micromachined accelerometers.

The LIS2DW12 has user-selectable full scales of ±2g/±4g/±8g/±16*g* and is capable of measuring accelerations with output data rates from 1.6 Hz to 1600 Hz.

The LIS2DW12 has an integrated 32-level first-in, first-out (FIFO) buffer allowing the user to store data in order to limit intervention by the host processor.

The embedded self-test capability allows the user to check the functioning of the sensor in the final application.

The LIS2DW12 has a dedicated internal engine to process motion and acceleration detection including free-fall, wakeup, highly configurable single/double-tap recognition, activity/inactivity, stationary/motion detection, portrait/landscape detection and 6D/4D orientation.

The LIS2DW12 is available in a small thin plastic land grid array package (LGA) and it is guaranteed to operate over an extended temperature range from -40 °C to +85 °C.

Table 1. Device summary

Order codes	Temp. range [°C]	Package	Packaging
LIS2DW12	-40 to +85	LGA-12	Tray
LIS2DW12TR	-40 to +85	LGA-12	Tape and reel

Contents

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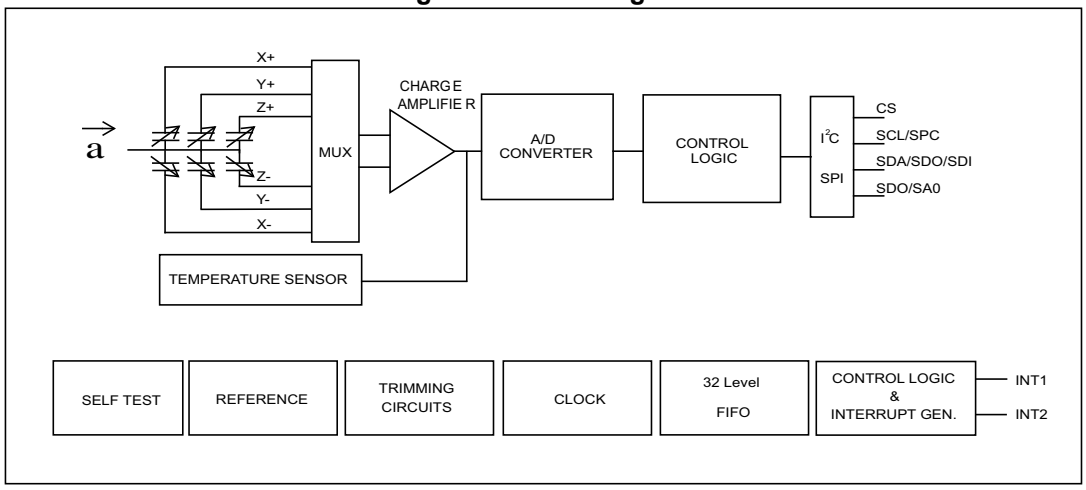
List of figures

1 Block diagram and pin description

1.1 Block diagram

Figure 1. Block diagram



1.2 Pin description

Figure 2. Pin connections

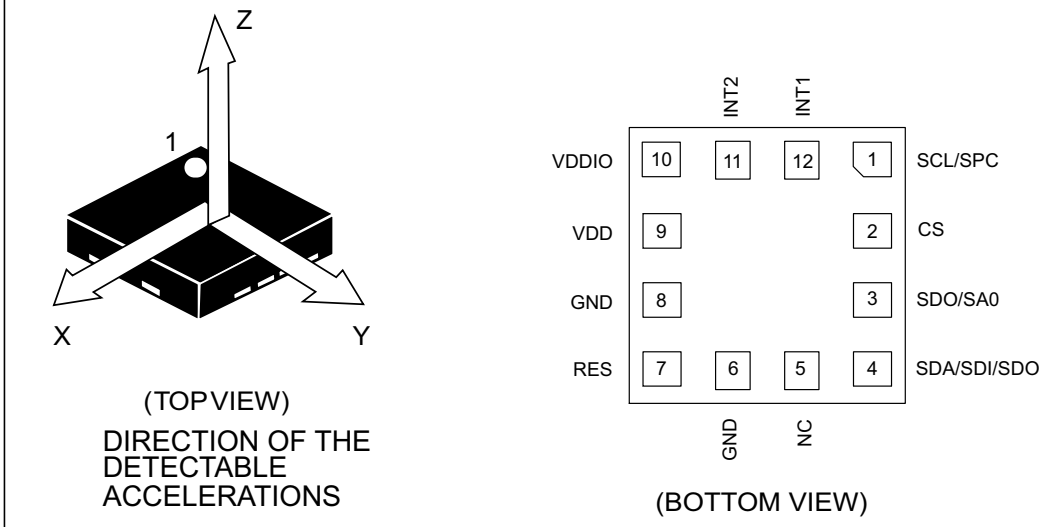


Table 2. Pin description

Pin#	Name	Function
1	SCL SPC	I^2C serial clock (SCL) SPI serial port clock (SPC)
2(1)	CS	SPI enable I^2C/SPI mode selection (1: SPI idle mode / I^2C communication enabled; 0: SPI communication mode / I^2C disabled)
3(1)	SDO SA0	SPI serial data output (SDO) I^2C less significant bit of the device address (SA0)
4	SDA SDI SDO	I^2C serial data (SDA) SPI serial data input (SDI) 3-wire interface serial data output (SDO)
5	NC	Internally not connected. Can be tied to VDD, VDDIO, or GND.
6	GND	0 V supply
7	RES	Connect to GND
8	GND	0 V supply
9	VDD	Power supply
10	VDD_IO	Power supply for I/O pins
11	INT2	Interrupt pin 2. Clock input when selected in single data conversion on demand.
12	INT1	Interrupt pin 1

1. SDO/SA0 and CS pins are internally pulled up. Refer to *Table 3* for the internal pull-up values (typ).

Table 3. Internal pull-up values (typ.) for SDO/SA0 and CS pins

Vdd_IO	Resistor value for SDO/SA0 and CS pins
	Typ. (kΩ)
1.7 V	54.4
1.8 V	49.2
2.5 V	30.4
3.6 V	20.4

2 Mechanical and electrical specifications

2.1 Mechanical characteristics

Table 4. Mechanical characteristics @ Vdd = 1.8 V, T = 25 °C unless otherwise noted (1)

Symbol	Parameter	Test conditions	Min.	Typ.(2)	Max.	Unit
FS	Measurement range			±2		*g*
				±4		
				±8		
				±16		
So	Sensitivity	@ FS ±2 *g* in High-Performance Mode and all Low-Power modes except Low-Power Mode 1		0.244		mg/digit
		@ FS ±4 *g* in High-Performance Mode and all Low-Power Modes except Low-Power Mode 1		0.488		
		@ FS ±8 *g* in High-Performance Mode and all Low-Power modes except Low-Power Mode 1		0.976		
		@ FS ±16 *g* in High-Performance Mode and all Low-Power modes except Low-Power Mode 1		1.952		
		@ FS ±2 *g* in Low-Power Mode 1		0.976		
		@ FS ±4 *g* in Low-Power Mode 1		1.952		
		@ FS ±8 *g* in Low-Power Mode 1		3.904		
		@ FS ±16 *g* in Low-Power Mode 1		7.808		
An	Noise density - High-performance Mode(3)	@ FS ±2 *g*		90		µg/√Hz
RMS	RMS noise - Low-Power Modes(4) @ FS ±2 *g*	Low-Power Mode 4		1.3		mg(RMS)
		Low-Power Mode 3		1.8		
		Low-Power Mode 2		2.4		
		Low-Power Mode 1		4.5		
TyOff	Zero-*g* level offset accuracy(5)			±20		mg
TCO	Zero-*g* offset change vs. temperature			±0.2		mg/°C

Table 4. Mechanical characteristics @ Vdd = 1.8 V, T = 25 °C unless otherwise noted (1)

Symbol	Parameter	Test conditions	Min.	Typ.(2)	Max.	Unit
TCS	Sensitivity change vs. temperature			0.01		%/°C
ST	Self-test positive difference		70		1500	mg

1. The product is factory calibrated at 1.8 V. The operational power supply range is from 1.62 V to 3.6 V.
2. Typical specifications are not guaranteed.
3. Noise density is the same for all ODRs. Low-noise setting enabled.
4. RMS noise is the same for all ODRs. Low-noise setting enabled.
5. Values after factory calibration test and trimming.

2.2 Electrical characteristics

Table 5. Electrical characteristics @ Vdd = 1.8 V, T = 25 °C unless otherwise noted (1)

Symbol	Parameter	Test conditions	Min.	Typ.(2)	Max.	Unit
Vdd	Supply voltage		1.62	1.8	3.6	V
Vdd_IO	I/O pins supply voltage(3)		1.62		Vdd+0.1	V
IddHR	Current consumption in High-Performance Mode(4)	@ ODR range 12.5 Hz - 1600 Hz, 14-bit		90		µA
IddLP	Current consumption in Low-Power Mode(5)	ODR 100 Hz		5		µA
		ODR 50 Hz		3		
		ODR 12.5 Hz		1		
		ODR 1.6 Hz		0.38		
Idd_PD	Current consumption in power-down			50		nA
V_{IH}	Digital high-level input voltage		0.8*Vdd_IO			V
V_{IL}	Digital low-level input voltage				0.2*Vdd_IO	V
V_{OH}	Digital high-level output voltage	I_{OH} = 4 mA(6)	VDD_IO - 0.2 V			
V_{OL}	Digital low-level output voltage	I_{OL} = 4 mA(6)			0.2 V	

1. The product is factory calibrated at 1.8 V. The operational power supply range is from 1.62 V to 3.6 V.
2. Typical specifications are not guaranteed.
3. It is possible to remove Vdd maintaining Vdd_IO without blocking the communication busses. In this condition the measurement chain is powered off.
4. Low-noise setting disabled.
5. Low-Power Mode 1. Low-noise setting disabled.
6. 4 mA is the maximum driving capability, ie. the maximum DC current that can be sourced/sunk by the digital pad in order to guarantee the correct digital output voltage levels V_{OH} and V_{OL}.

2.3 Temperature sensor characteristics

@ Vdd = 1.8 V, T = 25 °C unless otherwise noted

Table 6. Temperature sensor characteristics

Symbol	Parameter	Min.	Typ.(1)	Max.	Unit
Top	Operating temperature range	-40		+85	°C
Toff	Temperature offset(2)	-15		+15	°C
TSDr	Temperature sensor output change vs. temperature		1(3)		LSB/°C
			16(4)		
TODR	Temperature refresh rate in High-Performance Mode for all ODRs or in Low-Power Modes for ODRs equal to 200/100/50 Hz		50		Hz
	Temperature refresh rate in Low-Power Modes for ODR equal to 25 Hz		25		
	Temperature refresh rate in Low-Power Modes for ODR equal to 12.5 Hz		12.5		
	Temperature refresh rate in Low-Power Modes for ODR equal to 1.6 Hz		1.6		

1. Typical specifications are not guaranteed.
2. The output of the temperature sensor is 0 LSB (typ.) at 25 °C.
3. 8-bit resolution.
4. 12-bit resolution.

2.4 Communication interface characteristics

2.4.1 SPI - serial peripheral interface

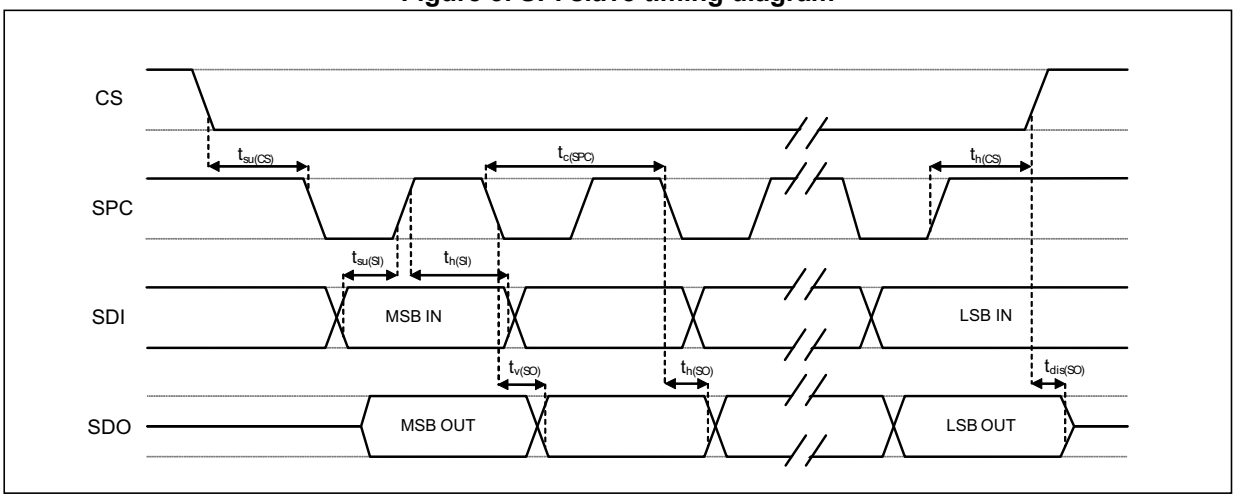
Subject to general operating conditions for Vdd and Top.

Table 7. SPI slave timing values

Symbol	Parameter	Value(1)		Unit
		Min	Max	
$t_{c(SPC)}$	SPI clock cycle	100		ns
$f_{c(SPC)}$	SPI clock frequency		10	MHz
$t_{su(CS)}$	CS setup time	6		ns
$t_{h(CS)}$	CS hold time	8		
$t_{su(SI)}$	SDI input setup time	12		
$t_{h(SI)}$	SDI input hold time	15		
$t_{v(SO)}$	SDO valid output time		50	
$t_{h(SO)}$	SDO output hold time	9		
$t_{dis(SO)}$	SDO output disable time		50	

1. 10 MHz clock frequency for SPI with both 4 and 3 wires, based on characterization results, not tested in production.

Figure 3. SPI slave timing diagram



Measurement points are done at 0.2·Vdd_IO and 0.8·Vdd_IO, for both input and output ports.

2.4.2 I²C - inter-IC control interface

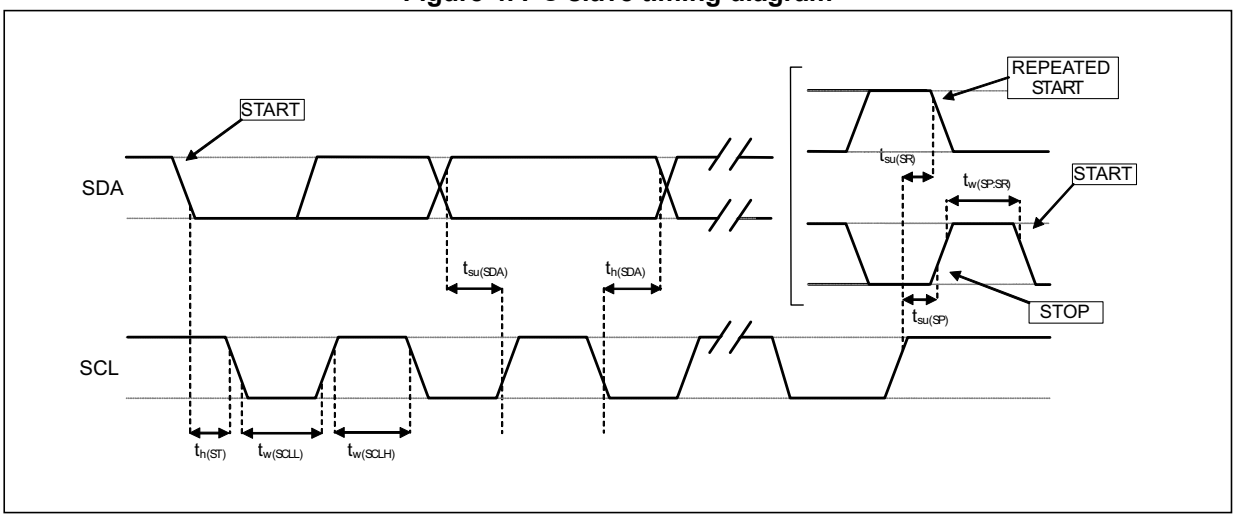
Subject to general operating conditions for Vdd and Top.

Table 8. I²C slave timing values

Symbol	Parameter	I²C standard mode (1)		I²C fast mode (1)		Unit
		Min	Max	Min	Max	
$f_{(SCL)}$	SCL clock frequency	0	100	0	400	kHz
$t_{w(SCLL)}$	SCL clock low time	4.7		1.3		µs
$t_{w(SCLH)}$	SCL clock high time	4.0		0.6		
$t_{su(SDA)}$	SDA setup time	250		100		ns
$t_{h(SDA)}$	SDA data hold time	0.01	3.45	0.01	0.9	µs
$t_{h(ST)}$	START condition hold time	4		0.6		µs
$t_{su(SR)}$	Repeated START condition setup time	4.7		0.6		
$t_{su(SP)}$	STOP condition setup time	4		0.6		
$t_{w(SP:SR)}$	Bus free time between STOP and START condition	4.7		1.3		

1. Data based on standard I²C protocol requirement, not tested in production

Figure 4. I²C slave timing diagram



Note: Measurement points are done at 0.2·Vdd_IO and 0.8·Vdd_IO, for both ports.

Table 9. I²C high-speed mode specifications at 1 MHz and 3.4 MHz

	Symbol	Parameter	Min	Max	Unit
Fast mode plus(1)	f_{SCL}	SCL clock frequency	0	1	MHz
	$t_{HD;STA}$	Hold time (repeated) START condition	260	-	ns
	t_{LOW}	Low period of the SCL clock	500	-	
	t_{HIGH}	High period of the SCL clock	260	-	
	$t_{SU;STA}$	Setup time for a repeated START condition	260	-	
	$t_{HD;DAT}$	Data hold time	0	-	
	$t_{SU;DAT}$	Data setup time	50	-	
	t_{rDA}	Rise time of SDA signal	-	120	
	t_{fDA}	Fall time of SDA signal	-	120	
	t_{rCL}	Rise time of SCL signal	20*Vdd/5.5	120	
	t_{fCL}	Fall time of SCL signal	20*Vdd/5.5	120	
	$t_{SU;STO}$	Setup time for STOP condition	260	-	
	C_b	Capacitive load for each bus line	-	550	pF
	$t_{VD;DAT}$	Data valid time	-	450	ns
	$t_{VD;ACK}$	Data valid acknowledge time	-	450	
	V_{nL}	Noise margin at low level	0.1Vdd	-	V
	V_{nH}	Noise margin at high level	0.2Vdd	-	
	t_{SP}	Pulse width of spikes that must be suppressed by the input filter	0	50	ns
High-speed mode(1)	f_{SCLH}	SCLH clock frequency	0	3.4	MHz
	$t_{SU;STA}$	Setup time for a repeated START condition	160	-	ns
	$t_{HD;STA}$	Hold time (repeated) START condition	160	-	
	t_{LOW}	Low period of the SCLH clock	160	-	
	t_{HIGH}	High period of the SCLH clock	60	-	
	$t_{SU;DAT}$	Data setup time	10	-	
	$t_{HD;DAT}$	Data hold time	0	70	
	t_{rCL}	Rise time of SCLH signal	10	40	
	t_{rCL1}	Rise time of SCLH signal after a repeated START condition and after an acknowledge bit	10	80	
	t_{fCL}	Fall time of SCLH signal	10	40	
	t_{rDA}	Rise time of SDAH signal	10	80	
	t_{fDA}	Fall time of SDAH signal	10	80	
	$t_{SU;STO}$	Setup time for STOP condition	160	-	
	C_b	Capacitive load for each bus line	-	100	pF
	V_{nH}	Noise margin at high level	0.2Vdd	-	V
	t_{SP}	Pulse width of spikes that must be suppressed by the input filter	0	10	ns

1. Data based on characterization, not tested in production

2.5 Absolute maximum ratings

Stresses above those listed as “absolute maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 10. Absolute maximum ratings

Symbol	Ratings	Maximum value	Unit
Vdd	Supply voltage	-0.3 to 4.8	V
Vdd_IO	I/O pins supply voltage	-0.3 to 4.8	V
Vin	Input voltage on any control pin (CS, SCL/SPC, SDA/SDI/SDO, SDO/SA0)	-0.3 to Vdd_IO +0.3	V
A_{POW}	Acceleration (any axis, powered, Vdd = 1.8 V)	3000 *g* for 0.5 ms	*g*
		10000 *g* for 0.2 ms	*g*
A_{UNP}	Acceleration (any axis, unpowered)	3000 *g* for 0.5 ms	*g*
		10000 *g* for 0.2 ms	*g*
T_{OP}	Operating temperature range	-40 to +85	°C
T_{STG}	Storage temperature range	-40 to +125	°C
ESD	Electrostatic discharge protection	2 (HBM)	kV

Note: Supply voltage on any pin should never exceed 4.8 V.

This device is sensitive to mechanical shock, improper handling can cause permanent damage to the part.

This device is sensitive to electrostatic discharge (ESD), improper handling can cause permanent damage to the part.

3 Terminology and functionality

3.1 Terminology

3.1.1 Sensitivity

Sensitivity describes the gain of the sensor and can be determined by applying 1 *g* acceleration to it. As the sensor can measure DC accelerations this can be done easily by pointing the axis of interest towards the center of the Earth, noting the output value, rotating the sensor by 180 degrees (pointing to the sky) and noting the output value again. By doing so, ±1 *g* acceleration is applied to the sensor. Subtracting the larger output value from the smaller one, and dividing the result by 2, leads to the actual sensitivity of the sensor. This value changes very little over temperature and time. The sensitivity tolerance describes the range of sensitivities of a large population of sensors.

3.1.2 Zero-*g* level offset

Zero-*g* level offset describes the deviation of an actual output signal from the ideal output signal if no acceleration is present. A sensor in a steady state on a horizontal surface will measure 0 *g* on the X-axis and 0 *g* on the Y-axis whereas the Z-axis will measure 1 *g*. The output is ideally in the middle of the dynamic range of the sensor (content of OUT registers 00h, data expressed as two's complement number). A deviation from ideal value in this case is called Zero-*g* level offset. Offset is to some extent a result of stress to the MEMS sensor and therefore the offset can slightly change after mounting the sensor onto a printed circuit board or exposing it to extensive mechanical stress. Offset changes little over temperature, see "Zero-*g* level offset change vs. temperature".

3.2 Functionality

3.2.1 Operating modes

Two sets of operating modes have been designed to offer the customer a broad choice of noise/power consumption combinations:

- Low-noise disabled (see *Table 11*)
- Low-noise enabled (see *Table 12*)

Writing the LOW_NOISE bit in *CTRL6 (25h)* selects the operating mode (low-noise).

From each of these two sets, five operating modes have been designed:

- 1 High-Performance Mode: focus on low noise
- 4 Low-Power Modes: trade-off between noise and power consumption

These operating modes are selected by writing the MODE[1:0] and LP_MODE[1:0] bits in *CTRL1 (20h)*.

Table 11. Operating modes - low-noise setting disabled

Parameter		High-Performance Mode	Low-Power Mode 4	Low-Power Mode 3	Low-Power Mode 2	Low-Power Mode 1
Resolution [bit]		14-bit	14-bit	14-bit	14-bit	12-bit
ODR [Hz]		12.5 - 1600	1.6 - 200	1.6 - 200	1.6 - 200	1.6 - 200
BW [Hz]		ODR/2 (N/A for 1600 Hz), ODR/4, ODR/10, ODR/20	180 ODR/4, ODR/10, ODR/20	360 ODR/4, ODR/10, ODR/20	720 ODR/4, ODR/10, ODR/20	3200 ODR/4, ODR/10, ODR/20
Noise density [µg/√Hz] @ FS = ±2 *g*, ODR=200 Hz		110	160	210	300	550
Current consumption [µA] @ Vdd=1.8 V	ODR=1.6 Hz	-	0.65	0.55	0.45	0.38
	ODR=12.5 Hz	90	4	2.5	1.6	1
	ODR=25 Hz	90	8.5	4.5	3	1.5
	ODR=50 Hz	90	16	9	5.5	3
	ODR=100 Hz	90	32	17.5	10.5	5
	ODR=200 Hz	90	63	34.5	20.5	10
	ODR=400, 800, 1600 Hz	90	-	-	-	-

Table 12. Operating modes - low-noise setting enabled

Parameter		High-Performance Mode	Low-Power Mode 4	Low-Power Mode 3	Low-Power Mode 2	Low-Power Mode 1
Resolution [bit]		14-bit	14-bit	14-bit	14-bit	12-bit
ODR [Hz]		12.5 - 1600	1.6 - 200	1.6 - 200	1.6 - 200	1.6 - 200
BW [Hz]		ODR/2 (N/A for 1600 Hz), ODR/4, ODR/10, ODR/20	180 ODR/4, ODR/10, ODR/20	360 ODR/4, ODR/10, ODR/20	720 ODR/4, ODR/10, ODR/20	3200 ODR/4, ODR/10, ODR/20
Noise density [µg/√Hz] @ FS = ±2 *g*, ODR=200 Hz		90	130	180	240	450
Current consumption [µA] @ Vdd=1.8 V	ODR=1.6 Hz	-	0.7	0.6	0.5	0.4
	ODR=12.5 Hz	120	5	3	2	1.1
	ODR=25 Hz	120	10	6	3.5	2
	ODR=50 Hz	120	20	11	7	3.5
	ODR=100 Hz	120	39	21.5	13	6
	ODR=200 Hz	120	77	42	25	12
	ODR=400, 800, 1600 Hz	120	-	-	-	-

3.2.2 Single data conversion on demand mode

The device features a single data conversion on demand mode which is valid for both sets of operating modes (low-noise disabled or enabled) in the 4 low-power modes. This mode is enabled by writing the MODE[1:0] bits to '10' in *CTRL1 (20h)*. Low power modes are selected by writing the LP_MODE[1:0] bits in *CTRL1 (20h)*.

The trigger for output data generation can be managed through the I^2C/SPI or by applying a clock signal on the INT2 pin acting here as an input by writing the SLP_MODE_ SEL bit in *CTRL3 (22h)*:

- When SLP_MODE_SEL = '0', output data generation is triggered by the clock signal on the INT2 pin (see *Figure 5*).
- When SLP_MODE_SEL = '1', output data generation starts when the SLP_MODE_1 bit is set to '1' logic through the I^2C/SPI. When XL data are available in the registers, this bit is automatically set to '0' and the device is ready for another triggered session.

Output data are generated according to the selected low-power mode.

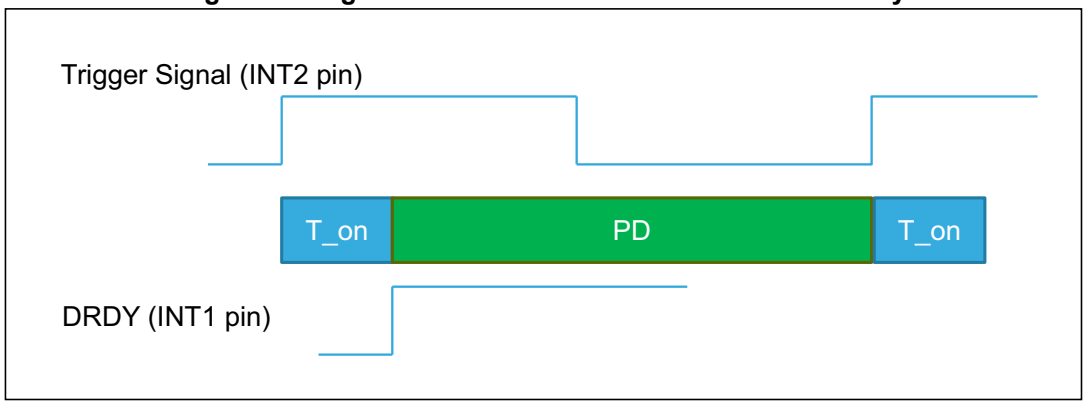
When output data is saved in an output register or FIFO, the device goes to power-down mode and waits for a new trigger.

All ODRs in the range from 0 to up to 200 Hz are supported due to the INT2 clock input.

A DRDY signal or FIFO flags are available on the INT1 pin.

Power consumption is the same as that of standard low-power modes for the same ODR.

Figure 5. Single data conversion on demand functionality



At the end of turn-on time T_on, the DRDY interrupt is activated, output data are available to be read and the device goes into power-down. T_on values depend on the low-power mode as follows:

T_on (typ.) =

- 1.20 ms for Low-Power Mode 1
- 1.70 ms for Low-Power Mode 2
- 2.30 ms for Low-Power Mode 3
- 3.55 ms for Low-Power Mode 4

3.2.3 Self-test

The self-test allows checking the sensor functionality without moving it. The self-test function is off when the self-test bits (ST) are programmed to '00'. When the self-test bits are changed, an actuation force is applied to the sensor, simulating a definite input acceleration. In this case the sensor outputs will exhibit a change in their DC levels which are related to the selected full scale through the device sensitivity. When the self-test is activated, the device output level is given by the algebraic sum of the signals produced by the acceleration acting on the sensor and by the electrostatic test-force. If the output signals change within the amplitude specified in *Table 4*, then the sensor is working properly and the parameters of the interface chip are within the defined specifications.

3.2.4 Activity/Inactivity, Android stationary/motion detection functions

The activity/inactivity function recognizes the device's sleep state and allows reducing system power consumption.

When the activity/inactivity function is activated by setting the SLEEP_ON bit in *WAKE_UP_THS (34h)*, the LIS2DW12 automatically goes to 12.5 Hz ODR in the low-power mode previously selected by the LP_MODE[1:0] bits in *CTRL1 (20h)* if the sleep state condition is detected and wakes up as soon as the interrupt event has been detected, increasing the output data rate and bandwidth.

With this feature the system may be efficiently switched from low-power mode to full performance depending on user-selectable positioning and acceleration events, thus ensuring power saving and flexibility.

The Android stationary/motion detection function only recognizes the device's sleep state.

When the Android stationary/motion detection function is activated by setting the STATIONARY bit in *WAKE_UP_DUR (35h)*, the LIS2DW12 detects acceleration below a fixed threshold but does not change either ODR or operating mode (High-Performance mode or Low-Power mode) after sleep state detection.

The Activity/Inactivity recognition and Android stationary/motion detection functions are activated by writing the desired threshold in the *WAKE_UP_THS (34h)* register. The high-pass filter is automatically enabled.

If the device is in sleep (inactivity/stationary) mode, when at least one of the axes exceeds the threshold in *WAKE_UP_THS (34h)*, the device goes into a sleep-to-wake state (as wake-up).

For the activity/inactivity function, the device, in a wake-up state, will return to the operating mode (HP or LP) and ODR before sleep state detection.

Activity/Inactivity, Android stationary/motion detection threshold and duration can be configured in the following control registers:

WAKE_UP_THS (34h)

WAKE_UP_DUR (35h)

3.2.5 High tap/double-tap user configurability

The device embeds the possibility to select the following parameters:

- single axis or multiple axes in *TAP_THS_Z (32h)*
- axis priority in *TAP_THS_Y (31h)*
- threshold value of each axis in *TAP_THS_X (30h)*, *TAP_THS_Y (31h)*, and *TAP_THS_Z (32h)*
- max time threshold between 2 consecutive taps for double-tap recognition, min time threshold between 2 consecutive taps to detect a new tap event in *INT_DUR (33h)*

3.2.6 Offset management

The user can manage offset in the output or for wakeup detection using dedicated embedded hardware (see *Section 5.1: Block diagram of filters*).

3.3 Sensing element

A proprietary process is used to create a surface micromachined accelerometer. The technology allows processing suspended silicon structures which are attached to the substrate in a few points called anchors and are free to move in the direction of the sensed acceleration. In order to be compatible with the traditional packaging techniques, a cap is placed on top of the sensing element to avoid blocking the moving parts during the molding phase of the plastic encapsulation. When an acceleration is applied to the sensor the proof mass displaces from its nominal position, causing an imbalance in the capacitive half-bridge. This imbalance is measured using charge integration in response to a voltage pulse applied to the capacitor.

At steady-state the nominal value of the capacitors are a few pF and when an acceleration is applied, the maximum variation of the capacitive load is in the fF range.

3.4 IC interface

The complete measurement chain is composed of a low-noise capacitive amplifier which converts the capacitive unbalancing of the MEMS sensor into an analog voltage using an analog-to-digital converter.

The acceleration data may be accessed through an I^2C/SPI interface thus making the device particularly suitable for direct interfacing with a microcontroller.

The LIS2DW12 features a data-ready signal which indicates when a new set of measured acceleration data is available, thus simplifying data synchronization in the digital system that uses the device.

3.5 Factory calibration

The IC interface is factory-calibrated for sensitivity (So) and Zero-*g* level offset.

The trim values are stored inside the device in nonvolatile memory. Any time the device is turned on, the trimming parameters are downloaded into the registers to be used during active operation. This allows using the device without further calibration. If an accidental write occurs in the registers where trimming parameters are stored, the BOOT bit in *CTRL2 (21h)* can help to retrieve the correct trimming parameters from nonvolatile memory without the need to switch on/off the device. This bit is automatically reset at the end of the download operation. Setting this bit has no impact on the control registers.

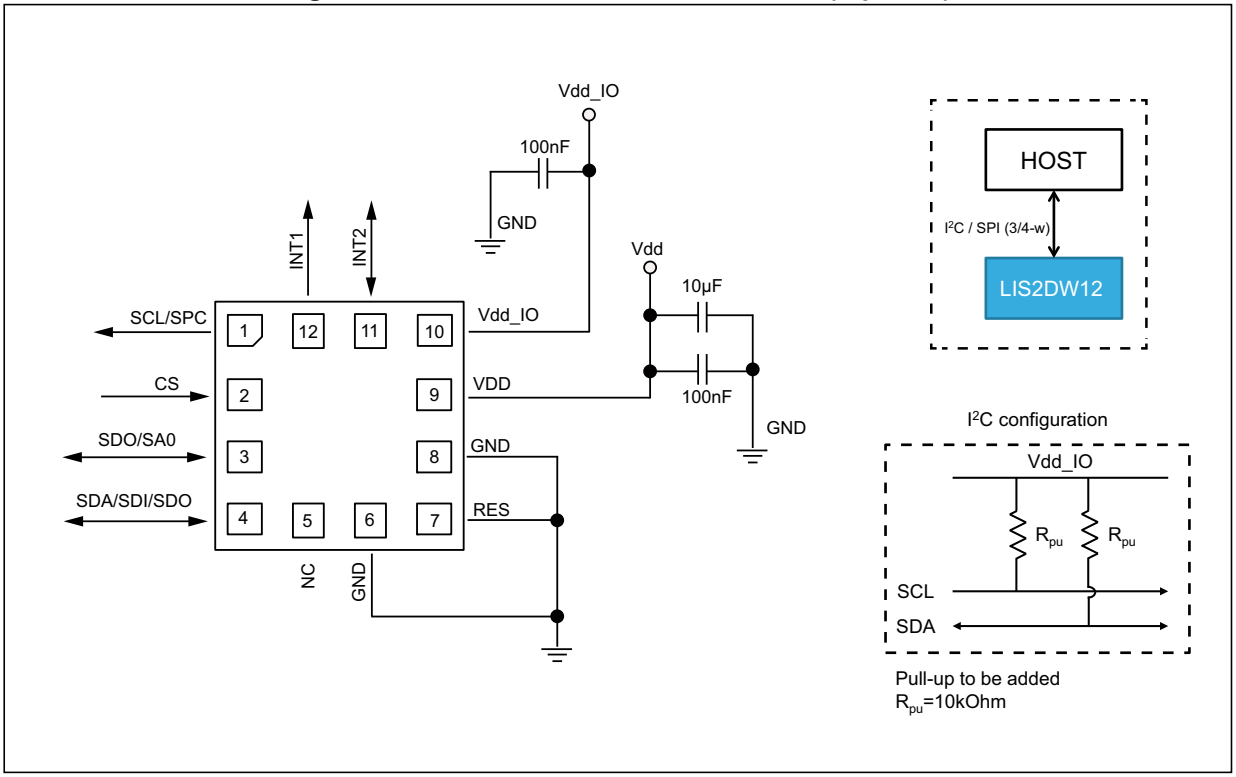
3.6 Temperature sensor

The temperature is available in *OUT_T_L (0Dh)*, *OUT_T_H (0Eh)* stored as two's complement data, left-justified in 12-bit mode and in *OUT_T (26h)* stored as two's complement data, left-justified in 8-bit mode.

Refer to *Table 6: Temperature sensor characteristics* for the conversion factor.

4 Application hints

Figure 6. LIS2DW12 electrical connections (top view)



The device core is supplied through the Vdd line while the I/O pads are supplied through the Vdd_IO line. Power supply decoupling capacitors (100 nF ceramic, 10 µF aluminum) should be placed as near as possible to pin 9 of the device (common design practice).

All the voltage and ground supplies must be present at the same time to have proper behavior of the IC (refer to *Figure 6*). It is possible to remove Vdd while maintaining Vdd_IO without blocking the communication bus, in this condition the measurement chain is powered off.

The functionality of the device and the measured acceleration data are selectable and accessible through the I^2C or SPI interfaces. When using the I^2C, CS must be tied high (i.e. connected to Vdd_IO).

The functions, the threshold and the timing of the two interrupt pins (INT1 and INT2) can be completely programmed by the user through the I^2C/SPI interface.