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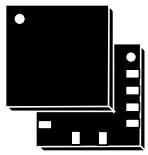
LIS2HH12

MEMS digital output motion sensor: ultra-low-power high-performance 3-axis "pico" accelerometer

Datasheet - production data



LGA-12 (2.0x2.0x1.0 mm)

Features

- Wide supply voltage, 1.71 V to 3.6 V
- Independent IOs supply (1.8 V) and supply voltage compatible
- Ultra-low power consumption
- ±2g/±4g/±8*g* full-scale
- I^2C/SPI digital output interface
- 16-bit data output
- Embedded temperature sensor
- Embedded self-test
- Embedded FIFO
- 10000 *g* high shock survivability
- ECOPACK®, RoHS and “Green” compliant

Applications

- Motion-controlled user interfaces
- Gaming and virtual reality
- Pedometers
- Intelligent power saving for handheld devices
- Display orientation
- Click/double-click recognition
- Impact recognition and logging
- Vibration monitoring and compensation

Description

The LIS2HH12 is an ultra-low-power high-performance three-axis linear accelerometer belonging to the “pico” family.

The LIS2HH12 has full scales of ±2g/±4g/±8g and is capable of measuring accelerations with output data rates from 10 Hz to 800 Hz.

The self-test capability allows the user to check the functioning of the sensor in the final application.

The LIS2HH12 has an integrated first-in, first-out (FIFO) buffer allowing the user to store data in order to limit intervention by the host processor.

The LIS2HH12 is available in a small thin plastic land grid array package (LGA) and it is guaranteed to operate over an extended temperature range from -40 °C to +85 °C

Table 1. Device summary

Order codes	Temperature range [°C]	Package	Packaging
LIS2HH12	-40 to +85	LGA-12	Tray
LIS2HH12TR	-40 to +85	LGA-12	Tape and reel

Contents

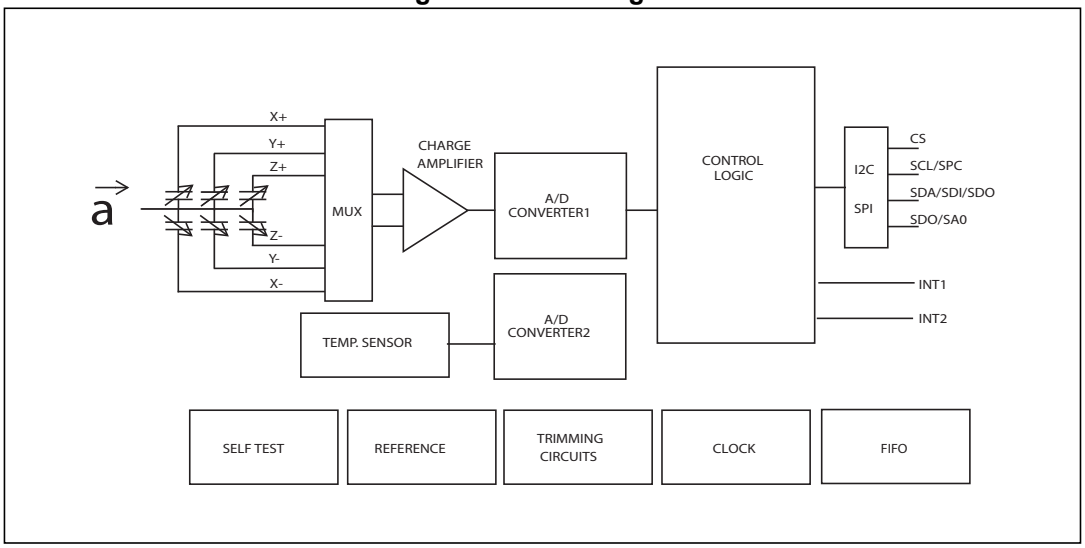
List of tables

List of figures

1 Block diagram and pin description

1.1 Block diagram

Figure 1. Block diagram



1.2 Pin description

Figure 2. Pin connections

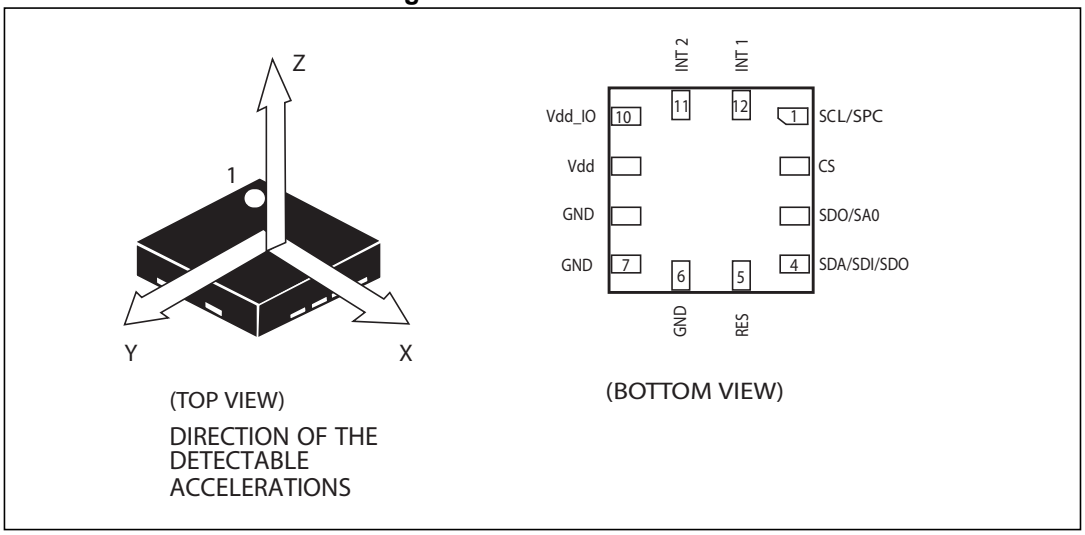


Table 2. Pin description

Pin#	Name	Function
1	SCL SPC	I^2C serial clock (SCL) SPI serial port clock (SPC)
2	CS	SPI enable I^2C/SPI mode selection (1: SPI idle mode / I^2C communication enabled; 0: SPI communication mode / I^2C disabled)
3	SDO SA0	SPI serial data output (SDO) I^2C less significant bit of the device address (SA0)
4	SDA SDI SDO	I^2C serial data (SDA) SPI serial data input (SDI) 3-wire interface serial data output (SDO)
5	RES	Connect to GND
6	GND	0 V supply
7	GND	0 V supply
8	GND	0 V supply
9	Vdd	Power supply
10	Vdd_IO	Power supply for I/O pins
11	INT2	Interrupt pin 2
12	INT1	Interrupt pin 1

2 Mechanical and electrical specifications

2.1 Mechanical characteristics

Table 3. Mechanical characteristics @ Vdd = 2.5 V, T = 25 °C unless otherwise noted (1)

Symbol	Parameter	Test conditions	Min.	Typ.(2)	Max.	Unit
FS	Measurement range(3)			±2.0		g
				±4.0		g
				±8.0		g
So	Sensitivity	@ FS ±2.0 *g*		0.061		mg/digit
		@ FS ±4.0 *g*		0.122		mg/digit
		@ FS ±8.0 *g*		0.244		mg/digit
TCSo	Sensitivity change vs. temperature			0.01		%/°C
TyOff	Typical zero-*g* level offset accuracy(4)			±30		m*g*
TCOff	Zero-*g* level change vs. temperature(4)	Delta from 25 °C		±0.25		mg/°C
Ton	Turn-on time	Number of samples to be discarded from power-down to active mode *CTRL4 (23h)* (BW_SCALE_ODR) = 0	1			# of samples
ST	Self-test positive difference(5)		70		1500	m*g*
Top	Operating temperature range		-40		+85	°C

1. The product is factory calibrated at 2.5 V. The operational power supply range is from 1.71 V to 3.6 V.
2. Typical specifications are not guaranteed.
3. Verified by wafer level test and measurement of initial offset and sensitivity.
4. Offset can be eliminated by enabling the built-in high-pass filter.
5. “Self-test positive difference” is defined as: OUTPUT[m*g*]$_{(CTRL5\ ST2,\ ST1\ bits=01)}$ - OUTPUT[m*g*]$_{(CTRL5\ ST2,\ ST1\ bits=00)}$.

2.2 Electrical characteristics

Table 4. Electrical characteristics @ Vdd = 2.5 V, T = 25 °C unless otherwise noted (1)

Symbol	Parameter	Test conditions	Min.	Typ.(2)	Max.	Unit
Vdd	Supply voltage		1.71	2.5	3.6	V
Vdd_IO	I/O pins supply voltage(3)		1.71		Vdd+0.1	V
IddA	Current consumption in active mode	ODR 100-800 Hz		180		µA
		ODR 50 Hz		110		µA
		ODR 10 Hz		50		µA
IddPdn	Current consumption in power-down mode			5		µA
VIH	Digital high-level input voltage		0.8*Vdd_IO			V
VIL	Digital low-level input voltage				0.2*Vdd_IO	V
Tboot	Boot time(4)				20	ms
Top	Operating temperature range		-40		+85	°C

1. The product is factory calibrated at 2.5 V. The operational power supply range is from 1.71 V to 3.6 V.
2. Typical specifications are not guaranteed.
3. It is possible to remove Vdd maintaining Vdd_IO without blocking the communication busses, in this condition the measurement chain is powered off.
4. Time to complete the entire boot sequence: from Vdd on until all configuration and calibration parameters are correctly loaded into device registers.

2.3 Temperature sensor characteristics

@ Vdd =2.5 V, T=25 °C unless otherwise noted

Table 5. Temperature sensor characteristics

Symbol	Parameter	Min.	Typ.(1)	Max.	Unit
TSDr	Temperature sensor output change vs. temperature		8		digit/°C(2)
TODR	Temperature refresh rate		10		Hz
Top	Operating temperature range	-40		+85	°C

1. Typical specifications are not guaranteed.
2. 11-bit resolution.

2.4 Communication interface characteristics

2.4.1 SPI - serial peripheral interface

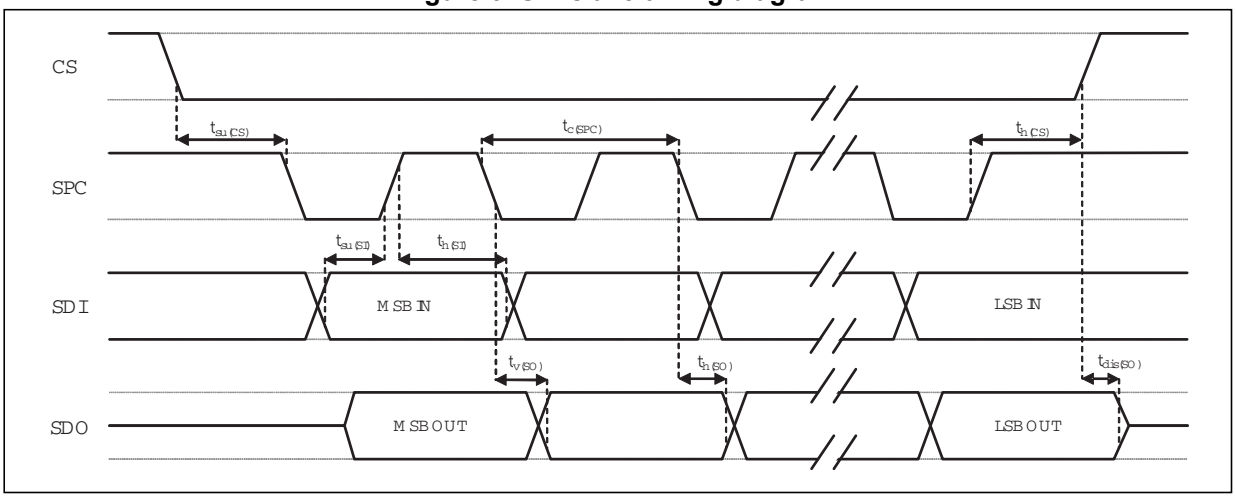
Subject to general operating conditions for Vdd and Top.

Table 6. SPI slave timing values

Symbol	Parameter	Value(1)		Unit
		Min	Max	
$t_{c(SPC)}$	SPI clock cycle	100		ns
$f_{c(SPC)}$	SPI clock frequency		10	MHz
$t_{su(CS)}$	CS setup time	6		ns
$t_{h(CS)}$	CS hold time	8		
$t_{su(SI)}$	SDI input setup time	5		
$t_{h(SI)}$	SDI input hold time	15		
$t_{v(SO)}$	SDO valid output time		50	
$t_{h(SO)}$	SDO output hold time	9		
$t_{dis(SO)}$	SDO output disable time		50	

1. Values are guaranteed at 10 MHz clock frequency for SPI with both 4 and 3 wires, based on characterization results, not tested in production.

Figure 3. SPI slave timing diagram



Note: Measurement points are done at 0.2·Vdd_IO and 0.8·Vdd_IO, for both input and output ports.

2.4.2 I²C - inter-IC control interface

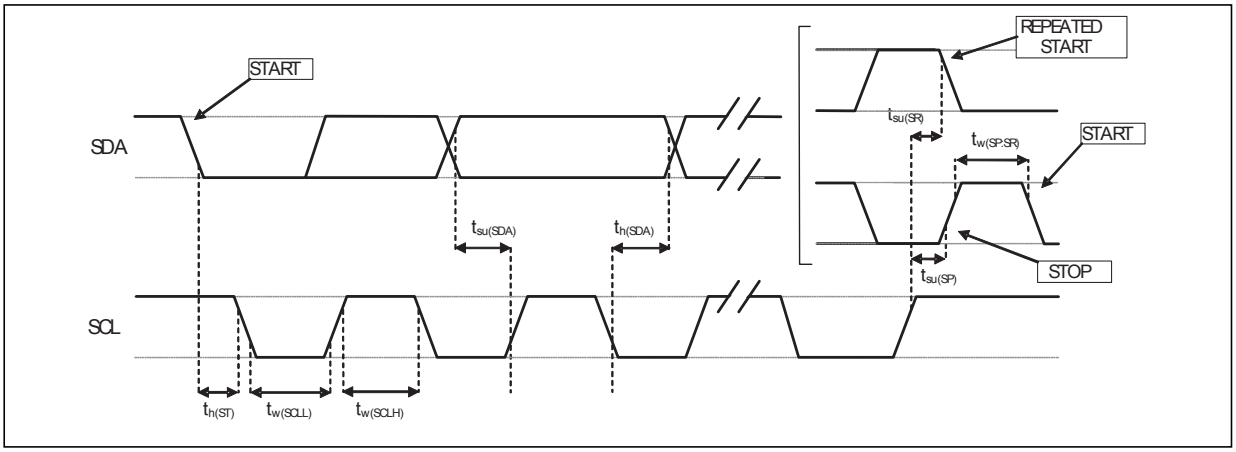
Subject to general operating conditions for Vdd and Top.

Table 7. I²C slave timing values

Symbol	Parameter	I²C standard mode (1)		I²C fast mode (1)		Unit
		Min	Max	Min	Max	
$f_{(SCL)}$	SCL clock frequency	0	100	0	400	kHz
$t_{w(SCLL)}$	SCL clock low time	4.7		1.3		µs
$t_{w(SCLH)}$	SCL clock high time	4.0		0.6		
$t_{su(SDA)}$	SDA setup time	250		100		ns
$t_{h(SDA)}$	SDA data hold time	0.01	3.45	0.01	0.9	µs
$t_{h(ST)}$	START condition hold time	4		0.6		µs
$t_{su(SR)}$	Repeated START condition setup time	4.7		0.6		
$t_{su(SP)}$	STOP condition setup time	4		0.6		
$t_{w(SP:SR)}$	Bus free time between STOP and START condition	4.7		1.3		

1. Data based on standard I²C protocol requirement, not tested in production

Figure 4. I²C slave timing diagram



Note: Measurement points are done at 0.2·Vdd_IO and 0.8·Vdd_IO, for both ports.

2.5 Absolute maximum ratings

Stresses above those listed as “absolute maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 8. Absolute maximum ratings

Symbol	Ratings	Maximum value	Unit
Vdd	Supply voltage	-0.3 to 4.8	V
Vdd_IO	I/O pins supply voltage	-0.3 to 4.8	V
Vin	Input voltage on any control pin (CS, SCL/SPC, SDA/SDI/SDO, SDO/SA0)	-0.3 to Vdd_IO +0.3	V
A_{POW}	Acceleration (any axis, powered, Vdd = 2.5 V)	3000 for 0.5 ms	*g*
		10000 for 0.2 ms	*g*
A_{UNP}	Acceleration (any axis, unpowered)	3000 for 0.5 ms	*g*
		10000 for 0.2 ms	*g*
T_{OP}	Operating temperature range	-40 to +85	°C
T_{STG}	Storage temperature range	-40 to +125	°C
ESD	Electrostatic discharge protection	2 (HBM)	kV

Note: Supply voltage on any pin should never exceed 4.8 V

This device is sensitive to mechanical shock, improper handling can cause permanent damage to the part.

This device is sensitive to electrostatic discharge (ESD), improper handling can cause permanent damage to the part.

2.6 Terminology and functionality

Terminology

2.6.1 Sensitivity

Sensitivity describes the gain of the sensor and can be determined by applying 1 *g* acceleration to it. As the sensor can measure DC accelerations this can be done easily by pointing the axis of interest towards the center of the Earth, noting the output value, rotating the sensor by 180 degrees (pointing to the sky) and noting the output value again. By doing so, ±1 *g* acceleration is applied to the sensor. Subtracting the larger output value from the smaller one, and dividing the result by 2, leads to the actual sensitivity of the sensor. This value changes very little over temperature and time. The sensitivity tolerance describes the range of sensitivities of a large population of sensors.

2.6.2 Zero-*g* level

Zero-*g* level offset (TyOff) describes the deviation of an actual output signal from the ideal output signal if no acceleration is present. A sensor in a steady state on a horizontal surface will measure 0 *g* on the X-axis and 0 *g* on the Y-axis whereas the Z-axis will measure 1 *g*. The output is ideally in the middle of the dynamic range of the sensor (content of OUT registers 00h, data expressed as two's complement number). A deviation from ideal value in this case is called Zero-*g* offset. Offset is to some extent a result of stress to the MEMS sensor and therefore the offset can slightly change after mounting the sensor onto a printed circuit board or exposing it to extensive mechanical stress. Offset changes little over temperature, see "Zero-*g* level change vs. temperature". The Zero-*g* level tolerance (TyOff) describes the standard deviation of the range of Zero-*g* levels of a population of sensors.

Functionality

2.6.3 Self-test

The self-test allows checking the sensor functionality without moving it. The self-test function is off when the self-test bits (ST) are programmed to '00'. When the self-test bits are changed, an actuation force is applied to the sensor, simulating a definite input acceleration. In this case the sensor outputs will exhibit a change in their DC levels which are related to the selected full scale through the device sensitivity. When the self-test is activated, the device output level is given by the algebraic sum of the signals produced by the acceleration acting on the sensor and by the electrostatic test-force. If the output signals change within the amplitude specified in *Table 3*, then the sensor is working properly and the parameters of the interface chip are within the defined specifications.

2.7 Sensing element

A proprietary process is used to create a surface micromachined accelerometer. The technology allows processing suspended silicon structures which are attached to the substrate in a few points called anchors and are free to move in the direction of the sensed acceleration. In order to be compatible with the traditional packaging techniques, a cap is placed on top of the sensing element to avoid blocking the moving parts during the molding phase of the plastic encapsulation.

When an acceleration is applied to the sensor the proof mass displaces from its nominal position, causing an imbalance in the capacitive half-bridge. This imbalance is measured using charge integration in response to a voltage pulse applied to the capacitor.

At steady-state the nominal value of the capacitors are a few pF and when an acceleration is applied, the maximum variation of the capacitive load is in the fF range.

2.8 IC interface

The complete measurement chain is composed of a low-noise capacitive amplifier which converts the capacitive unbalancing of the MEMS sensor into an analog voltage using an analog-to-digital converter.

The acceleration data may be accessed through an I^2C/SPI interface thus making the device particularly suitable for direct interfacing with a microcontroller.

The LIS2HH12 features a data-ready signal which indicates when a new set of measured acceleration data is available, thus simplifying data synchronization in the digital system that uses the device.

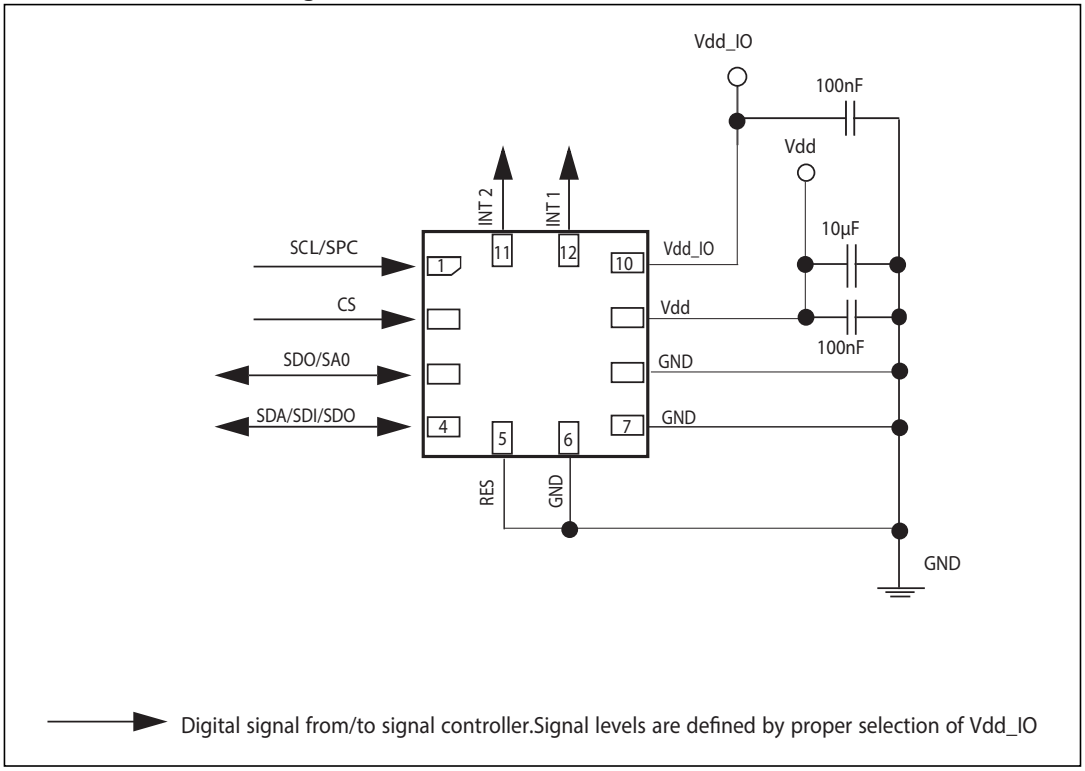
3 Factory calibration

The IC interface is factory calibrated for sensitivity (So) and Zero-*g* level (TyOff).

The trim values are stored inside the device in nonvolatile memory. Any time the device is turned on, the trimming parameters are downloaded into the registers to be used during the active operation. This allows using the device without further calibration.

4 Application hints

Figure 5. LIS2HH12 electrical connections



The device core is supplied through the Vdd line while the I/O pads are supplied through the Vdd_IO line. Power supply decoupling capacitors (100 nF ceramic, 10 µF aluminum) should be placed as near as possible to pin 9 of the device (common design practice).

All the voltage and ground supplies must be present at the same time to have proper behavior of the IC (refer to *Figure 5*). It is possible to remove Vdd while maintaining Vdd_IO without blocking the communication bus, in this condition the measurement chain is powered off.

The functionality of the device and the measured acceleration data are selectable and accessible through the I^2C or SPI interfaces. When using the I^2C, CS must be tied high (i.e. connected to Vdd_IO).

The functions, the threshold and the timing of the two interrupt pins (INT1 and INT2) can be completely programmed by the user through the I^2C/SPI interface.

4.1 Soldering information

The LGA package is compliant with the ECOPACK®, RoHS and “Green” standard.
It is qualified for soldering heat resistance according to JEDEC J-STD-020.

Leave “Pin 1 Indicator” unconnected during soldering.

Land pattern and soldering recommendations are available at www.st.com.

5 Digital main blocks

5.1 Activity/Inactivity function

The Activity/Inactivity recognition function allows reducing the power consumption of the system in order to develop new smart applications.

When the Activity/Inactivity recognition function is activated, the LIS2HH12 is able to automatically go to 10Hz sampling rate and to wake up as soon as the interrupt event has been detected, increasing the output data rate and bandwidth.

With this feature the system may be efficiently switched from low-power mode to full performance depending on user-selectable positioning and acceleration events, thus ensuring power saving and flexibility.

The Activity/Inactivity recognition function is activated by writing the desired threshold in the *ACT_THS (1Eh)* register. The high-pass filter is automatically enabled.

Table 9. Activity/Inactivity function control registers

Register	LSB value
ACT_THS	Full scale / 128 [mg]
ACT_DUR	8/ODR [s]

When the acceleration falls below the threshold for a duration of at least (8 ACT_DUR +1)/ODR, the *CTRL1 (20h)* (ODR [2:0]) bits of CTRL1 are bypassed (Inactivity) and internally set to 10Hz (ODR [2:0] = 001), but the content of the *CTRL1 (20h)* (ODR [2:0]) bits are left untouched.

When the acceleration exceeds the threshold (*ACT_THS (1Eh)*), the ODR setting in *CTRL1 (20h)* is restored immediately (Activity).

Once the Activity/Inactivity detection function is enabled, the status can be brought out on INT1 by setting the *CTRL3 (22h)* (INT1_INACT) bit to 1.

To disable the Activity/Inactivity detection function, set the content of the *ACT_THS (1Eh)* register to 00h.

5.2 Data stabilization time / ODR change

The data stabilization time required when an ODR change is applied in order to have valid usable data depends on the BW and ODR selected.

The table below provides the number of samples to be discarded in order to obtain valid usable data.

Table 10. Number of samples to be discarded

ODR [Hz]	BW = 400 Hz	BW = 200 Hz	BW = 100 Hz	BW = 50 Hz
10	1	-	-	-
50	1	-	-	-
100	1	1	1	1
200	1	1	1	4
400	1	1	4	7
800	1	4	7	14

5.3 FIFO

The LIS2HH12 embeds an acceleration data FIFO for each of the three output channels, X, Y and Z. This allows consistent power saving for the system, since the host processor does not need to continuously poll data from the sensor, but it can wake up only when needed and burst the significant data out from the FIFO. This buffer can work according to the following different modes: Bypass mode, FIFO-mode, Stream mode, Stream-to-FIFO mode, Bypass-to-Stream, Bypass-to-FIFO. Each mode is selected by the FIFO_MODE bits in the *FIFO_CTRL (2Eh)* register. Programmable FIFO threshold level, FIFO empty or FIFO overrun events are available in the *FIFO_CTRL (2Eh)* register and can be set to generate dedicated interrupts on the INT1 or INT2 pin.

FIFO_SRC (2Fh) (EMPTY) is equal to '1' when no samples are available.

FIFO_SRC (2Fh)(FTH) goes to '1' if new data arrives and *FIFO_SRC (2Fh)*(FSS [4:0]) is greater than or equal to *FIFO_CTRL (2Eh)* (FTH [4:0]). *FIFO_SRC (2Fh)* (FTH) goes to '0' if reading X, Y, Z data slot from *FIFO* and *FIFO_SRC (2Fh)* (FSS [4:0]) is less than or equal to *FIFO_CTRL (2Eh)* (FTH [4:0]).

FIFO_SRC (2Fh) (OVR) is equal to '1' if a FIFO slot is overwritten.

The FIFO feature is enabled by writing the *CTRL3 (22h)* (FIFO_EN) bit to '1' in control register 3.

In order to guarantee the correct acquisition of data during the switching into and out of FIFO mode, the first sample acquired must be discarded.

5.3.1 Bypass mode

In Bypass mode (*FIFO_CTRL (2Eh)* (FMODE [2:0])= 000), the FIFO is not operational and it remains empty.

Bypass mode is also used to reset the FIFO when in FIFO mode.

5.3.2 FIFO mode

In FIFO mode (*FIFO_CTRL (2Eh)* (FMODE [2:0])= 001) data from the X, Y and Z channels are stored in the FIFO until it is full. An overrun interrupt can be enabled, *CTRL3 (22h)* (INT1_OVR)= '1', in order to be raised when the FIFO stops collecting data. When the overrun interrupt occurs, the first set of data has been overwritten and the FIFO stops collecting data from the input channels. To reset the FIFO content, Bypass mode should be written in the *FIFO_CTRL (2Eh)* register, setting the FMODE [2:0] bits to '000'. After this reset command, it is possible to restart FIFO mode, writing the value '001' in *FIFO_CTRL (2Eh)* (FMODE [2:0]).

The FIFO buffer can memorize 32 slots of X, Y and Z data, but the depth of the FIFO can be reduced using the *CTRL3 (22h)* (STOP_ FTH) bit. Setting the STOP_FTH bit to '1', FIFO depth is limited to *FIFO_CTRL (2Eh)* (FTH [4:0]) - 1.

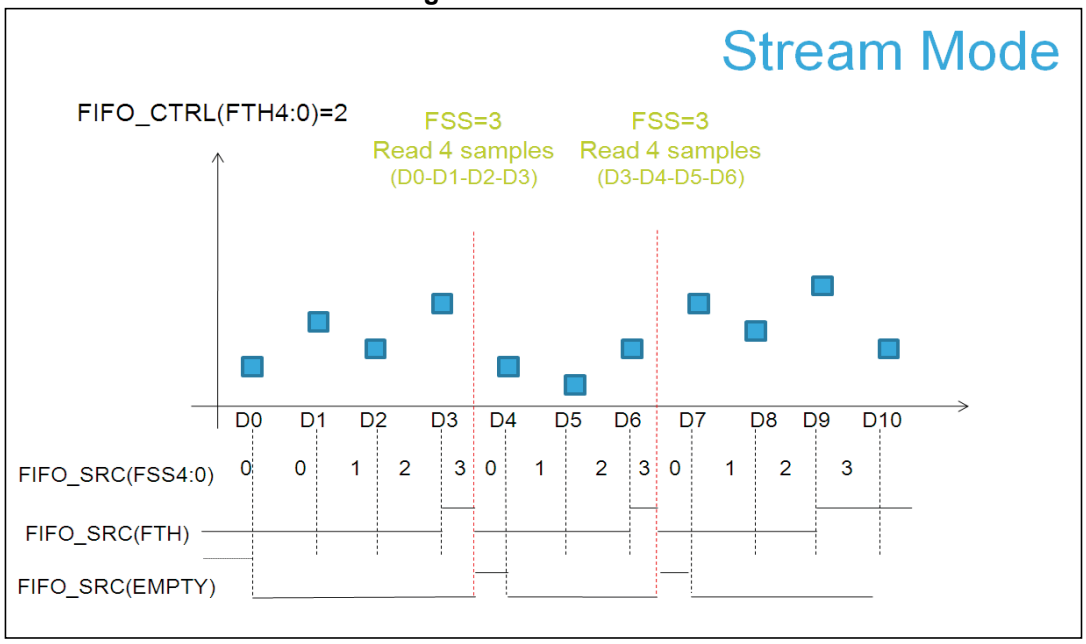
5.3.3 Stream mode

Stream mode (*FIFO_CTRL (2Eh)* (FMODE [2:0]) = 010) provides a continuous FIFO update: as new data arrives, the older data is discarded.

An overrun interrupt can be enabled, *CTRL3 (22h)* (INT1_OVR) = '1', in order to read the entire content of the FIFO at once. If in the application no data can be lost and it is not possible to read at least one sample for each axis within one ODR period, a watermark interrupt can be enabled in order to read partially the FIFO and leave free memory slots for incoming data. Setting the *FIFO_CTRL (2Eh)* (FTH [4:0]) to value N, the number of X, Y and Z data samples that should be read at the rise of the watermark interrupt is up to (N+1).

In the latter case, reading all FIFO content before an overrun interrupt has occurred, the first data read is equal to the last data already read in previous burst, so the number of new data available in the FIFO depends on the previous reading (see *FIFO_SRC (2Fh)*behavior depicted in the following figures).

Figure 6. Stream mode



A watermark interrupt *CTRL3 (22h)* (INT1_FTH), *CTRL6 (25h)*(INT2_FTH) can be enabled in order to read data from the FIFO and leave free memory slots for incoming data. Setting the *FIFO_CTRL (2Eh)* (FTH [4:0]) to value N, the number of X, Y and Z data samples that should be read at the rise of the watermark interrupt, in order to read the entire FIFO content, is N + 1.

5.3.4 Stream-to-FIFO mode

In Stream-to-FIFO mode (*FIFO_CTRL (2Eh)*(FMODE2:0) = 011), FIFO behavior changes according to the *IG_SRC1 (31h)* (IA) bit. When the *IG_SRC1 (31h)* (IA) bit is equal to '1' FIFO operates in FIFO mode, when the *IG_SRC1 (31h)* (IA) bit is equal to '0', FIFO operates in Stream mode.

Interrupt generator 1 should be set to the desired configuration using *IG_CFG1 (30h)*, *IG_THS_X1 (32h), IG_THS_Y1 (33h), IG_THS_Z1 (34h)*.

The *CTRL7 (26h)* (LIR1) bit should be set to '1' in order to have latched interrupt.

5.3.5 Bypass-to-Stream mode

In Bypass-to-Stream mode (*FIFO_CTRL (2Eh)* (FMODE [2:0]) = '100'), X, Y and Z measurement storage inside FIFO operates in Stream mode when *IG_SRC1 (31h)* (IA) is equal to '1', otherwise FIFO content is reset (Bypass mode).

Interrupt generator 1 should be set to the desired configuration using *IG_CFG1 (30h)*, *IG_THS_X1 (32h), IG_THS_Y1 (33h), IG_THS_Z1 (34h)*.

The *CTRL7 (26h)* (LIR1) bit should be set to '1' in order to have latched interrupt.

5.3.6 Bypass-to-FIFO mode

In Bypass-to-FIFO mode (*FIFO_CTRL (2Eh)* (FMODE [2:0]) = '111', FIFO behavior changes according to the *IG_SRC1 (31h)* (IA) bit. When the *IG_SRC1 (31h)*(IA) bit is equal to '1', FIFO operates in FIFO mode, when the *IG_SRC1 (31h)* (IA) bit is equal to '0', FIFO operates in Bypass mode (FIFO content reset). If a latched interrupt is generated, FIFO starts collecting data until the first data in the FIFO buffer is overwritten. Interrupt generator 1 should be set to the desired configuration using *IG_CFG1 (30h)*, *IG_THS_X1 (32h), IG_THS_Y1 (33h), IG_THS_Z1 (34h)*.

The *CTRL7 (26h)* (LIR1) bit should be set to '1' in order to have latched interrupt.

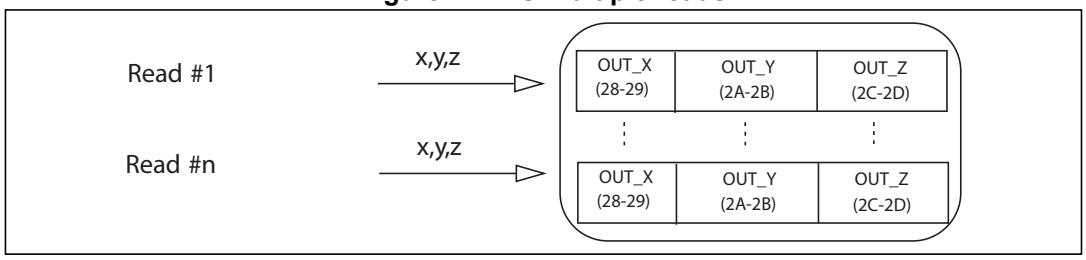
5.3.7 Retrieving data from FIFO

FIFO data is read through the *OUT_X_L (28h) - OUT_X_H (29h)*, *OUT_Y_L (2Ah) - OUT_Y_H (2Bh)*, *OUT_Z_L (2Ch) - OUT_Z_H (2Dh)* registers. A read operation by means of serial interface of OUT_X, OUT_Y or OUT_Z output registers provides the data stored into the FIFO. Each time data is read from the FIFO, the oldest X, Y and Z data are placed into the OUT_X, OUT_Y and OUT_Z registers and both single read and read_burst operations can be used.

5.3.8 FIFO multiple reads (burst)

Starting from Addr 28h multiple reads can be performed. Once the read reaches Addr 2Dh the system automatically restarts from Addr 28h.

Figure 7. FIFO multiple reads



6 Digital interfaces

The registers embedded inside the LIS2HH12 may be accessed through both the I^2C and SPI serial interfaces. The latter may be SW configured to operate either in 3-wire or 4-wire interface mode.

The serial interfaces are mapped to the same pins. To select/exploit the I^2C interface, the CS line must be tied high (i.e. connected to Vdd_IO).

Table 11. Serial interface pin description

Pin name	Pin description
CS	SPI enable I^2C/SPI mode selection (1: SPI idle mode / I^2C communication enabled; 0: SPI communication mode / I^2C disabled)
SCL SPC	I^2C serial clock (SCL) SPI serial port clock (SPC)
SDA SDI SDO	I^2C serial data (SDA) SPI serial data input (SDI) 3-wire interface serial data output (SDO)
SA0 SDO	I^2C address selection (SA0) SPI serial data output (SDO)

6.1 I^2C serial interface

The LIS2HH12 I^2C is a bus slave. The I^2C is employed to write data into registers whose content can also be read back.

The relevant I^2C terminology is given in the table below.

Table 12. I^2C terminology

Term	Description
Transmitter	The device which sends data to the bus
Receiver	The device which receives data from the bus
Master	The device which initiates a transfer, generates clock signals and terminates a transfer
Slave	The device addressed by the master

There are two signals associated with the I^2C bus: the serial clock line (SCL) and the Serial DAta line (SDA). The latter is a bidirectional line used for sending and receiving the data to/from the interface. Both the lines must be connected to Vdd_IO through an external pull-up resistor. When the bus is free, both the lines are high.

The I^2C interface is compliant with fast mode (400 kHz) I^2C standards as well as with normal mode.

In order to disable the I^2C block, *CTRL4 (23h)* (I2C_DISABLE) = 1 must be set.

6.1.1 I²C operation

The transaction on the bus is started through a START (ST) signal. A START condition is defined as a high-to-low transition on the data line while the SCL line is held high. After this has been transmitted by the master, the bus is considered busy. The next byte of data transmitted after the start condition contains the address of the slave in the first 7 bits and the eighth bit tells whether the master is receiving data from the slave or transmitting data to the slave. When an address is sent, each device in the system compares the first seven bits after a start condition with its address. If they match, the device considers itself addressed by the master.

The Slave Address (SAD) associated to the LIS2HH12 is 00111xxb where the xx bits are modified by the SA0/SDO pin in order to modify the device address. If the SA0/SDO pin is connected to the supply voltage, the address is 0011101b, otherwise if the SA0/SDO pin is connected to ground, the address is 0011110b. This solution permits to connect and address two different accelerometers to the same I²C lines.

Data transfer with acknowledge is mandatory. The transmitter must release the SDA line during the acknowledge pulse. The receiver must then pull the data line low so that it remains stable low during the high period of the acknowledge clock pulse. A receiver which has been addressed is obliged to generate an acknowledge after each byte of data received.

The I²C embedded inside the LIS2HH12 behaves like a slave device and the following protocol must be adhered to. After the start condition (ST) a slave address is sent. Once a slave acknowledge (SAK) has been returned, an 8-bit sub-address (SUB) is transmitted: the 7 LSb represents the actual register address while the *CTRL4 (23h)* (IF_ADD_INC) bit defines the address increment.

The slave address is completed with a Read/Write bit. If the bit is '1' (Read), a repeated START (SR) condition must be issued after the two sub-address bytes. If the bit is '0' (Write) the master will transmit to the slave with direction unchanged. *Table 13* explains how the SAD+Read/Write bit pattern is composed, listing all the possible configurations.

Table 13. SAD+Read/Write patterns

Command	SAD[6:2]	SAD[1] = $\overline{SA0}$	SAD[0] = SA0	R/W	SAD+R/W
Read	00111	1	0	1	00111101
Write	00111	1	0	0	00111100
Read	00111	0	1	1	00111011
Write	00111	0	1	0	00111010

Table 14. Transfer when master is writing one byte to slave

Master	ST	SAD + W		SUB		DATA		SP
Slave			SAK		SAK		SAK	

Table 15. Transfer when master is writing multiple bytes to slave

Master	ST	SAD + W		SUB		DATA		DATA		SP
Slave			SAK		SAK		SAK		SAK	

Table 16. Transfer when master is receiving (reading) one byte of data from slave

Master	ST	SAD + W		SUB		SR	SAD + R			NMAK	SP
Slave			SAK		SAK			SAK	DATA		

Table 17. Transfer when master is receiving (reading) multiple bytes of data from slave

Master	ST	SAD+W		SUB		SR	SAD+R			MAK		MAK		NMAK	SP
Slave			SAK		SAK			SAK	DATA		DAT A		DATA		

Data are transmitted in byte format (DATA). Each data transfer contains 8 bits. The number of bytes transferred per transfer is unlimited. Data is transferred with the Most Significant bit (MSb) first. If a receiver can't receive another complete byte of data until it has performed some other function, it can hold the clock line, SCL low to force the transmitter into a wait state. Data transfer only continues when the receiver is ready for another byte and releases the data line. If a slave receiver doesn't acknowledge the slave address (i.e. it is not able to receive because it is performing some real-time function) the data line must be left high by the slave. The master can then abort the transfer. A low-to-high transition on the SDA line while the SCL line is high is defined as a STOP condition. Each data transfer must be terminated by the generation of a STOP (SP) condition.

In the presented communication format MAK is Master acknowledge and NMAK is No Master Acknowledge.

6.2 SPI bus interface

The LIS2HH12 SPI is a bus slave. The SPI allows to write and read the registers of the device.

The serial interface interacts with the outside world with 4 wires: **CS**, **SPC**, **SDI** and **SDO**.

Figure 8. Read and write protocol