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Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China



INERTIAL SENSOR: 2Axis - 2g/6g LINEAR ACCELEROMETER

1 FEATURES

- 2.4V TO 5.25V SINGLE SUPPLY OPERATION
- 0.5mg RESOLUTION OVER 100Hz BW
- 2g/6g USER SELECTABLE FULL-SCALE
- OUTPUT VOLTAGE, OFFSET AND SENSITIVITY RATIOMETRIC TO THE SUPPLY VOLTAGE
- FACTORY TRIMMED DEVICE SENSITIVITY AND OFFSET
- EMBEDDED SELF TEST
- HIGH SHOCK SURVIVABILITY

2 DESCRIPTION

The LIS2L02AQ is a dual-axis linear accelerometer that includes a sensing element and an IC interface able to take the information from the sensing element and to provide an analog signal to the external world.

The sensing element, capable to detect the acceleration, is manufactured using a dedicated process called THELMA (Thick Epi-Poly Layer for Microactuators and Accelerometers) developed by ST to produce inertial sensors and actuators in silicon.

The IC interface instead is manufactured using a CMOS process that allows high level of integration to design a dedicated circuit which is trimmed to better match the sensing element characteristics.

The LIS2L02AQ has a user selectable full scale of

Figure 1. Package



Table 1. Order Codes

| Part Number | Package |
|-------------|---------|
| LIS2L02AQ | QFN-44 |

2g, 6g and it is capable of measuring accelerations over a maximum bandwidth of 4.0 KHz for both the X and Y axis. The device bandwidth may be reduced by using external capacitances. A self-test capability allows the user to check the functioning of the system.

The LIS2L02AQ is available in plastic SMD package and it is specified over a temperature range extending from -40°C to +85°C.

The LIS2L02AQ belongs to a family of products suitable for a variety of applications:

- Motion activated functions in mobile terminals
- Gaming and Virtual Reality input devices
- Virtual reality input devices
- Antitheft systems and Inertial Navigation
- Appliance Control and Robotics

Figure 2. Block Diagram

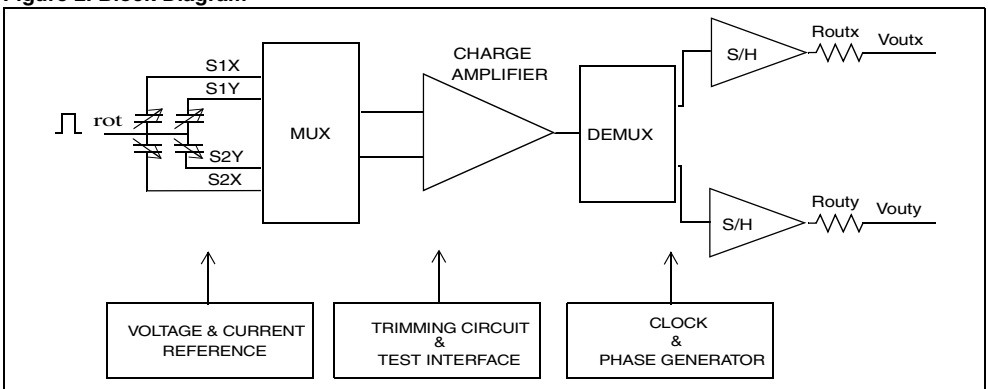


Figure 3. Pin Description

| N° | Pin | Function |
|--------|----------|---|
| 1 to 3 | NC | Internally not connected |
| 4 | GND | 0V supply |
| 5 | Vdd | Power supply |
| 6 | Vouty | Output Voltage |
| 7 | ST | Self Test (Logic 0: normal mode; Logic 1: Self-test) |
| 8 | Voutx | Output Voltage |
| 9-13 | NC | Internally not connected |
| 14 | PD | Power Down (Logic 0: normal mode; Logic 1: Power-Down mode) |
| 15 | NC | Internally not connected |
| 16 | FS | Full Scale selection (Logic 0: 2g Full-scale; Logic 1: 6g Full-scale) |
| 17-18 | Reserved | Leave unconnected |
| 19 | NC | Internally not connected |
| 20 | Reserved | Leave unconnected |
| 21 | NC | Internally not connected |
| 22-23 | Reserved | Leave unconnected |
| 24-25 | NC | Internally not connected |
| 26 | Reserved | Connect to Vdd or GND |
| 27 | Reserved | Leave unconnected or connect to Vdd |
| 28 | Reserved | Leave unconnected or connect to GND |
| 29-44 | NC | Internally not connected |

Figure 4. Pin Connection (Top view)

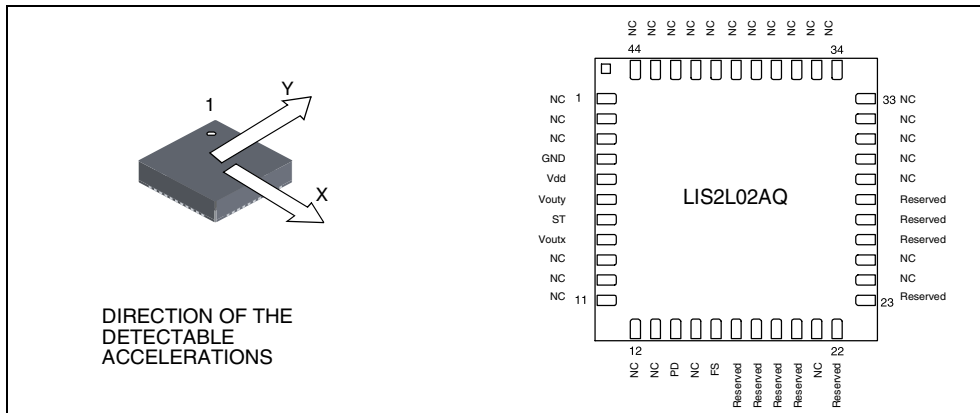


Table 2. Electrical Characteristics

(Temperature range -40°C to +85°C) All the parameters are specified @ Vdd =3.3V, T=25°C unless otherwise noted

| Symbol | Parameter | Test Condition | Min. | Typ. ¹ | Max. | Unit |
|---------|--|--|------------|-------------------|------------|------------|
| Vdd | Supply voltage | | 2.4 | 3.3 | 5.25 | V |
| Idd | Supply current | mean value PD pin connected to GND | | 0.85 | 1.5 | mA |
| IddPdn | Supply current in Power Down Mode | rms value PD pin connected to Vdd | | 2 | 5 | μA |
| Voff | Zero-g level ² | T = 25°C | Vdd/2-10% | Vdd/2 | Vdd/2+10% | V |
| OffDr | Zero-g level Vs temperature | Delta from +25°C | | ±1.5 | | mg/°C |
| Ar | Acceleration range ³ | FS pin connected to GND | ±1.8 | ±2.0 | | g |
| | | FS pin connected to Vdd | ±5.4 | ±6.0 | | g |
| So | Sensitivity ² | Full-scale = 2g | Vdd/5-10% | Vdd/5 | Vdd/5+10% | V/g |
| | | Full-scale = 6g | Vdd/15-10% | Vdd/15 | Vdd/15+10% | V/g |
| SoDr | Sensitivity drift Vs temperature | Delta from +25°C | | ±0.01 | | %/°C |
| NL | Non Linearity ⁴ | Best fit straight line Full-scale = 2g X, Y axis | | ±0.3 | ±1.5 | % FS |
| CrossAx | Cross-Axis ⁵ | | | ±2 | ±4 | % |
| fuc | Sensing Element Resonant Frequency ⁶ | X, Y axis | 3.2 | 4.0 | 4.8 | KHz |
| an | Acceleration noise density | Vdd=3.3V; Full-scale = 2g | | 50 | | μg/ √Hz |
| Vt | Self test output voltage delta change ^{7,8,9} | T = 25°C Vdd=3.3V Full-scale = 2g X axis | -20 | 40 | | mV |
| | | T = 25°C Vdd=3.3V Full-scale = 2g Y axis | 20 | -40 | | mV |
| | | | | | | |
| | | | | | | |
| Vst | Self test input | Logic 0 level | 0 | | 0.8 | V |
| | | Logic 1 level | 2.2 | | Vdd | V |
| Rout | Output impedance | | 80 | 110 | 140 | kΩ |

Table 2. Electrical Characteristics (continued)

(Temperature range -40°C to +85°C) All the parameters are specified @ Vdd =3.3V, T=25°C unless otherwise noted

| Symbol | Parameter | Test Condition | Min. | Typ. ¹ | Max. | Unit |
|--------|---|-----------------|------|-------------------|------|------|
| Cload | Capacitive load drive ¹⁰ | | 320 | | | pF |
| Ton | Turn-On Time at exit from Power Down mode | Load in μ F | | 550*Cload +0.3 | | ms |

- Notes: 1. Typical specifications are not guaranteed
 2. Offset and sensitivity are essentially ratiometric to supply voltage
 3. Guaranteed by wafer level test and measurement of initial offset and sensitivity
 4. Guaranteed by design through measurements done up to 1g
 5. Contribution to the measuring output of the inclination/acceleration along the perpendicular axis
 6. Guaranteed by design
 7. Self test "output voltage delta change" is defined as $V_{out}(V_{st=Logic1}) - V_{out}(V_{st=Logic0})$
 8. Self test "output voltage delta change" varies cubically with supply voltage
 9. When full-scale is set to 6g, self-test "output delta change" is one third of the specified value
 10. Bandwidth = $1/(2 * \pi * 110K\Omega * Cload)$

ABSOLUTE MAXIMUM RATING

Stresses above those listed as "absolute maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 3. Absolute Maximum Rating

| Symbol | Ratings | Maximum Value | Unit |
|------------------|---|-------------------|------|
| Vdd | Supply voltage | -0.3 to 7 | V |
| Vin | Input voltage on any control pin (FS, PD, ST) | -0.3 to Vdd +0.3 | V |
| A _{POW} | Acceleration (Any axis, Powered, Vdd=3.3V) | 3000g for 0.5 ms | |
| | | 10000g for 0.1 ms | |
| A _{UNP} | Acceleration (Any axis, Unpowered) | 3000g for 0.5 ms | |
| | | 10000g for 0.1 ms | |
| T _{OP} | Operating Temperature Range | -40 to +85 | °C |
| T _{STG} | Storage Temperature Range | -40 to +105 | °C |
| ESD | Electrostatic discharge protection | 2KV HBM | |

3 FUNCTIONALITY

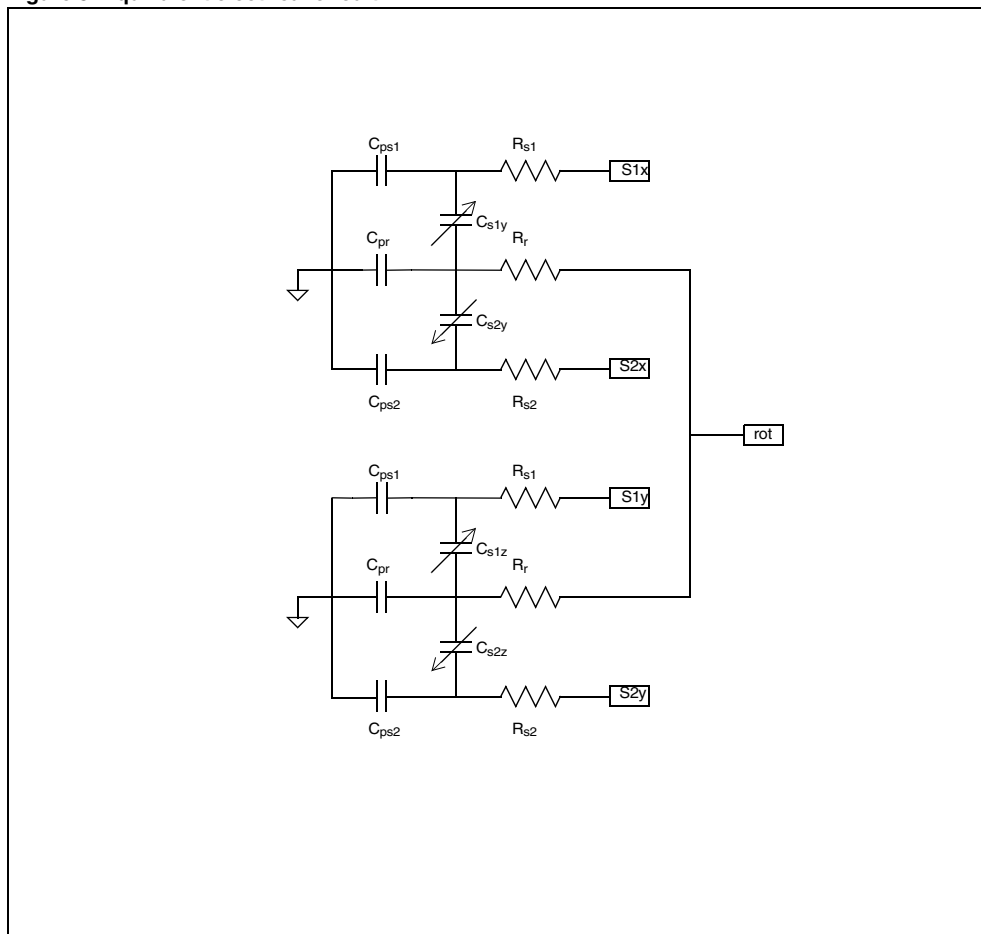
The LIS2L02AQ is a low-cost, low-power, analog output dual-axis linear accelerometer packaged in QFN package. The complete device includes a sensing element and an IC interface able to take the information from the sensing element and to provide an analog signal to the external world.

3.1 Sensing element

The THELMA process is utilized to create a surface micro-machined accelerometer. The technology allows to carry out suspended silicon structures which are attached to the substrate in a few points called anchors and free to move on a plane parallel to the substrate itself. To be compatible with the traditional packaging techniques a cap is placed on top of the sensing element to avoid blocking the moving parts during the molding phase.

The equivalent circuit for the sensing element is shown in the figure below; when a linear acceleration is applied, the proof mass displaces from its nominal position, causing an imbalance in the capacitive half-bridge. This imbalance is measured using charge integration in response to a voltage pulse applied to the sense capacitor.

Figure 5. Equivalent electrical circuit



The nominal value of the capacitors, at steady state, is few pF and when an acceleration is applied the maximum variation of the capacitive load is few hundredths of pF.

3.2 IC Interface

The complete signal processing uses a fully differential structure, while the final stage converts the differential signal into a single-ended one to be compatible with the external world.

The first stage is a low-noise capacitive amplifier that implements a Correlated Double Sampling (CDS) at its output to cancel the offset and the $1/f$ noise. The produced signal is then sent to two different S&Hs, one for each channel, and made available to the outside.

The low noise input amplifier operates at 200 kHz while the two S&Hs operate at a sampling frequency of 66 kHz. This allows a large oversampling ratio, which leads to in-band noise reduction and to an accurate output waveform.

All the analog parameters (output offset voltage and sensitivity) are ratiometric to the voltage supply. Increasing or decreasing the voltage supply, the sensitivity and the offset will increase or decrease linearly. The feature provides the cancellation of the error related to the voltage supply along an analog to digital conversion chain.

3.3 Factory calibration

The IC interface is factory calibrated to provide to the final user a device ready to operate.

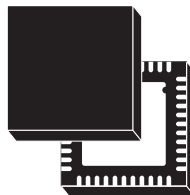
The trimming values are stored inside the device by a non volatile structure. Any time the device is turned on, the trimming parameters are downloaded into the registers to be employed during the normal operation thus allowing the final user to utilize the device without any need for further calibration.

4 PACKAGE INFORMATION

Figure 6. QFN-44 Mechanical Data & Package Dimensions

| DIM. | mm | | | inch | | |
|------|------|--------|------|-------|--------|-------|
| | MIN. | TYP. | MAX. | MIN. | TYP. | MAX. |
| A | 1.70 | 1.80 | 1.90 | 0.067 | 0.071 | 0.075 |
| A1 | 0.19 | | 0.21 | 0.007 | | 0.008 |
| b | 0.20 | 0.25 | 0.30 | 0.008 | 0.01 | 0.012 |
| D | | 7.0 | | | 0.276 | |
| E | | 7.0 | | | 0.276 | |
| e | | 0.50 | | | 0.020 | |
| J | 5.04 | | 5.24 | 0.198 | | 0.206 |
| K | 5.04 | | 5.24 | 0.198 | | 0.206 |
| L | 0.38 | 0.48 | 0.58 | 0.015 | 0.019 | 0.023 |
| P | | 45 REF | | | 45 REF | |

OUTLINE AND MECHANICAL DATA



QFN-44 (7x7x1.8mm)
Quad Flat Package No lead

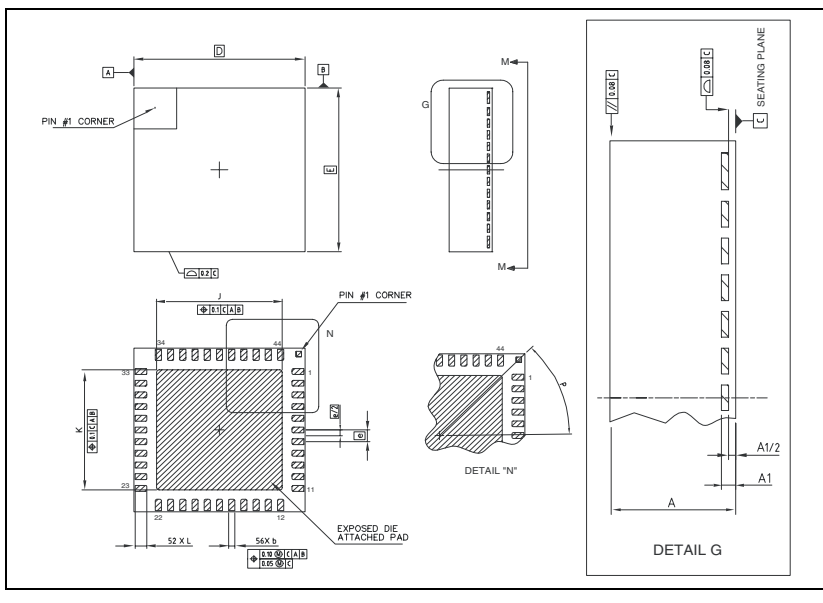


Table 4. Revision History

| Date | Revision | Description of Changes |
|---------------|-----------------|--|
| January 2004 | 1 | First Issue |
| February 2004 | 2 | Values of some parameters have been changed in Electrical characteristics table. |
| November 2004 | 3 | Changed the maturity from Product Preview to Final. Modified/added some values in the table 2 Electrical characteristics. |

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