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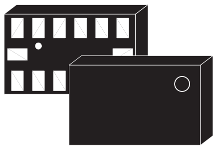
LIS35DE

MEMS motion sensor
3-axis - ±2g/±8g smart digital output “piccolo” accelerometer



LGA14 (3x5x0.9mm)

Feature

- 2.16 V to 3.6 V supply voltage
- 1.8V compatible IOs
- < 1 mW power consumption
- ±2g/±8g dynamically selectable full-scale
- I^2C/SPI digital output interface
- Programmable multiple interrupt generator
- Click and double click recognition
- Embedded high pass filter
- 10000g high shock survivability
- ECOPACK® RoHS and “Green” compliant (see *Section 8*)

Applications

- Free-fall detection
- Motion activated functions
- Gaming and virtual reality input devices
- Vibration monitoring and compensation

Description

The LIS35DE is an ultra compact low-power three axis linear accelerometer. It includes a sensing element and an IC interface able to provide the measured acceleration to the external world through I^2C/SPI serial interface.

The sensing element, capable of detecting the acceleration, is manufactured using a dedicated process developed by ST to produce inertial sensors and actuators in silicon.

The IC interface is manufactured using a CMOS process that allows to design a dedicated circuit which is trimmed to better match the sensing element characteristics.

The LIS35DE has dynamically user selectable full scales of ±2g/±8g and it is capable of measuring accelerations with an output data rate of 100 Hz or 400 Hz.

The device may be configured to generate inertial wake-up/free-fall interrupt signals when a programmable acceleration threshold is crossed at least in one of the three axes. Thresholds and timing of interrupt generators are programmable by the end user on the fly.

The LIS35DE is available in plastic Thin Land Grid Array package (TGA) and it is designed to operate over an extended temperature range from -40°C to +85°C.

Table 1. Device summary

Order code	Temp range, °C	Package	Packing
LIS35DE	-40 to +85	LGA14	Tray
LIS35DETR	-40 to +85	LGA14	Tape and reel

Contents

List of tables

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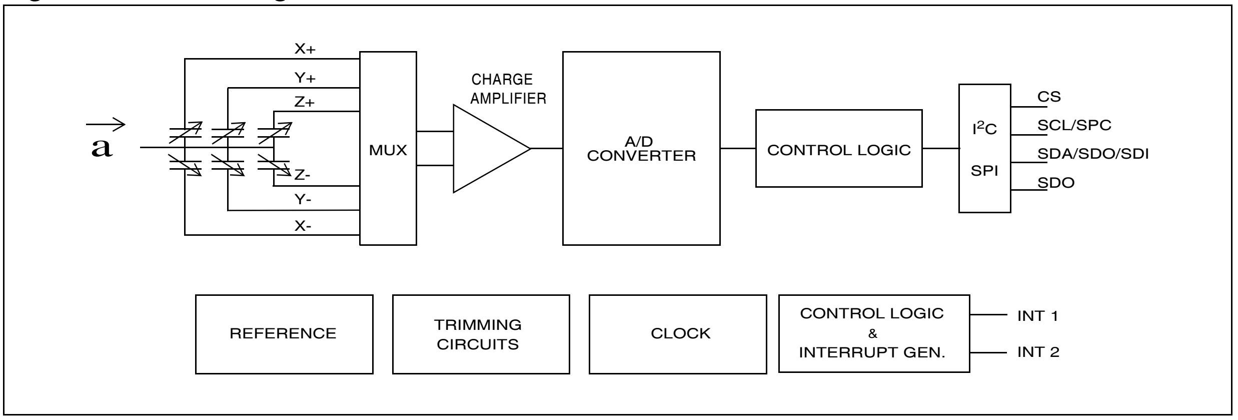
1 Block diagram and pin description

1.1 Block diagram

Figure 1. Block diagram



1.2 Pin description

Figure 2. Pin connection

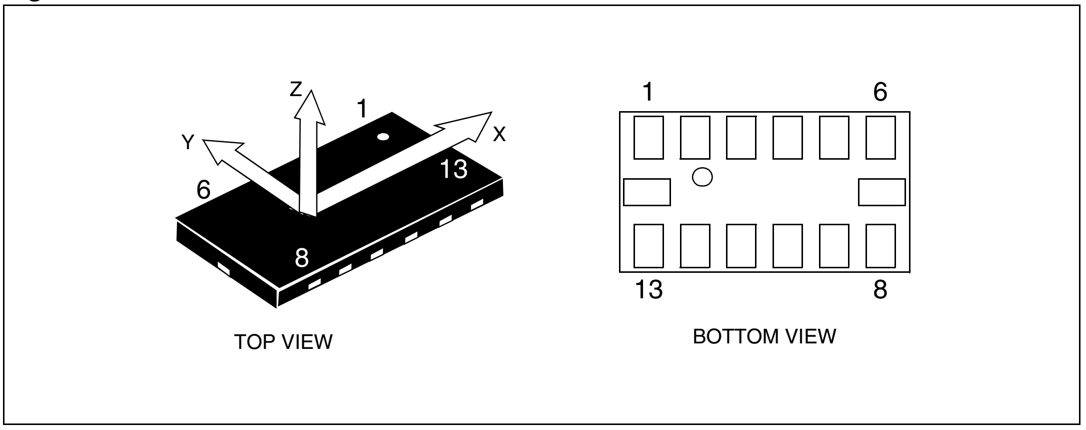


Table 2. Pin description

Pin#	Name	Function
1	Vdd_IO	Power supply for I/O pins
2	GND	0V supply
3	Reserved	Connect to Vdd
4	GND	0V supply
5	GND	0V supply
6	Vdd	Power supply
7	CS	SPI enable I^2C/SPI mode selection (1: I^2C mode; 0: SPI enabled)
8	INT 1	Inertial interrupt 1
9	INT 2	Inertial interrupt 2
10	GND	0V supply
11	Reserved	Connect to Gnd
12	SDO	SPI serial data output I^2C less significant bit of the device address
13	SDA SDI SDO	I^2C serial data (SDA) SPI serial data input (SDI) 3-wire interface serial data output (SDO)
14	SCL SPC	I^2C serial clock (SCL) SPI serial port clock (SPC)

2 Mechanical and electrical specifications

2.1 Mechanical characteristics

T = 25°C unless otherwise noted

Table 3. Mechanical characteristics @ Vdd=2.5 V(1)

Symbol	Parameter	Test conditions	Min.	Typ.(2)	Max.	Unit
FS	Measurement range	FS bit set to 0(3)	±2.0	±2.3		g
		FS bit set to 1		±9.2		
Dres	Device resolution	FS bit set to 0		72		mg
So	Sensitivity	FS bit set to 0	15	18	21	mg/digit
		FS bit set to 1	61	72	83	
TCSO	Sensitivity change vs temperature	FS bit set to 0		±0.01		%/°C
TyOff	Typical zero-g level offset accuracy(4)	FS bit set to 0		±60		mg
		FS bit set to 1		±80		mg
TCOff	Zero-g level change vs temperature	Max delta from 25°C		±0.5		mg/°C
BW	System bandwidth(5)			ODR/2		Hz
Top	Operating temperature range		-40		+85	°C
Wh	Product weight			20		mgram

1. The product is factory calibrated at 2.5 V. The device can be used from 2.16 V to 3.6 V.
2. Typical specifications are not guaranteed.
3. Verified by wafer level test and measurement of initial offset and sensitivity.
4. Typical zero-g level offset value after MSL3 preconditioning.
5. ODR is output data rate. Refer to *Table 4* for specifications.

2.2 Electrical characteristics

T = 25°C unless otherwise noted

Table 4. Electrical characteristics @ Vdd=2.5 V (1)

Symbol	Parameter	Test conditions	Min.	Typ.(2)	Max.	Unit
Vdd	Supply voltage		2.16	2.5	3.6	V
Vdd_IO	I/O pins supply voltage(3)		1.71		Vdd+0.1	V
Idd	Supply current	T = 25°C, ODR=100 Hz		0.3	0.45	mA
IddPdn	Current consumption in power-down mode	T = 25°C		1	5	μA
VIH	Digital high level input voltage		0.8*Vdd_IO			V
VIL	Digital low level input voltage				0.2*Vdd_IO	V
VOH	High level output voltage		0.9*Vdd_IO			V
VOL	Low level output voltage				0.1*Vdd_IO	V
ODR	Output data rate	DR=0		100		Hz
		DR=1		400		
BW	System bandwidth(4)			ODR/2		Hz
Ton	Turn-on time(5)			3/ODR		s
Top	Operating temperature range		-40		+85	°C

1. The product is factory calibrated at 2.5V. The device can be used from 2.16 V to 3.6 V.
2. Typical specification are not guaranteed.
3. It is possible to remove Vdd maintaining Vdd_IO without blocking the communication busses, in this condition the measurement chain is powered off.
4. Filter cut-off frequency.
5. Time to obtain valid data after exiting power-down mode.

2.3 Communication interface characteristics

2.3.1 SPI - serial peripheral interface

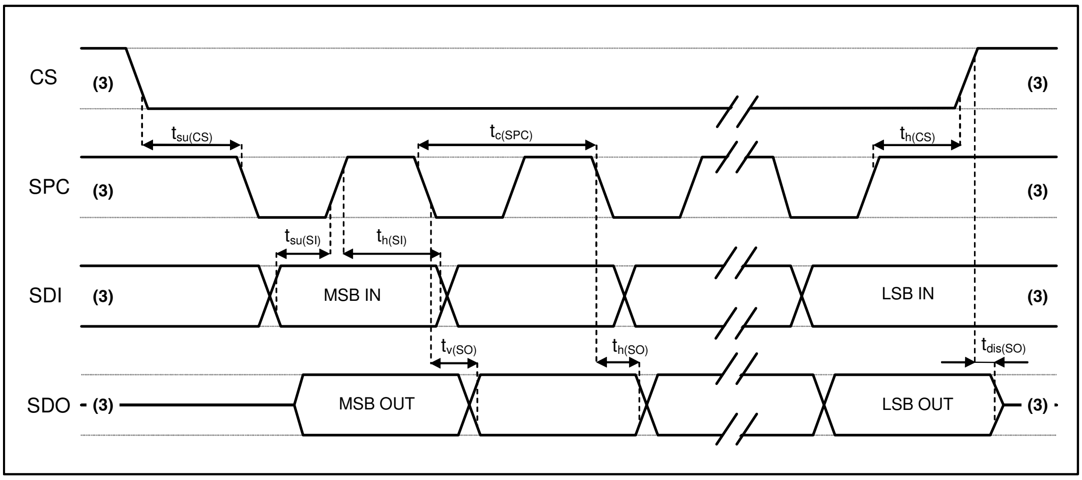
Subject to general operating conditions for Vdd and Top.

Table 5. SPI slave timing values

Symbol	Parameter	Value [(1)]		Unit
		Min.	Max.	
tc(SPC)	SPI clock cycle	100		ns
fc(SPC)	SPI clock frequency		10	MHz
tsu(CS)	CS setup time	5		ns
th(CS)	CS hold time	8		
tsu(SI)	SDI input setup time	5		
th(SI)	SDI input hold time	15		
tv(SO)	SDO valid output time		50	
th(SO)	SDO output hold time	6		
tdis(SO)	SDO output disable time		50	

1. Values are guaranteed at 10 MHz clock frequency for SPI with both 4 and 3 wires, based on characterization results, not tested in production

Figure 3. SPI slave timing diagram [(a)]



3. When no communication is on-going, data on CS, SPC, SDI and SDO are driven by internal pull-up resistors

a. Measurement points are done at 0.2·Vdd_IO and 0.8·Vdd_IO, for both input and output port

2.3.2 I²C - Inter IC control interface

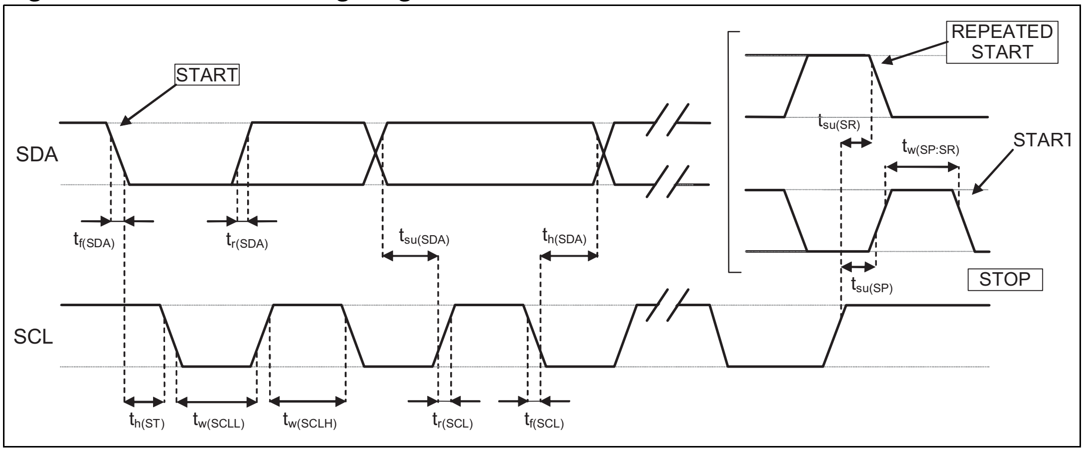
Subject to general operating conditions for Vdd and top.

Table 6. I²C slave timing values

Symbol	Parameter	I²C standard mode [(1)]		I²C fast mode [(1)]		Unit
		Min	Max	Min	Max	
$f_{(SCL)}$	SCL clock frequency	0	100	0	400	KHz
$t_{w(SCLL)}$	SCL clock low time	4.7		1.3		µs
$t_{w(SCLH)}$	SCL clock high time	4.0		0.6		
$t_{su(SDA)}$	SDA setup time	250		100		ns
$t_{h(SDA)}$	SDA data hold time	0.01	3.45	0.01	0.9	µs
$t_{r(SDA)}$ $t_{r(SCL)}$	SDA and SCL rise time		1000	$20 + 0.1C_b$ [(2)]	300	ns
$t_{f(SDA)}$ $t_{f(SCL)}$	SDA and SCL fall time		300	$20 + 0.1C_b$ [(2)]	300	
$t_{h(ST)}$	START condition hold time	4		0.6		µs
$t_{su(SR)}$	Repeated START condition setup time	4.7		0.6		
$t_{su(SP)}$	STOP condition setup time	4		0.6		
$t_{w(SP:SR)}$	Bus free time between STOP and START condition	4.7		1.3		

1. Data based on standard I²C protocol requirement, not tested in production
2. Cb = total capacitance of one bus line, in pF

Figure 4. I²C Slave timing diagram [(b)]



b. Measurement points are done at 0.2·Vdd_IO and 0.8·Vdd_IO, for both port

2.4 Absolute maximum ratings

Stresses above those listed as “absolute maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 7. Absolute maximum ratings

Symbol	Ratings	Maximum value	Unit
Vdd	Supply voltage	-0.3 to 6	V
Vdd_IO	I/O pins supply voltage	-0.3 to 6	V
Vin	Input voltage on any control pin (CS, SCL/SPC, SDA/SDI/SDO)	-0.3 to Vdd_IO +0.3	V
A_{POW}	Acceleration (any axis, powered, Vdd=2.5V)	3000g for 0.5 ms	
		10000g for 0.1 ms	
A_{UNP}	Acceleration (any axis, unpowered)	3000g for 0.5 ms	
		10000g for 0.1 ms	
T_{OP}	Operating temperature range	-40 to +85	°C
T_{STG}	Storage temperature range	-40 to +125	°C
ESD	Electrostatic discharge protection	4 (HBM)	kV
		1.5 (CDM)	kV
		200 (MM)	V

Note: Supply voltage on any pin should never exceed 6.0 V

This is a mechanical shock sensitive device, improper handling can cause permanent damages to the part

This is an ESD sensitive device, improper handling can cause permanent damages to the part

2.5 Terminology

2.5.1 Sensitivity

Sensitivity describes the gain of the sensor and can be determined e.g. by applying 1g acceleration to it. As the sensor can measure DC accelerations this can be done easily by pointing the axis of interest towards the center of the Earth, noting the output value, rotating the sensor by 180 degrees (point to the sky) and noting the output value again. By doing so, ±1g acceleration is applied to the sensor. Subtracting the larger output value from the smaller one and dividing the result by 2 leads to the actual sensitivity of the sensor. This value changes very little over temperature and also very little over time. The Sensitivity Tolerance describes the range of Sensitivities of a large population of sensor.

2.5.2 Zero-g level

Zero-g level Offset (Off) describes the deviation of an actual output signal from the ideal output signal if there is no acceleration present. A sensor in a steady state on a horizontal surface will measure 0g in X axis and 0g in Y axis whereas the Z axis will measure 1g. The output is ideally in the middle of the dynamic range of the sensor (content of OUT registers 00h, data expressed as 2's complement number). A deviation from ideal value in this case is called Zero-g offset. Offset is to some extent a result of stress to a precise MEMS sensor and therefore the offset can slightly change after mounting the sensor onto a printed circuit board or exposing it to extensive mechanical stress. Offset changes little over temperature, see "Zero-g level change vs. temperature". The Zero-g level of an individual sensor is stable over lifetime. The Zero-g level tolerance describes the range of Zero-g levels of a population of sensors.

2.5.3 Click and double click recognition

The click and double click recognition functions help to create man-machine interface with little software overload. The device can be configured to output an interrupt signal on dedicated pin when tapped in any direction.

If the sensor is exposed to a single input stimulus it generates an interrupt request on inertial interrupt pin (INT1 and/or INT2). A more advanced feature allows to generate and interrupt request when a "double click" with programmable time between the two events enabling a "mouse button like" use.

This function can be fully programmed by the user in terms of expected amplitude and timing of the stimuli.

3 Functionality

The LIS35DE is a ultracompact, low-power, digital output 3-axis linear accelerometer packaged in a LGA package. The complete device includes a sensing element and an IC interface able to take the information from the sensing element and to provide a signal to the external world through an I^2C/SPI serial interface.

3.1 Sensing element

A proprietary process is used to create a surface micro-machined accelerometer. The technology allows to carry out suspended silicon structures which are attached to the substrate in a few points called anchors and are free to move in the direction of the sensed acceleration. To be compatible with the traditional packaging techniques a cap is placed on top of the sensing element to avoid blocking the moving parts during the moulding phase of the plastic encapsulation.

When an acceleration is applied to the sensor the proof mass displaces from its nominal position, causing an imbalance in the capacitive half-bridge. This imbalance is measured using charge integration in response to a voltage pulse applied to the sense capacitor.

At steady state the nominal value of the capacitors are few pF and when an acceleration is applied the maximum variation of the capacitive load is in fF range.

3.2 IC interface

The complete measurement chain is composed by a low-noise capacitive amplifier which converts into an analog voltage the capacitive unbalancing of the MEMS sensor and by analog-to-digital converters.

The acceleration data may be accessed through an I^2C/SPI interface thus making the device particularly suitable for direct interfacing with a microcontroller.

The LIS35DE features a Data-Ready signal (RDY) which indicates when a new set of measured acceleration data is available thus simplifying data synchronization in the digital system that uses the device.

The LIS35DE may also be configured to generate an inertial Wake-Up and Free-Fall interrupt signal accordingly to a programmed acceleration event along the enabled axes. Both Free-Fall and Wake-Up can be available simultaneously on two different pins.

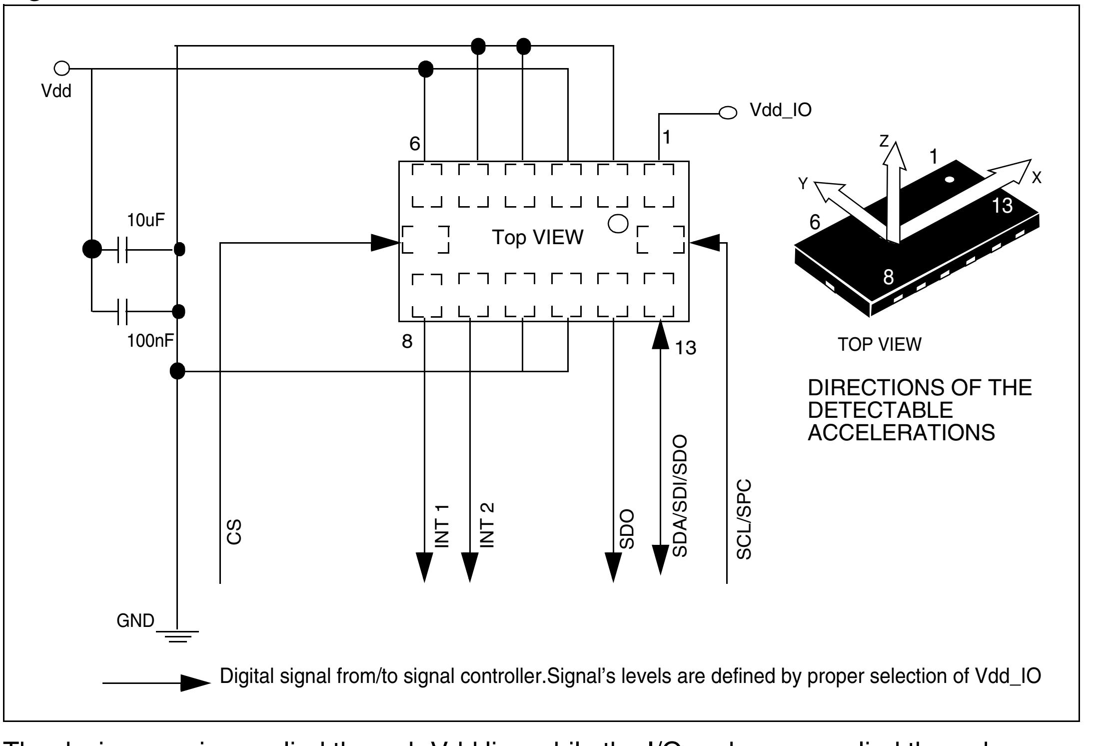
3.3 Factory calibration

The IC interface is factory calibrated for sensitivity (So) and Zero-g level (Off).

The trimming values are stored inside the device by a non volatile memory. Any time the device is turned on, the trimming parameters are downloaded into the registers to be used during the normal operation. This allows the user to use the device without further calibration.

4 Application hints

Figure 5. LIS35DE electrical connection



The device core is supplied through Vdd line while the I/O pads are supplied through Vdd_IO line. Power supply decoupling capacitors (100 nF ceramic, 10 µF Al) should be placed as near as possible to the pin 6 of the device (common design practice).

All the voltage and ground supplies must be present at the same time to have proper behavior of the IC (refer to *Figure 5*). It is possible to remove Vdd maintaining Vdd_IO without blocking the communication busses, in this condition the measurement chain is powered off.

The functionality of the device and the measured acceleration data is selectable and accessible through the I^2C/SPI interface.When using the I^2C, CS must be tied high.

The functions, the threshold and the timing of the two interrupt pins (INT 1 and INT 2) can be completely programmed by the user though the I^2C/SPI interface.

4.1 Soldering information

The LGA package is compliant with the ECOPACK®, RoHS and “Green” standard. It is qualified for soldering heat resistance according to JEDEC J-STD-020C.

Leave “Pin 1 Indicator” unconnected during soldering.

Land pattern and soldering recommendation are available at www.st.com.

5 Digital interfaces

The registers embedded inside the LIS35DE may be accessed through both the I^2C and SPI serial interfaces. The latter may be SW configured to operate either in 3-wire or 4-wire interface mode.

The serial interfaces are mapped onto the same pads. To select/exploit the I^2C interface, CS line must be tied high (i.e connected to Vdd_IO).

Table 8. Serial interface pin description

PIN Name	PIN description
CS	SPI enable I^2C/SPI mode selection (1: I^2C mode; 0: SPI enabled)
SCL/SPC	I^2C serial clock (SCL) SPI Serial port clock (SPC)
SDA/SDI/SDO	I^2C serial data (SDA) SPI serial data input (SDI) 3-wire interface serial data output (SDO)
SDO	SPI serial data output (SDO)

5.1 I^2C serial interface

The LIS35DE I^2C is a bus slave. The I^2C is employed to write the data into the registers whose content can also be read back.

The relevant I^2C terminology is given in the table below.

Table 9. Serial interface pin description

Term	Description
Transmitter	The device which sends data to the bus
Receiver	The device which receives data from the bus
Master	The device which initiates a transfer, generates clock signals and terminates a transfer
Slave	The device addressed by the master

There are two signals associated with the I^2C bus: the Serial Clock Line (SCL) and the Serial DAta line (SDA). The latter is a bidirectional line used for sending and receiving the data to/from the interface. Both the lines are connected to Vdd_IO through a pull-up resistor embedded inside the LIS35DE. When the bus is free both the lines are high.

The I^2C interface is compliant with fast mode (400 kHz) I^2C standards as well as the normal mode.

5.1.1 I²C operation

The transaction on the bus is started through a START (ST) signal. A START condition is defined as a HIGH to LOW transition on the data line while the SCL line is held HIGH. After this has been transmitted by the Master, the bus is considered busy. The next byte of data transmitted after the start condition contains the address of the slave in the first 7 bits and the eighth bit tells whether the Master is receiving data from the slave or transmitting data to the slave. When an address is sent, each device in the system compares the first seven bits after a start condition with its address. If they match, the device considers itself addressed by the Master.

The Slave ADdress (SAD) associated to the LIS35DE is 001110xb. **SDO** pad can be used to modify less significant bit of the device address. If SDO pad is connected to voltage supply LSb is '1' (address 0011101b) else if SDO pad is connected to ground LSb value is '0' (address 0011100b). This solution permits to connect and address two different accelerometer to the same I²C lines.

Data transfer with acknowledge is mandatory. The transmitter must release the SDA line during the acknowledge pulse. The receiver must then pull the data line LOW so that it remains stable low during the HIGH period of the acknowledge clock pulse. A receiver which has been addressed is obliged to generate an acknowledge after each byte of data has been received.

The I²C embedded inside the LIS35DE behaves like a slave device and the following protocol must be adhered to. After the start condition (ST) a salve address is sent, once a slave acknowledge (SAK) has been returned, a 8-bit sub-address is transmitted: the 7 LSb represent the actual register address while the MSB enables address auto increment. If the MSb of the SUB field is 1, the SUB (register address) is automatically incremented to allow multiple data read/write.

The slave address is completed with a Read/Write bit. If the bit is '1' (Read), a repeated START (SR) condition must be issued after the two sub-address bytes; if the bit is '0' (Write) the Master will transmits to the slave with direction unchanged. *Table 10* explains how the SAD+Read/Write bit pattern is composed, listing all the possible configurations.

Table 10. SAD+Read/Write patterns

Command	SAD[6:1]	SAD[0] = SDO	R/W	SAD+R/W
Read	001110	0	1	00111001 (39h)
Write	001110	0	0	00111000 (38h)
Read	001110	1	1	00111011 (3Bh)
Write	001110	1	0	00111010 (3Ah)

Table 11. Transfer when Master is writing one byte to slave

Master	ST	SAD + W		SUB		DATA		SP
Slave			SAK		SAK		SAK	

Table 12. Transfer when Master is writing multiple bytes to slave

Master	ST	SAD + W		SUB		DATA		DATA		SP
Slave			SAK		SAK		SAK		SAK	

Table 13. Transfer when Master is receiving (reading) one byte of data from slave

Master	ST	SAD + W		SUB		SR	SAD + R			NMAK	SP
Slave			SAK		SAK			SAK	DATA		

Table 14. Transfer when Master is receiving (reading) multiple bytes of data from slave

Master	ST	SAD + W		SUB		SR	SAD + R			MAK
Slave			SAK		SAK			SAK	DATA	

Table 15. Transfer when Master is receiving (reading) multiple bytes of data from slave

Master		MAK		NMAK	SP
Slave	DATA		DATA		

Data are transmitted in byte format (DATA). Each data transfer contains 8 bits. The number of bytes transferred per transfer is unlimited. Data is transferred with the Most Significant bit (MSb) first. If a receiver can't receive another complete byte of data until it has performed some other function, it can hold the clock line, SCL LOW to force the transmitter into a wait state. Data transfer only continues when the receiver is ready for another byte and releases the data line. If a slave receiver doesn't acknowledge the slave address (i.e. it is not able to receive because it is performing some real time function) the data line must be left HIGH by the slave. The Master can then abort the transfer. A LOW to HIGH transition on the SDA line while the SCL line is HIGH is defined as a STOP condition. Each data transfer must be terminated by the generation of a STOP (SP) condition.

In order to read multiple bytes, it is necessary to assert the most significant bit of the sub-address field. In other words, SUB(7) must be equal to 1 while SUB(6-0) represents the address of first register to read.

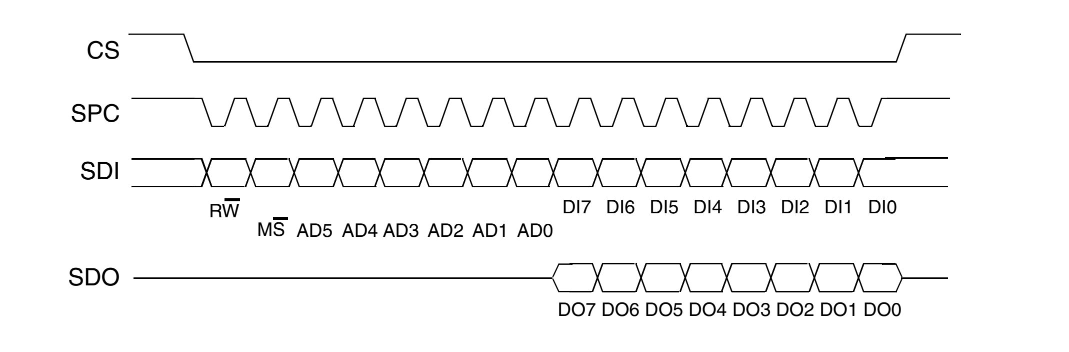
In the presented communication format MAK is Master Acknowledge and NMAK is No Master Acknowledge.

5.2 SPI bus interface

The LIS35DE SPI is a bus slave. The SPI allows to write and read the registers of the device.

The Serial Interface interacts with the outside world with 4 wires: **CS**, **SPC**, **SDI** and **SDO**.

Figure 6. Read and write protocol



CS is the Serial Port Enable and it is controlled by the SPI master. It goes low at the start of the transmission and goes back high at the end. **SPC** is the Serial Port Clock and it is controlled by the SPI master. It is stopped high when **CS** is high (no transmission). **SDI** and **SDO** are respectively the Serial Port Data Input and Output. Those lines are driven at the falling edge of **SPC** and should be captured at the rising edge of **SPC**.

Both the Read Register and Write Register commands are completed in 16 clock pulses or in multiple of 8 in case of multiple byte read/write. Bit duration is the time between two falling edges of **SPC**. The first bit (bit 0) starts at the first falling edge of **SPC** after the falling edge of **CS** while the last bit (bit 15, bit 23, ...) starts at the last falling edge of SPC just before the rising edge of **CS**.

bit 0: R$\overline{\text{W}}$ bit. When 0, the data DI(7:0) is written into the device. When 1, the data DO(7:0) from the device is read. In latter case, the chip will drives **SDO** at the start of bit 8.

bit 1: M$\overline{\text{S}}$ bit. When 0, the address will remains unchanged in multiple read/write commands. When 1, the address is auto incremented in multiple read/write commands.

bit 2-7: address AD(5:0). This is the address field of the indexed register.

bit 8-15: data DI(7:0) (write mode). This is the data that is written into the device (MSb first).

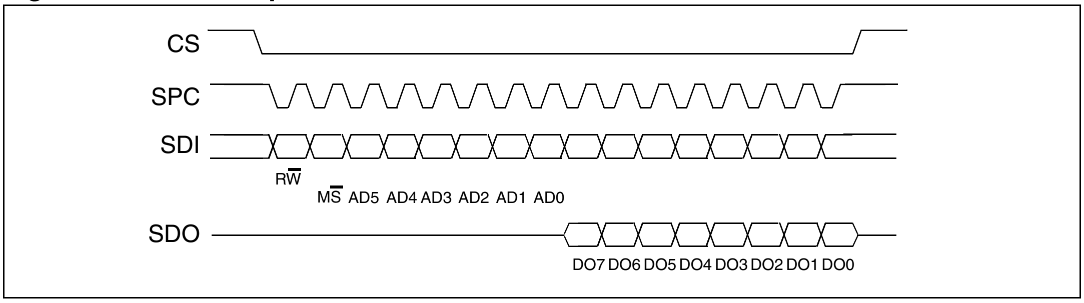
bit 8-15: data DO(7:0) (read mode). This is the data that will be read from the device (MSb first).

In multiple read/write commands further blocks of 8 clock periods will be added. When M$\overline{\text{S}}$ bit is 0 the address used to read/write data remains the same for every block. When M$\overline{\text{S}}$ bit is 1 the address used to read/write data is incremented at every block.

The function and the behavior of **SDI** and **SDO** remain unchanged.

5.2.1 SPI read

Figure 7. SPI read protocol



The SPI read command is performed with 16 clock pulses. Multiple byte read command is performed adding blocks of 8 clock pulses at the previous one.

bit 0: READ bit. The value is 1.

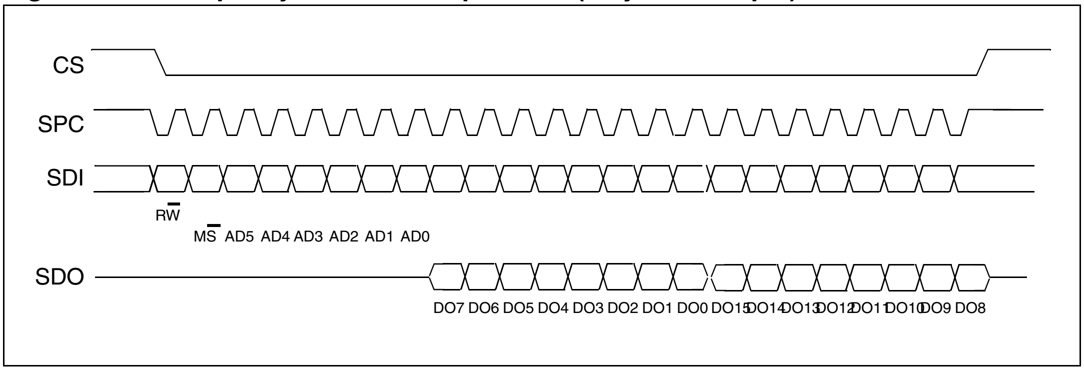
bit 1: M$\overline{S}$ bit. When 0 do not increment address, when 1 increment address in multiple reading.

bit 2-7: address AD(5:0). This is the address field of the indexed register.

bit 8-15: data DO(7:0) (read mode). This is the data that will be read from the device (MSb first).

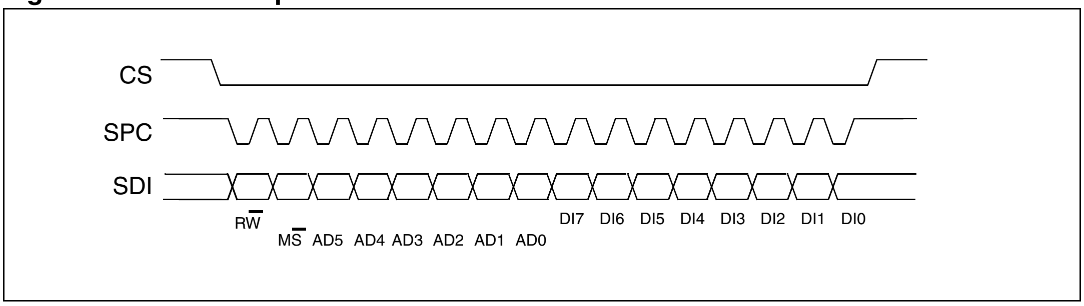
bit 16-... : data DO(...-8). Further data in multiple byte reading.

Figure 8. Multiple bytes SPI Read protocol (2 bytes example)



5.2.2 SPI write

Figure 9. SPI write protocol



The SPI write command is performed with 16 clock pulses. Multiple byte write command is performed adding blocks of 8 clock pulses at the previous one.

bit 0: WRITE bit. The value is 0.

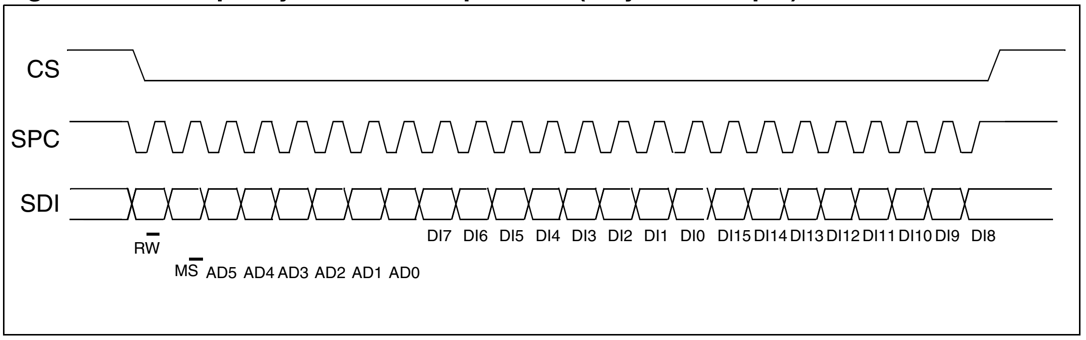
bit 1: M$\overline{S}$ bit. When 0 do not increment address, when 1 increment address in multiple writing.

bit 2 -7: address AD(5:0). This is the address field of the indexed register.

bit 8-15: data DI(7:0) (write mode). This is the data that will be written inside the device (MSb first).

bit 16-... : data DI(...-8). Further data in multiple byte writing.

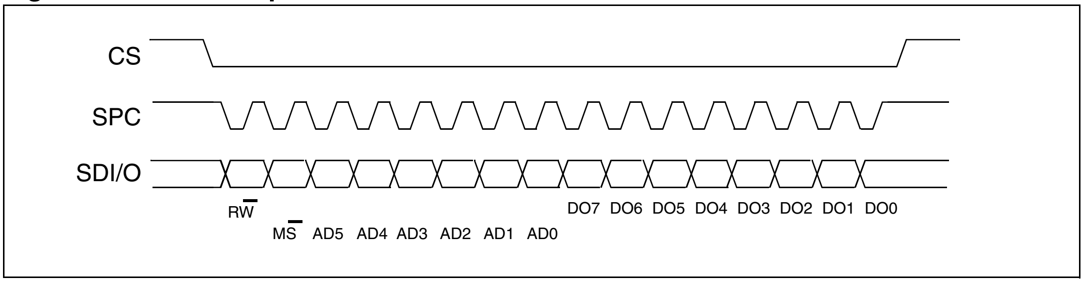
Figure 10. Multiple bytes SPI Write protocol (2 bytes example)



5.2.3 SPI read in 3-wires mode

3-wires mode is entered by setting to 1 bit SIM (SPI serial interface mode selection) in CTRL_REG2.

Figure 11. SPI read protocol in 3-wires mode



The SPI read command is performed with 16 clock pulses:

bit 0: READ bit. The value is 1.

bit 1: M$\overline{S}$ bit. When 0 do not increment address, when 1 increment address in multiple reading.

bit 2-7: address AD(5:0). This is the address field of the indexed register.

bit 8-15: data DO(7:0) (read mode). This is the data that will be read from the device (MSb first).

Multiple read command is also available in 3-wires mode.

6 Register mapping

The table given below provides a listing of the 8 bit registers embedded in the device and the related address:

Table 16. Register address map

Name	Type	Register address		Default	Comment
		Hex	Binary		
Reserved (do not modify)		00-1F			Reserved
Ctrl_Reg1	rw	20	010 0000	00000111	
Ctrl_Reg2	rw	21	010 0001	00000000	
Ctrl_Reg3	rw	22	010 0010	00000000	
HP_filter_reset	r	23	010 0011	dummy	Dummy register
Reserved (do not modify)		24-26			Reserved
Status_Reg	r	27	010 0111	00000000	
--	r	28	010 1000		Not used
OutX	r	29	010 1001	output	
--	r	2A	010 1010		Not used
OutY	r	2B	010 1011	output	
--	r	2C	010 1100		Not used
OutZ	r	2D	010 1101	output	
Reserved (do not modify)		2E-2F			Reserved
FF_WU_CFG_1	rw	30	011 0000	00000000	
FF_WU_SRC_1(ack1)	r	31	011 0001	00000000	
FF_WU_THS_1	rw	32	011 0010	00000100	
FF_WU_DURATION_1	rw	33	011 0011	00000000	
FF_WU_CFG_2	rw	34	011 0100	00000000	
FF_WU_SRC_2 (ack2)	r	35	011 0101	00000000	
FF_WU_THS_2	rw	36	011 0110	00000000	
FF_WU_DURATION_2	rw	37	011 0111	00000000	
CLICK_CFG	rw	38	011 1000	00000000	
CLICK_SRC (ack)	r	39	011 1001	00000000	
--		3A			Not used
CLICK_THSY_X	rw	3B	011 1011	00000000	
CLICK_THSZ	rw	3C	011 1100	00000000	
CLICK_TimeLimit	rw	3D	011 1101	00000000	

Table 16. Register address map (continued)

Name	Type	Register address		Default	Comment
		Hex	Binary		
CLICK_Latency	rw	3E	011 1110	00000000	
CLICK_Window	rw	3F	011 1111	00000000	

Registers marked as *Reserved* must not be changed. The writing to those registers may cause permanent damages to the device.

The content of the registers that are loaded at boot should not be changed. They contain the factory calibration values. Their content is automatically restored when the device is powered-up.

7 Register description

The device contains a set of registers which are used to control its behavior and to retrieve acceleration data. The registers address, made of 7 bits, is used to identify them and to write the data through serial interface.

7.1 CTRL_REG1 (20h)

Table 17. CTRL_REG1 (20h) register

DR	PD	FS	0(1)	0(1)	Zen	Yen	Xen

1. CTRL_REG1[4:3] value is loaded at boot, ‘0’ value must not be changed.

Table 18. CTRL_REG1 (20h) register description

DR	Data rate selection. Default value: 0 (0: 100 Hz output data rate; 1: 400 Hz output data rate)
PD	Power Down Control. Default value: 0 (0: power down mode; 1: active mode)
FS	Full Scale selection. Default value: 0 (refer to *Table 2* for typical full scale value)
Zen	Z axis enable. Default value: 1 (0: Z axis disabled; 1: Z axis enabled)
Yen	Y axis enable. Default value: 1 (0: Y axis disabled; 1: Y axis enabled)
Xen	X axis enable. Default value: 1 (0: X axis disabled; 1: X axis enabled)

DR bit allows to select the data rate at which acceleration samples are produced.
The default value is 0 which corresponds to a data-rate of 100Hz. By changing the content of DR to “1” the selected data-rate will be set equal to 400Hz.

PD bit allows to turn on the turn the device out of power-down mode. The device is in power-down mode when PD = “0” (default value after boot). The device is in normal mode when PD is set to 1.

Zen bit enables the generation of Data Ready signal for Z-axis measurement channel when set to 1. The default value is 1.

Yen bit enables the generation of Data Ready signal for Y-axis measurement channel when set to 1. The default value is 1.

Xen bit enables the generation of Data Ready signal for X-axis measurement channel when set to 1. The default value is 1.