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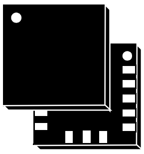
LIS3DSH

MEMS digital output motion sensor: ultra-low-power high-performance three-axis "nano" accelerometer

Datasheet - production data



LGA-16 (3x3x1 mm)

Features

- Wide supply voltage, 1.71 V to 3.6 V
- Independent IOs supply (1.8 V) and supply voltage compatible
- Ultra-low power consumption
- ±2*g*/±4*g*/±6*g*/±8*g*/±16*g* dynamically selectable full scale
- I^{2}C/SPI digital output interface
- 16-bit data output
- Programmable embedded state machines
- Embedded temperature sensor
- Embedded self-test
- Embedded FIFO
- 10000 *g* high shock survivability
- ECOPACK®, RoHS and “Green” compliant

Applications

- Motion-controlled user interface
- Gaming and virtual reality
- Pedometers
- Intelligent power saving for handheld devices
- Display orientation
- Click/double-click recognition
- Impact recognition and logging
- Vibration monitoring and compensation

Description

The LIS3DSH is an ultra-low-power high-performance three-axis linear accelerometer belonging to the “nano” family with an embedded state machine that can be programmed to implement autonomous applications.

The LIS3DSH has dynamically selectable full scales of ±2*g*/±4*g*/±6*g*/±8*g*/±16*g* and is capable of measuring accelerations with output data rates from 3.125 Hz to 1.6 kHz.

The self-test capability allows the user to check the functioning of the sensor in the final application.

The device can be configured to generate interrupt signals activated by user-defined motion patterns.

The LIS3DSH has an integrated first-in, first-out (FIFO) buffer allowing the user to store data in order to limit intervention by the host processor.

The LIS3DSH is available in a small thin plastic land grid array package (LGA) and is guaranteed to operate over an extended temperature range from -40 °C to +85 °C.

Table 1. Device summary

Order codes	Temperature range [°C]	Package	Packaging
LIS3DSHTR	-40 to +85	LGA-16	Tape and reel

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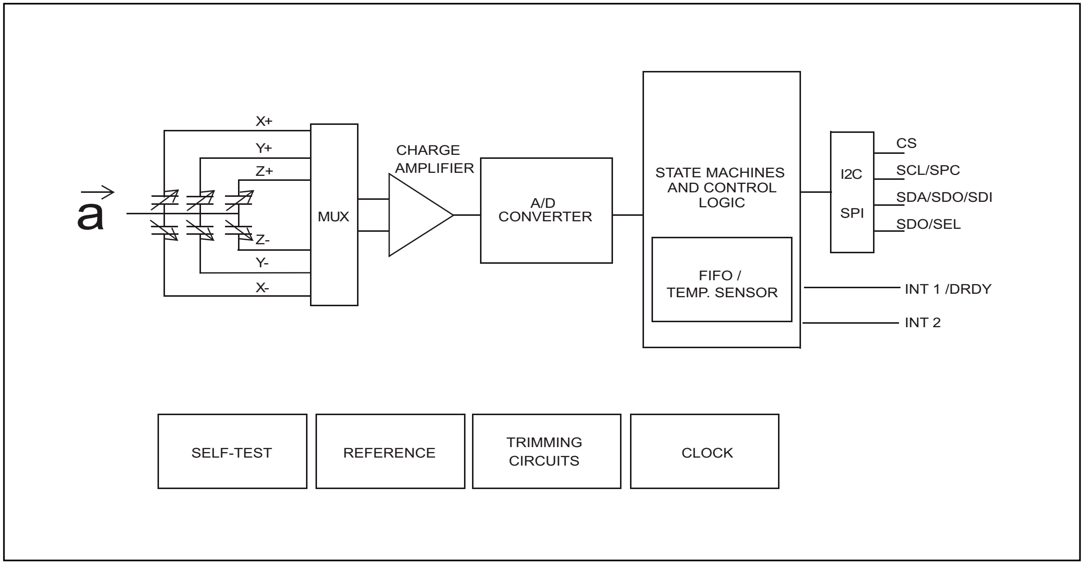
1 Block diagram and pin description

1.1 Block diagram

Figure 1. Block diagram



1.2 Pin description

Figure 2. Pin connections

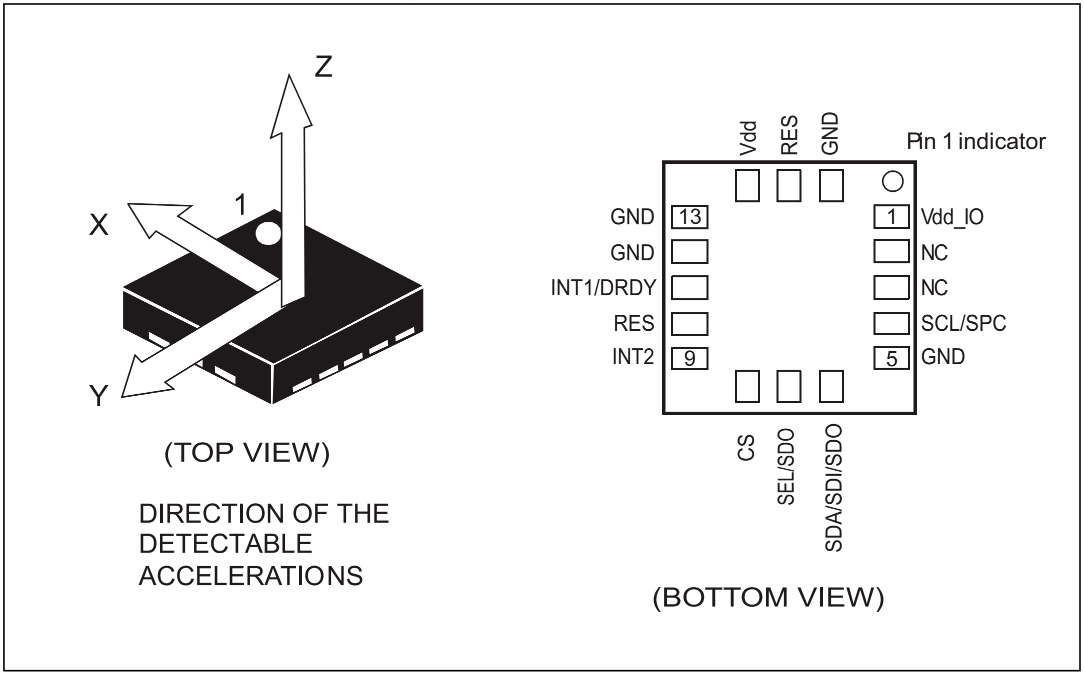


Table 2. Pin description

Pin#	Name	Function
1	Vdd_IO	Power supply for I/O pins
2	NC	Not connected
3	NC	Not connected
4	SCL SPC	I^2C serial clock (SCL) SPI serial port clock (SPC)
5	GND	0 V supply
6	SDA SDI SDO	I^2C serial data (SDA) SPI serial data input (SDI) 3-wire interface serial data output (SDO)
7	SEL SDO	I^2C address selection SPI serial data output (SDO)
8	CS	SPI enable I^2C/SPI mode selection (1: SPI idle mode / I^2C communication enabled; 0: SPI communication mode / I^2C disabled)
9	INT 2	Interrupt 2
10	Reserved	Connect to GND
11	INT 1/DRDY	Interrupt 1/ DRDY
12	GND	0 V supply
13	GND	0 V supply
14	Vdd	Power supply
15	Reserved	Connect to Vdd, connect to GND, or leave unconnected
16	GND	0 V supply

2 Mechanical and electrical specifications

2.1 Mechanical characteristics

@ Vdd = 2.5 V, T = 25 °C unless otherwise noted(a).

Table 3. Mechanical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.(1)	Max.	Unit
FS	Measurement range(2)	FS bit set to 000		±2.0		*g*
		FS bit set to 001		±4.0		
		FS bit set to 010		±6.0		
		FS bit set to 011		±8.0		
		FS bit set to 100		±16.0		
So	Sensitivity	FS bit set to 000		0.06		m*g*/digit
		FS bit set to 001		0.12		
		FS bit set to 010		0.18		
		FS bit set to 011		0.24		
		FS bit set to 100		0.73		
TCSo	Sensitivity change vs. temperature	FS bit set to 00		0.01		%/°C
TyOff	Typical zero-*g* level offset accuracy(3)	FS bit set to 00		±40		m*g*
TCOff	Zero-*g* level change vs. temperature	Max. delta from 25 °C		±0.5		m*g*/°C
An	Acceleration noise density	FS bit set to 00, normal mode, ODR = 100 Hz		150		μ*g*/ sqrt(Hz)
ST	Self test positive difference(4)	± 2 *g* range, X, Y-axis ST2,ST1 = [01] see *Figure 23*		140		m*g*
		± 2 *g* range, Z-axis ST2,ST1 = [01] see *Figure 23*		590		
Top	Operating temperature range		-40		+85	°C

1. Typical specifications are not guaranteed.
2. Verified by wafer level test and measurement of initial offset and sensitivity.
3. Typical zero-*g* level offset value after MSL3 preconditioning.
4. Self-test output change” is defined as: OUTPUT[m*g*]$_{\text{(CNTL5 ST2, ST1 bits=01)}}$ - OUTPUT[m*g*]$_{\text{(CNTL5 ST2, ST1 bits=00)}}$

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a. The product is factory calibrated at 2.5 V. The operational power supply range is from 1.71 V to 3.6 V.

2.2 Electrical characteristics

@ Vdd = 2.5 V, T = 25 °C unless otherwise noted[b].

Table 4. Electrical characteristics (1)

Symbol	Parameter	Test conditions	Min.	Typ.(2)	Max.	Unit
Vdd	Supply voltage		1.71	2.5	3.6	V
Vdd_IO	I/O pins supply voltage(3)		1.71		Vdd+0.1	V
IddA	Current consumption in active mode	1.6 kHz ODR		225		µA
		3.125 Hz ODR		11		µA
IddPdn	Current consumption in power-down/standby mode			2		µA
VIH	Digital high-level input voltage		0.8*Vdd_IO			V
VIL	Digital low-level input voltage				0.2*Vdd_IO	V
VOH	High-level output voltage		0.9*Vdd_IO			V
VOL	Low-level output voltage				0.1*Vdd_IO	V
Top	Operating temperature range		-40		+85	°C

1. The product is factory calibrated at 2.5 V. The operational power supply range is from 1.71 V to 3.6 V.
2. Typical specifications are not guaranteed.
3. It is possible to remove Vdd while maintaining Vdd_IO without blocking the communication busses, in this condition the measurement chain is powered off.

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[b] The product is factory calibrated at 2.5 V. The operational power supply range is from 1.71 V to 3.6 V.

2.3 Communication interface characteristics

2.3.1 SPI - serial peripheral interface

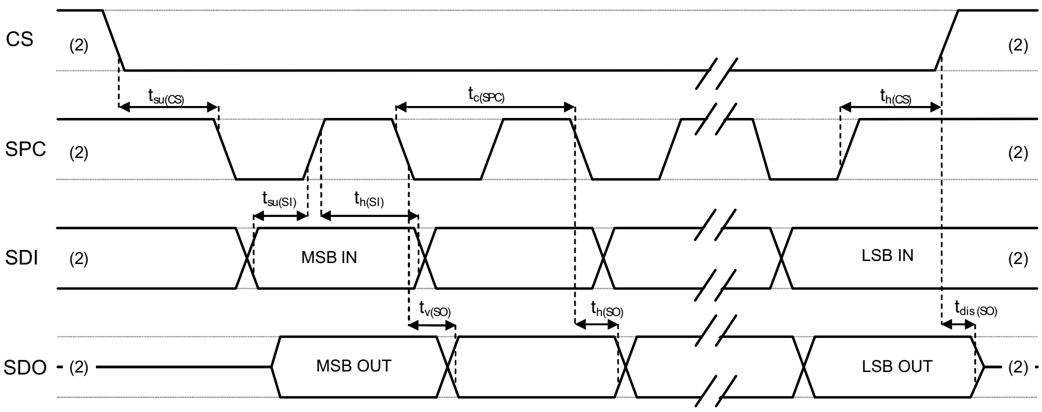
Subject to general operating conditions for Vdd and Top.

Table 5. SPI slave timing values

		Value [1]		Unit
Symbol	**Parameter**	**Min.**	**Max.**	
$t_{c(SPC)}$	SPI clock cycle	100		ns
$f_{c(SPC)}$	SPI clock frequency		10	MHz
$t_{su(CS)}$	CS setup time	6		ns
$t_{h(CS)}$	CS hold time	8		
$t_{su(SI)}$	SDI input setup time	5		
$t_{h(SI)}$	SDI input hold time	15		
$t_{v(SO)}$	SDO valid output time		50	
$t_{h(SO)}$	SDO output hold time	9		
$t_{dis(SO)}$	SDO output disable time		50	

1. Values are guaranteed at 10 MHz clock frequency for SPI with both 4 and 3 wires, based on characterization results, not tested in production.

Figure 3. SPI slave timing diagram



2. When no ongoing communication, data on SDO is driven by internal pull-up resistor.

Note: Measurement points are done at 0.2·Vdd_IO and 0.8·Vdd_IO, for both input and output ports.

2.3.2 I^2C - inter-IC control interface

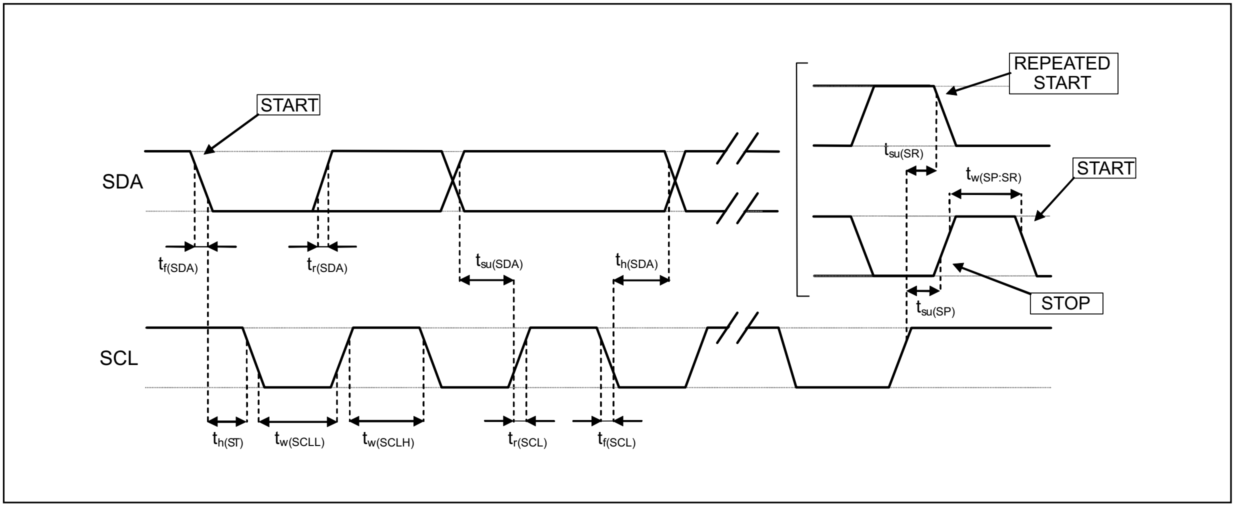
Subject to general operating conditions for Vdd and Top.

Table 6. I^2C slave timing values

		I^2C		I^2C fast		
Symbol	**Parameter**	**Min.**	**Max.**	**Min.**	**Max.**	**Unit**
$f_{(SCL)}$	SCL clock frequency	0	100	0	400	kHz
$t_{w(SCLL)}$	SCL clock low time	4.7		1.3		µs
$t_{w(SCLH)}$	SCL clock high time	4.0		0.6		
$t_{su(SDA)}$	SDA setup time	250		100		ns
$t_{h(SDA)}$	SDA data hold time	0.01	3.45	0.01	0.9	µs
$t_{r(SDA)}$ $t_{r(SCL)}$	SDA and SCL rise time		1000	$20 + 0.1C_b$ (2)	300	ns
$t_{f(SDA)}$ $t_{f(SCL)}$	SDA and SCL fall time		300	$20 + 0.1C_b$ (2)	300	
$t_{h(ST)}$	START condition hold time	4		0.6		µs
$t_{su(SR)}$	Repeated START condition setup time	4.7		0.6		
$t_{su(SP)}$	STOP condition setup time	4		0.6		
$t_{w(SP:SR)}$	Bus free time between STOP and START condition	4.7		1.3		

1. Data based on standard I^2C protocol requirement, not tested in production.
2. C_b = total capacitance of one bus line, in pF.

Figure 4. I^2C slave timing diagram



Note: Measurement points are done at 0.2·Vdd_IO and 0.8·Vdd_IO, for both ports.

2.4 Absolute maximum ratings

Stresses above those listed as “absolute maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 7. Absolute maximum ratings

Symbol	Ratings	Maximum value	Unit
Vdd	Supply voltage	-0.3 to 4.8	V
Vdd_IO	I/O pins supply voltage	-0.3 to 4.8	V
Vin	Input voltage on any control pin (CS, SCL/SPC, SDA/SDI/SDO, SDO/SEL)	-0.3 to Vdd_IO +0.3	V
A_{POW}	Acceleration (any axis, powered, Vdd = 2.5 V)	3000 for 0.5 ms	*g*
		10000 for 0.1 ms	*g*
A_{UNP}	Acceleration (any axis, unpowered)	3000 for 0.5 ms	*g*
		10000 for 0.1 ms	*g*
T_{OP}	Operating temperature range	-40 to +85	°C
T_{STG}	Storage temperature range	-40 to +125	°C
ESD	Electrostatic discharge protection	2 (HBM)	kV

Note: Supply voltage on any pin should never exceed 4.8 V

This device is sensitive to mechanical shock, improper handling can cause permanent damage to the part.

This device is sensitive to electrostatic discharge (ESD), improper handling can cause permanent damage to the part.

2.5 Terminology

2.5.1 Sensitivity

Sensitivity describes the gain of the sensor and can be determined, for example, by applying 1 *g* acceleration to it. As the sensor can measure DC accelerations this can be done easily by pointing the axis of interest towards the center of the Earth, noting the output value, rotating the sensor by 180 degrees (pointing to the sky) and noting the output value again. By doing so, ±1 *g* acceleration is applied to the sensor. Subtracting the larger output value from the smaller one, and dividing the result by 2, leads to the actual sensitivity of the sensor. This value changes very little over temperature and also time. The sensitivity tolerance describes the range of sensitivities of a large population of sensors.

2.5.2 Zero-*g* level

Zero-*g* level offset (TyOff) describes the deviation of an actual output signal from the ideal output signal if no acceleration is present. A sensor in a steady-state on a horizontal surface measures 0 *g* for the X-axis and 0 *g* for the Y-axis, whereas the Z-axis measures 1 *g*. The output is ideally in the middle of the dynamic range of the sensor (content of OUT registers 00h, data expressed as 2’s complement number). A deviation from the ideal value in this case is called Zero-*g* offset. Offset is to some extent a result of stress to MEMS sensor and therefore the offset can slightly change after mounting the sensor on a printed circuit board or exposing it to extensive mechanical stress. Offset changes little over temperature, see “Zero-*g* level change vs. temperature”. The Zero-*g* level tolerance (TyOff) describes the standard deviation of the range of Zero-*g* levels of a population of sensors.

2.6 Functionality

2.6.1 Self-test

The self-test allows checking the sensor functionality without moving it. The self-test function is off when the self-test bit (ST) is programmed to ‘0‘. When the self-test bit is programmed to ‘1’, an actuation force is applied to the sensor, simulating a definite input acceleration. In this case the sensor outputs exhibit a change in their DC levels which are related to the selected full scale through the device sensitivity. When the self-test is activated, the device output level is given by the algebraic sum of the signals produced by the acceleration acting on the sensor and by the electrostatic test-force. If the output signals change within the amplitude specified in *Table 3*, then the sensor is working properly and the parameters of the chip interface are within the defined specifications.

2.7 Sensing element

A proprietary process is used to create a surface micromachined accelerometer. The technology allows processing suspended silicon structures which are attached to the substrate in a few points called anchors and are free to move in the direction of the sensed acceleration. In order to be compatible with traditional packaging techniques, a cap is placed on top of the sensing element to avoid blocking the moving parts during the molding phase of the plastic encapsulation.

When an acceleration is applied to the sensor, the proof mass displaces from its nominal position, causing an imbalance in the capacitive half bridge. This imbalance is measured using charge integration in response to a voltage pulse applied to the capacitor.

At steady-state the nominal value of the capacitors are a few pF and when an acceleration is applied, the maximum variation of the capacitive load is in the fF range.

2.8 IC interface

The complete measurement chain is made up of a low-noise capacitive amplifier which converts the capacitive unbalancing of the MEMS sensor into an analog voltage that is available to the user through an analog-to-digital converter.

The acceleration data may be accessed through an I^2C/SPI interface, therefore making the device particularly suitable for direct interfacing with a microcontroller.

The LIS3DSH features a Data-Ready signal (DRDY) which indicates when a new set of measured acceleration data is available, therefore simplifying data synchronization in the digital system that uses the device.

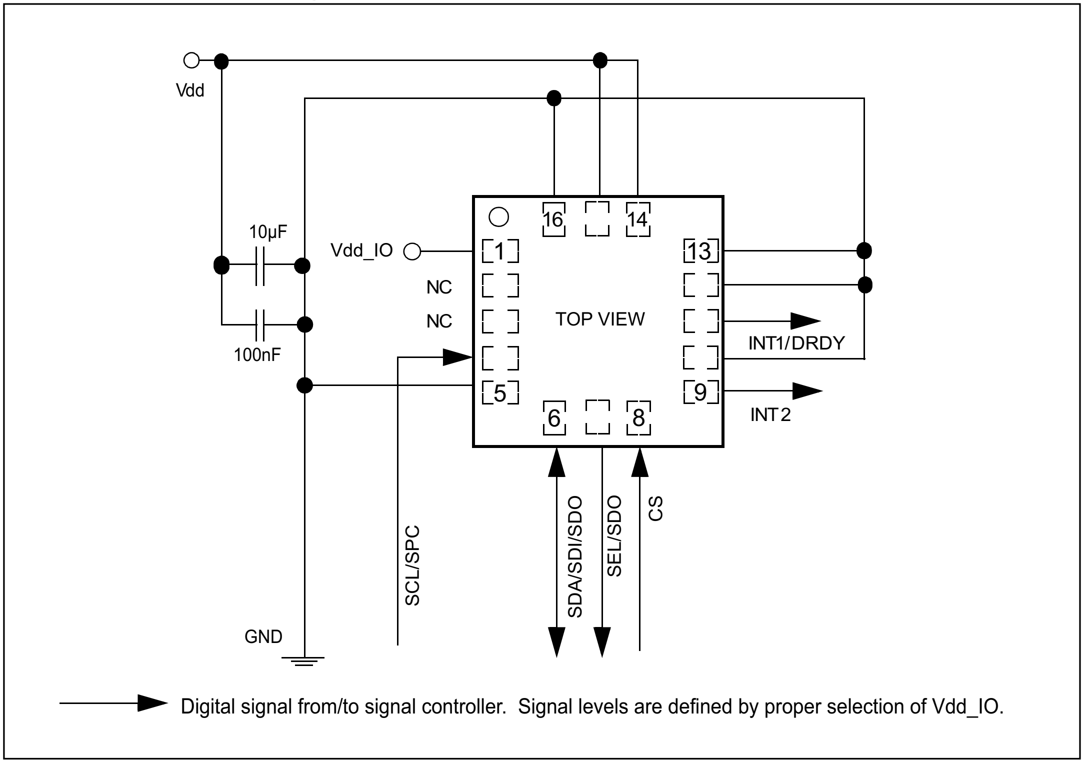
2.9 Factory calibration

The IC interface is factory calibrated for sensitivity (So) and Zero-*g* level (TyOff).

The trimming values are stored inside the device in nonvolatile memory. Any time the device is turned on, the trimming parameters are downloaded into the registers to be used during the active operation. This allows using the device without further calibration.

3 Application hints

Figure 5. LIS3DSH electrical connections



Note: Pin 15 can be connected to Vdd or GND or left unconnected.

The device core is supplied through the Vdd line while the I/O pins are supplied through the Vdd_IO line. Power supply decoupling capacitors (100 nF ceramic, 10 µF) should be placed as near as possible to pin 14 of the device (common design practice).

All the voltage and ground supplies must be present at the same time to have proper behavior of the IC (refer to *Figure 5*). It is possible to remove Vdd while maintaining Vdd_IO without blocking the communication bus, in this condition the measurement chain is powered off.

The functionality of the device and the measured acceleration data are selectable and accessible through the I^2C or SPI interfaces. When using the I^2C, CS must be tied high.

3.1 Soldering information

The LGA package is compliant with the ECOPACK®, RoHS and “Green” standard.
It is qualified for soldering heat resistance according to JEDEC J-STD-020.

Leave “Pin 1 Indicator” unconnected during soldering.

Land pattern and soldering recommendations are available at www.st.com.

4 Digital main blocks

4.1 State machine

The LIS3DSH embeds two state machines able to run a user-defined program.

The program is made up of a set of instructions that define the transition to successive states. Conditional branches are possible.

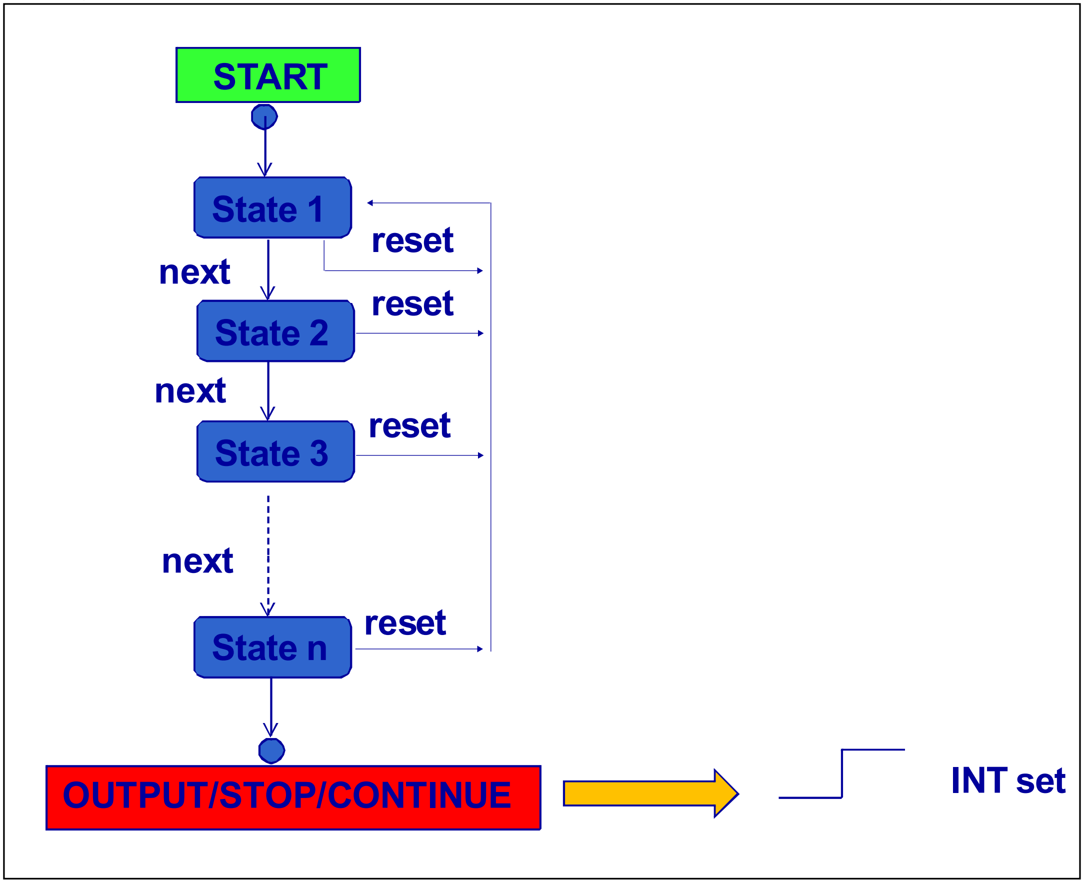
From each state (n) it is possible to have a transition to the next state (n+1) or to a reset state. The transition to the reset point happens when “RESET condition” is true; The transition to the next step happens when “NEXT condition” is true.

An interrupt is triggered when the output/stop/continue state is reached.

Each state machine allows implementing gesture recognition in a flexible way, free-fall, wake-up, 4D/6D orientation, pulse counter and step recognition, click/double-click, shake/double-shake, face-up/face-down, turn/double-turn:

- Code and parameters are loaded by the host into dedicated memory areas for the state program
- State program with timing based on ODR or decimated time
- Possibility of conditional branches

Figure 6. LIS3DSH state machines: sequence of state to execute an algorithm



4.2 FIFO

The LIS3DSH embeds an acceleration data FIFO for each of the three output channels, X, Y, and Z. This allows consistent power saving for the system since the host processor does not need to continuously poll data from the sensor, but it can wake up only when needed and burst the significant data out from the FIFO. This buffer can work according to four different modes: Bypass mode, FIFO mode, Stream mode and Stream-to-FIFO mode. Each mode is selected by the FIFO_MODE bits. Programmable watermark level, FIFO_empty or FIFO_Full events can be enabled to generate dedicated interrupts on the INT1/2 pins.

4.2.1 Bypass mode

In Bypass mode, the FIFO is not operational and for this reason it remains empty. For each channel only the first address is used. The remaining FIFO slots are empty.

4.2.2 FIFO mode

In FIFO mode, data from the X, Y, and Z channels are stored in the FIFO. A watermark interrupt can be enabled in order to be raised when the FIFO is filled to the level specified by the internal register. The FIFO continues filling until it is full. When full, the FIFO stops collecting data from the input channels.

4.2.3 Stream mode

In Stream mode, data from the X, Y, and Z measurements are stored in the FIFO. A watermark interrupt can be enabled and set as in the FIFO mode. The FIFO continues filling until it’s full. When full, the FIFO discards the older data as the new arrive.

4.2.4 Stream-to-FIFO mode

In Stream-to-FIFO mode, data from the X, Y, and Z measurements are stored in the FIFO. A watermark interrupt can be enabled in order to be raised when the FIFO is filled to the level specified by the internal register. The FIFO continues filling until it’s full. When full, the FIFO discards the older data as the new arrive. Once a trigger event occurs, the FIFO starts operating in FIFO mode.

4.2.5 Retrieving data from FIFO

FIFO data is read from the OUT_X, OUT_Y and OUT_Z registers. When the FIFO is in Stream, Bypass or FIFO mode, a read operation to the OUT_X, OUT_Y or OUT_Z registers provides the data stored in the FIFO. Each time data is read from the FIFO, the oldest X, Y, and Z data are placed in the OUT_X, OUT_Y and OUT_Z registers and both single-read and read-burst operations can be used.

5 Digital interfaces

The registers embedded inside the LIS3DSH may be accessed through both the I^2C and SPI serial interfaces. The latter may be SW configured to operate either in 3-wire or 4-wire interface mode.

The serial interfaces are mapped to the same pins. To select/exploit the I^2C interface, the CS line must be tied high (i.e. connected to Vdd_IO).

Table 8. Serial interface pin description

Pin name	Pin description
CS	SPI enable I^2C/SPI mode selection (1: SPI idle mode / I^2C communication enabled; 0: SPI communication mode / I^2C disabled)
SCL SPC	I^2C serial clock (SCL) SPI serial port clock (SPC)
SDA SDI SDO	I^2C serial data (SDA) SPI serial data input (SDI) 3-wire interface serial data output (SDO)
SEL SDO	I^2C address selection SPI serial data output (SDO)

5.1 I^2C serial interface

The LIS3DSH I^2C is a bus slave. The I^2C is employed to write data into registers whose content can also be read back.

The relevant I^2C terminology is given in the table below.

Table 9. I^2C terminology

Term	Description
Transmitter	The device which sends data to the bus
Receiver	The device which receives data from the bus
Master	The device which initiates a transfer, generates clock signals and terminates a transfer
Slave	The device addressed by the master

There are two signals associated with the I^2C bus: the serial clock line (SCL) and the serial data line (SDA). The latter is a bidirectional line used for sending and receiving the data to/from the interface. Both lines must be connected to Vdd_IO through an external pull-up resistor. When the bus is free, both lines are high.

The I^2C interface is compliant with fast mode (400 kHz) I^2C standards as well as with normal mode.

5.1.1 I^2C operation

The transaction on the bus is started through a start (ST) signal. A start condition is defined as a HIGH to LOW transition on the data line while the SCL line is held HIGH. After this has been transmitted by the master, the bus is considered busy. The next byte of data transmitted after the start condition contains the address of the slave in the first 7 bits and the eighth bit tells whether the master is receiving data from the slave or transmitting data to the slave. When an address is sent, each device in the system compares the first seven bits after a start condition with its address. If they match, the device considers itself addressed by the master.

The slave address (SAD) associated to the LIS3DSH is 00111xxb where the xx bits are modified by the SEL/SDO pin in order to modify the device address. If the SEL pin is connected to the voltage supply, the address is 0011101b, otherwise the address is 0011110b if the SEL pin is connected to ground. This solution allows connecting and addressing two different accelerometers to the same I^2C lines.

Data transfer with acknowledge is mandatory. The transmitter must release the SDA line during the acknowledge pulse. The receiver must then pull the data line LOW so that it remains stable low during the HIGH period of the acknowledge clock pulse. A receiver which has been addressed is obliged to generate an acknowledge after each byte of data received.

The I^2C embedded inside the LIS3DSH behaves as a slave device and the following protocol must be adhered to. After the start condition (ST) a slave address is sent, once a slave acknowledge (SAK) has been returned, an 8-bit sub-address (SUB) is transmitted: the 7 LSb represents the actual register address while the ADD_INC bit (CTRL_REG6) defines the address increment.

The slave address is completed with a read/write bit. If the bit is ‘1’ (Read), a repeated start (SR) condition must be issued after the two sub-address bytes; if the bit is ‘0’ (Write), the master transmits to the slave with direction unchanged. *Table 10* explains how the SAD+Read/Write bit pattern is composed, listing all the possible configurations.

Table 10. SAD+Read/Write patterns

Command	SAD[6:2]	SAD[1] = $\overline{\text{SEL}}$	SAD[0] = SEL	R/W	SAD+R/W
Read	00111	1	0	1	00111101
Write	00111	1	0	0	00111100
Read	00111	0	1	1	00111011
Write	00111	0	1	0	00111010

Table 11. Transfer when master is writing one byte to slave

Master	ST	SAD + W		SUB		DATA		SP
Slave			SAK		SAK		SAK	

Table 12. Transfer when master is writing multiple bytes to slave

Master	ST	SAD + W		SUB		DATA		DATA		SP
Slave			SAK		SAK		SAK		SAK	

Table 13. Transfer when master is receiving (reading) one byte of data from slave

Master	ST	SAD + W		SUB		SR	SAD + R			NMAK	SP
Slave			SAK		SAK			SAK	DATA		

Table 14. Transfer when master is receiving (reading) multiple bytes of data from slave

Master	ST	SAD+W		SUB		SR	SAD+R			MAK		MAK		NMAK	SP
Slave			SAK		SAK			SAK	DATA		DATA		DATA		

Data are transmitted in byte format (DATA). Each data transfer contains 8 bits. The number of bytes transferred per transfer is unlimited. Data is transferred with the Most Significant bit (MSb) first. If a receiver can't receive another complete byte of data until it has performed some other function, it can hold the clock line, SCL LOW, to force the transmitter into a wait state. Data transfer only continues when the receiver is ready for another byte and releases the data line. If a slave receiver doesn't acknowledge the slave address (i.e. it is not able to receive because it is performing some real-time function) the data line must be left HIGH by the slave. The master can then abort the transfer. A LOW to HIGH transition on the SDA line while the SCL line is HIGH is defined as a STOP condition. Each data transfer must be terminated by the generation of a STOP (SP) condition.

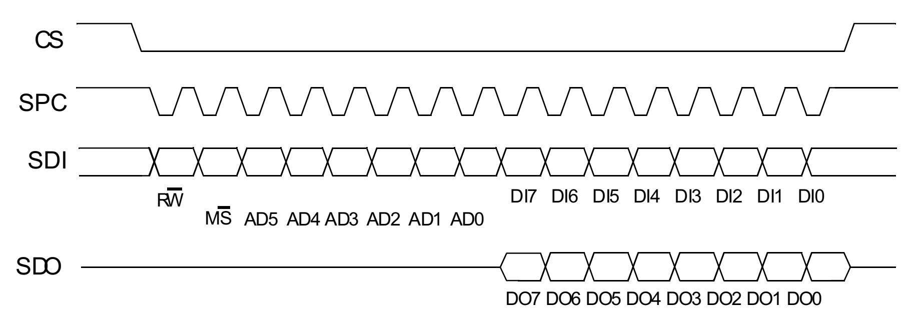
In the communication format presented, MAK is Master acknowledge and NMAK is No Master Acknowledge.

5.2 SPI bus interface

The LIS3DSH SPI is a bus slave. The SPI allows writing to and reading from the registers of the device.

The serial interface interacts with the outside world with 4 wires: CS, SPC, SDI and SDO.

Figure 7. Read and write protocol



CS is the serial port enable and it is controlled by the SPI master. It goes low at the start of the transmission and goes back high at the end. SPC is the serial port clock and it is controlled by the SPI master. It is stopped high when CS is high (no transmission). SDI and SDO are respectively the serial port data input and output. Those lines are driven at the falling edge of SPC and should be captured at the rising edge of SPC.

Both the read register and write register commands are completed in 16 clock pulses or in multiples of 8 in case of multiple read/write bytes. Bit duration is the time between two falling edges of SPC. The first bit (bit 0) starts at the first falling edge of SPC after the falling edge of CS while the last bit (bit 15, bit 23, ...) starts at the last falling edge of SPC just before the rising edge of CS.

bit 0: $R\overline{W}$ bit. When 0, the data DI(7:0) is written into the device. When 1, the data DO(7:0) from the device is read. In the latter case, the chip drives **SDO** at the start of bit 8.

bit 1-7: address AD(6:0). This is the address field of the indexed register.

bit 8-15: data DI(7:0) (write mode). This is the data that is written into the device (MSb first).

bit 8-15: data DO(7:0) (read mode). This is the data that is read from the device (MSb first).

In multiple read/write commands further blocks of 8 clock periods are added. When the ADD_INC *CTRL_REG6 (25h)* bit is ‘0’, the address used to read/write data remains the same for every block. When the ADD_INC bit is ‘1’, the address used to read/write data is increased at every block.

The function and the behavior of **SDI** and **SDO** remain unchanged.