Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

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We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

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Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
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LN60A01

600V, Triple N-Channel MOSFET with Common Gate Control

The Future of Analog IC Technology

DESCRIPTION

The LN60A01 is a three channel, 600V N-Channel, enhancement mode power FET manufactured in MPS's proprietary, high-voltage DMOS technology.

This advanced technology has been especially tailored to minimize the on-state resistance, provide superior switching performance, and withstand high energy pulses in the avalanche and commutation modes. This device is well suited for high efficiency switched mode power supplies and active power factor correction.

The LN60A01 is available in PDIP8 and SOIC8 package.

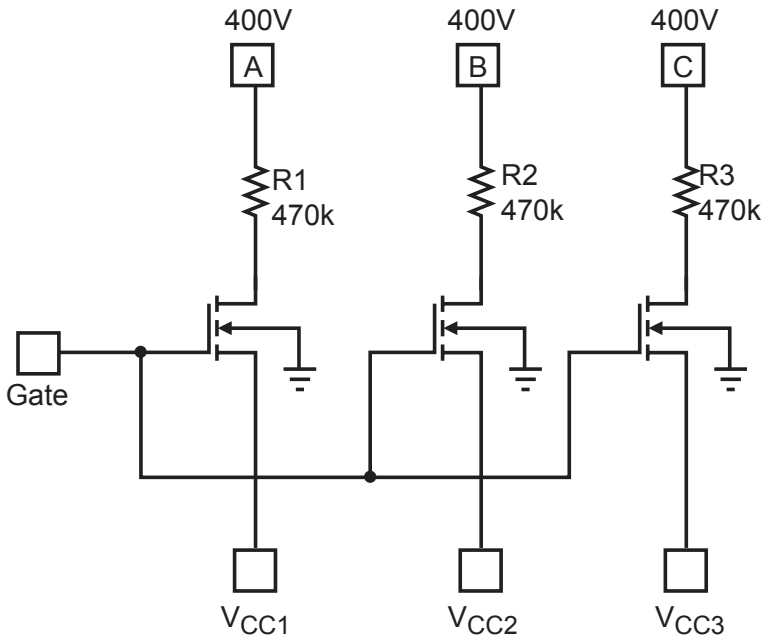
FEATURES

- 600V Breakdown Voltage
- Three N-Channel MOSFETs
- One Gate control to All Three FETs
- Rds(on)=200Ω at Vgs=10V
- Switching Current>0.1A
- Fast Switching

APPLICATIONS

- High Efficiency AC/DC Adaptor
- Offline Switching Power Supply
- Active Power Factor Correction

TYPICAL APPLICATION



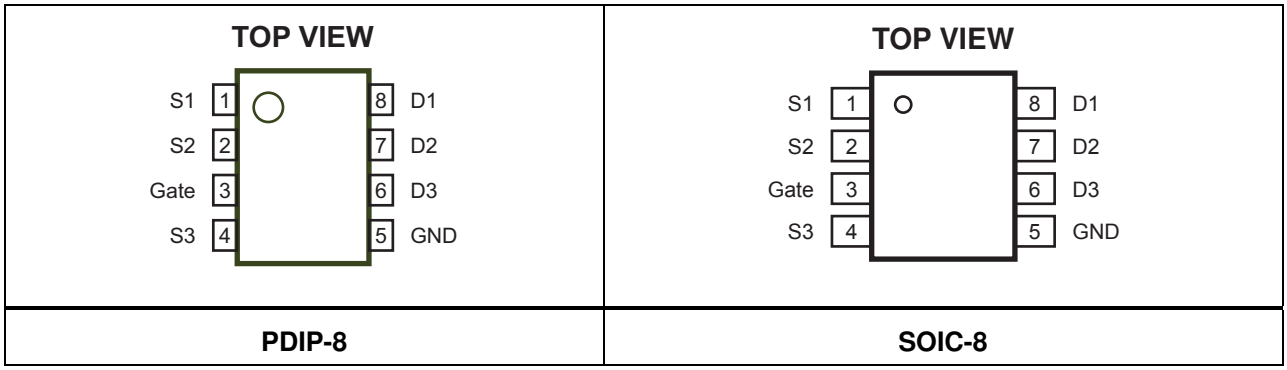
ORDERING INFORMATION

Part Number*	Package	Top Marking	Free Air Temperature (T_A)
LN60A01EP	PDIP-8	LN60A01E	-20ºC to 85ºC
Part Number**	**Package**	**Top Marking**	**Free Air Temperature (T_A)**
LN60A01ES	SOIC-8	LN60A01E	-20ºC to 85ºC

*For RoHS compliant packaging, add suffix –LF (e.g. LN60A01EP–LF)

** For Tape & Reel, add suffix –Z (e.g. LN60A01ES–Z).
For RoHS compliant packaging, add suffix –LF (e.g. LN60A01ES–LF–Z)

PACKAGE REFERENCE



PDIP-8	SOIC-8

ABSOLUTE MAXIMUM RATINGS (1)

Drain-Source Voltage V_{DS} 600V
Gate-Source Voltage V_{GS}.....15V
Continuous Drain Current (1) I_D 0.08A
Pulsed Drain Current (2) I_{DM} 0.4A
Power Dissipation (1) (2) P_D 1.3W
Storage Temperature..... –55°C to +150°C

Recommended Operating Conditions

Operating Junct. Temp (T_J)..... –20°C to +125°C

Thermal Resistance (3)

	θ_{JA}	θ_{JC}
SOIC8	90 ... 45...	°C/W
PDIP8	105... . 45. .	°C/W

Notes:
1) Surface Mounted on 1”×1” FR4 Board..
2) Pulse width limited by maximum junction temperature.
3) Measured on JESD51-7, 4-layer PCB

ELECTRICAL CHARACTERISTICS

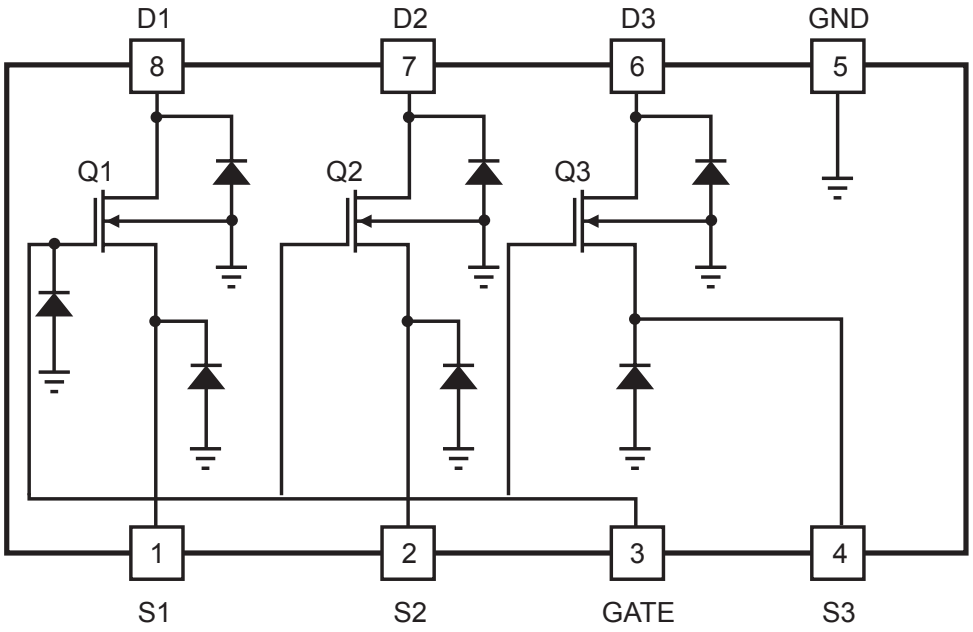
T_A = +25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS}=0V, I_D=30uA		600		V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=250uA	0.8	1.0	1.2	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=400V, V_{GS}=0V		15		μA
Drain-Source On-Resistance	$r_{DS(on)}$	V_{GS}=10V, I_D=10mA		190		Ω
		V_{GS}=5V, I_D=10mA		200		
Switching Parameter						
Turn-On Delay Time	$t_{(on)}$	V_{DS}=350V, I_{DS}=10mA		50		ns
Turn-Off Delay Time	$t_{(off)}$			3000		

PIN FUNCTIONS

Pin Number	Pin Name	Description
1	S1	Source 1
2	S2	Source 2
3	Gate	Gate
4	S3	Source 3
5	GND	Ground
6	D3	Drain 3
7	D2	Drain 2
8	D1	Drain 1

DEVICE CIRCUIT

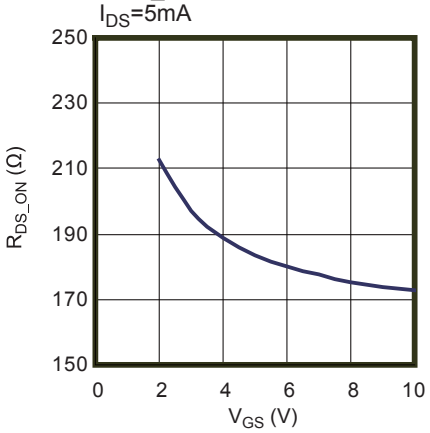


TYPICAL PERFORMANCE CHARACTERISTICS

T_A =25° C, unless otherwise noted.

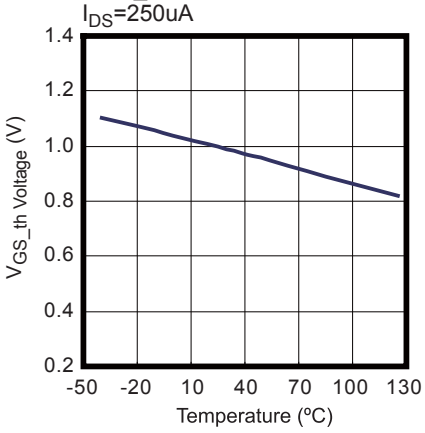
R_{DS_ON} vs. V_{GS}

I_{DS}=5mA



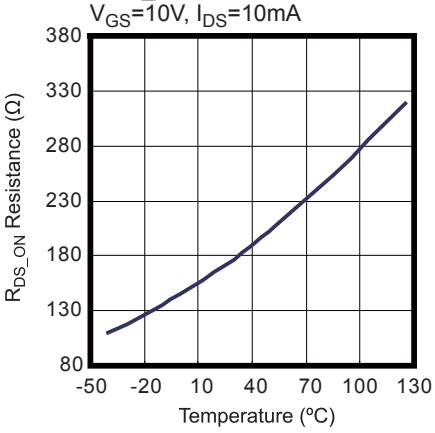
V_{GS_th} vs. Temperature

I_{DS}=250uA



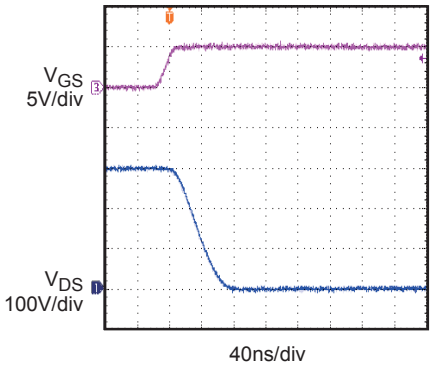
R_{DS_ON} vs. Temperature

V_{GS}=10V, I_{DS}=10mA



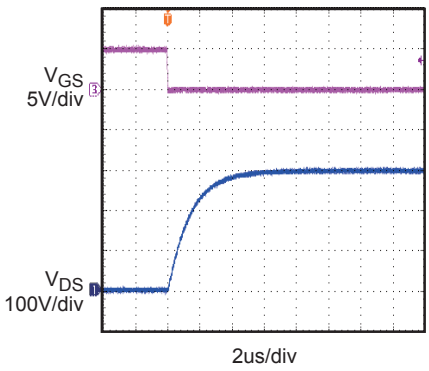
Switching ON

V_{DS}=300V, I_{DS}=4mA, V_{GS}=5V



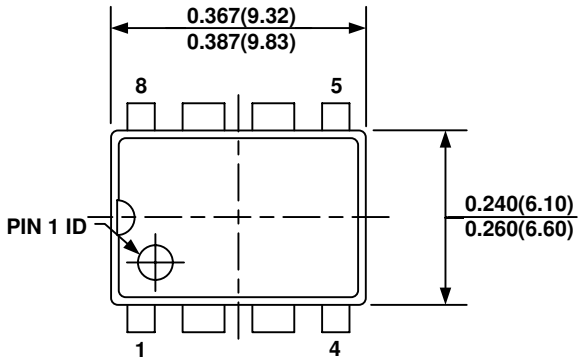
Switching OFF

V_{DS}=300V, I_{DS}=4mA, V_{GS}=5V

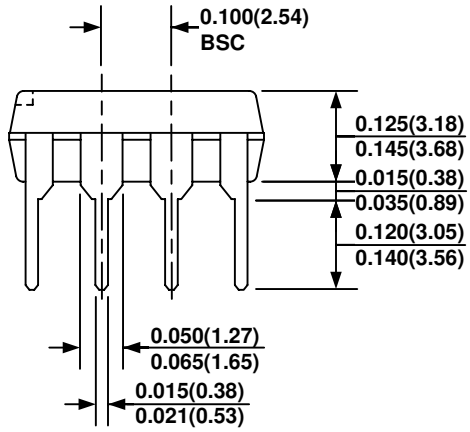


PACKAGE INFORMATION

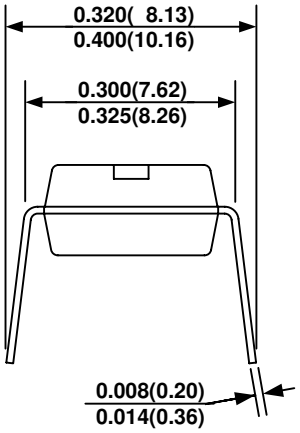
PDIP-8



TOP VIEW



FRONT VIEW



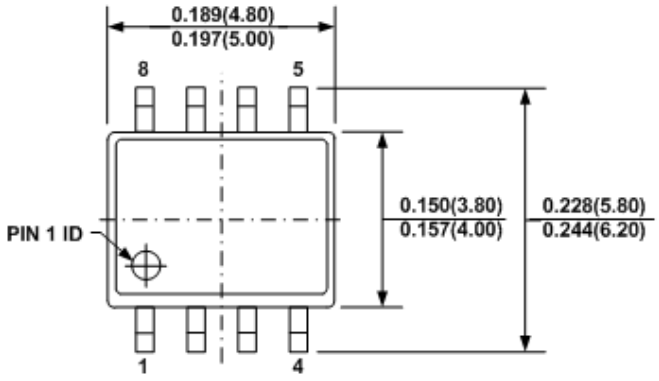
SIDE VIEW

NOTE:

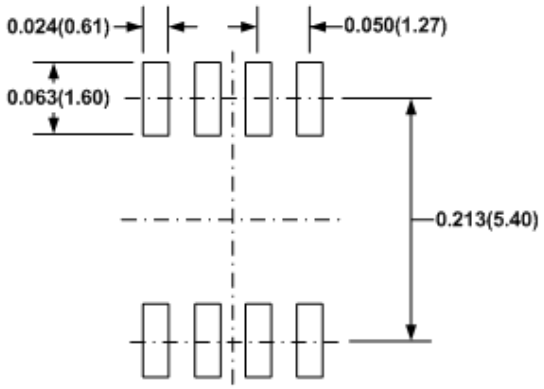
1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
2) PACKAGE LENGTH AND WIDTH DO NOT INCLUDE MOLD FLASH, OR PROTRUSIONS.
3) DRAWING CONFORMS TO JEDEC MS-001, VARIATION BA.
4) DRAWING IS NOT TO SCALE.

PACKAGE INFORMATION

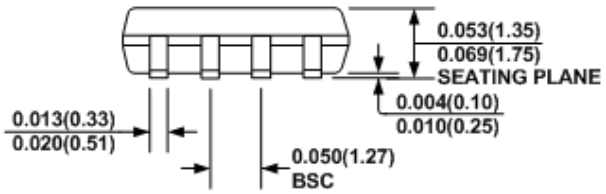
SOIC8



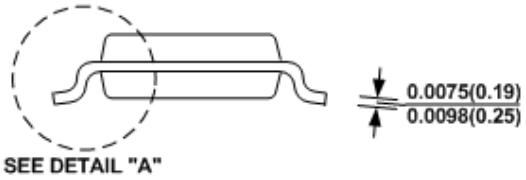
TOP VIEW



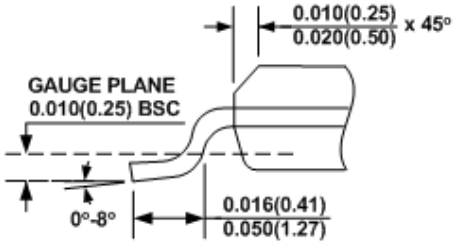
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW



DETAIL "A"

NOTE:

1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
5) DRAWING CONFORMS TO JEDEC MS-012, VARIATION AA.
6) DRAWING IS NOT TO SCALE.