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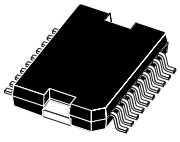
LNBS21

LNB SUPPLY AND CONTROL IC WITH STEP-UP CONVERTER AND I²C INTERFACE

- COMPLETE INTERFACE BETWEEN LNB AND I²C™ BUS
- BUILT-IN DC/DC CONTROLLER FOR SINGLE 12V SUPPLY OPERATION
- ACCURATE BUILT-IN 22KHz TONE OSCILLATOR
- SUITS WIDELY ACCEPTED STANDARDS
- FAST OSCILLATOR START-UP FACILITATES DiSEqC™ ENCODING
- BUILT-IN 22KHz TONE DETECTOR SUPPORTS BI-DIRECTIONAL DiSEqC™
- LOOP-THROUGH FUNCTION FOR SLAVE OPERATION
- LNB SHORT CIRCUIT PROTECTION AND DIAGNOSTIC
- CABLE LENGTH DIGITAL COMPENSATION
- INTERNAL OVER TEMPERATURE PROTECTION



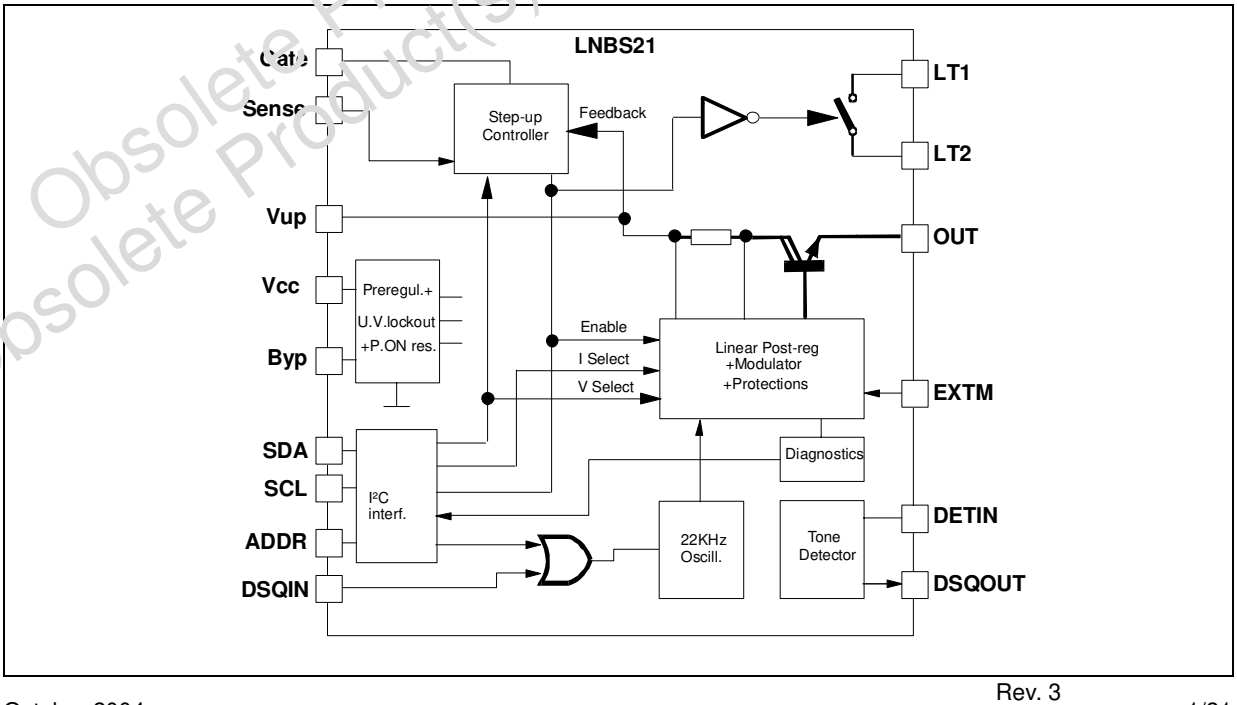
PowerSO-20

DESCRIPTION

Intended for analog and digital satellite STB receivers/SatTV, sets/PC cards, the LNBS21 is a monolithic voltage regulator and interface IC, assembled in PowerSO-20, specifically designed to provide the power and the 13/18V, 22KHz tone signalling to the LNB downconverter in the antenna or to the multiswitch box. In this application field, it offers a complete solution with extremely low component count, low power dissipation together with simple design and I²C™ standard interfacing.

This IC has a built in DC/DC step-up controller that, from a single supply source ranging from 8 to 15V, generates the voltages that let the linear

Figure 1: Schematic Diagram



post-regulator to work at a minimum dissipated power. An UnderVoltage Lockout circuit will disable the whole circuit when the supplied V_{CC} drops below a fixed threshold (6.7V typically). The internal 22KHz tone generator is factory trimmed in accordance to the standards, and can be controlled either by the I^2C^{TM} interface or by a dedicated pin (DSQIN) that allows immediate DiSEqC™ data encoding (*). All the functions of this IC are controlled via I^2C^{TM} bus by writing 6 bits on the System Register (SR, 8 bits). The same register can be read back, and two bits will report the diagnostic status. When the IC is put in Stand-by (EN bit LOW), the power blocks are disabled and the loop-through switch between LT1 and LT2 pins is closed, thus leaving all LNB powering and control functions to the Master Receiver (**). When the regulator blocks are active (EN bit HIGH), the output can be logic controlled to be 13 or 18 V (typ.) by mean of the VSEL bit (Voltage SELect) for remote controlling of non-DiSEqC LNBs. Additionally, it is possible to increment by 1V (typ.) the selected voltage value to compensate for the excess voltage drop along the coaxial cable (LLC bit HIGH). In order to minimize the power dissipation, the output voltage of the internal step-up converter is adjusted to allow the linear regulator to work at minimum dropout. Another bit of the SR is addressed to the remote control of non-DiSEqC LNBs: the TEN (Tone ENable) bit. When it is set to HIGH, a continuous 22KHz tone is generated regardless of the DSQIN pin logic status. The TEN bit must be set LOW when the DSQIN pin is used for DiSEqC™ encoding. The fully bi-directional DiSEqC™ interfacing is completed by the built-in 22KHz tone detector. Its input pin (DETIN) must be AC coupled to the DiSEqC™ bus, and the extracted FWK data are available on the DSQOUT pin (*).

In order to improve design flexibility and to allow implementation of newcoming LNB remote control standards, an analogic modulation input pin is available (EXTM). An appropriate DC blocking capacitor must be used to couple the modulating signal source to the EXTM pin. When external modulation is not used, the relevant pin can be left open.

The current limitation block has two thresholds that can be selected by the I_{SEL} bit of the SR; the lower threshold is between 650 and 900mA (I_{SEL}=HIGH), while the higher threshold is between 750 and 1000mA (I_{SEL}=LOW).

The current protection block is SOA type. This limits the short circuit current (I_{SC}) typically at 300mA with I_{SEL}=HIGH and at 400mA with I_{SEL}=LOW when the output port is connected to ground.

It is possible to set the Short Circuit Current protection either statically (simple current clamp) or dynamically by the PCL bit of the SR; when the PCL (Pulsed Current Limiting) bit is set to LOW, the overcurrent protection circuit works dynamically: as soon as an overload is detected, the output is shut-down for a time t_{off}, typically 900ms. Simultaneously the OLF bit of the System Register is set to HIGH. After this time has elapsed, the output is resumed for a time t_{on}=1/10t_{off} (typ.). At the end of t_{on}, if the overload is still detected, the protection circuit will cycle again through T_{on} and T_{on}. At the end of a full Ton in which no overload is detected, normal operation is resumed and the OLF bit is reset to LOW. Typical T_{on}+T_{off} time is 990ms and it is determined by an internal timer. This dynamic operation can greatly reduce the power dissipation in short circuit condition, still ensuring excellent power-on start up in most conditions (**).

However, there could be some cases in which an highly capacitive load on the output may cause a difficult start-up when the dynamic protection is chosen. This can be solved by initiating any power start-up in static mode (PCL=HIGH) and then switching to the dynamic mode (PCL=LOW) after a chosen amount of time. When in static mode, the OLF bit goes HIGH when the current clamp limit is reached and returns LOW when the overload condition is cleared.

This IC is also protected against overheating: when the junction temperature exceeds 150°C (typ.), the step-up converter and the linear regulator are shut off, the loop-trough switch is opened, and the OTF bit of the SR is set to HIGH. Normal operation is resumed and the OTF bit is reset to LOW when the junction is cooled down to 140°C (typ.).

(*): External components are needed to comply to bi-directional DiSEqC™ bus hardware requirements. Full compliance of the whole application to DiSEqC™ specifications is not implied by the use of this IC.

(**): The current limitation circuit has no effect on the loop-through switch. When EN bit is LOW, the current flowing from LT1 to LT2 must be externally limited.

Table 1: Ordering Codes

TYPE	PowerSO-20 (Tube)	PowerSO-20 (Tape & Reel)
LNBS21	LNBS21PD	LNBS21PD-TR

Table 2: Absolute Maximum Ratings

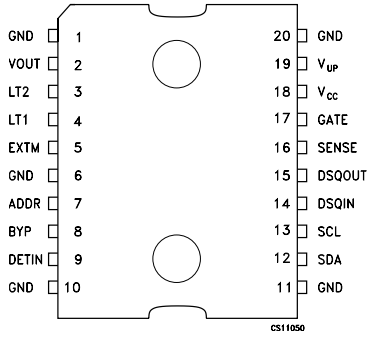
Symbol	Parameter	Value	Unit
V_{CC}	DC Input Voltage	16	V
V_{UP}	DC Input Voltage	25	V
V_{LT1}, V_{LT2}	DC Input Voltage	20	V
I_O	Output Current	Internally Limited	mA
V_O	DC Output Pin Voltage	-0.3 to 22	V
V_I	Logic Input Voltage (SDA, SCL, DSQIN)	-0.3 to 7	V
V_{DETIN}	Detector Input Signal Amplitude	2	V_{PP}
V_{OH}	Logic High Output Voltage (DSQOUT)	7	V
I_{LT}	Bypass Switch ON Current	500	mA
V_{LT}	Bypass Switch OFF Voltage	±20	V
I_{GATE}	Gate Current	±400	mA
V_{SENSE}	Current Sense Voltage	-0.3 to 1	V
$V_{ADDRESS}$	Address Pin Voltage	-0.3 to 7	V
T_{stg}	Storage Temperature Range	-40 to +150	°C
T_{op}	Operating Junction Temperature Range	-40 to +125	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

Table 3: Thermal Data

Symbol	Parameter	PowerSO-20	Unit
$R_{thj\text{-}case}$	Thermal Resistance Junction-case	2	°C/W

Figure 2: Pin Connection (top view)

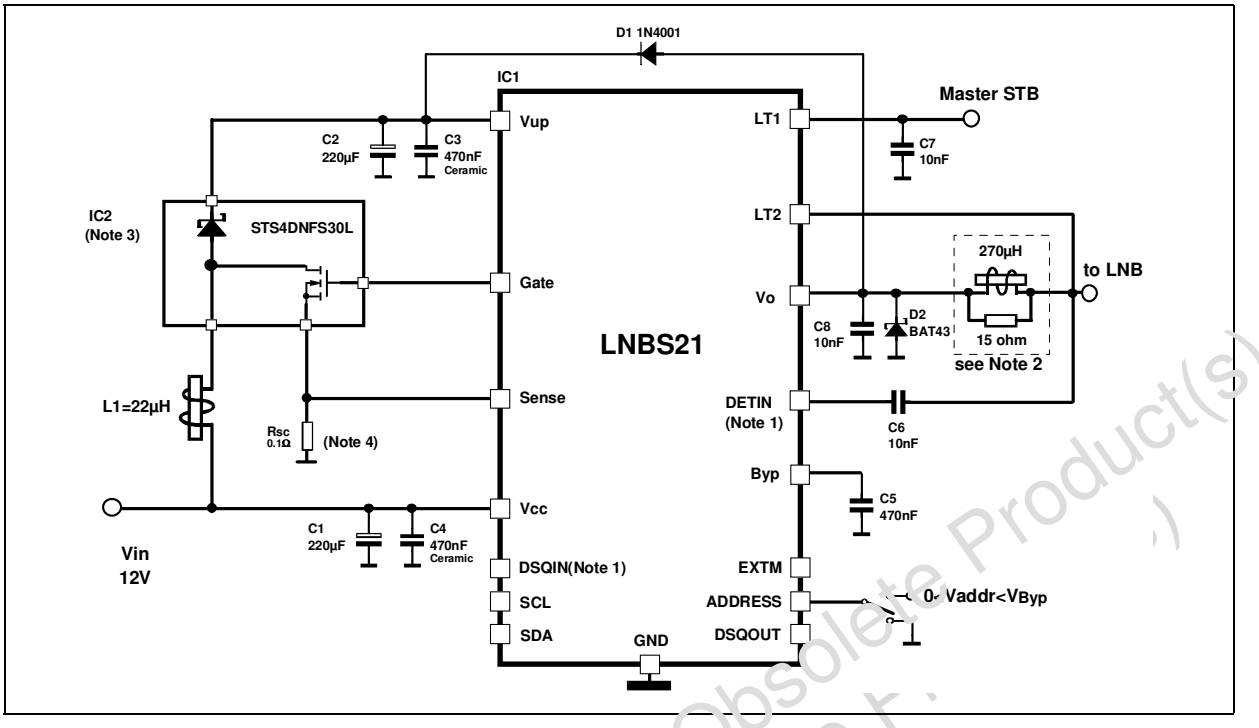


PowerSO-20

Table 4: Pin Description

SYMBOL	NAME	FUNCTION	PIN NUMBER vs. PACKAGE
V_{CC}	Supply Input	8V to 15V supply. A 220µF bypass capacitor to GND with a 470nF (ceramic) in parallel is recommended	18
GATE	External Switch Gate	External MOS switch Gate connection of the step-up converter	17
SENSE	Current Sense Input	Current Sense comparator input. Connected to current sensing resistor	16
V_{up}	Step-up Voltage	Input of the linear post-regulator. The voltage on this pin is monitored by internal step-ut controller to keep a minimum dropout across the linear pass transistor	19
OUT	Output Port	Output of the linear post regulator modulator to the LNB. See truth table for voltage selections.	2
SDA	Serial Data	Bidirectional data from/to I^2C bus.	12
SCL	Serial Clock	Clock from I^2C bus.	13
DSQIN	DiSEqC Input	When the TEN bit of the System Register is LOW, this pin will accept the DiSEqC code from the main µcontroller. The LNBS21 will use this code to modulate the internally generated 22kHz carrier. Set to GND the pin if not used.	14
DETIN	Detector In	22kHz Tone Detector Input. Must be AC coupled to the DiSEqC bus.	9
DSQOUT	DiSEqC Output	Open collector output of the Tone Detector to the main µcontroller for DiSEqC data decoding. It is LOW when tone is detected.	15
EXTM	External Modulator	External Modulation Input. Need DC decoupling to the AC source. If not used, can be left open.	5
GND	Ground	Pins to be connected to ground.	1, 6, 10, 11, 20
BYP	Bypass Capacitor	Needed for internal preregulator filtering	8
LT1	Loop Through Switch	In standby mode the power switch between LT1 and LT2 is closed. Max allowed current is 900mA. this pin can be left open if loop through function is not needed.	4
LT2	Loop Through Switch	Same as above	3
ADDR	Address Setting	Four I^2C bus addresses available by setting the Address Pin level voltage	7

Figure 3: Typical Application Circuit



(*) Set to GND if not used
(**) filter to be used according to EUTELSAT recommendation to implement the DiSEqC™ 2.x, not needed if bidirectional DiSEqC™ 2.x is not implemented (see DiSEqC implementation note)
(***) IC2 is a ST Fettky, STS4DNFS30L, that includes both the schottky diode and the N-Channel MosFet, needed for the DC/DC converter, in a So-8 package. It can be replaced by a schottky diode (STPS2L30A or similar) and a N-Channel MosFet (STN4NF03L or similar)

I²C BUS INTERFACE

Data transmission from main µP to the LNBS21 and viceversa takes place through the 2 wires I²C bus interface, consisting of the two lines SDA and SCL (pull-up resistors to positive supply voltage must be externally connected).

DATA VALIDITY

As shown in fig. 1, the data on the SDA line must be stable during the high period of the clock. The HIGH and LOW state of the data line can only change when the clock signal on the SCL line is LOW.

START AND STOP CONDITIONS

As shown in fig.2 a start condition is a HIGH to LOW transition of the SDA line while SCL is HIGH. The stop condition is a LOW to HIGH transition of the SDA line while SCL is HIGH. A STOP conditions must be sent before each START condition.

BYTE FORMAT

Every byte transferred to the SDA line must contain 8 bits. Each byte must be followed by an acknowledge bit. The MSB is transferred first.

ACKNOWLEDGE

The master (µP) puts a resistive HIGH level on the SDA line during the acknowledge clock pulse (see fig. 3). The peripheral (LNBS21) that acknowledges has to pull-down (LOW) the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during this clock pulse. The peripheral which has been addressed has to generate an acknowledge after the reception of each byte, otherwise the SDA line remains at the HIGH level during the ninth clock pulse time. In this case the master transmitter can generate the STOP information in order to abort the transfer. The LNBS21 won't generate the acknowledge if the V_{CC} supply is below the Undervoltage Lockout threshold (6.7V typ.).

TRANSMISSION WITHOUT ACKNOWLEDGE

Avoiding to detect the acknowledge of the LNBS21, the µP can use a simpler transmission:

simply it waits one clock without checking the slave acknowledging, and sends the new data. This approach of course is less protected from misworking and decreases the noise immunity.

Figure 4: Data Validity On The I²C Bus

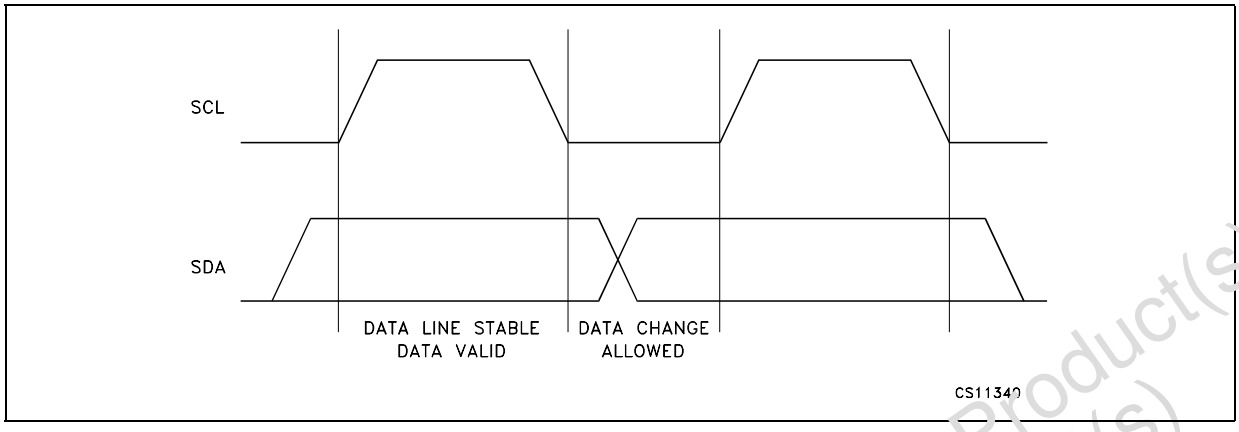


Figure 5: Timing Diagram On I²C Bus

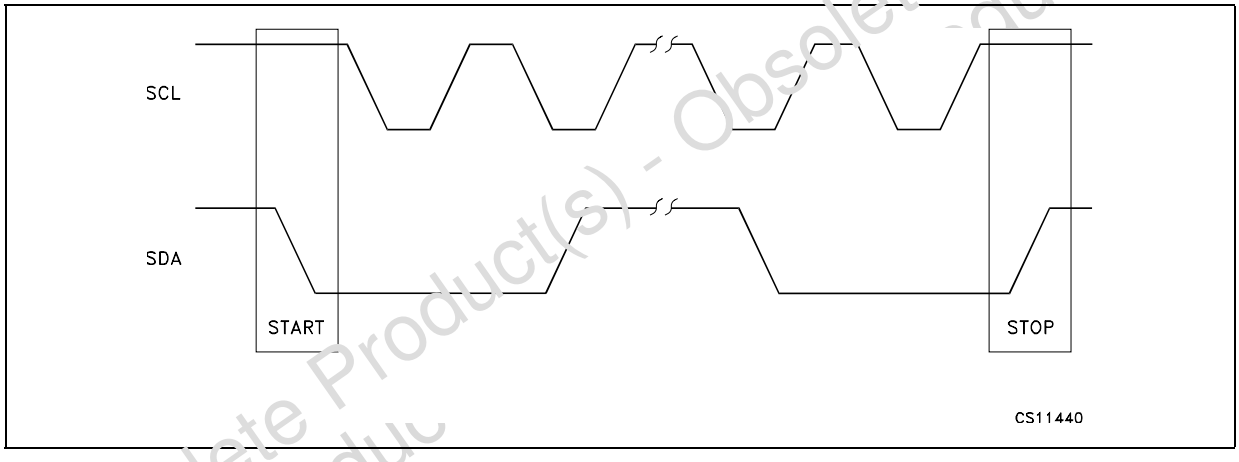
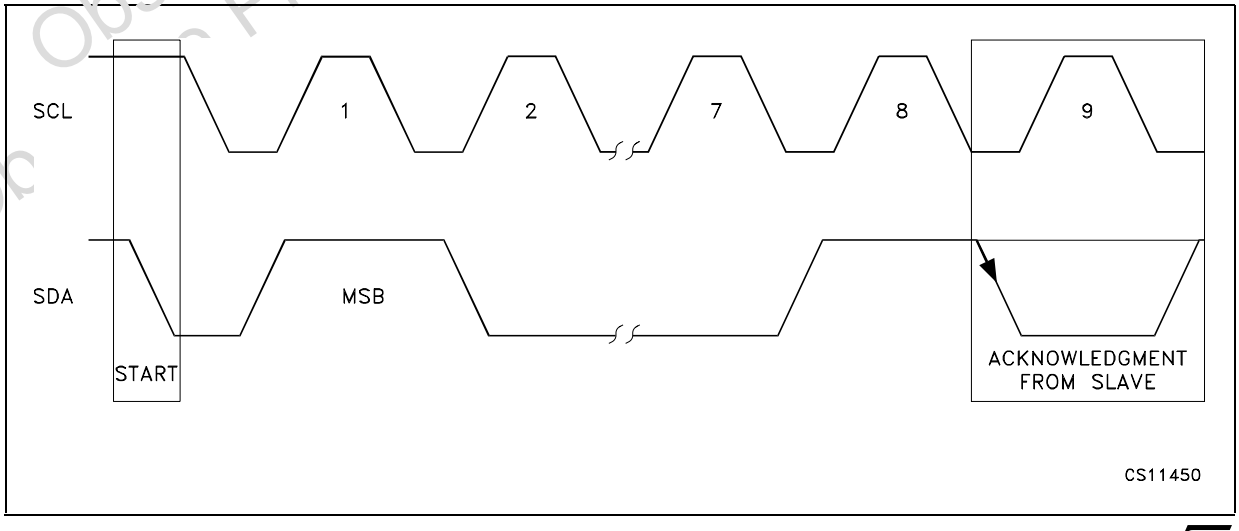


Figure 6: Acknowledge On I²C Bus



LNBS1 SOFTWARE DESCRIPTION

INTERFACE PROTOCOL

The interface protocol comprises:

- A start condition (S)
- A chip address byte = hex 10 / 11 (the LSB bit determines read(=1)/write(=0) transmission)
- A sequence of data (1 byte + acknowledge)
- A stop condition (P)

	CHIP ADDRESS									DATA									
	MSB						LSB			MSB							LSB		
S	0	0	0	1	0	0	0	R/W	ACK									ACK	P

ACK= Acknowledge
S= Start
P= Stop
R/W= Read/Write

SYSTEM REGISTER (SR, 1 BYTE)

MSB							LSB
R, W	R, W	R, W	R, W	R, W	R, W	R	R
PCL	ISEL	TEN	LLC	VSEL	EN	OTF	OLF

R,W= read and write bit
R= Read-only bit
All bits reset to 0 at Power-On

TRANSMITTED DATA (I^2C BUS WRITE MODE)

When the R/W bit in the chip address is set to 0, the main µP can write on the System Register (SR) of the LNBS21 via I^2C bus. Only 6 bits out of the 8 available can be written by the µP, since the remaining 2 are left to the diagnostic flags, and are read-only.

PCL	ISEL	TEN	LLC	VSEL	EN	OTF	OLF	Function
			0	0	1	X	X	V_{OUT}=13V, V_{UP}=16V Loopthrough switch open
			0	1	1	X	X	V_{OUT}=18V, V_{UP}=21V Loopthrough switch open
			1	0	1	X	X	V_{OUT}=14V, V_{UP}=17V Loopthrough switch open
			1	1	1	X	X	V_{OUT}=19V, V_{UP}=22V Loopthrough switch open
		0			1	X	X	22KHz tone is controlled by DSQIN pin
		1			1	X	X	22KHz tone is ON, DSQIN pin disabled
	0				1	X	X	$I_{OUT(min)}$=500mA, $I_{OUT(max)}$=650mA I_{SC}=300mA
	1				1	X	X	$I_{OUT(min)}$=400mA, $I_{OUT(max)}$=550mA I_{SC}=300mA
0					1	X	X	Pulsed (dynamic) current limiting is selected
1					1	X	X	Static current limiting is selected
X	X	X	X	X	0	X	X	Power blocks disabled, Loopthrough switch closed

X= don't care.
Values are typical unless otherwise specified

RECEIVED DATA (I^2C bus READ MODE)

The LNBS21 can provide to the Master a copy of the SYSTEM REGISTER information via I^2C bus in read mode. The read mode is Master activated by sending the chip address with R/W bit set to 1. At the following master generated clocks bits, the LNBS21 issues a byte on the SDA data bus line (MSB transmitted first).

At the ninth clock bit the MCU master can:

- acknowledge the reception, starting in this way the transmission of another byte from the LNBS21;
- no acknowledge, stopping the read mode communication.

While the whole register is read back by the µP, only the two read-only bits OLF and OTF convey diagnostic informations about the LNBS21.

PCL	ISEL	TEN	LLC	VSEL	EN	OTF	OLF	Function
These bits are read exactly the same as they were left after last write operation						0		T_J<140°C, normal operation
						1		T_J>150°C, power block disabled, Loothrough switch open
							0	$I_{OUT}<I_{OMAX}$, normal operation
							1	$I_{OUT}>I_{OMAX}$, overload protection triggered

Values are typical unless otherwise specified

POWER-ON I^2C INTERFACE RESET

The I^2C interface built in the LNBS21 is automatically reset at power-on. As long as the V_{CC} stays be-low the UnderVoltage Lockout threshold (6.7V typ.), the interface will not respond to any I^2C command and the System Register (SR) is initialized to all zeroes, thus keeping the power blocks disabled. Once the V_{CC} rises above 7.3V, the I^2C interface becomes operative and the SR can be configured by the main µP. This is due to About 500mV of hysteresis provided in the UVL threshold to avoid false retriggering of the Power-On reset circuit.

DiSEqC™ IMPLEMENTATION

The LNBS21 helps the system designer to implement the bi-directional (2.x) DiSEqC protocol by allowing an easy PWK modulation/ demodulation of the 22KHz carrier. The PWK data are exchanged between the LNBS21 and the main µP using logic levels that are compatible with both 3.3 and 5V microcontrollers. This data exchange is made through two dedicated pins, DSQIN and DSQOUT, in order to maintain the timing relationships between the PWK data and the PWK modulation as accurate as possible. These two pins should be directly connected to two I/O pins of the µP, thus leaving to the resident firmware the task of encoding and decoding the PWK data in accordance to the DiSEqC protocol. Full compliance of the system to the specification is thus not implied by the bare use of the LNBS21.

The system designer should also take in consideration the bus hardware requirements. that include the source impedance of the Master Transmitter measured at 22KHz. To limit the attenuation at carrier frequency, this impedance has to be 15ohm at 22KHz, dropping to zero ohm at DC to allow the power flow towards the peripherals. This can be simply accomplished by the LR termination put on the OUT pin of the LNBS, as shown in the Typical Application Circuit on page 5.

Unidirectional (1.x) DiSEqC and non-DiSEqC systems normally don't need this termination, and the OUT pin can be directly connected to the LNB supply port of the Tuner. There is also no need of Tone Decoding, thus, it is recommended to connect the DETIN and DSQOUT pins to ground to avoid EMI.

ADDRESS PIN

Connecting this pin to GND the Chip I^2C interface address is 0001000, but, it is possible to choice among 4 different addresses simply setting this pin at 4 fixed voltage levels (see table on page 10).

Table 5: Electrical Characteristics For LNBS Series (T_J = 0 to 85°C, EN=1, LLC=0, TEN=0, ISEL=0, PCL=0, DSQIN=0, V_{IN}=12V, I_{OUT}=50mA, unless otherwise specified. See software description section for I^2C access to the system register)

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
V_{IN}	Supply Voltage	I_O = 750 mA TEN=VSEL=LLC=1		8		15	V
V_{LT1}	LT1 Input Voltage					20	V
I_{IN}	Supply Current	I_O = 0mA TEN=VSEL=LLC=1	EN=1		20	40	mA
			EN=0		2.5	5	mA
V_O	Output Voltage	I_O = 750 mA VSEL=1	LLC=0	17.3	18	18.7	V
			LLC=1		19		V
V_O	Output Voltage	I_O = 750 mA VSEL=0	LLC=0	12.5	13	13.5	V
			LLC=1		14		V

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
ΔV_O	Line Regulation	V_{IN1}=15 to 18V	VSEL=0		5	40	mV
			VSEL=1		5	60	mV
ΔV_O	Load Regulation	VSEL=0 or 1 I_{OUT} = 50 to 750mA				200	mV
I_{MAX}	Output Current Limiting		ISEL=1	650		900	mA
			ISEL=0	750		1000	mA
I_{SC}	Output Short Circuit Current		ISEL=1		300		mA
			ISEL=0		400		mA
t_{OFF}	Dynamic Overload protection OFF Time	PCL=0 Output Shorted			900		ms
t_{ON}	Dynamic Overload protection ON Time	PCL=0 Output Shorted			t_{OFF}/10		ms
f_{TONE}	Tone Frequency	TEN=1		20	22	24	KHz
A_{TONE}	Tone Amplitude	TEN=1		0.55	0.72	0.9	Vpp
D_{TONE}	Tone Duty Cycle	TEN=1		40	50	60	%
t_r, t_f	Tone Rise and Fall Time	TEN=1		5	10	15	µs
G_{EXTM}	External Modulation Gain	$\Delta V_{OUT}/\Delta V_{EXTM}$, f = 10Hz to 40KHz			6		
V_{EXTM}	External Modulation Input Voltage	AC Coupling				400	mVpp
Z_{EXTM}	External Modulation Impedance	f = 10Hz to 50KHz			260		Ω
V_{LT}	Loopthrough Switch Voltage Drop (lt1 to LT2)	EN=0, I_{LT}=300mA, V_{IN}=12 or 19V			0.35	0.6	V
f_{SW}	DC/DC Converter Switch Frequency				220		kHz
f_{DETIN}	Tone Detector Frequency Capture Range	0.4Vpp sinewave		18		24	kHz
V_{DETIN}	Tone Detector Input Amplitude	f_{IN}=22kHz sinewave		0.2		1.5	Vpp
Z_{DETIN}	Tone Detector Input Impedance				150		kΩ
V_{OL}	Overload Flag Pin Logic LOW	Tone present I_{OL}=2mA			0.3	0.5	V
I_{OZ}	Overload Flag Pin OFF State Leakage Current	Tone absent V_{OH} = 6V				10	µA
V_{IL}	DSQIN Input Pin Logic LOW					0.8	V
V_{IH}	DSQIN Input Pin Logic HIGH			2			V
I_{IH}	DSQIN Pins Input Current	V_{IH} = 5V			15		µA
I_{OBK}	Output Backward Current	EN=0 V_{OBK} = 18V			-4	-10	mA
T_{SHDN}	Temperature Shutdown Threshold				150		°C
ΔT_{SHDN}	Temperature Shutdown Hysteresis				15		°C

Table 6: Gate And Sense Electrical Characteristics (T_J = 0 to 85°C, V_{IN}=12V)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
R_{DSON-L}	Gate LOW R_{DSON}	I_{GATE}=-100mA		4.5		Ω
R_{DSON-H}	Gate LOW R_{DSON}	I_{GATE}=100mA		4.5		Ω
V_{SENSE}	Current Limit Sense Voltage			200		mV

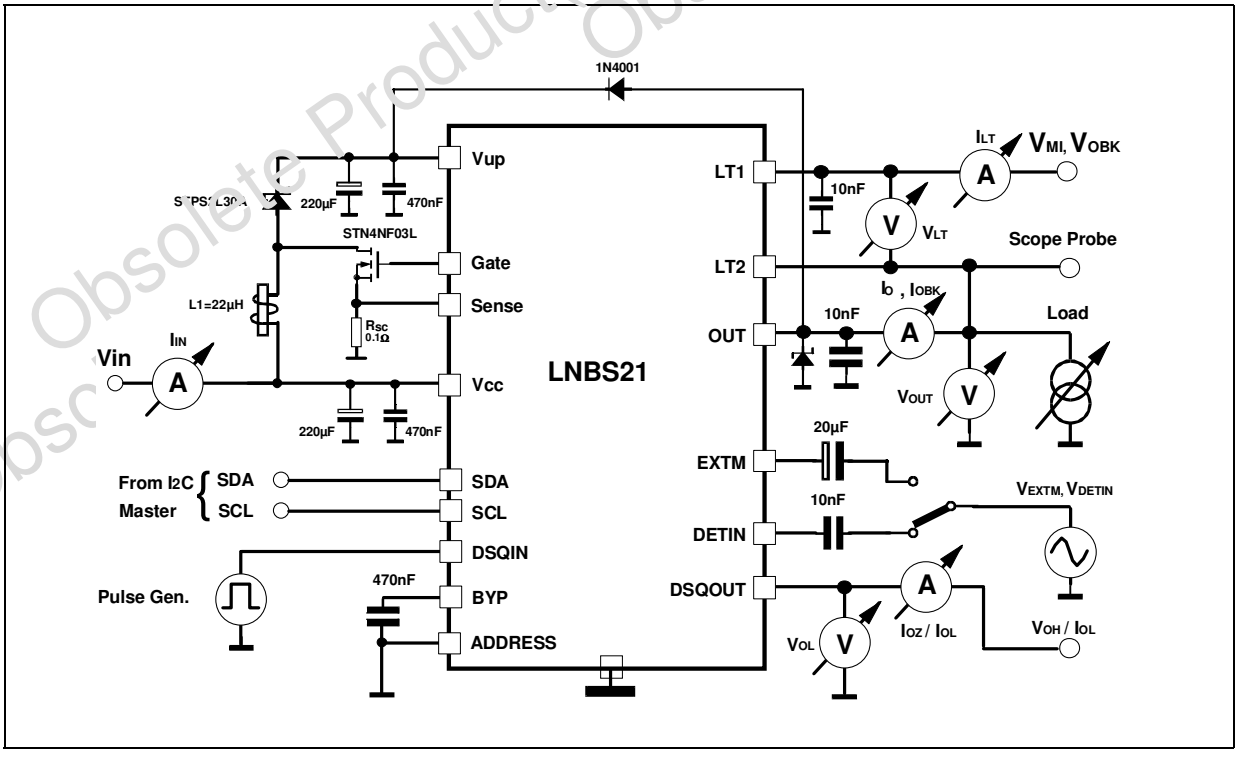
Table 7: I^2C Electrical Characteristics (T_J = 0 to 85°C, V_{IN}=12V)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{IL}	LOW Level Input Voltage	SDA, SCL			0.8	V
V_{IH}	HIGH Level Input Voltage	SDA, SCL	2			V
I_{IH}	Input Current	SDA, SCL, V_{IN}= 0.4 to 4.5v	-10		10	µA
V_{IL}	DSQIN Input Pin Logic LOW	SDA (open drain), I_{OL} = 6mA			0.6	V
f_{MAX}	Maximum Clock Frequency	SCL	500			KHz

Table 8: Address Pin Characteristics (T_J = 0 to 85°C, V_{IN}=12V)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{ADDR-1}	"0001000" Addr Pin Voltage		0		0.7	V
V_{ADDR-2}	"0001001" Addr Pin Voltage		1.3		1.7	V
V_{ADDR-3}	"0001010" Addr Pin Voltage		2.3		2.7	V
V_{ADDR-4}	"0001011" Addr Pin Voltage		3.3		5	V

Figure 7: Test Circuit



TYPICAL CHARACTERISTICS (unless otherwise specified T_j = 25°C)

Figure 8: Output Voltage vs Temperature

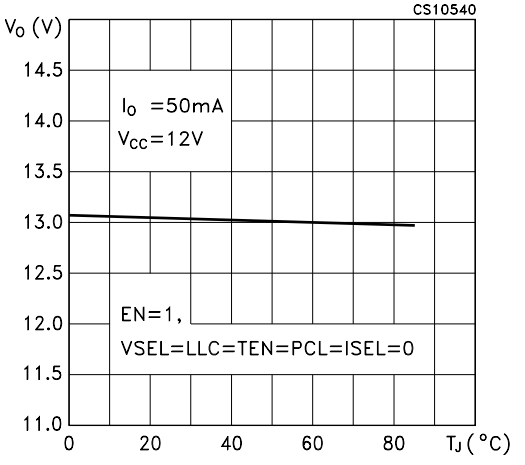


Figure 9: Output Voltage vs Temperature

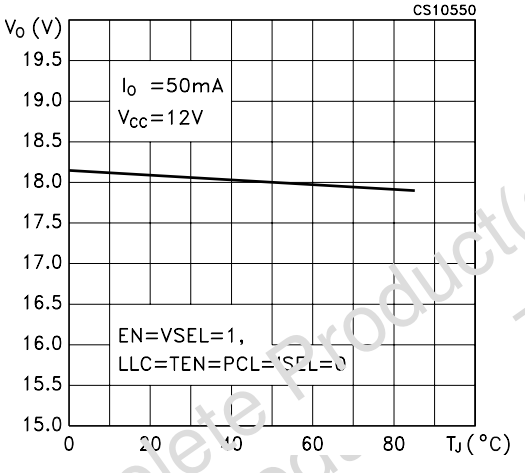


Figure 10: Line Regulation vs Temperature

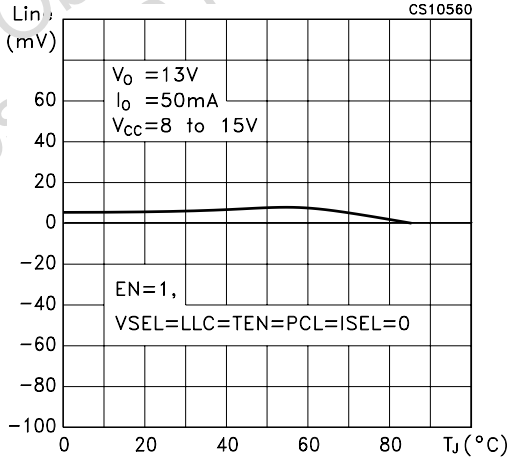


Figure 11: Line Regulation vs Temperature

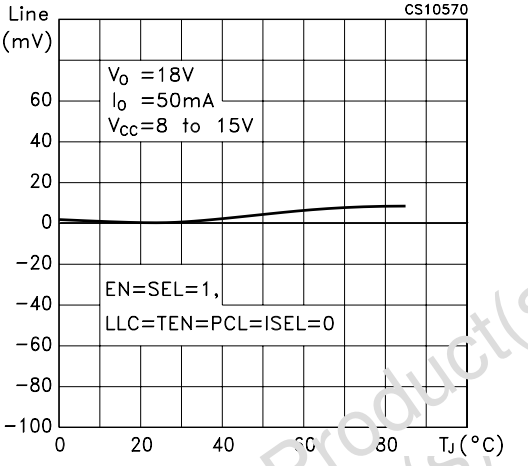


Figure 12: Load Regulation vs Temperature

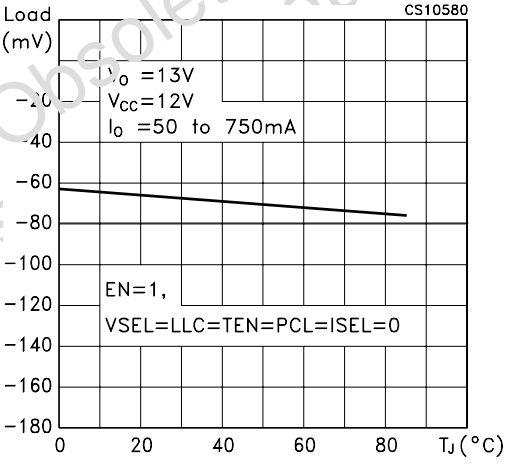


Figure 13: Load Regulation vs Temperature

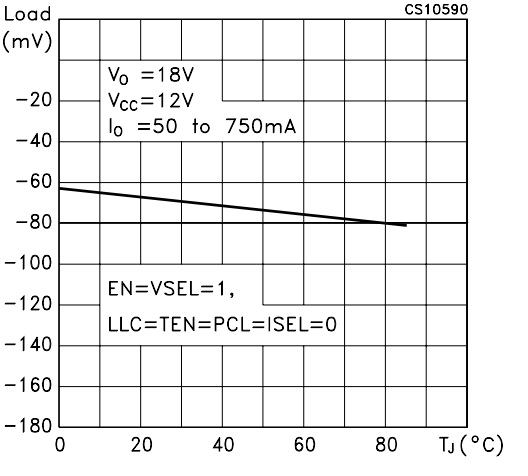


Figure 14: Supply Current vs Temperature

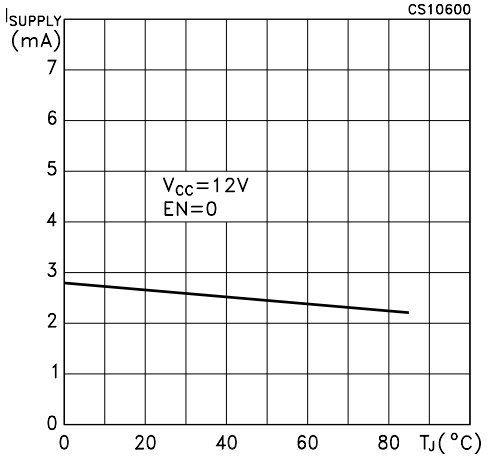


Figure 15: Supply Current vs Temperature

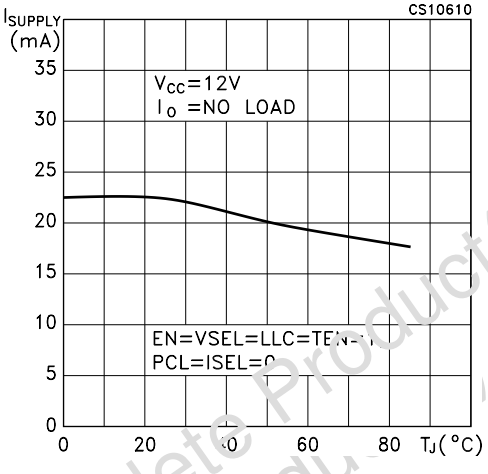


Figure 16: Dynamic Overload Protection ON Time vs Temperature

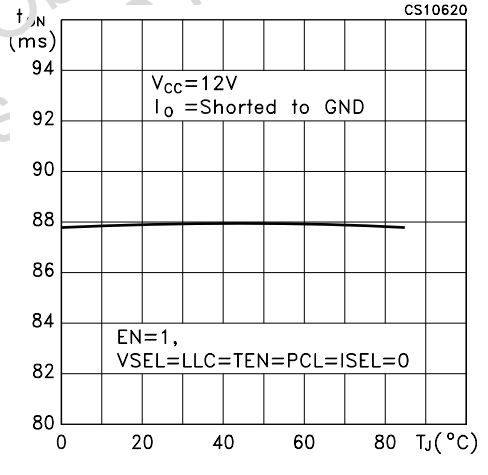


Figure 17: Dynamic Overload Protection OFF Time vs Temperature

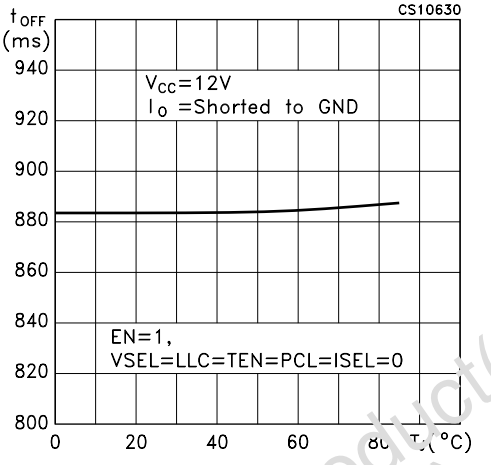


Figure 18: Output Current Limiting vs Temperature

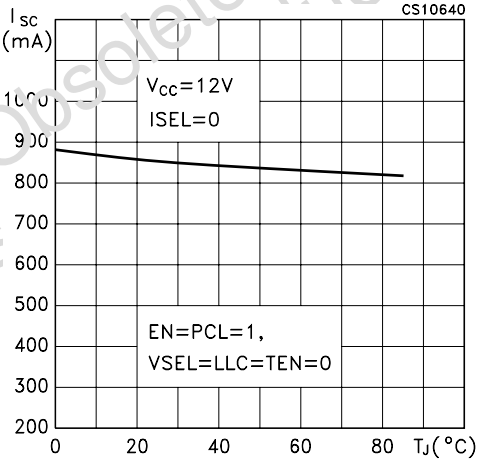


Figure 19: Output Current Limiting vs Temperature

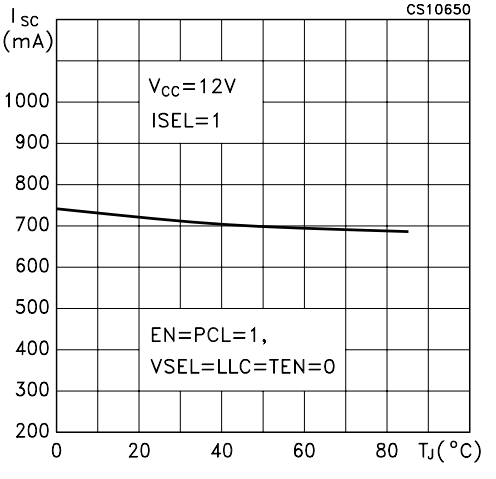


Figure 20: Tone Frequency vs Temperature

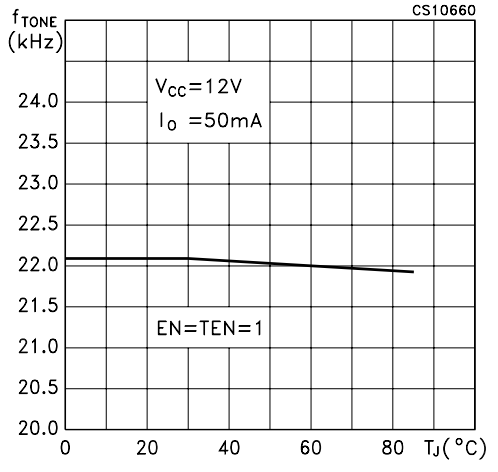


Figure 21: Tone Amplitude vs Temperature

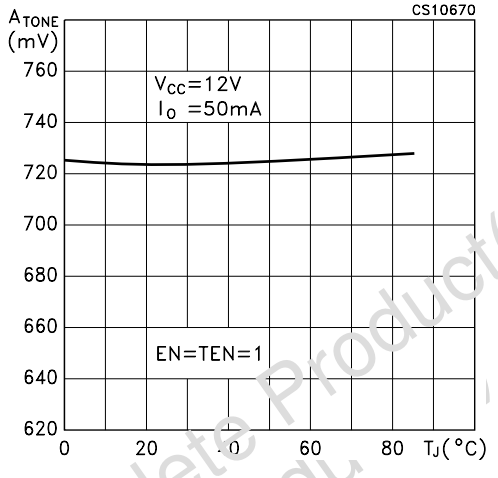


Figure 22: Tone Duty Cycle vs Temperature

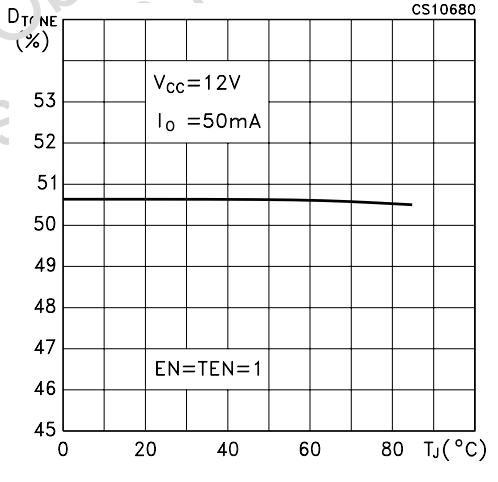


Figure 23: Tone Rise Time vs Temperature

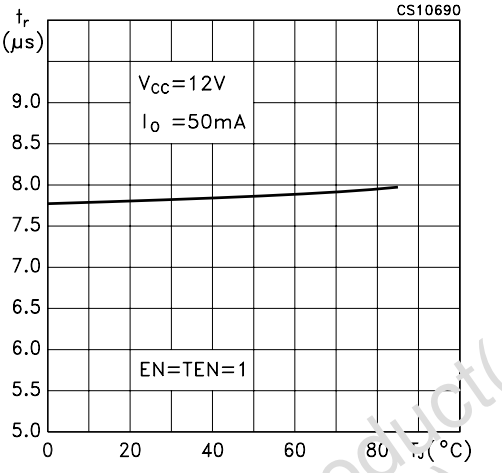


Figure 24: Tone Fall Time vs Temperature

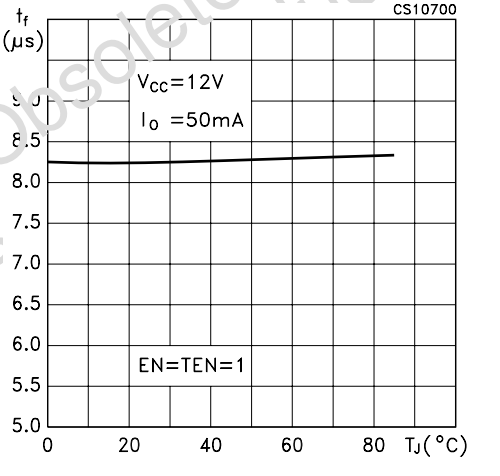


Figure 25: Loopthrought Switch Drop Voltage vs Temperature

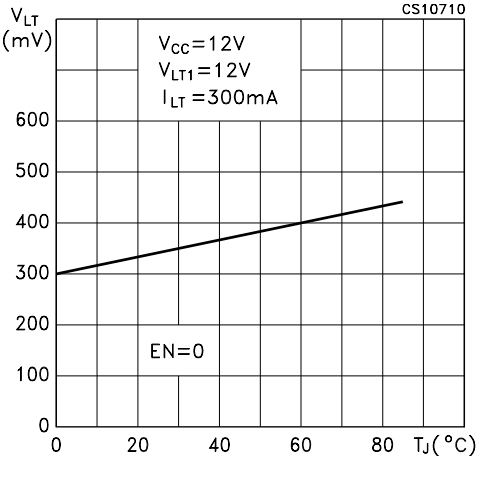


Figure 26: Loopthrought Switch Drop Voltage vs Temperature

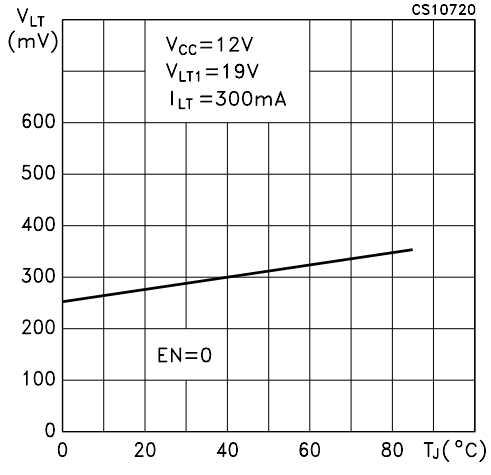


Figure 27: Loopthrought Switch Drop Voltage vs Loopthrought Current

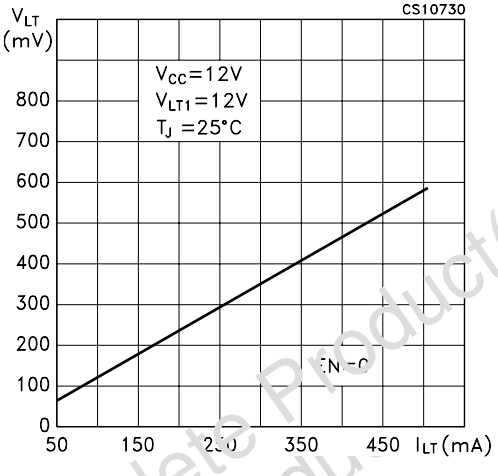


Figure 28: Loopthrought Switch Drop Voltage vs Loopthrought Current

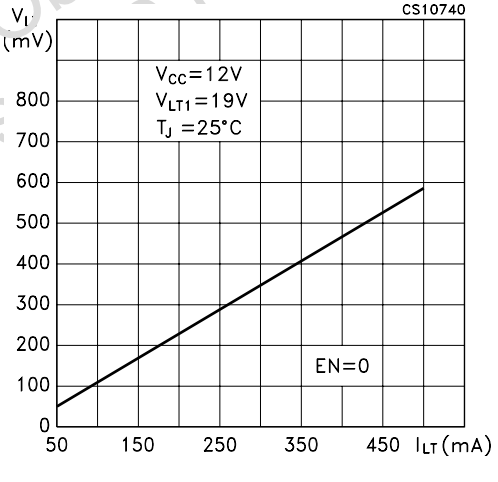


Figure 29: DSQOUT Pin Logic Low vs Temperature

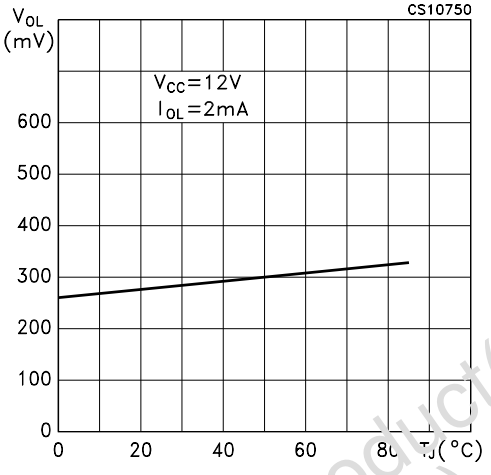


Figure 30: Undervoltage Lockout Threshold vs Temperature

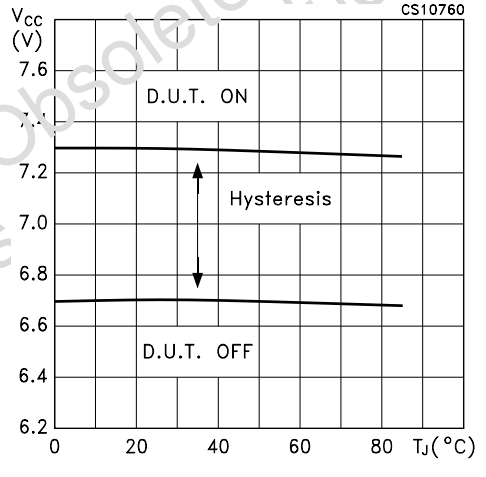


Figure 31: Output Backward Current vs Temperature

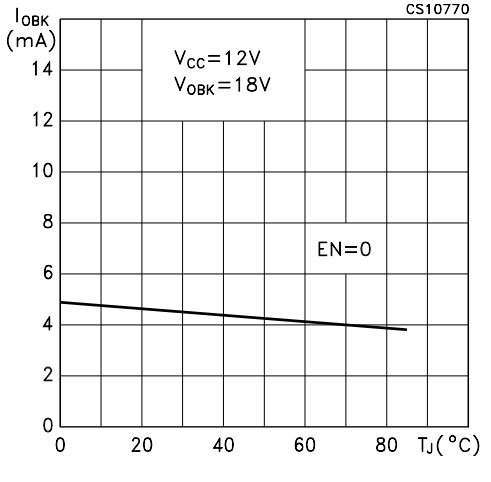


Figure 32: DC/DC Converter Efficiency vs Temperature

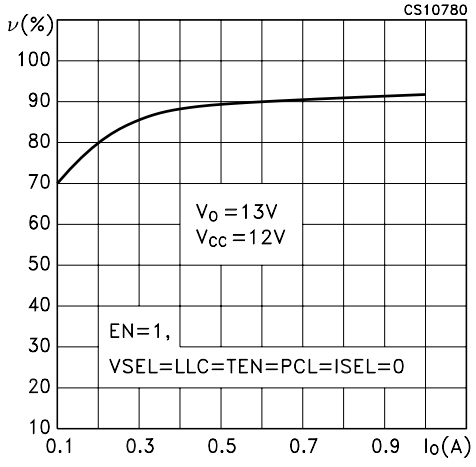


Figure 33: Current Limit Sense vs Temperature

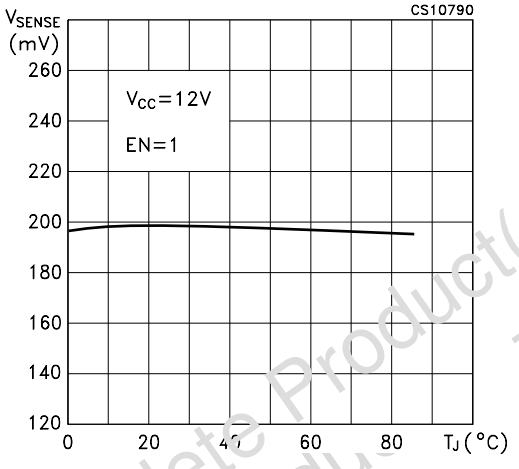
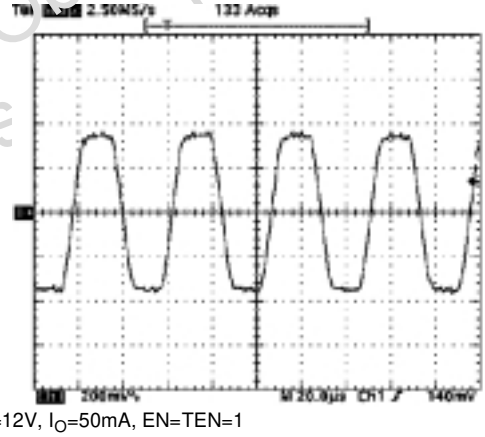
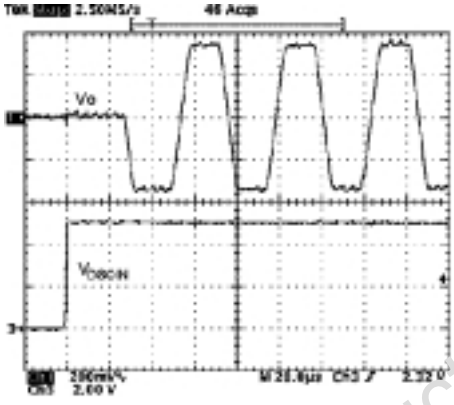


Figure 34: 22kHz Tone



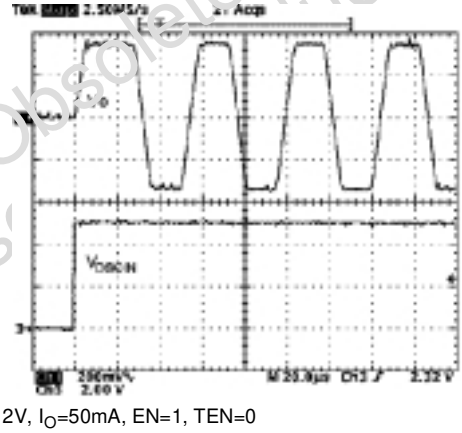
V_{CC}=12V, I_O=50mA, EN=TEN=1

Figure 35: DSQIN Tone Enable Transient Response



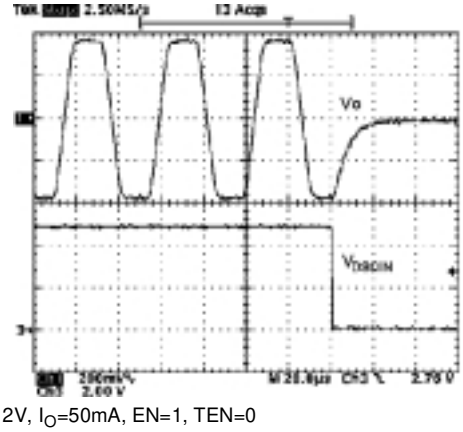
V_{CC}=12V, I_O=50mA, EN=1, TEN=0

Figure 36: DSQIN Tone Enable Transient Response



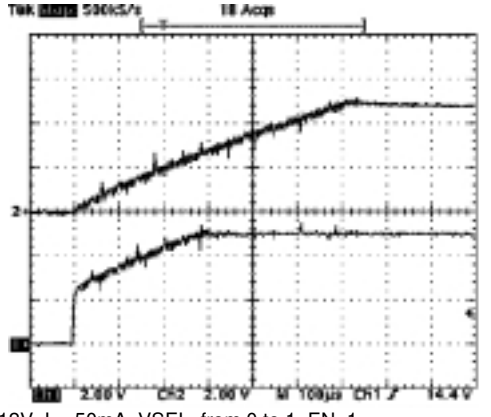
V_{CC}=12V, I_O=50mA, EN=1, TEN=0

Figure 37: DSQIN Tone Disable Transient Response



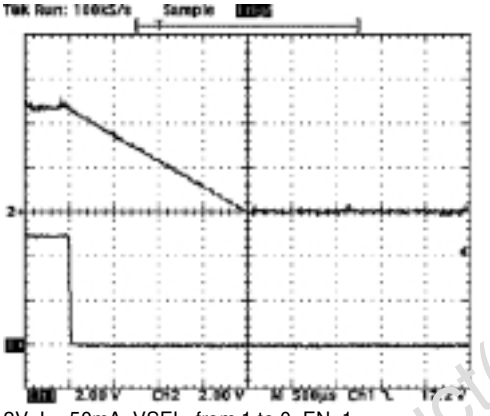
V_{CC}=12V, I_O=50mA, EN=1, TEN=0

Figure 38: Output Voltage Transient Response from 13V to 18V



V_{CC}=12V, I_O=50mA, VSEL=from 0 to 1, EN=1

Figure 39: Output Voltage Transient Response from 13V to 18V



V_{CC}=12V, I_O=50mA, VSEL=from 1 to 0, EN=1

TERMAL DESIGN NOTES

During normal operation, this device dissipates some power. At maximum rated output current (500mA), the voltage drop on the linear regulator lead to a total dissipated power that is of about 1.7W. The heat generated requires a suitable heatsink to keep the junction temperature below the overtemperature protection threshold. Assuming a 40°C temperature inside the Set-Top-Box case, the total Rthj-amb has to be less than 50°C/W.

While this can be easily achieved using a through-hole power package that can be attached to a small heatsink or to the metallic frame of the receiver, a surface mount power package must rely on PCB solutions whose thermal efficiency is often limited. The simplest solution is to use a large, continuous copper area of the GND layer to dissipate the heat coming from the IC body.

The SO-20 package of this IC has 4 GND pins that are not just intended for electrical GND connection, but also to provide a low thermal resistance path between the silicon chip and the PCB heatsink. Given an Rthj-c equal to 15°C/W, a maximum of 35°C/W are left to the PCB heatsink. This figure is achieved if a minimum of 25cm^2 copper area is placed just below the IC body. This area can be the inner GND layer of a multi-layer PCB, or, in a dual layer PCB, an unbroken GND area even on the opposite side where the IC is placed. In both cases, the thermal path between the IC GND pins and the dissipating copper area must exhibit a low thermal resistance.

In figure 40, it is shown a suggested layout for the SO-20 package with a dual layer PCB, where the IC Ground pins and the square dissipating area are thermally connected through 32 vias holes, filled by solder. This arrangement, when L=50mm, achieves an Rthc-a of about 25°C/W.

Different layouts are possible, too. Basic principles, however, suggest to keep the IC and its ground pins approximately in the middle of the dissipating area; to provide as many vias as possible; to design a dissipating area having a shape as square as possible and not interrupted by other copper traces.

Due to presence of an exposed pad connected to GND below the IC body, the PowerSO-20 package has a Rthj-c much lower than the SO-20, only 2°C/W. As a result, much lower copper area must be provided to dissipate the same power and minimum of 12cm^2 copper area is enough, see figure 41.

Figure 40: SO-20 Suggested Pcb Heatsink Layout

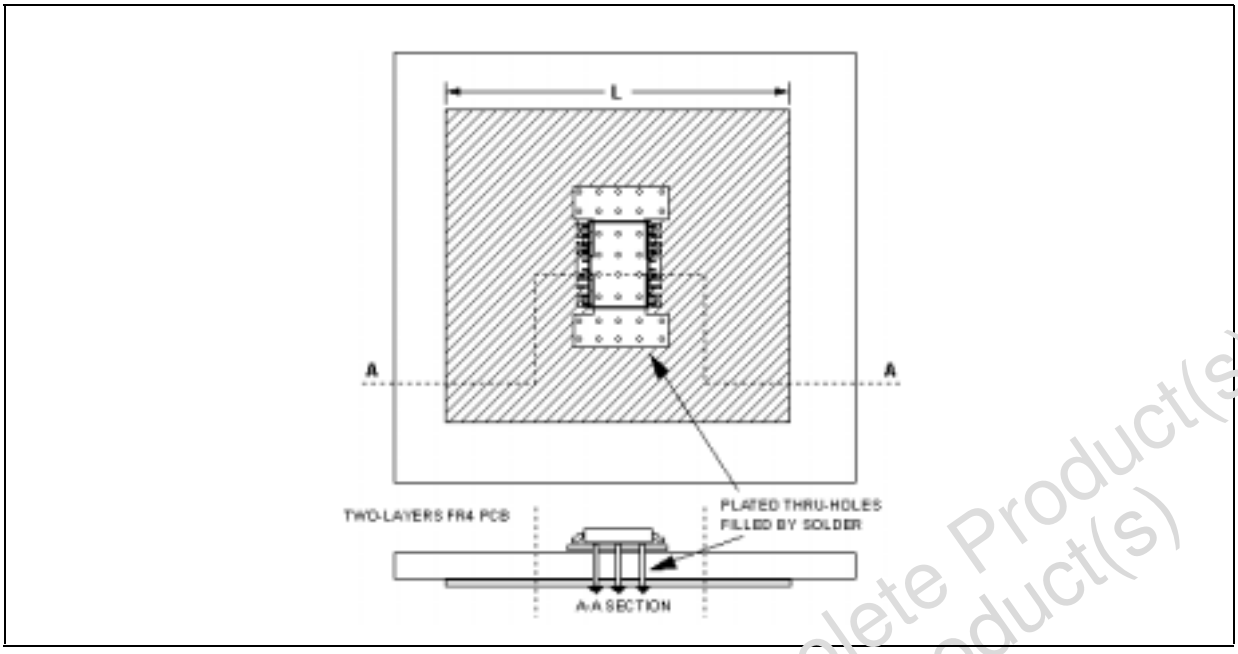
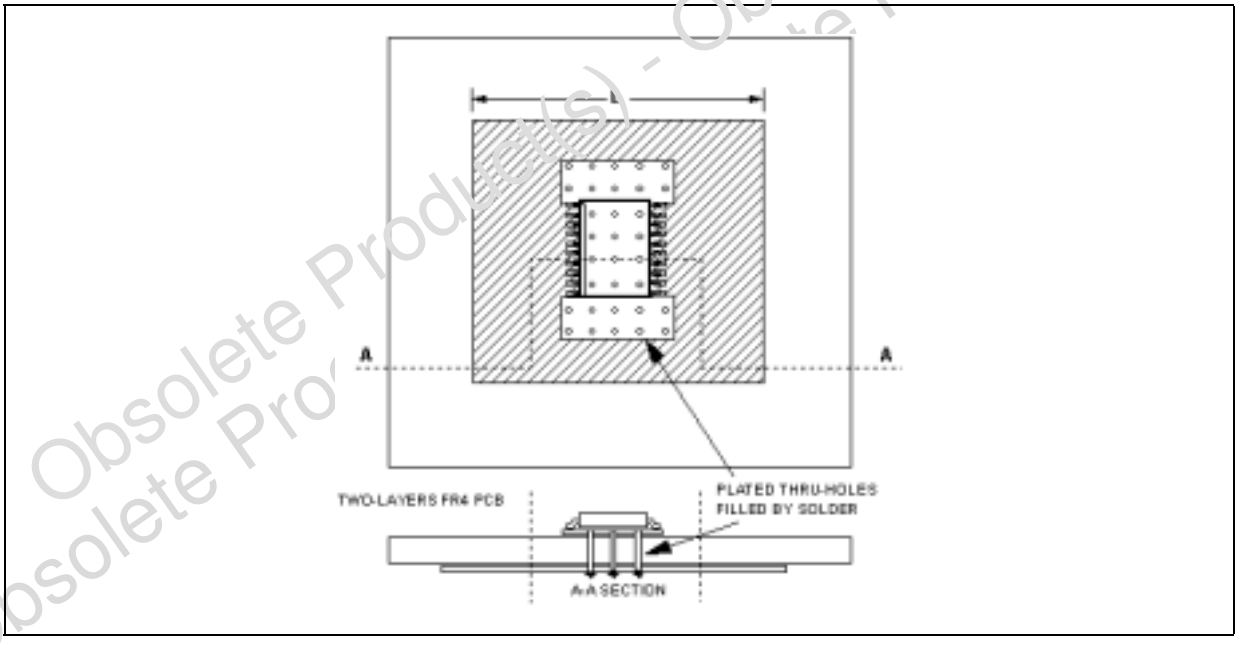


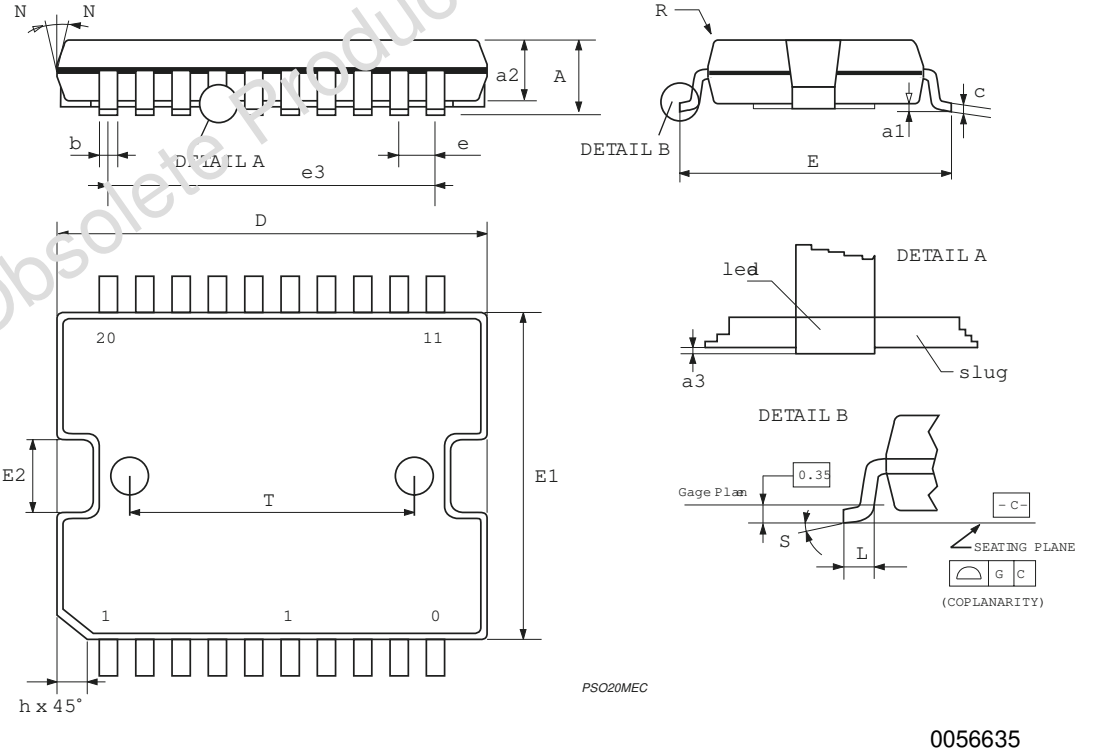
Figure 41: PowerSO-20 Suggested Pcb Heatsink Layout



PowerSO-20 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			3.60			0.1417
a1	0.10		0.30	0.0039		0.0118
a2			3.30			0.1299
a3	0		0.10	0		0.0039
b	0.40		0.53	0.0157		0.0209
c	0.23		0.32	0.0090		0.0013
D (1)	15.80		16.00	0.6220		0.630
E	13.90		14.50	0.5472		0.5710
e		1.27			0.0500	
e3		11.43			0.4500	
E1 (1)	10.90		11.10	0.4291		0.4370
E2			2.90			0.1141
G	0		0.10	0.0000		0.0039
h			1.10			0.0433
L	0.80		1.10	0.0314		0.0433
N			10˚			10˚
S	0˚		8˚	0˚		8˚
T		10.0			0.3937	

(1) “D and E1” do not include mold flash or protusions - Mold flash or protusions shall not exceed 0.15mm (0.006”)



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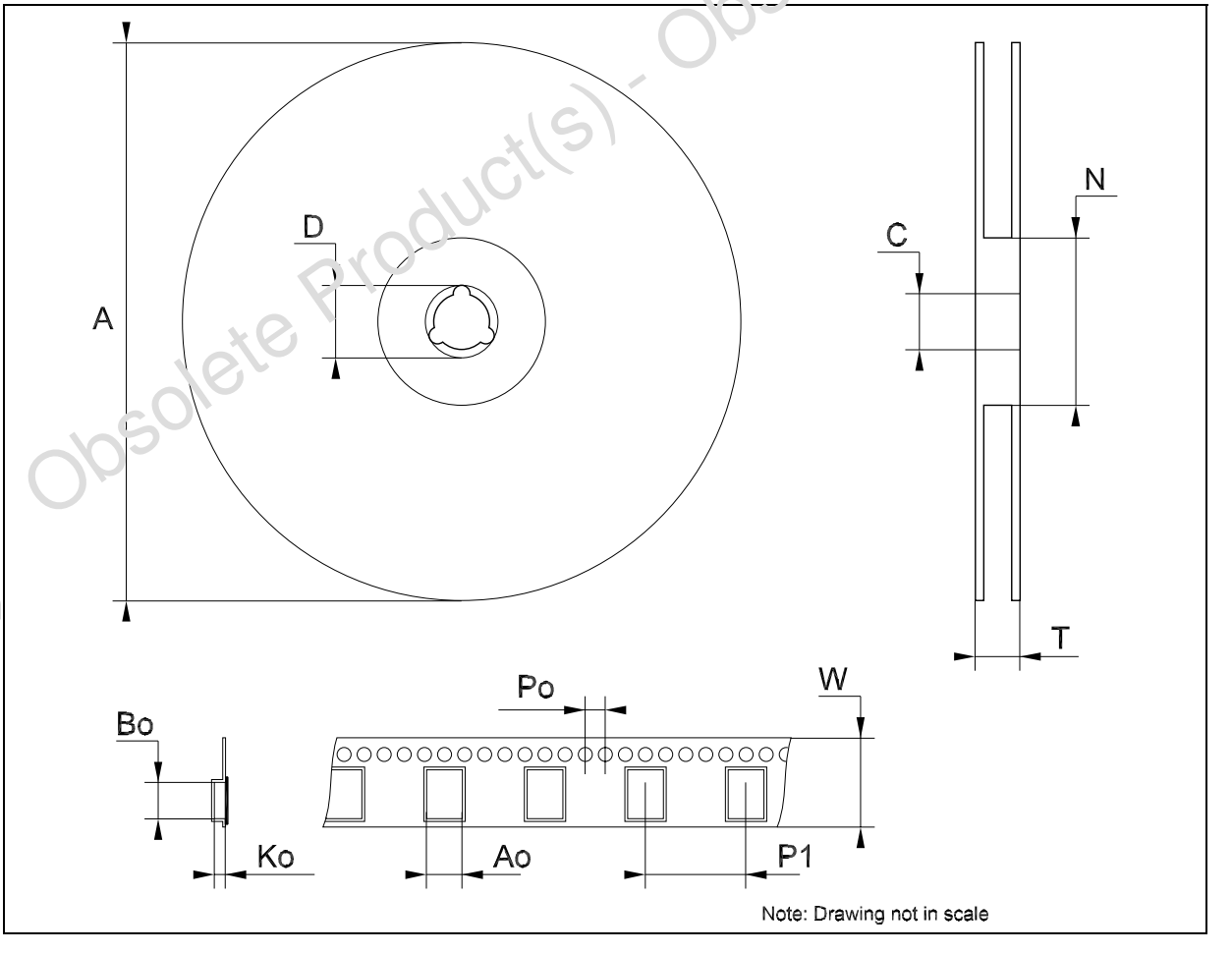
Tape & Reel PowerSO-20 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			330			12.992
C	12.8		13.2	0.504		0.519
D	20.2			0.795		
N	60			2.362		
T			30.4			1.197
Ao	15.1		15.3	0.594		0.602
Bo	16.5		16.7	0.650		0.658
Ko	3.8		4.0	0.149		0.157
Po	3.9		4.1	0.153		0.161
P	23.9		24.1	0.941		0.949
W	23.7		24.3	0.933		0.957



Note: Drawing not in scale

Table 9: Revision History

Date	Revision	Description of Changes
05-Oct-2004	3	Mistake Pin 6 - Table 4.