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Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China





LPC1110/11/12/13/14/15

32-bit ARM Cortex-M0 microcontroller; up to 64 kB flash and 8 kB SRAM

Rev. 9.2 — 26 March 2014

Product data sheet

1. General description

The LPC1110/11/12/13/14/15 are an ARM Cortex-M0 based, low-cost 32-bit MCU family, designed for 8/16-bit microcontroller applications, offering performance, low power, simple instruction set and memory addressing together with reduced code size compared to existing 8/16-bit architectures.

The LPC1110/11/12/13/14/15 operate at CPU frequencies of up to 50 MHz.

The peripheral complement of the LPC1110/11/12/13/14/15 includes up to 64 kB of flash memory, up to 8 kB of data memory, one Fast-mode Plus I²C-bus interface, one RS-485/EIA-485 UART, up to two SPI interfaces with SSP features, four general purpose counter/timers, a 10-bit ADC, and up to 42 general purpose I/O pins.

Remark: The LPC111x series consists of the LPC1100 series (parts LPC111x/101/201/301), LPC1100L series (parts LPC111x/002/102/202/302), and the LPC1100XL series (parts LPC111x/103/203/303/323/333). The LPC1100L and LPC1100XL series include the power profiles, a windowed watchdog timer, and a configurable open-drain mode.

For related documentation, see [Section 16 “References”](#).

2. Features and benefits

- System:
 - ◆ ARM Cortex-M0 processor, running at frequencies of up to 50 MHz.
 - ◆ ARM Cortex-M0 built-in Nested Vectored Interrupt Controller (NVIC).
 - ◆ Non-Maskable Interrupt (NMI) input selectable from several input sources (LPC1100XL series only).
 - ◆ Serial Wire Debug.
 - ◆ System tick timer.
- Memory:
 - ◆ 64 kB (LPC1115), 56 kB (LPC1114/333), 48 kB (LPC1114/323), 32 kB (LPC1114/102/201/202/203/301/302/303), 24 kB (LPC1113), 16 kB (LPC1112), 8 kB (LPC1111), or 4 kB (LPC1110) on-chip flash programming memory.
 - ◆ 256 byte page erase function (LPC1100XL series only)
 - ◆ 8 kB, 4 kB, 2 kB, or 1 kB SRAM.
 - ◆ In-System Programming (ISP) and In-Application Programming (IAP) via on-chip bootloader software.



- Digital peripherals:
 - ◆ Up to 42 General Purpose I/O (GPIO) pins with configurable pull-up/pull-down resistors. In addition, a configurable open-drain mode is supported on the LPC1100L and LPC1100XL series.
 - ◆ GPIO pins can be used as edge and level sensitive interrupt sources.
 - ◆ High-current output driver (20 mA) on one pin.
 - ◆ High-current sink drivers (20 mA) on two I²C-bus pins in Fast-mode Plus (not on LPC1112FDH20/102).
 - ◆ Four general purpose counter/timers with up to eight capture inputs and up to 13 match outputs.
 - ◆ Programmable WatchDog Timer (WDT) the LPC1100 series only.
 - ◆ Programmable windowed WDT on the LPC1100L and LPC1100XL series only.
- Analog peripherals:
 - ◆ 10-bit ADC with input multiplexing among 5, 6, or 8 pins depending on package size.
- Serial interfaces:
 - ◆ UART with fractional baud rate generation, internal FIFO, and RS-485 support.
 - ◆ Two SPI controllers with SSP features and with FIFO and multi-protocol capabilities (second SPI on LPC1100 and LPC1100L series LQFP48 package only).
 - ◆ I²C-bus interface supporting full I²C-bus specification and Fast-mode Plus with a data rate of 1 Mbit/s with multiple address recognition and monitor mode (not on LPC1112FDH20/102).
- Clock generation:
 - ◆ 12 MHz internal RC oscillator trimmed to 1 % accuracy that can optionally be used as a system clock.
 - ◆ Crystal oscillator with an operating range of 1 MHz to 25 MHz.
 - ◆ Programmable watchdog oscillator with a frequency range of 9.4 kHz to 2.3 MHz.
 - ◆ PLL allows CPU operation up to the maximum CPU rate without the need for a high-frequency crystal. May be run from the system oscillator or the internal RC oscillator.
 - ◆ Clock output function with divider that can reflect the system oscillator clock, IRC clock, CPU clock, and the Watchdog clock.
- Power control:
 - ◆ Integrated PMU (Power Management Unit) to minimize power consumption during Sleep, Deep-sleep, and Deep power-down modes.
 - ◆ Power profiles residing in boot ROM allowing to optimize performance and minimize power consumption for any given application through one simple function call. (LPC1100L and LPC1100XL series only.)
 - ◆ Three reduced power modes: Sleep, Deep-sleep, and Deep power-down.
 - ◆ Processor wake-up from Deep-sleep mode via a dedicated start logic using up to 13 of the functional pins.
 - ◆ Power-On Reset (POR).
 - ◆ Brownout detect with up to four separate thresholds for interrupt and forced reset.
- Unique device serial number for identification.
- Single power supply (1.8 V to 3.6 V).
- Available as LQFP48 package, HVQFN33 package, and TFBGA48 package.

- LPC1100L series available as TSSOP28 package, DIP28 package, TSSOP20 package, and SO20 package.
- Extended temperature (–40 °C to +105 °C) for selected parts (see [Table 2](#)).

3. Applications

- eMetering
- Lighting
- Alarm systems
- White goods

4. Ordering information

Table 1. Ordering information

Type number	Package		Version
	Name	Description	
SO20, TSSOP20, TSSOP28, and DIP28 packages			
LPC1110FD20	SO20	SO20: plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1
LPC1111FDH20/002	TSSOP20	TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm	SOT360-1
LPC1112FD20/102	SO20	SO20: plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1
LPC1112FDH20/102	TSSOP20	TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm	SOT360-1
LPC1112FDH28/102	TSSOP28	TSSOP28: plastic thin shrink small outline package; 28 leads; body width 4.4 mm	SOT361-1
LPC1114FDH28/102	TSSOP28	TSSOP28: plastic thin shrink small outline package; 28 leads; body width 4.4 mm	SOT361-1
LPC1114FN28/102	DIP28	DIP28: plastic dual in-line package; 28 leads (600 mil)	SOT117-1
HVQFN24/33, LQFP48, and TFBGA48 packages			
LPC1111FHN33/101	HVQFN33	HVQFN: plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 7 × 7 × 0.85 mm	n/a
LPC1111FHN33/102	HVQFN33	HVQFN: plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 7 × 7 × 0.85 mm	n/a
LPC1111FHN33/201	HVQFN33	HVQFN: plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 7 × 7 × 0.85 mm	n/a
LPC1111FHN33/202	HVQFN33	HVQFN: plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 7 × 7 × 0.85 mm	n/a
LPC1111FHN33/103	HVQFN33	HVQFN: plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 7 × 7 × 0.85 mm	n/a
LPC1111JHN33/103	HVQFN33	HVQFN: plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 7 × 7 × 0.85 mm	n/a
LPC1111FHN33/203	HVQFN33	HVQFN: plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 7 × 7 × 0.85 mm	n/a
LPC1111JHN33/203	HVQFN33	HVQFN: plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 7 × 7 × 0.85 mm	n/a
LPC1112FHN33/101	HVQFN33	HVQFN: plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 7 × 7 × 0.85 mm	n/a
LPC1112FHN33/102	HVQFN33	HVQFN: plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 7 × 7 × 0.85 mm	n/a

Table 1. Ordering information ...continued

Type number	Package		Version
	Name	Description	
LPC1112FHN33/201	HVQFN33	HVQFN: plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 7 × 7 × 0.85 mm	n/a
LPC1112FHN33/202	HVQFN33	HVQFN: plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 7 × 7 × 0.85 mm	n/a
LPC1112FHN24/202	HVQFN24	HVQFN24: plastic thermal enhanced very thin quad flat package; no leads; 24 terminals; body 4 × 4 × 0.85 mm	SOT616-3
LPC1112FHI33/102	HVQFN33	HVQFN: plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 5 × 5 × 0.85 mm	n/a
LPC1112FHI33/202	HVQFN33	HVQFN: plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 5 × 5 × 0.85 mm	n/a
LPC1112FHI33/203	HVQFN33	HVQFN: plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 5 × 5 × 0.85 mm	n/a
LPC1112JHI33/203	HVQFN33	HVQFN: plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 5 × 5 × 0.85 mm	n/a
LPC1112FHN33/103	HVQFN33	HVQFN: plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 7 × 7 × 0.85 mm	n/a
LPC1112JHN33/103	HVQFN33	HVQFN: plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 7 × 7 × 0.85 mm	n/a
LPC1112JHN33/203	HVQFN33	HVQFN: plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 7 × 7 × 0.85 mm	n/a
LPC1112FHN33/203	HVQFN33	HVQFN: plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 7 × 7 × 0.85 mm	n/a
LPC1113FHN33/201	HVQFN33	HVQFN: plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 7 × 7 × 0.85 mm	n/a
LPC1113FHN33/202	HVQFN33	HVQFN: plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 7 × 7 × 0.85 mm	n/a
LPC1113FHN33/203	HVQFN33	HVQFN: plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 7 × 7 × 0.85 mm	n/a
LPC1113JHN33/203	HVQFN33	HVQFN: plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 7 × 7 × 0.85 mm	n/a
LPC1113FHN33/301	HVQFN33	HVQFN: plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 7 × 7 × 0.85 mm	n/a
LPC1113FHN33/302	HVQFN33	HVQFN: plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 7 × 7 × 0.85 mm	n/a
LPC1113FHN33/303	HVQFN33	HVQFN: plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 7 × 7 × 0.85 mm	n/a
LPC1113JHN33/303	HVQFN33	HVQFN: plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 7 × 7 × 0.85 mm	n/a
LPC1114FHN33/201	HVQFN33	HVQFN: plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 7 × 7 × 0.85 mm	n/a
LPC1114FHN33/202	HVQFN33	HVQFN: plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 7 × 7 × 0.85 mm	n/a
LPC1114FHN33/301	HVQFN33	HVQFN: plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 7 × 7 × 0.85 mm	n/a
LPC1114FHN33/302	HVQFN33	HVQFN: plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 7 × 7 × 0.85 mm	n/a

Table 1. Ordering information ...continued

Type number	Package		Version
	Name	Description	
LPC1114FHI33/302	HVQFN33	HVQFN: plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 5 × 5 × 0.85 mm	n/a
LPC1114FHI33/303	HVQFN33	HVQFN: plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 5 × 5 × 0.85 mm	n/a
LPC1114JHI33/303	HVQFN33	HVQFN: plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 5 × 5 × 0.85 mm	n/a
LPC1114FHN33/203	HVQFN33	HVQFN: plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 7 × 7 × 0.85 mm	n/a
LPC1114JHN33/203	HVQFN33	HVQFN: plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 7 × 7 × 0.85 mm	n/a
LPC1114FHN33/303	HVQFN33	HVQFN: plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 7 × 7 × 0.85 mm	n/a
LPC1114JHN33/303	HVQFN33	HVQFN: plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 7 × 7 × 0.85 mm	n/a
LPC1114FHN33/333	HVQFN33	HVQFN: plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 7 × 7 × 0.85 mm	n/a
LPC1114JHN33/333	HVQFN33	HVQFN: plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 7 × 7 × 0.85 mm	n/a
LPC1113FBD48/301	LQFP48	LQFP48: plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2
LPC1113FBD48/302	LQFP48	LQFP48: plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2
LPC1113FBD48/303	LQFP48	LQFP48: plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2
LPC1113JBD48/303	LQFP48	LQFP48: plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2
LPC1114FBD48/301	LQFP48	LQFP48: plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2
LPC1114FBD48/302	LQFP48	LQFP48: plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2
LPC1114FBD48/303	LQFP48	LQFP48: plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2
LPC1114JBD48/303	LQFP48	LQFP48: plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2
LPC1114FBD48/323	LQFP48	LQFP48: plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2
LPC1114JBD48/323	LQFP48	LQFP48: plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2
LPC1114FBD48/333	LQFP48	LQFP48: plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2
LPC1114JBD48/333	LQFP48	LQFP48: plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2
LPC1115FBD48/303	LQFP48	LQFP48: plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2

Table 1. Ordering information ...continued

Type number	Package		
	Name	Description	Version
LPC1115JBD48/303	LQFP48	LQFP48: plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2
LPC1115FET48/303	TFBGA48	plastic thin fine-pitch ball grid array package; 48 balls; body 4.5 × 4.5 × 0.7 mm	SOT1155-2
LPC1115JET48/303	TFBGA48	plastic thin fine-pitch ball grid array package; 48 balls; body 4.5 × 4.5 × 0.7 mm	SOT1155-2

4.1 Ordering options

Table 2. Ordering options

Type number	Series	Flash	Total SRAM	Power profiles	UART	I ² C/Fast+	SPI	ADC channel	GPIO	Package	Temp ^[1]
LPC1110											
LPC1110FD20	LPC1100L	4 kB	1 kB	yes	1	1	1	5	16	SO20	F
LPC1111											
LPC1111FDH20/002	LPC1100L	8 kB	2 kB	yes	1	1	1	5	16	TSSOP20	F
LPC1111FHN33/101	LPC1100	8 kB	2 kB	no	1	1	1	8	28	HVQFN33	F
LPC1111FHN33/102	LPC1100L	8 kB	2 kB	yes	1	1	1	8	28	HVQFN33	F
LPC1111FHN33/103	LPC1100XL	8 kB	2 kB	yes	1	1	2	8	28	HVQFN33	F
LPC1111JHN33/103	LPC1100XL	8 kB	2 kB	yes	1	1	2	8	28	HVQFN33	J
LPC1111FHN33/201	LPC1100	8 kB	4 kB	no	1	1	1	8	28	HVQFN33	F
LPC1111FHN33/202	LPC1100L	8 kB	4 kB	yes	1	1	1	8	28	HVQFN33	F
LPC1111FHN33/203	LPC1100XL	8 kB	4 kB	yes	1	1	2	8	28	HVQFN33	F
LPC1111JHN33/203	LPC1100XL	8 kB	4 kB	yes	1	1	2	8	28	HVQFN33	J
LPC1112											
LPC1112FD20/102	LPC1100L	16 kB	4 kB	yes	1	1	1	5	16	SO20	F
LPC1112FDH20/102	LPC1100L	16 kB	4 kB	yes	1	-	1	5	14	TSSOP20	F
LPC1112FDH28/102	LPC1100L	16 kB	4 kB	yes	1	1	1	6	22	TSSOP28	F
LPC1112FHN24/202	LPC1100L	16 kB	4 kB	yes	1	1	1	6	19	HVQFN24	F
LPC1112FHN33/101	LPC1100	16 kB	2 kB	no	1	1	1	8	28	HVQFN33	F
LPC1112FHN33/102	LPC1100L	16 kB	2 kB	yes	1	1	1	8	28	HVQFN33	F
LPC1112FHN33/103	LPC1100XL	16 kB	2 kB	yes	1	1	2	8	28	HVQFN33	F
LPC1112JHN33/103	LPC1100XL	16 kB	2 kB	yes	1	1	2	8	28	HVQFN33	J
LPC1112FHN33/201	LPC1100	16 kB	4 kB	no	1	1	1	8	28	HVQFN33	F
LPC1112FHN33/202	LPC1100L	16 kB	4 kB	yes	1	1	1	8	28	HVQFN33	F
LPC1112FHN33/203	LPC1100XL	16 kB	4 kB	yes	1	1	2	8	28	HVQFN33	F
LPC1112JHN33/203	LPC1100XL	16 kB	4 kB	yes	1	1	2	8	28	HVQFN33	J
LPC1112FHI33/102	LPC1100L	16 kB	2 kB	yes	1	1	1	8	28	HVQFN33	F
LPC1112FHI33/202	LPC1100L	16 kB	4 kB	yes	1	1	1	8	28	HVQFN33	F
LPC1112FHI33/203	LPC1100XL	16 kB	4 kB	yes	1	1	2	8	28	HVQFN33	F
LPC1112JHI33/203	LPC1100XL	16 kB	4 kB	yes	1	1	2	8	28	HVQFN33	J

Table 2. Ordering options ...continued

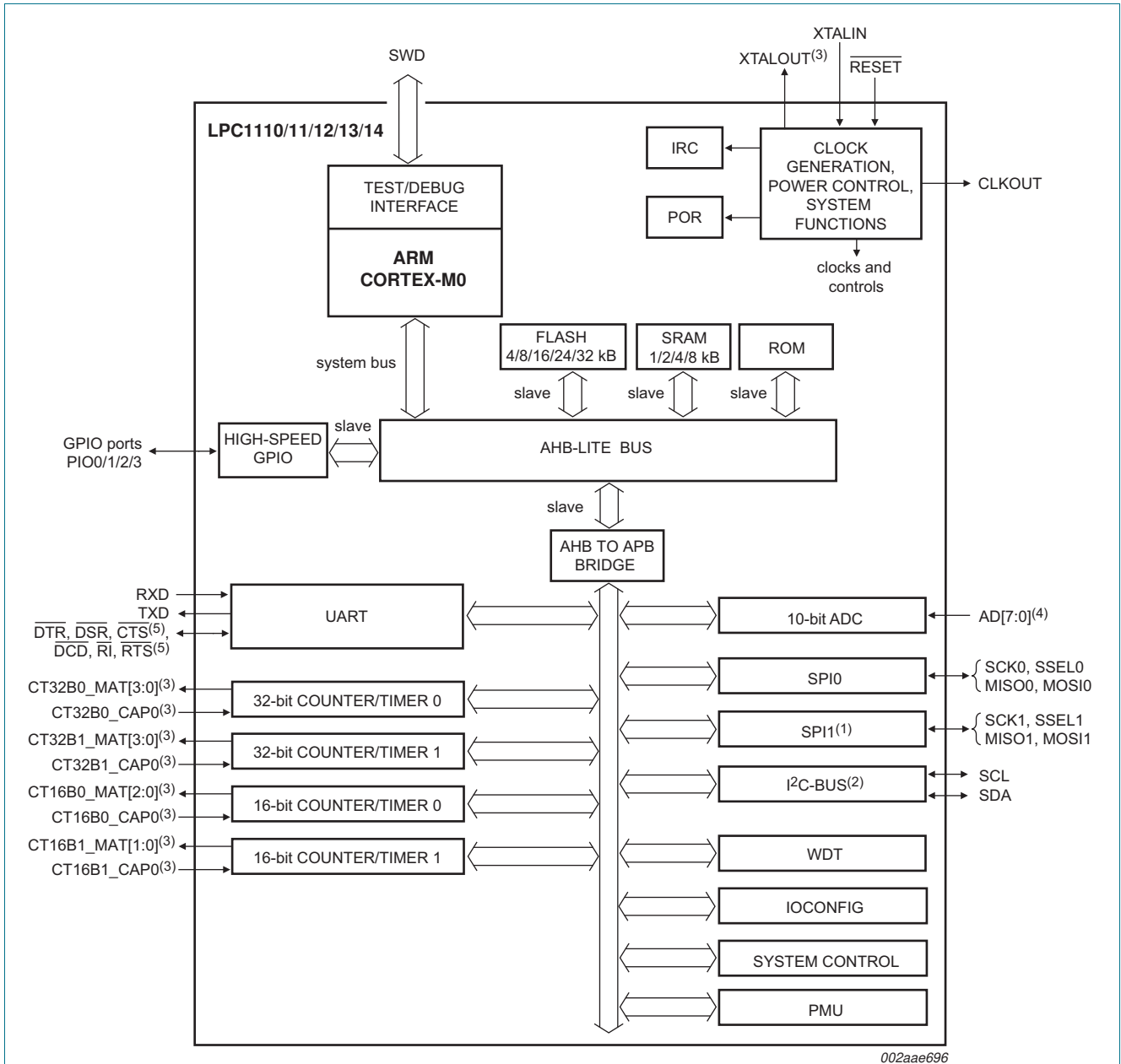
Type number	Series	Flash	Total SRAM	Power profiles	UART	I ² C/ Fast+	SPI	ADC channel	GPIO	Package	Temp ^[1]
LPC1113											
LPC1113FHN33/201	LPC1100	24 kB	4 kB	no	1	1	1	8	28	HVQFN33	F
LPC1113FHN33/202	LPC1100L	24 kB	4 kB	yes	1	1	1	8	28	HVQFN33	F
LPC1113FHN33/203	LPC1100XL	24 kB	4 kB	yes	1	1	2	8	28	HVQFN33	F
LPC1113JHN33/203	LPC1100XL	24 kB	4 kB	yes	1	1	2	8	28	HVQFN33	J
LPC1113FHN33/301	LPC1100	24 kB	8 kB	no	1	1	1	8	28	HVQFN33	F
LPC1113FHN33/302	LPC1100L	24 kB	8 kB	yes	1	1	1	8	28	HVQFN33	F
LPC1113FHN33/303	LPC1100XL	24 kB	8 kB	yes	1	1	2	8	28	HVQFN33	F
LPC1113JHN33/303	LPC1100XL	24 kB	8 kB	yes	1	1	2	8	28	HVQFN33	J
LPC1113FBD48/301	LPC1100	24 kB	8 kB	no	1	1	2	8	42	LQFP48	F
LPC1113FBD48/302	LPC1100L	24 kB	8 kB	yes	1	1	2	8	42	LQFP48	F
LPC1113FBD48/303	LPC1100XL	24 kB	8 kB	yes	1	1	2	8	42	LQFP48	F
LPC1113JBD48/303	LPC1100XL	24 kB	8 kB	yes	1	1	2	8	42	LQFP48	J
LPC1114											
LPC1114FDH28/102	LPC1100L	32 kB	4 kB	yes	1	1	1	6	22	TSSOP28	F
LPC1114FN28/102	LPC1100L	32 kB	4 kB	yes	1	1	1	6	22	DIP28	F
LPC1114FHN33/201	LPC1100	32 kB	4 kB	no	1	1	1	8	28	HVQFN33	F
LPC1114FHN33/202	LPC1100L	32 kB	4 kB	yes	1	1	1	8	28	HVQFN33	F
LPC1114FHN33/203	LPC1100XL	32 kB	4 kB	yes	1	1	2	8	28	HVQFN33	F
LPC1114JHN33/203	LPC1100XL	32 kB	4 kB	yes	1	1	2	8	28	HVQFN33	J
LPC1114FHN33/301	LPC1100	32 kB	8 kB	no	1	1	1	8	28	HVQFN33	F
LPC1114FHN33/302	LPC1100L	32 kB	8 kB	yes	1	1	1	8	28	HVQFN33	F
LPC1114FHN33/303	LPC1100XL	32 kB	8 kB	yes	1	1	2	8	28	HVQFN33	F
LPC1114JHN33/303	LPC1100XL	32 kB	8 kB	yes	1	1	2	8	28	HVQFN33	J
LPC1114FHN33/333	LPC1100XL	56 kB	8 kB	yes	1	1	2	8	28	HVQFN33	F
LPC1114JHN33/333	LPC1100XL	56 kB	8 kB	yes	1	1	2	8	28	HVQFN33	J
LPC1114FHI33/302	LPC1100L	32 kB	8 kB	yes	1	1	1	8	28	HVQFN33	F
LPC1114FHI33/303	LPC1100XL	32 kB	8 kB	yes	1	1	2	8	28	HVQFN33	F
LPC1114JHI33/303	LPC1100XL	32 kB	8 kB	yes	1	1	2	8	28	HVQFN33	J
LPC1114FBD48/301	LPC1100	32 kB	8 kB	no	1	1	2	8	42	LQFP48	F
LPC1114FBD48/302	LPC1100L	32 kB	8 kB	yes	1	1	2	8	42	LQFP48	F
LPC1114FBD48/303	LPC1100XL	32 kB	8 kB	yes	1	1	2	8	42	LQFP48	F
LPC1114JBD48/303	LPC1100XL	32 kB	8 kB	yes	1	1	2	8	42	LQFP48	J
LPC1114FBD48/323	LPC1100XL	48 kB	8 kB	yes	1	1	2	8	42	LQFP48	F
LPC1114JBD48/323	LPC1100XL	48 kB	8 kB	yes	1	1	2	8	42	LQFP48	J
LPC1114FBD48/333	LPC1100XL	56 kB	8 kB	yes	1	1	2	8	42	LQFP48	F
LPC1114JBD48/333	LPC1100XL	56 kB	8 kB	yes	1	1	2	8	42	LQFP48	J
LPC1115											
LPC1115FBD48/303	LPC1100XL	64 kB	8 kB	yes	1	1	2	8	42	LQFP48	F

Table 2. Ordering options ...continued

Type number	Series	Flash	Total SRAM	Power profiles	UART	I ² C/ Fast+	SPI	ADC channel	GPIO	Package	Temp ^[1]
LPC1115JBD48/303	LPC1100XL	64 kB	8 kB	yes	1	1	2	8	42	LQFP48	J
LPC1115FET48/303	LPC1100XL	64 kB	8 kB	yes	1	1	2	8	42	TFBGA48	F
LPC1115JET48/303	LPC1100XL	64 kB	8 kB	yes	1	1	2	8	42	TFBGA48	J

[1] F = -40 °C to +85 °C, J = -40 °C to +105 °C.

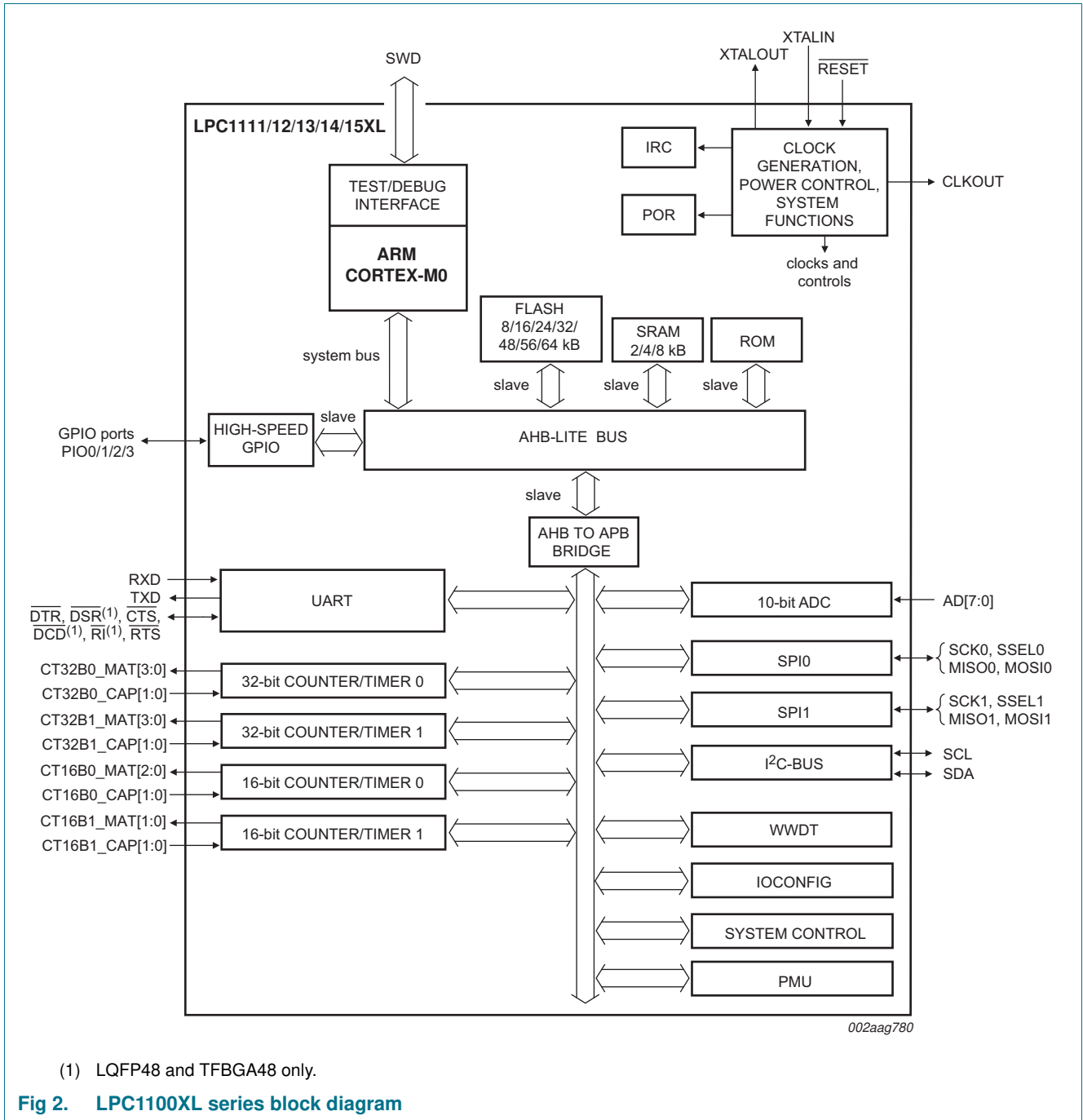
5. Block diagram



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- (1) LQFP48 packages only.
- (2) Not on LPC1112FDH20/102.
- (3) All pins available on LQFP48 and HVQFN33 packages. CT16B1_MAT1 not available on TSSOP28/DIP28 packages. CT32B1_MAT3, CT16B1_CAP0, CT16B1_MAT[1:0], CT32B0_CAP0 not available on TSSOP20/SO20 packages. CT16B1_MAT[1:0], CT32B0_CAP0 not available on the HVQFN24 package. XTALOUT not available on LPC1112FHN24.
- (4) AD[7:0] available on LQFP48 and HVQFN33 packages. AD[5:0] available on TSSOP28/DIP28 packages. AD[4:0] available on TSSOP20/SO20 packages.
- (5) All pins available on LQFP48 packages. RXD, TXD, \overline{DTR} , \overline{CTS} , \overline{RTS} available on HVQFN 33 packages. RXD, TXD, \overline{CTS} , \overline{RTS} available on TSSOP28/DIP28 packages. RXD, TXD, \overline{CTS} available on HVQFN24 packages. RXD, TXD available on TSSOP20/SO20 packages.

Fig 1. LPC1100/LPC1100L series block diagram



6. Pinning information

6.1 Pinning

Table 3. Pin description overview

Part	Pin description table	Pinning diagram
LPC1110FD20	Table 4	Figure 8
LPC1111FDH20/002	Table 4	Figure 9
LPC1112FD20/102	Table 4	Figure 10
LPC1112FDH20/102	Table 5	Figure 9
LPC1112FHN24/202	Table 6	Figure 11
LPC1112FDH28/102	Table 7	Figure 12
LPC1114FDH28/102	Table 7	Figure 13
LPC1114FN28/102	Table 7	Figure 13
LPC1111FHN33/101	Table 9	Figure 6
LPC1111FHN33/102	Table 9	Figure 6
LPC1111JHN33/103	Table 11	Figure 7
LPC1111FHN33/103	Table 11	Figure 7
LPC1111FHN33/201	Table 9	Figure 6
LPC1111FHN33/202	Table 9	Figure 6
LPC1111FHN33/203	Table 11	Figure 7
LPC1111JHN33/203	Table 11	Figure 7
LPC1112FHN33/101	Table 9	Figure 6
LPC1112FHN33/102	Table 9	Figure 6
LPC1112FHN33/103	Table 11	Figure 7
LPC1112JHN33/103	Table 11	Figure 7
LPC1112FHN33/201	Table 9	Figure 6
LPC1112FHN33/202	Table 9	Figure 6
LPC1112FHN33/203	Table 11	Figure 7
LPC1112JHN33/203	Table 11	Figure 7
LPC1112FHI33/202	Table 9	Figure 6
LPC1112FHI33/203	Table 11	Figure 7
LPC1112JHI33/203	Table 11	Figure 7
LPC1113FHN33/201	Table 9	Figure 6
LPC1113FHN33/202	Table 9	Figure 6
LPC1113FHN33/203	Table 11	Figure 7
LPC1113JHN33/203	Table 11	Figure 7
LPC1113FHN33/301	Table 9	Figure 6
LPC1113FHN33/302	Table 9	Figure 6
LPC1113FHN33/303	Table 11	Figure 7
LPC1113JHN33/303	Table 11	Figure 7
LPC1114FHN33/201	Table 9	Figure 6
LPC1114FHN33/202	Table 9	Figure 6

Table 3. Pin description overview

Part	Pin description table	Pinning diagram
LPC1114FHN33/203	Table 11	Figure 7
LPC1114JHN33/203	Table 11	Figure 7
LPC1114FHN33/301	Table 9	Figure 6
LPC1114FHN33/302	Table 9	Figure 6
LPC1114JHN33/303	Table 11	Figure 7
LPC1114FHN33/303	Table 11	Figure 7
LPC1114FHN33/333	Table 11	Figure 7
LPC1114JHN33/333	Table 11	Figure 7
LPC1114FHI33/302	Table 9	Figure 6
LPC1114FHI33/303	Table 11	Figure 7
LPC1114JHI33/303	Table 11	Figure 7
LPC1113FBD48/301	Table 8	Figure 3
LPC1113FBD48/302	Table 8	Figure 3
LPC1113FBD48/303	Table 10	Figure 4
LPC1113JBD48/303	Table 10	Figure 4
LPC1114FBD48/301	Table 8	Figure 3
LPC1114FBD48/302	Table 8	Figure 3
LPC1114FBD48/303	Table 10	Figure 4
LPC1114JBD48/303	Table 10	Figure 4
LPC1114FBD48/323	Table 10	Figure 4
LPC1114JBD48/323	Table 10	Figure 4
LPC1114FBD48/333	Table 10	Figure 4
LPC1114JBD48/333	Table 10	Figure 4
LPC1115FBD48/303	Table 10	Figure 4
LPC1115JBD48/303	Table 10	Figure 4
LPC1115FET48/303	Table 10	Figure 5
LPC1115JET48/303	Table 10	Figure 5

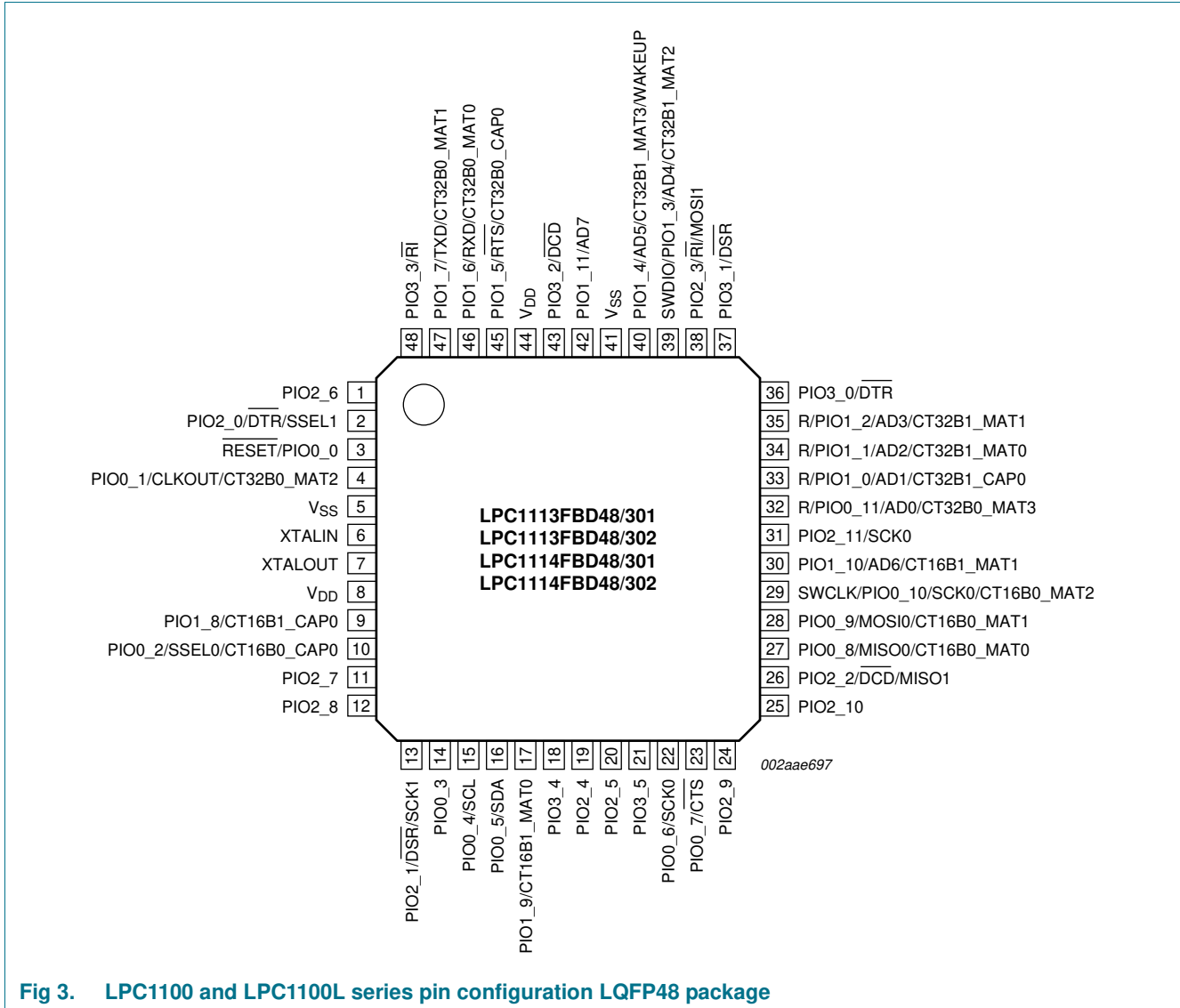


Fig 3. LPC1100 and LPC1100L series pin configuration LQFP48 package

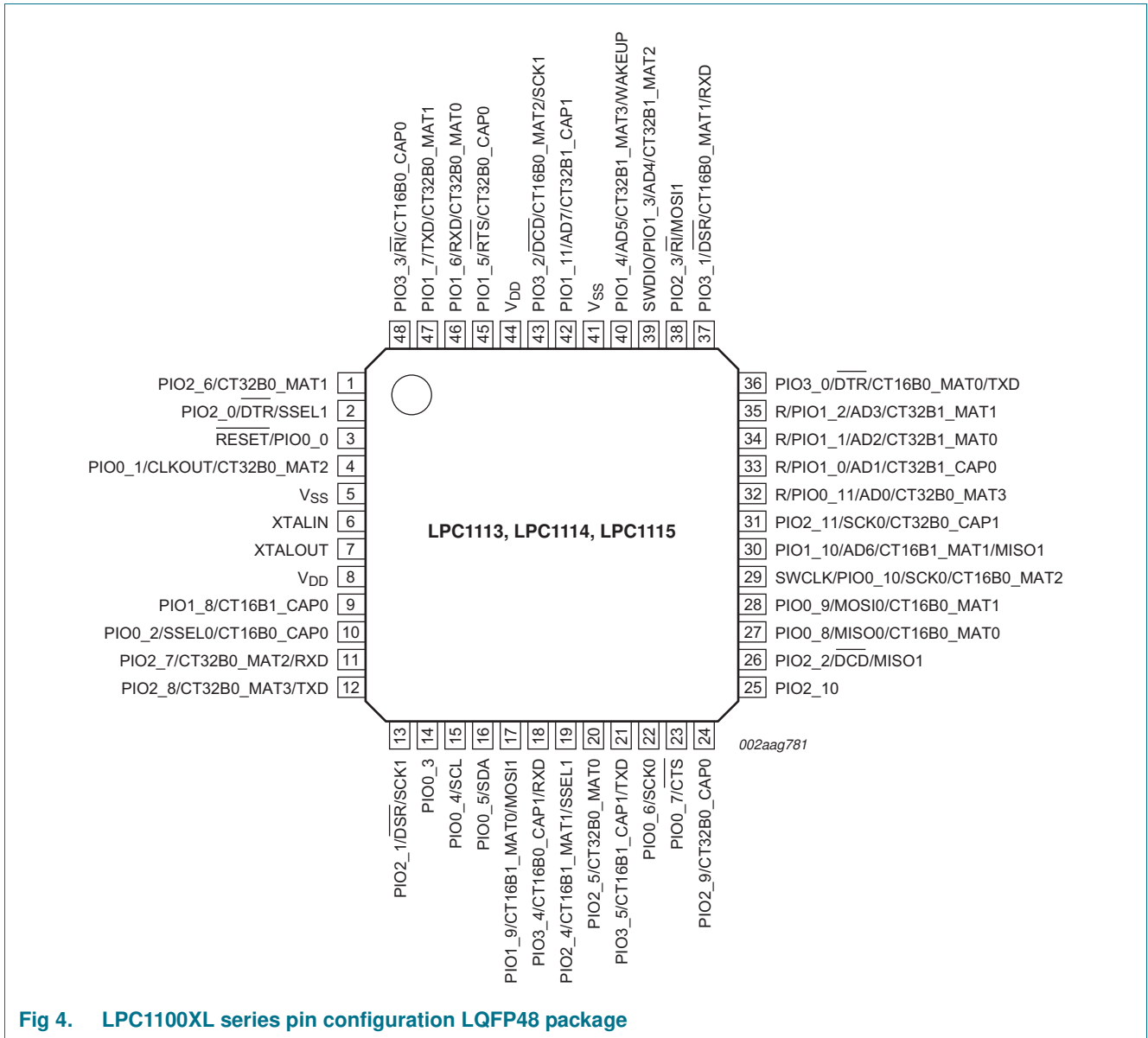


Fig 4. LPC1100XL series pin configuration LQFP48 package

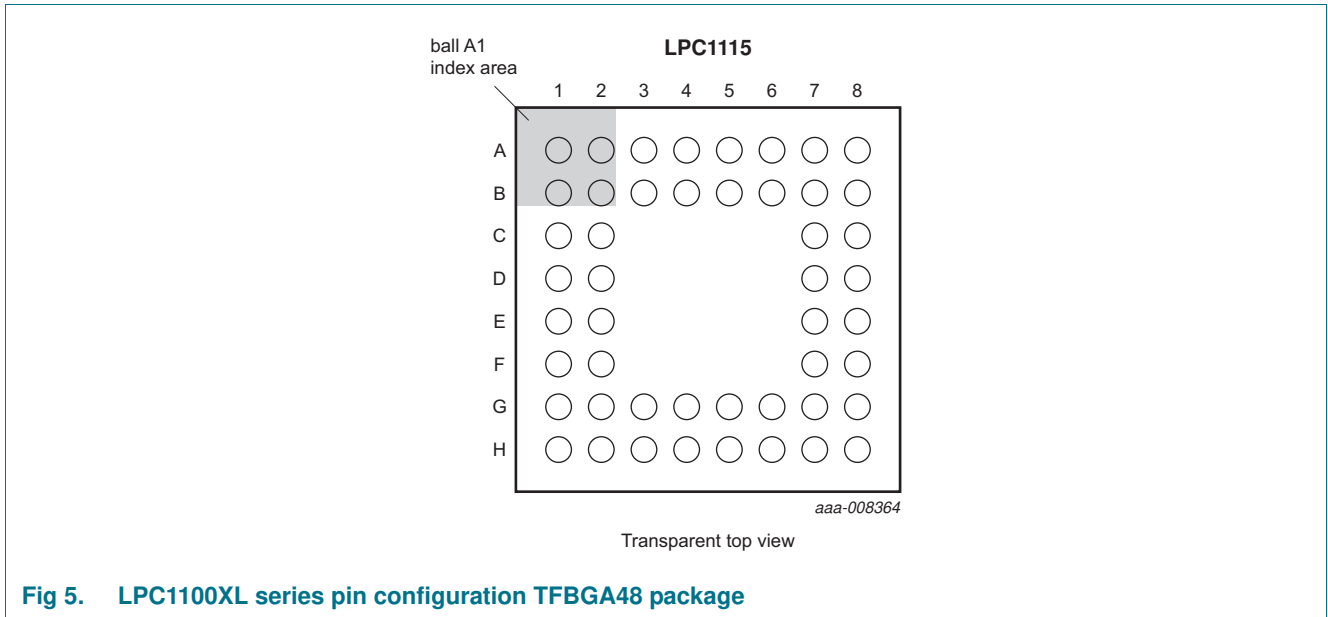


Fig 5. LPC1100XL series pin configuration TFBGA48 package

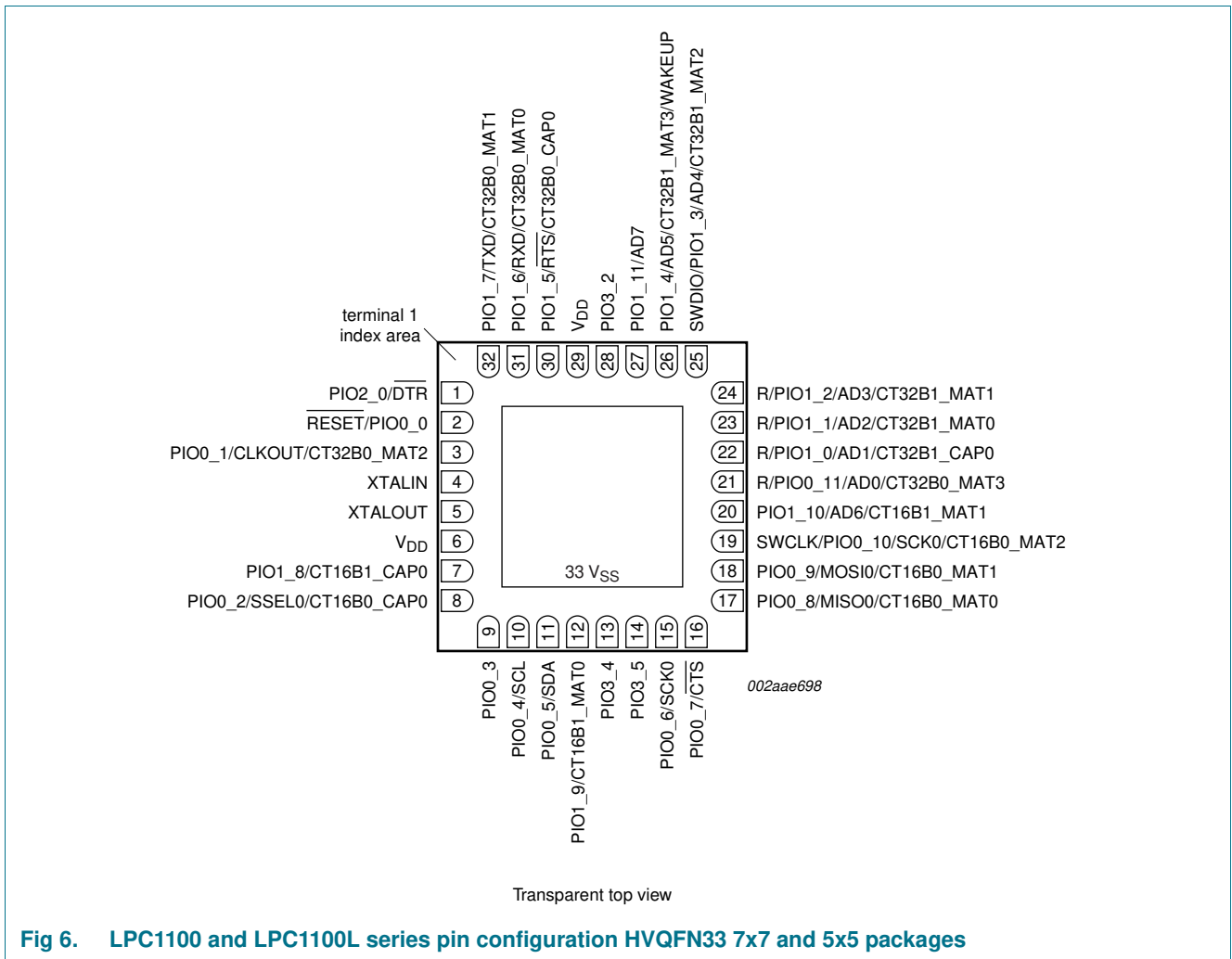


Fig 6. LPC1100 and LPC1100L series pin configuration HVQFN33 7x7 and 5x5 packages

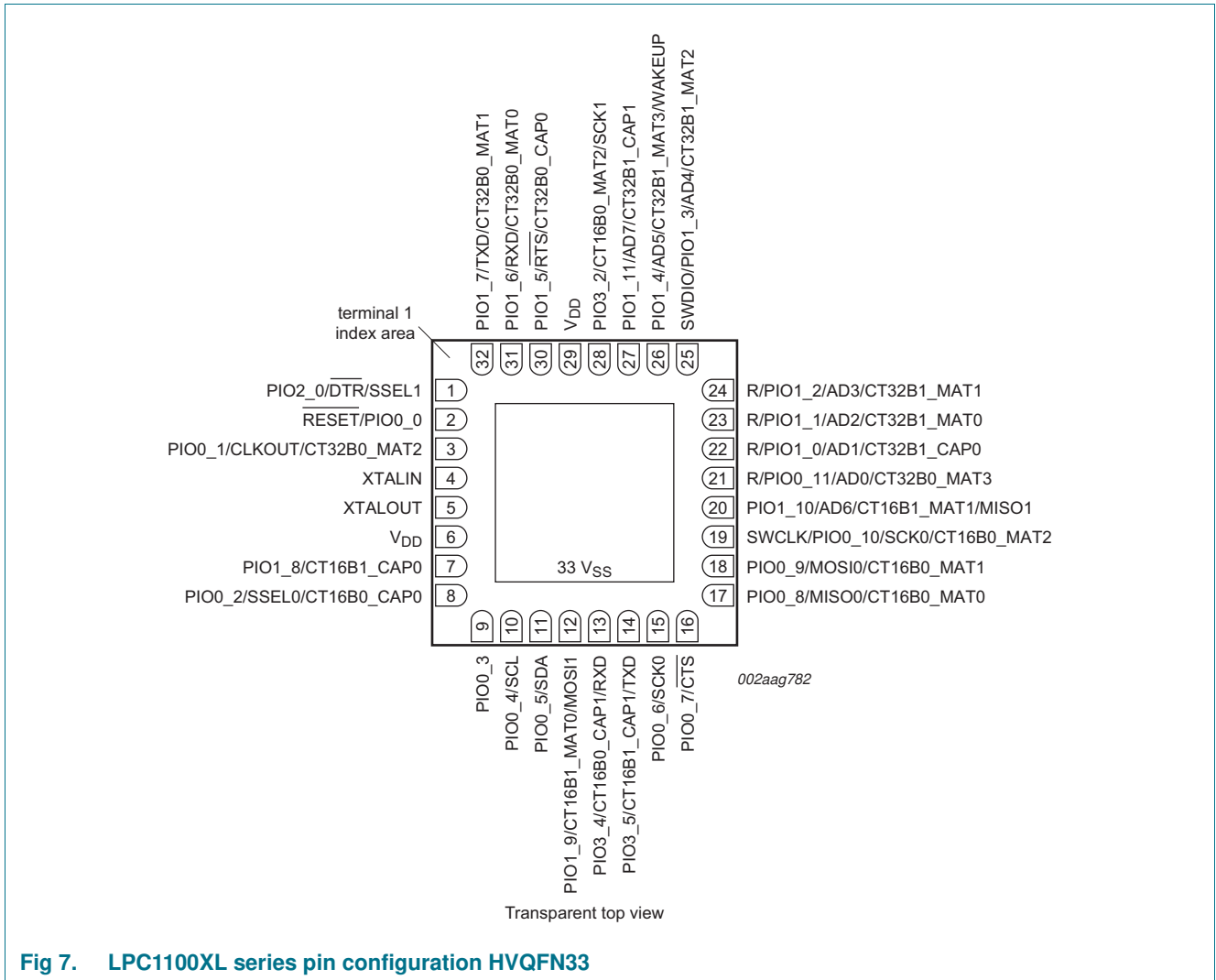


Fig 7. LPC1100XL series pin configuration HVQFN33

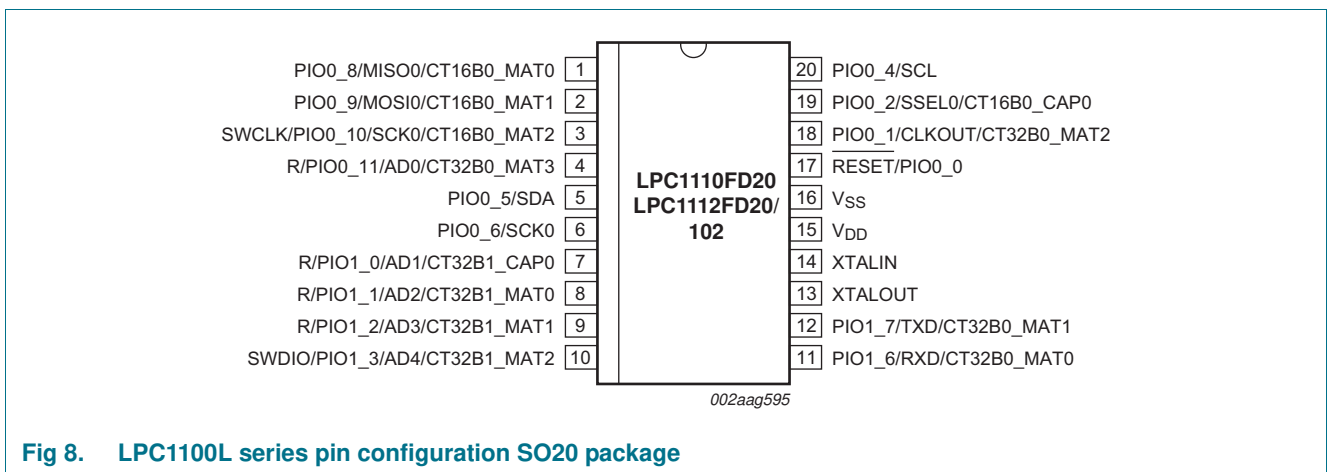
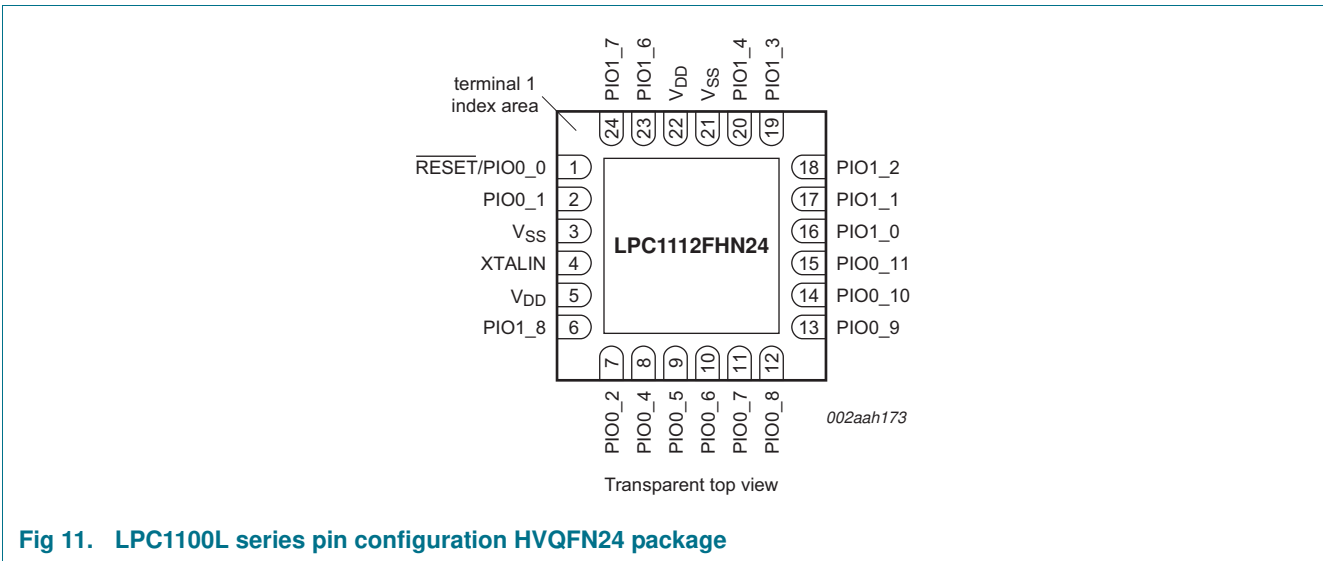
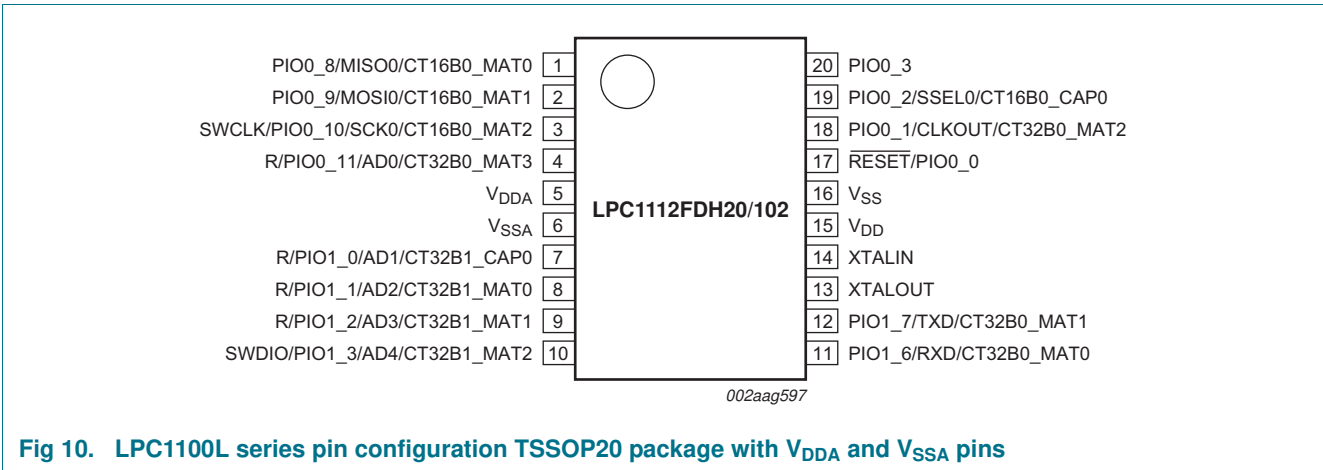
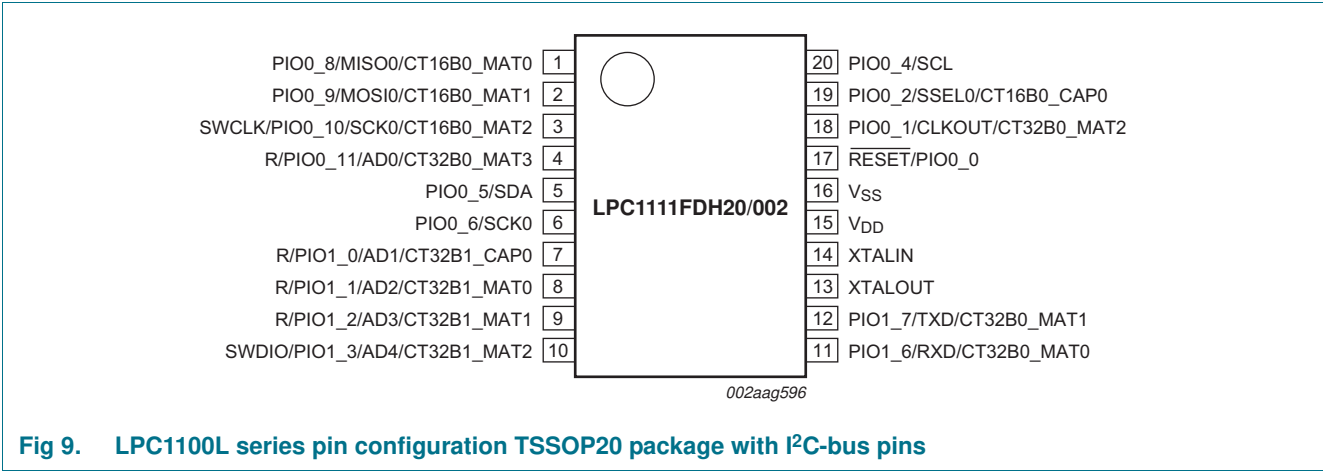


Fig 8. LPC1100L series pin configuration SO20 package



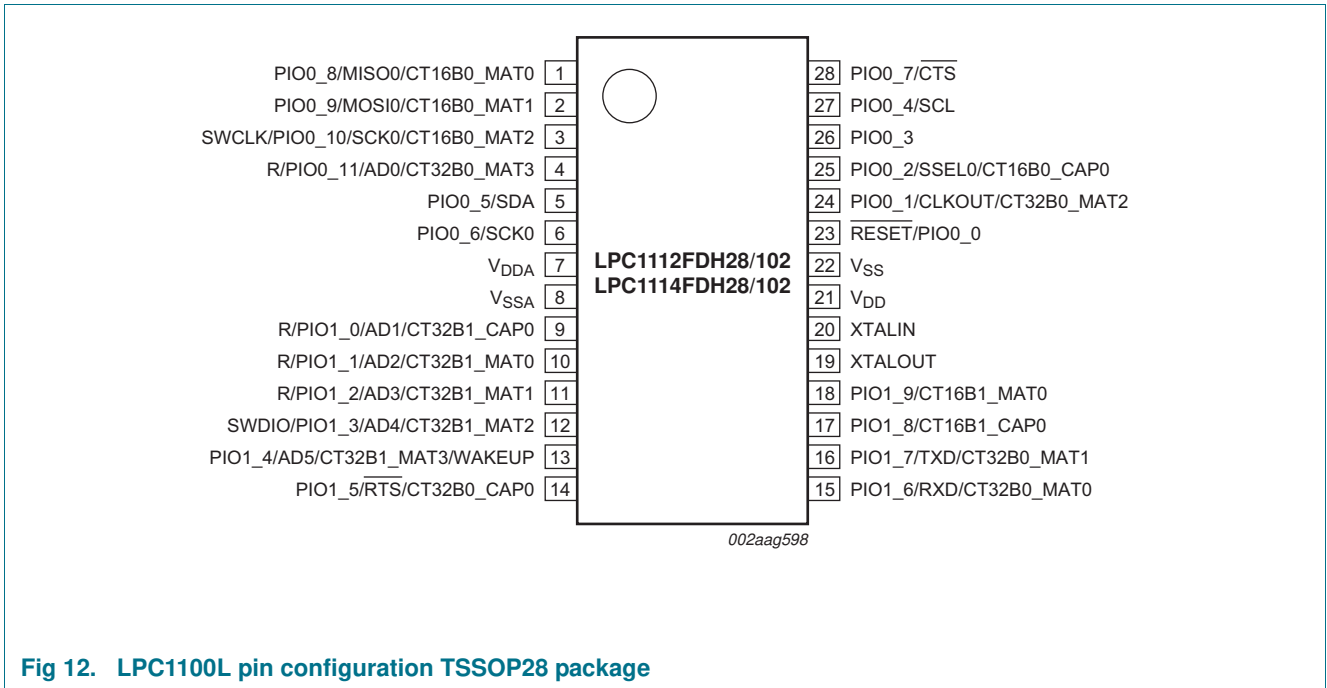


Fig 12. LPC1100L pin configuration TSSOP28 package

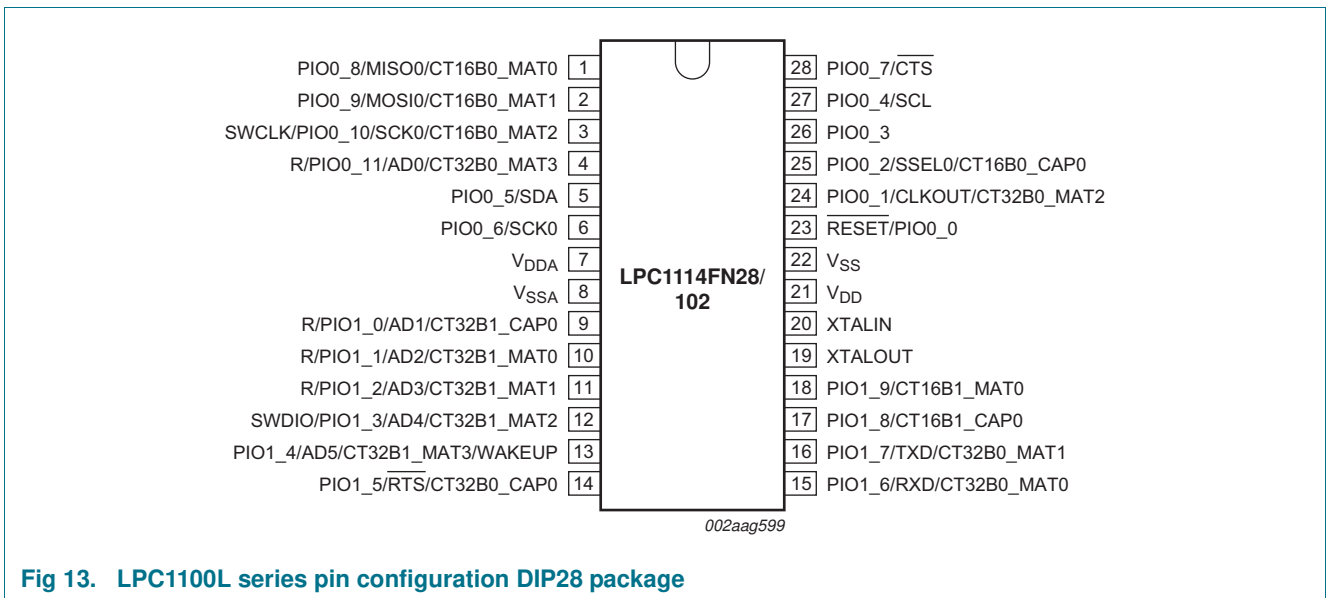


Fig 13. LPC1100L series pin configuration DIP28 package

6.2 Pin description

Table 4. LPC1100L series: LPC1110/11/12 pin description table (SO20 and TSSOP20 package with I²C-bus pins)

Symbol	Pin SO20/ TSSOP20	Start logic input	Type	Reset state [1]	Description
PIO0_0 to PIO0_11			I/O		Port 0 — Port 0 is a 12-bit I/O port with individual direction and function controls for each bit. The operation of port 0 pins depends on the function selected through the IOCONFIG register block.
RESET/PIO0_0	17	[2] yes	I	I; PU	RESET — External reset input with 20 ns glitch filter. A LOW-going pulse as short as 50 ns on this pin resets the device, causing I/O ports and peripherals to take on their default states, and processor execution to begin at address 0. In deep power-down mode, this pin must be pulled HIGH externally. The RESET pin can be left unconnected or be used as a GPIO pin if an external RESET function is not needed and Deep power-down mode is not used.
			I/O	-	PIO0_0 — General purpose digital input/output pin with 10 ns glitch filter.
PIO0_1/CLKOUT/ CT32B0_MAT2	18	[3] yes	I/O	I; PU	PIO0_1 — General purpose digital input/output pin. A LOW level on this pin during reset starts the ISP command handler.
			O	-	CLKOUT — Clockout pin.
			O	-	CT32B0_MAT2 — Match output 2 for 32-bit timer 0.
PIO0_2/SSEL0/ CT16B0_CAP0	19	[3] yes	I/O	I; PU	PIO0_2 — General purpose digital input/output pin.
			I/O	-	SSEL0 — Slave Select for SPI0.
			I	-	CT16B0_CAP0 — Capture input 0 for 16-bit timer 0.
PIO0_4/SCL	20	[4] yes	I/O	I; IA	PIO0_4 — General purpose digital input/output pin (open-drain).
			I/O	-	SCL — I ² C-bus, open-drain clock input/output. High-current sink only if I ² C Fast-mode Plus is selected in the I/O configuration register.
PIO0_5/SDA	5	[4] yes	I/O	I; IA	PIO0_5 — General purpose digital input/output pin (open-drain).
			I/O	-	SDA — I ² C-bus, open-drain data input/output. High-current sink only if I ² C Fast-mode Plus is selected in the I/O configuration register.
PIO0_6/SCK0	6	[3] yes	I/O	I; PU	PIO0_6 — General purpose digital input/output pin.
			I/O	-	SCK0 — Serial clock for SPI0.
PIO0_8/MISO0/ CT16B0_MAT0	1	[3] yes	I/O	I; PU	PIO0_8 — General purpose digital input/output pin.
			I/O	-	MISO0 — Master In Slave Out for SPI0.
			O	-	CT16B0_MAT0 — Match output 0 for 16-bit timer 0.
PIO0_9/MOSI0/ CT16B0_MAT1	2	[3] yes	I/O	I; PU	PIO0_9 — General purpose digital input/output pin.
			I/O	-	MOSI0 — Master Out Slave In for SPI0.
			O	-	CT16B0_MAT1 — Match output 1 for 16-bit timer 0.
SWCLK/PIO0_10/ SCK0/ CT16B0_MAT2	3	[3] yes	I	I; PU	SWCLK — Serial wire clock.
			I/O	-	PIO0_10 — General purpose digital input/output pin.
			I/O	-	SCK0 — Serial clock for SPI0.
			O	-	CT16B0_MAT2 — Match output 2 for 16-bit timer 0.

Table 4. LPC1100L series: LPC1110/11/12 pin description table (SO20 and TSSOP20 package with I²C-bus pins) ...continued

Symbol	Pin SO20/ TSSOP20	Start logic input	Type	Reset state [1]	Description
R/PIO0_11/ AD0/CT32B0_MAT3	4	[5] yes	I	I; PU	R — Reserved. Configure for an alternate function in the IOCONFIG block.
			I/O	-	PIO0_11 — General purpose digital input/output pin.
			I	-	AD0 — A/D converter, input 0.
			O	-	CT32B0_MAT3 — Match output 3 for 32-bit timer 0.
PIO1_0 to PIO1_7			I/O		Port 1 — Port 1 is a 12-bit I/O port with individual direction and function controls for each bit. The operation of port 1 pins depends on the function selected through the IOCONFIG register block.
R/PIO1_0/ AD1/CT32B1_CAP0	7	[5] yes	I	I; PU	R — Reserved. Configure for an alternate function in the IOCONFIG block.
			I/O	-	PIO1_0 — General purpose digital input/output pin.
			I	-	AD1 — A/D converter, input 1.
			I	-	CT32B1_CAP0 — Capture input 0 for 32-bit timer 1.
R/PIO1_1/ AD2/CT32B1_MAT0	8	[5] no	O	I; PU	R — Reserved. Configure for an alternate function in the IOCONFIG block.
			I/O	-	PIO1_1 — General purpose digital input/output pin.
			I	-	AD2 — A/D converter, input 2.
			O	-	CT32B1_MAT0 — Match output 0 for 32-bit timer 1.
R/PIO1_2/ AD3/CT32B1_MAT1	9	[5] no	I	I; PU	R — Reserved. Configure for an alternate function in the IOCONFIG block.
			I/O	-	PIO1_2 — General purpose digital input/output pin.
			I	-	AD3 — A/D converter, input 3.
			O	-	CT32B1_MAT1 — Match output 1 for 32-bit timer 1.
SWDIO/PIO1_3/ AD4/CT32B1_MAT2	10	[5] no	I/O	I; PU	SWDIO — Serial wire debug input/output.
			I/O	-	PIO1_3 — General purpose digital input/output pin.
			I	-	AD4 — A/D converter, input 4.
			O	-	CT32B1_MAT2 — Match output 2 for 32-bit timer 1.
PIO1_6/RXD/ CT32B0_MAT0	11	[3] no	I/O	I; PU	PIO1_6 — General purpose digital input/output pin.
			I	-	RXD — Receiver input for UART.
			O	-	CT32B0_MAT0 — Match output 0 for 32-bit timer 0.
PIO1_7/TXD/ CT32B0_MAT1	12	[3] no	I/O	I; PU	PIO1_7 — General purpose digital input/output pin.
			O	-	TXD — Transmitter output for UART.
			O	-	CT32B0_MAT1 — Match output 1 for 32-bit timer 0.
V _{DD}	15	-		-	3.3 V supply voltage to the internal regulator, the external rail, and the ADC. Also used as the ADC reference voltage.
XTALIN	14	[6] -	I	-	Input to the oscillator circuit and internal clock generator circuits. Input voltage must not exceed 1.8 V.
XTALOUT	13	[6] -	O	-	Output from the oscillator amplifier.
V _{SS}	16	-		-	Ground.

- [1] Pin state at reset for default function: I = Input; O = Output; PU = internal pull-up enabled (pins pulled up to full V_{DD} level); IA = inactive, no pull-up/down enabled.
- [2] 5 V tolerant pad. $\overline{\text{RESET}}$ functionality is not available in Deep power-down mode.
- [3] 5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors and configurable hysteresis (see [Figure 51](#)).
- [4] I²C-bus pin compliant with the I²C-bus specification for I²C standard mode and I²C Fast-mode Plus. The pin requires an external pull-up to provide output functionality. When power is switched off, this pin is floating and does not disturb the I²C lines. Open-drain configuration applies to all functions on this pin.
- [5] 5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors, configurable hysteresis, and analog input. When configured as a ADC input, digital section of the pad is disabled and the pin is not 5 V tolerant (see [Figure 51](#)).
- [6] When the system oscillator is not used, connect XTALIN and XTALOUT as follows: XTALIN can be left floating or can be grounded (grounding is preferred to reduce susceptibility to noise). XTALOUT should be left floating.

Table 5. LPC1100L series: LPC1112 pin description table (TSSOP20 with V_{DDA} and V_{SSA} pins)

Symbol	Pin TSSOP20	Start logic input	Type	Reset state [1]	Description
PIO0_0 to PIO0_11			I/O		Port 0 — Port 0 is a 12-bit I/O port with individual direction and function controls for each bit. The operation of port 0 pins depends on the function selected through the IOCONFIG register block.
$\overline{\text{RESET}}$ /PIO0_0	17 [2]	yes	I	I; PU	RESET — External reset input with 20 ns glitch filter. A LOW-going pulse as short as 50 ns on this pin resets the device, causing I/O ports and peripherals to take on their default states, and processor execution to begin at address 0. In deep power-down mode, this pin must be pulled HIGH externally. The $\overline{\text{RESET}}$ pin can be left unconnected or be used as a GPIO pin if an external $\overline{\text{RESET}}$ function is not needed and Deep power-down mode is not used.
			I/O	-	PIO0_0 — General purpose digital input/output pin with 10 ns glitch filter.
PIO0_1/CLKOUT/ CT32B0_MAT2	18 [3]	yes	I/O	I; PU	PIO0_1 — General purpose digital input/output pin. A LOW level on this pin during reset starts the ISP command handler.
			O	-	CLKOUT — Clockout pin.
			O	-	CT32B0_MAT2 — Match output 2 for 32-bit timer 0.
PIO0_2/SSEL0/ CT16B0_CAP0	19 [3]	yes	I/O	I; PU	PIO0_2 — General purpose digital input/output pin.
			I/O	-	SSEL0 — Slave Select for SPI0.
			I	-	CT16B0_CAP0 — Capture input 0 for 16-bit timer 0.
PIO0_3	20 [3]	yes	I/O	I; PU	PIO0_3 — General purpose digital input/output pin.
PIO0_8/MISO0/ CT16B0_MAT0	1 [3]	yes	I/O	I; PU	PIO0_8 — General purpose digital input/output pin.
			I/O	-	MISO0 — Master In Slave Out for SPI0.
			O	-	CT16B0_MAT0 — Match output 0 for 16-bit timer 0.
PIO0_9/MOSI0/ CT16B0_MAT1	2 [3]	yes	I/O	I; PU	PIO0_9 — General purpose digital input/output pin.
			I/O	-	MOSI0 — Master Out Slave In for SPI0.
			O	-	CT16B0_MAT1 — Match output 1 for 16-bit timer 0.

Table 5. LPC1100L series: LPC1112 pin description table (TSSOP20 with V_{DDA} and V_{SSA} pins) ...continued

Symbol	Pin TSSOP20		Start logic input	Type	Reset state [1]	Description
SWCLK/PIO0_10/ SCK0/ CT16B0_MAT2	3	[3]	yes	I	I; PU	SWCLK — Serial wire clock.
				I/O	-	PIO0_10 — General purpose digital input/output pin.
				I/O	-	SCK0 — Serial clock for SPI0.
				O	-	CT16B0_MAT2 — Match output 2 for 16-bit timer 0.
R/PIO0_11/ AD0/CT32B0_MAT3	4	[4]	yes	I	I; PU	R — Reserved. Configure for an alternate function in the IOCONFIG block.
				I/O	-	PIO0_11 — General purpose digital input/output pin.
				I	-	AD0 — A/D converter, input 0.
				O	-	CT32B0_MAT3 — Match output 3 for 32-bit timer 0.
PIO1_0 to PIO1_7				I/O		Port 1 — Port 1 is a 12-bit I/O port with individual direction and function controls for each bit. The operation of port 1 pins depends on the function selected through the IOCONFIG register block.
R/PIO1_0/ AD1/CT32B1_CAP0	7	[4]	yes	I	I; PU	R — Reserved. Configure for an alternate function in the IOCONFIG block.
				I/O	-	PIO1_0 — General purpose digital input/output pin.
				I	-	AD1 — A/D converter, input 1.
				I	-	CT32B1_CAP0 — Capture input 0 for 32-bit timer 1.
R/PIO1_1/ AD2/CT32B1_MAT0	8	[4]	no	O	I; PU	R — Reserved. Configure for an alternate function in the IOCONFIG block.
				I/O	-	PIO1_1 — General purpose digital input/output pin.
				I	-	AD2 — A/D converter, input 2.
				O	-	CT32B1_MAT0 — Match output 0 for 32-bit timer 1.
R/PIO1_2/ AD3/CT32B1_MAT1	9	[4]	no	I	I; PU	R — Reserved. Configure for an alternate function in the IOCONFIG block.
				I/O	-	PIO1_2 — General purpose digital input/output pin.
				I	-	AD3 — A/D converter, input 3.
				O	-	CT32B1_MAT1 — Match output 1 for 32-bit timer 1.
SWDIO/PIO1_3/ AD4/CT32B1_MAT2	10	[4]	no	I/O	I; PU	SWDIO — Serial wire debug input/output.
				I/O	-	PIO1_3 — General purpose digital input/output pin.
				I	-	AD4 — A/D converter, input 4.
				O	-	CT32B1_MAT2 — Match output 2 for 32-bit timer 1.
PIO1_6/RXD/ CT32B0_MAT0	11	[3]	no	I/O	I; PU	PIO1_6 — General purpose digital input/output pin.
				I	-	RXD — Receiver input for UART.
				O	-	CT32B0_MAT0 — Match output 0 for 32-bit timer 0.
PIO1_7/TXD/ CT32B0_MAT1	12	[3]	no	I/O	I; PU	PIO1_7 — General purpose digital input/output pin.
				O	-	TXD — Transmitter output for UART.
				O	-	CT32B0_MAT1 — Match output 1 for 32-bit timer 0.
V _{DD}	15	-	-	I	-	3.3 V supply voltage to the internal regulator and the external rail.

Table 5. LPC1100L series: LPC1112 pin description table (TSSOP20 with V_{DDA} and V_{SSA} pins) ...continued

Symbol	Pin TSSOP20	Start logic input	Type	Reset state [1]	Description
V _{DDA}	5	-	I	-	3.3 V supply voltage to the ADC. Also used as the ADC reference voltage.
XTALIN	14 [5]	-	I	-	Input to the oscillator circuit and internal clock generator circuits. Input voltage must not exceed 1.8 V.
XTALOUT	13 [5]	-	O	-	Output from the oscillator amplifier.
V _{SS}	16	-	I	-	Ground.
V _{SSA}	6	-	I	-	Analog ground.

- [1] Pin state at reset for default function: I = Input; O = Output; PU = internal pull-up enabled (pins pulled up to full V_{DD} level); IA = inactive, no pull-up/down enabled.
- [2] 5 V tolerant pad. $\overline{\text{RESET}}$ functionality is not available in Deep power-down mode.
- [3] 5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors and configurable hysteresis (see Figure 51).
- [4] 5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors, configurable hysteresis, and analog input. When configured as a ADC input, digital section of the pad is disabled and the pin is not 5 V tolerant (see Figure 51).
- [5] When the system oscillator is not used, connect XTALIN and XTALOUT as follows: XTALIN can be left floating or can be grounded (grounding is preferred to reduce susceptibility to noise). XTALOUT should be left floating.

Table 6. LPC1100L series: LPC1112 (HVQFN24 package)

Symbol	HVQFN pin	Start logic input	Type	Reset state [1]	Description
$\overline{\text{RESET}}$ /PIO0_0	1[2]	yes	I	I; PU	RESET — External reset input with 20 ns glitch filter. A LOW-going pulse as short as 50 ns on this pin resets the device, causing I/O ports and peripherals to take on their default states, and processor execution to begin at address 0. In deep power-down mode, this pin must be pulled HIGH externally. The $\overline{\text{RESET}}$ pin can be left unconnected or be used as a GPIO pin if an external $\overline{\text{RESET}}$ function is not needed and Deep power-down mode is not used.
			I/O	-	PIO0_0 — General purpose digital input/output pin with 10 ns glitch filter.
PIO0_1/CLKOUT/CT32B0_MAT2	2[3]	yes	I/O	I; PU	PIO0_1 — General purpose digital input/output pin. A LOW level on this pin during reset starts the ISP command handler.
			O	-	CLKOUT — Clockout pin.
			O	-	CT32B0_MAT2 — Match output 2 for 32-bit timer 0.
PIO0_2/SSEL0/CT16B0_CAP0	7[3]	yes	I/O	I; PU	PIO0_2 — General purpose digital input/output pin.
			I/O	-	SSEL0 — Slave Select for SPI0.
			I	-	CT16B0_CAP0 — Capture input 0 for 16-bit timer 0.
PIO0_4/SCL	8[4]	yes	I/O	I; IA	PIO0_4 — General purpose digital input/output pin (open-drain).
			I/O	-	SCL — I ² C-bus, open-drain clock input/output. High-current sink only if I ² C Fast-mode Plus is selected in the I/O configuration register.

Table 6. LPC1100L series: LPC1112 (HVQFN24 package) ...continued

Symbol	HVQFN pin	Start logic input	Type	Reset state U	Description
PIO0_5/SDA	9 ^[4]	yes	I/O	I; IA	PIO0_5 — General purpose digital input/output pin (open-drain).
			I/O	-	SDA — I ² C-bus, open-drain data input/output. High-current sink only if I ² C Fast-mode Plus is selected in the I/O configuration register.
PIO0_6/SCK0	10 ^[3]	yes	I/O	I; PU	PIO0_6 — General purpose digital input/output pin.
			I/O	-	SCK0 — Serial clock for SPI0.
PIO0_7/ $\overline{\text{CTS}}$	11 ^[3]	yes	I/O	I; PU	PIO0_7 — General purpose digital input/output pin (high-current output driver).
			I	-	CTS — Clear To Send input for UART.
PIO0_8/MISO0/ CT16B0_MAT0	12 ^[3]	yes	I/O	I; PU	PIO0_8 — General purpose digital input/output pin.
			I/O	-	MISO0 — Master In Slave Out for SPI0.
			O	-	CT16B0_MAT0 — Match output 0 for 16-bit timer 0.
PIO0_9/MOSI0/ CT16B0_MAT1	13 ^[3]	yes	I/O	I; PU	PIO0_9 — General purpose digital input/output pin.
			I/O	-	MOSI0 — Master Out Slave In for SPI0.
			O	-	CT16B0_MAT1 — Match output 1 for 16-bit timer 0.
SWCLK/PIO0_10/ SCK0/ CT16B0_MAT2	14 ^[3]	yes	I	I; PU	SWCLK — Serial wire clock.
			I/O	-	PIO0_10 — General purpose digital input/output pin.
			I/O	-	SCK0 — Serial clock for SPI0.
			O	-	CT16B0_MAT2 — Match output 2 for 16-bit timer 0.
R/PIO0_11/ AD0/CT32B0_MAT3	15 ^[5]	yes	I	I; PU	R — Reserved. Configure for an alternate function in the IOCONFIG block.
			I/O	-	PIO0_11 — General purpose digital input/output pin.
			I	-	AD0 — A/D converter, input 0.
			O	-	CT32B0_MAT3 — Match output 3 for 32-bit timer 0.
R/PIO1_0/ AD1/CT32B1_CAP0	16 ^[5]	yes	I	I; PU	R — Reserved. Configure for an alternate function in the IOCONFIG block.
			I/O	-	PIO1_0 — General purpose digital input/output pin.
			I	-	AD1 — A/D converter, input 1.
			I	-	CT32B1_CAP0 — Capture input 0 for 32-bit timer 1.
R/PIO1_1/ AD2/CT32B1_MAT0	17 ^[5]	no	O	I; PU	R — Reserved. Configure for an alternate function in the IOCONFIG block.
			I/O	-	PIO1_1 — General purpose digital input/output pin.
			I	-	AD2 — A/D converter, input 2.
			O	-	CT32B1_MAT0 — Match output 0 for 32-bit timer 1.
R/PIO1_2/ AD3/CT32B1_MAT1	18 ^[5]	no	I	I; PU	R — Reserved. Configure for an alternate function in the IOCONFIG block.
			I/O	-	PIO1_2 — General purpose digital input/output pin.
			I	-	AD3 — A/D converter, input 3.
			O	-	CT32B1_MAT1 — Match output 1 for 32-bit timer 1.

Table 6. LPC1100L series: LPC1112 (HVQFN24 package) ...continued

Symbol	HVQFN pin	Start logic input	Type	Reset state [1]	Description
SWDIO/PIO1_3/ AD4/CT32B1_MAT2	19 ^[5]	no	I/O	I; PU	SWDIO — Serial wire debug input/output.
			I/O	-	PIO1_3 — General purpose digital input/output pin.
			I	-	AD4 — A/D converter, input 4.
			O	-	CT32B1_MAT2 — Match output 2 for 32-bit timer 1.
PIO1_4/AD5/ CT32B1_MAT3/ WAKEUP	20 ^[5]	no	I/O	I; PU	PIO1_4 — General purpose digital input/output pin with 10 ns glitch filter. In Deep power-down mode, this pin serves as the Deep power-down mode wake-up pin with 20 ns glitch filter. Pull this pin HIGH externally before entering Deep power-down mode. Pull this pin LOW to exit Deep power-down mode. A LOW-going pulse as short as 50 ns wakes up the part.
			I	-	AD5 — A/D converter, input 5.
			O	-	CT32B1_MAT3 — Match output 3 for 32-bit timer 1.
PIO1_6/RXD/ CT32B0_MAT0	23 ^[3]	no	I/O	I; PU	PIO1_6 — General purpose digital input/output pin.
			I	-	RXD — Receiver input for UART.
			O	-	CT32B0_MAT0 — Match output 0 for 32-bit timer 0.
PIO1_7/TXD/ CT32B0_MAT1	24 ^[3]	no	I/O	I; PU	PIO1_7 — General purpose digital input/output pin.
			O	-	TXD — Transmitter output for UART.
			O	-	CT32B0_MAT1 — Match output 1 for 32-bit timer 0.
PIO1_8/ CT16B1_CAP0	6 ^[3]	no	I/O	I; PU	PIO1_8 — General purpose digital input/output pin.
			I	-	CT16B1_CAP0 — Capture input 0 for 16-bit timer 1.
XTALIN	4 ^[6]	-	I	-	Input to the oscillator circuit and internal clock generator circuits. Input voltage must not exceed 1.8 V.
V _{DD}	5; 22	-	I	-	1.8 V supply voltage to the internal regulator, the external rail, and the ADC. Also used as the ADC reference voltage.
V _{SS}	3; 21	-	I	-	Ground.

- [1] Pin state at reset for default function: I = Input; O = Output; PU = internal pull-up enabled (pins pulled up to full V_{DD} level); IA = inactive, no pull-up/down enabled.
- [2] 5 V tolerant pad. $\overline{\text{RESET}}$ functionality is not available in Deep power-down mode. Use the WAKEUP pin to reset the chip and wake up from Deep power-down mode. An external pull-up resistor is required on this pin for the Deep power-down mode. See [Figure 52](#) for the reset pad configuration.
- [3] Pad providing digital I/O functions with configurable pull-up/pull-down resistors and configurable hysteresis (see [Figure 51](#)).
- [4] I²C-bus pads compliant with the I²C-bus specification for I²C standard mode and I²C Fast-mode Plus. The pin requires an external pull-up to provide output functionality. When power is switched off, this pin is floating and does not disturb the I2C lines. Open-drain configuration applies to all functions on this pin.
- [5] Pad providing digital I/O functions with configurable pull-up/pull-down resistors, configurable hysteresis, and analog input. When configured as a ADC input, digital section of the pad is disabled (see [Figure 51](#)).
- [6] When the system oscillator is not used, connect XTALIN and XTALOUT as follows: XTALIN can be left floating or can be grounded (grounding is preferred to reduce susceptibility to noise). XTALOUT should be left floating.