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LPC11Axx

32-bit ARM Cortex-M0 microcontroller; up to 32 kB flash, 8 kB SRAM, 4 kB EEPROM; configurable analog/mixed-signal

Rev. 4 — 30 October 2012 Product data sheet

1. General description

The LPC11Axx are an ARM Cortex-M0 based, low-cost 32-bit MCU family, designed for 8/16-bit microcontroller applications, offering performance, low power, simple instruction set and memory addressing together with reduced code size compared to existing 8/16-bit architectures.

The LPC11Axx operate at CPU frequencies of up to 50 MHz.

Analog/mixed-signal subsystems can be configured by software from interconnected digital and analog peripherals.

The digital peripherals on the LPC11Axx include up to 32 kB of flash memory, up to 4 kB of EEPROM data memory, up to 8 kB of SRAM data memory, a Fast-mode Plus I^2C-bus interface, a RS-485/EIA-485 USART, two SSP controllers, four general purpose counter/timers, and up to 42 general purpose I/O pins.

Analog peripherals include a 10-bit ADC, a 10-bit DAC, an analog comparator, a temperature sensor, an internal voltage reference, and UnderVoltage LockOut (UVLO) protection.

2. Features and benefits

- System:
  - ARM Cortex-M0 processor, running at frequencies of up to 50 MHz.
  - ARM Cortex-M0 built-in Nested Vectored Interrupt Controller (NVIC).
  - Serial Wire Debug (SWD)
  - JTAG boundary scan.
  - System tick timer.
- Memory:
  - Up to 32 kB on-chip flash program memory.
  - Up to 4 kB on-chip EEPROM data memory; byte erasable and byte programmable.
  - Up to 8 kB SRAM data memory.
  - 16 kB boot ROM.
  - In-System Programming (ISP) for flash and In-Application Programming (IAP) for flash and EEPROM via on-chip bootloader software.
  - Includes ROM-based 32-bit integer division and I^2C-bus driver routines.
- Digital peripherals:
  - Up to 42 General Purpose I/O (GPIO) pins with configurable pull-up/pull-down resistors, repeater mode, and open-drain mode.

- Up to 16 pins are configurable with a digital input glitch filter for removing glitches with widths of 10 ns or less and two pins are configurable for 50 ns glitch filters.
- GPIO pins can be used as edge and level sensitive interrupt sources.
- High-current source output driver (20 mA) on one pin (PIO0_21).
- High-current sink driver (20 mA) on true open-drain pins (PIO0_2 and PIO0_3).
- Four general purpose counter/timers with a total of up to 16 capture inputs and 14 match outputs.
- Programmable Windowed WatchDog Timer (WWDT) with a dedicated, internal low-power WatchDog Oscillator (WDOsc).

- Analog peripherals:
  - 10-bit ADC with input multiplexing among 8 pins.
  - 10-bit DAC with flexible conversion triggering.
  - Highly flexible analog comparator with a programmable voltage reference.
  - Integrated temperature sensor.
  - Internal voltage reference.
  - UnderVoltage Lockout (UVLO) protection against power-supply droop below 2.4 V.
- Serial interfaces:
  - USART with fractional baud rate generation, internal FIFO, support for RS-485/9-bit mode and synchronous mode.
  - Two SSP controllers with FIFO and multi-protocol capabilities. Support data rates of up to 25 Mbit/s.
  - I^2C-bus interface supporting the full I^2C-bus specification and Fast-mode Plus with a data rate of 1 Mbit/s with multiple address recognition and monitor mode.
- Clock generation:
  - Crystal Oscillator (SysOsc) with an operating range of 1 MHz to 25 MHz.
  - 12 MHz internal RC Oscillator (IRC) trimmed to 1% accuracy that can optionally be used as a system clock.
  - Internal low-power, Low-Frequency Oscillator (LFOsc) with programmable frequency output.
  - Clock input for external system clock (25 MHz typical).
  - PLL allows CPU operation up to the maximum CPU rate with the IRC, the external clock, or the SysOsc as clock sources.
  - Clock output function with divider that can reflect the SysOsc, the IRC, the main clock, or the LFOsc.
- Power control:
  - Supports one reduced power mode: The ARM Sleep mode.
  - Power profiles residing in boot ROM allowing to optimize performance and minimize power consumption for any given application through one simple function call.
  - Processor wake-up from reduced power mode using any interrupt.
  - Power-On Reset (POR).
  - Brown-Out Detect (BOD) with two programmable thresholds for interrupt and one hardware controlled reset trip point.
  - POR and BOD are always enabled for rapid UVLO protection against power supply voltage droop below 2.4 V.
- Unique device serial number for identification.

- Single 3.3 V power supply (2.6 V to 3.6 V).
- Temperature range −40 °C to +85 °C.
- Available as LQFP48 package, HVQFN33 (7 × 7) and HVQFN33 (5 × 5) packages, and in a very small WLCSP20 package.

3. Applications

- Power management
- Industrial control
- Remote monitoring
- Point-of-sale
- Test and measurement equipment
- Network appliances and services
- Factory automation
- Gaming equipment
- Motion control
- Medical instrumentation
- Fire and security
- Sensors
- Precision instrumentation
- HVAC and building control

4. Ordering information

Table 1. Ordering information

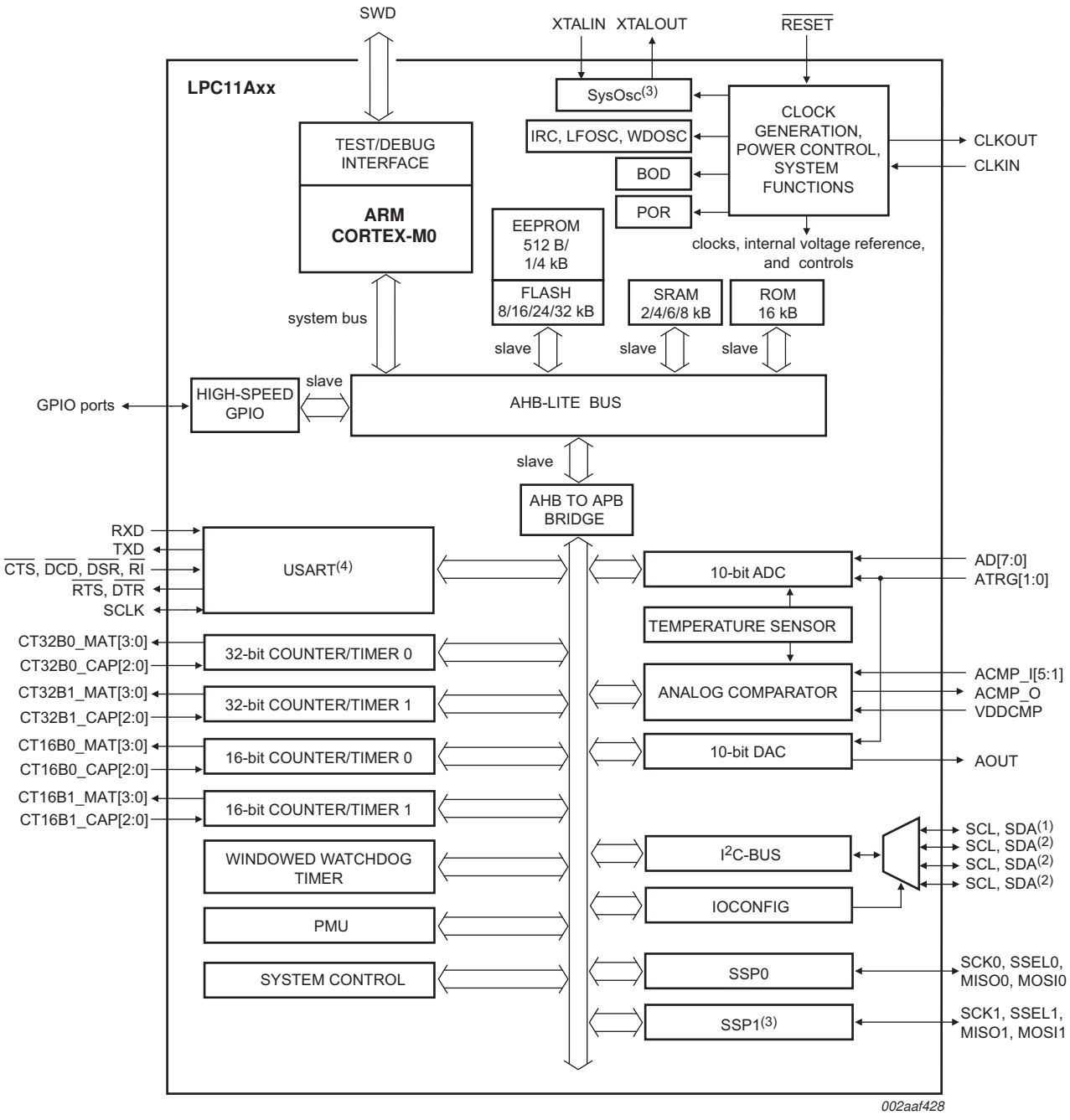
Type number	Package		
	Name	Description	Version
LPC11A02UK	WLCSP20	wafer level chip-size package; 20 bumps; 2.5 × 2.5 × 0.6 mm	-
LPC11A04UK	WLCSP20	wafer level chip-size package; 20 bumps; 2.5 × 2.5 × 0.6 mm	-
LPC11A11FHN33/001	HVQFN33	HVQFN: plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 7 × 7 × 0.85 mm	n/a
LPC11A12FHN33/101	HVQFN33	HVQFN: plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 7 × 7 × 0.85 mm	n/a
LPC11A13FHI33/201	HVQFN33	HVQFN: plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 5 × 5 × 0.85 mm	n/a
LPC11A14FHN33/301	HVQFN33	HVQFN: plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 7 × 7 × 0.85 mm	n/a
LPC11A12FBD48/101	LQFP48	LQFP48: plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2
LPC11A14FBD48/301	LQFP48	LQFP48: plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2

4.1 Ordering options

Table 2. Ordering options

Type number	Flash	SRAM	EEPROM	10-bit ADC channels	10-bit DAC	Temperature sensor	Analog comparator	USART	SSP/SPI	I^2C	GPIO	Package
LPC11A02UK	16 kB	4 kB	2 kB	8	1	1	1	1	1	1	18	WLCSP20
LPC11A04UK	32 kB	8 kB	4 kB	8	1	1	1	1	1	1	18	WLCSP20
LPC11A11FHN33/001	8 kB	2 kB	512 B	8	1	1	1	1	2	1	28	HVQFN33
LPC11A12FHN33/101	16 kB	4 kB	1 kB	8	1	1	1	1	2	1	28	HVQFN33
LPC11A12FBD48/101	16 kB	4 kB	1 kB	8	1	1	1	1	2	1	42	LQFP48
LPC11A13FHI33/201	24 kB	6 kB	2 kB	8	1	1	1	1	2	1	28	HVQFN33
LPC11A14FHN33/301	32 kB	8 kB	4 kB	8	1	1	1	1	2	1	28	HVQFN33
LPC11A14FBD48/301	32 kB	8 kB	4 kB	8	1	1	1	1	2	1	42	LQFP48

5. Block diagram



(1) Open-drain pins.

(2) Standard I/O pins.

(3) Not available on WLCSP packages.

(4) Modem control pins not available on WLCSP packages.

Fig 1. LPC11Axx block diagram

6. Pinning information

6.1 Pinning

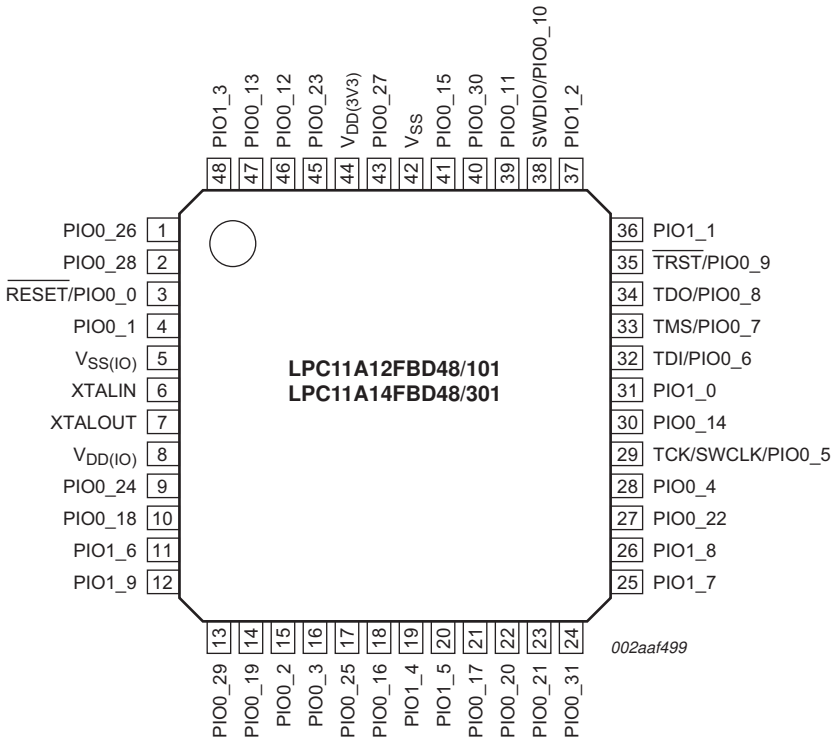
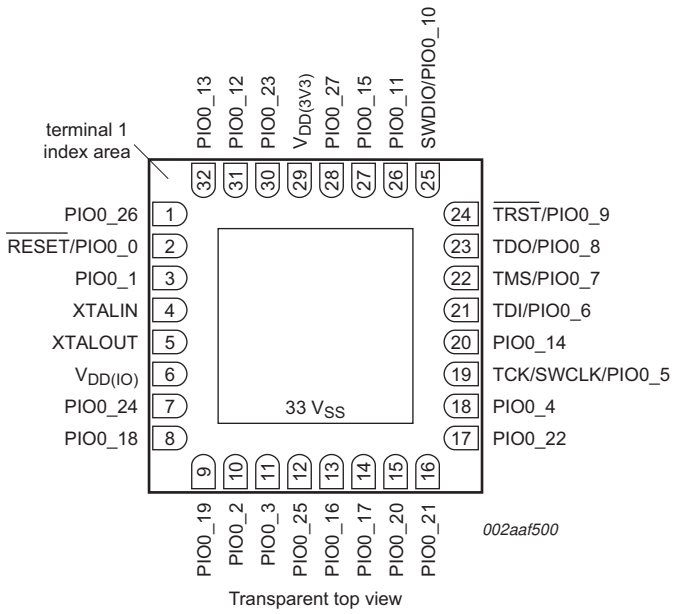
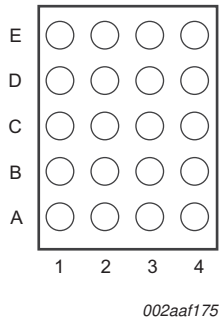


Fig 2. Pin configuration LQFP48 package



Parts: LPC11A11FHN33/001, LPC11A12FHN33/101, LPC11A13FHI33/201, LPC11A14FHN33/301

Fig 3. Pin configuration HVQFN 33 package



Parts: LPC11A02UK, LPC11A04UK

Fig 4. Pin configuration WLCSP20 package

6.2 Pin description

All functional pins on the LPC11Axx are mapped to GPIO port 0 and port 1 (see Table 4). The port pins are multiplexed to accommodate more than one function (see Table 3).

The pin function is controlled by the pin's IOCON register (see the *LPC11Axx user manual*). The standard I/O pad configuration is illustrated in Figure 31 and a detailed pin description is given in Table 4.

Table 3. Pin multiplexing

Function	Type			LQFP48	HVQFN33	WCSP20
		Port	Glitch filter	Pin	Pin	Ball
System clocks, reset, and wake-up						
CLKIN	I	PIO0_1	no	4	3	B2
		PIO0_12	no	46	31	E1
		PIO0_19	no	14	9	-
		PIO0_24	no	9	7	-
CLKOUT	O	PIO0_1	no	4	3	B2
		PIO0_19	no	14	9	-
XTALIN	I (analog)	-	-	6	4	-
XTALOUT	O (analog)	-	-	7	5	-
$\overline{\text{RESET}}$	I	PIO0_0	20 ns[1]	3	2	C1
Serial Wire Debug (SWD) and JTAG						
$\overline{\text{TRST}}$	I	PIO0_9	10 ns[2]	35	24	D4
TCK	I	PIO0_5	10 ns[2]	29	19	B3
TDI	I	PIO0_6	10 ns[2]	32	21	C3
TDO	O	PIO0_8	no	34	23	C2
TMS	I	PIO0_7	10 ns[2]	33	22	C4
SWCLK	I	PIO0_2	50 ns[2]	15	10	A1
		PIO0_5	10 ns[2]	29	19	B3
SWDIO	I/O	PIO0_3	50 ns[2]	16	11	B1
		PIO0_10	10 ns[2]	38	25	D3
Analog peripherals (ADC, DAC, comparator)						
ACMP_I1	I (analog)	PIO0_27	no	43	28	-
ACMP_I2	I (analog)	PIO0_13	no	47	32	D1
ACMP_I3	I (analog)	PIO0_16	no	18	13	A2
ACMP_I4	I (analog)	PIO0_17	no	21	14	A3
ACMP_I5	I (analog)	PIO0_22	no	27	17	-
ACMP_O	O (digital)	PIO0_2	no	15	10	A1
		PIO0_3	no	16	11	B1
		PIO0_12	no	46	31	E1
		PIO0_21	no	23	16	-
		PIO0_23	no	45	30	-
AD0	I (analog)	PIO0_6	no	32	21	C3
AD1	I (analog)	PIO0_7	no	33	22	C4

Table 3. Pin multiplexing

Function	Type			LQFP48	HVQFN33	WCSP20
		Port	Glitch filter	Pin	Pin	Ball
AD2	I (analog)	PIO0_8	no	34	23	C2
AD3	I (analog)	PIO0_9	no	35	24	D4
AD4	I (analog)	PIO0_10	no	38	25	D3
AD5	I (analog)	PIO0_11	no	39	26	D2
AD6	I (analog)	PIO0_14	no	30	20	B4
AD7	I (analog)	PIO0_15	no	41	27	E4
AOUT	O (analog)	PIO0_4	no	28	18	A4
ATRG0	I	PIO0_16	10 ns[2]	18	13	A2
ATRG1	I	PIO0_17	10 ns[2]	21	14	A3
VDDCMP	I (analog)	PIO0_14	no	30	20	-
		PIO0_5	no	-	-	B3
I²C-bus interface						
SCL	I/O	PIO0_2	50 ns[2]	15	10	A1
		PIO0_12	no	46	31	E1
		PIO0_16	10 ns[2]	18	13	A2
		PIO0_24	no	9	7	-
SDA	I/O	PIO0_3	50 ns[2]	16	11	B1
		PIO0_13	10 ns[2]	47	32	D1
		PIO0_15	10 ns[2]	41	27	E4
		PIO0_25	no	17	12	-
SSP0 controller						
MISO0	I/O	PIO0_6	10 ns[2]	32	21	C3
		PIO0_22	10 ns[2]	27	17	-
		PIO1_2	no	37	-	-
MOSI0	I/O	PIO0_4	10 ns[2]	28	18	A4
		PIO0_19	no	14	9	-
		PIO1_3	no	48	-	-
		PIO1_7	no	25	-	-
SCK0	I/O	PIO0_5	10 ns[2]	29	19	B3
		PIO0_20	no	22	15	-
		PIO1_0	no	31	-	-
SSEL0	I/O	PIO0_1	no	4	3	B2
		PIO0_18	no	10	8	-
		PIO1_1	no	36	-	-

Table 3. Pin multiplexing

Function	Type			LQFP48	HVQFN33	WCSP20
		Port	Glitch filter	Pin	Pin	Ball
SSP1 controller						
MISO1	I/O	PIO0_14	10 ns[2]	30	20	-
		PIO0_26	no	1	1	-
		PIO1_8	no	26	-	-
MOSI1	I/O	PIO0_27	10 ns[2]	43	28	-
		PIO0_31	no	24	-	-
		PIO0_30	no	40	-	-
		PIO1_6	no	11	-	-
SCK1	I/O	PIO0_8	10 ns[2]	34	23	-
		PIO1_5	no	20	-	-
		PIO0_29	no	13	-	-
SSEL1	I/O	PIO0_25	no	17	12	-
		PIO1_4	no	19	-	-
		PIO0_28	no	2	-	-
USART						
RXD	I	PIO0_1	no	4	3	B2
		PIO0_12	no	46	31	E1
		PIO1_4	no	19	-	-
		PIO1_8	no	26	-	-
TXD	O	PIO0_13	no	47	32	D1
		PIO0_15	no	41	27	E4
		PIO0_26	no	1	1	-
		PIO1_5	no	20	-	-
SCLK	I/O	PIO0_11	10 ns[2]	39	26	D2
		PIO0_21	no	23	16	-
		PIO0_23	no	45	30	-
$\overline{CTS}$	I	PIO0_9	10 ns[2]	35	24	D4
		PIO0_21	no	23	16	-
		PIO1_7	no	25	-	-
$\overline{RTS}$	O	PIO0_10	no	38	25	D3
		PIO0_23	no	45	30	-
		PIO1_6	no	11	-	-
$\overline{DCD}$	I	PIO1_9	no	12	-	-
		PIO1_0	no	31	-	-
$\overline{DSR}$	I	PIO0_29	no	13	-	-
		PIO1_2	no	37	-	-
$\overline{DTR}$	O	PIO0_28	no	2	-	-
		PIO1_1	no	36	-	-

Table 3. Pin multiplexing

Function	Type			LQFP48	HVQFN33	WCSP20
		Port	Glitch filter	Pin	Pin	Ball
$\overline{RI}$	I	PIO0_30	no	40	-	-
		PIO0_31	no	24	-	-
		PIO1_3	no	48	-	-
16-bit counter/timer CT16B0						
CT16B0_CAP0	I	PIO0_2	50 ns[2]	15	10	A1
		PIO0_18	no	10	8	-
		PIO0_30	no	40	-	-
CT16B0_CAP1	I	PIO0_16	10 ns[2]	18	13	A2
		PIO1_4	no	19	-	-
CT16B0_CAP2	I	PIO0_17	10 ns[2]	21	14	A3
		PIO1_5	no	20	-	-
CT16B0_MAT0	O	PIO0_7	no	33	22	C4
		PIO0_17	no	21	14	A3
		PIO1_6	no	11	-	-
CT16B0_MAT1	O	PIO0_4	no	28	18	A4
		PIO0_9	no	35	24	D4
		PIO1_0	no	31	-	-
CT16B0_MAT2	O	PIO0_5	no	29	19	B3
		PIO0_10	no	38	25	D3
		PIO1_7	no	25	-	-
16-bit counter/timer CT16B1						
CT16B1_CAP0	I	PIO0_3	50 ns[2]	16	11	B1
		PIO0_24	no	9	7	-
		PIO1_3	no	48	-	-
CT16B1_CAP1	I	PIO0_18	no	10	8	-
		PIO0_26	no	1	1	-
		PIO0_31	no	24	-	-
CT16B1_CAP2	I	PIO0_27	10 ns[2]	43	28	-
		PIO1_7	no	25	-	-
CT16B1_MAT0	O	PIO0_19	no	14	9	-
		PIO0_25	no	17	12	-
		PIO1_1	no	36	-	-
CT16B1_MAT1	O	PIO0_14	no	30	20	B4
		PIO1_2	no	37	-	-
		PIO1_8	no	26	-	-
CT16B1_MAT2	O	PIO0_20	no	22	15	-
		PIO1_2	no	37	-	-
		PIO1_9	no	12	-	-

Table 3. Pin multiplexing

Function	Type	Port	Glitch filter	LQFP48 Pin	HVQFN33 Pin	WCSP20 Ball
32-bit counter/timer CT32B0						
CT32B0_CAP0	I	PIO0_11	10 ns[2]	39	26	D2
		PIO0_23	no	45	30	-
		PIO0_28	no	2	-	-
CT32B0_CAP1	I	PIO0_14	10 ns[2]	30	20	B4
		PIO0_29	no	13	-	-
CT32B0_CAP2	I	PIO0_15	10 ns[2]	41	27	E4
		PIO0_26	no	1	1	-
CT32B0_MAT0	O	PIO0_12	no	46	31	E1
		PIO0_30	no	40	-	-
CT32B0_MAT1	O	PIO0_13	no	47	32	D1
		PIO1_4	no	19	-	-
CT32B0_MAT2	O	PIO0_1	no	4	3	B2
		PIO1_5	no	20	-	-
CT32B0_MAT3	O	PIO0_6	no	32	21	C3
		PIO1_6	no	11	-	-
32-bit counter/timer CT32B1						
CT32B1_CAP0	I	PIO0_7	10 ns[2]	33	22	C4
		PIO0_20	no	22	15	-
		PIO1_4	no	19	-	-
CT32B1_CAP1	I	PIO0_21	no	23	16	-
		PIO1_5	no	20	-	-
CT32B1_CAP2	I	PIO0_22	10 ns[2]	27	17	-
		PIO1_6	no	11	-	-
CT32B1_MAT0	O	PIO0_8	no	34	23	C2
		PIO0_31	no	24	-	-
		PIO1_8	no	26	-	-
CT32B1_MAT1	O	PIO0_9	no	35	24	D4
		PIO0_27	no	43	28	-
		PIO1_7	no	25	-	-
CT32B1_MAT2	O	PIO0_10	no	38	25	D3
		PIO0_22	no	27	17	-
		PIO1_9	no	12	-	-
CT32B1_MAT3	O	PIO0_11	no	39	26	D2
		PIO1_1	no	36	-	-
		PIO1_0	no	31	-	-
Supply and ground pins						
$V_{DD(IO)}$	Supply	-	-	8	6	E2

Table 3. Pin multiplexing

Function	Type			LQFP48	HVQFN33	WCSP20
		Port	Glitch filter	Pin	Pin	Ball
$V_{DD(3V3)}$	Supply	-	-	44	29	E2
V_{SS}	Ground	-	-	42	33	E3
$V_{SS(IO)}$	Ground	-	-	5	33	E3

[1] Always on.

[2] Programmable on/off. By default, the glitch filter is disabled.

Table 4 shows all pins in order of their port number. The default function after reset is listed first. All port pins PIO0_0 to PIO1_9 have internal pull-up resistors enabled after reset with the exception of the true open-drain pins PIO0_2 and PIO0_3.

Pull-up/pull-down configuration, repeater, and open-drain modes can be programmed through the IOCON registers for each of the port pins.

Table 4. LPC11Axx pin description table

Symbol	Pin/Ball				Type	Reset state [1]	Description
	LQFP48	HVQFN33	WLCSP20				
$\overline{\text{RESET}}$/PIO0_0	3	2	C1	[2]	I	I; PU	**$\overline{\text{RESET}}$ —** External reset input with fixed 20 ns glitch filter: A LOW on this pin resets the device, causing I/O ports and peripherals to take on their default states and processor execution to begin at address 0.
					I/O	-	**PIO0_0 —** General purpose digital input/output pin.
PIO0_1/RXD/CLKOUT/ CT32B0_MAT2/SSEL0/ CLKIN	4	3	B2	[3]	I/O	I; PU	**PIO0_1 —** General purpose digital input/output pin. A LOW level on this pin during reset starts the ISP command handler.
					I	-	**RXD —** Receiver data input for USART.
					O	-	**CLKOUT —** Clock output.
					O	-	**CT32B0_MAT2 —** Match output 2 for 32-bit timer 0.
					I/O	-	**SSEL0 —** Slave Select for SSP0.
					I	-	**CLKIN —** External clock input.
PIO0_2/SCL/ACMP_O/ TCK/SWCLK/ CT16B0_CAP0	15	10	A1	[4][5]	I/O	I; IA	**PIO0_2 —** General purpose digital input/output pin. High-current sink (20 mA) or standard-current sink (4 mA) programmable; true open-drain for all pin functions. Input glitch filter (50 ns) capable.
					I/O	-	**SCL —** I^2C-bus clock (true open-drain) input/output. Input glitch filter (50 ns) capable.
					O	-	**ACMP_O —** Analog comparator output.
					I	-	**TCK/SWCLK —** Serial Wire Debug Clock (secondary for LQFP and HVQFN packages). Input glitch filter (50 ns) capable. For the WLCSP20 package only, this pin is configured to the SWCLK function by the boot loader after reset.
					I	-	**CT16B0_CAP0 —** Capture input 0 for 16-bit timer 0. Input glitch filter (50 ns) capable.

Table 4. LPC11Axx pin description table

Symbol	Pin/Ball				Type	Reset state [1]	Description
	LQFP48	HVQFN33	WLCSP20				
PIO0_3/SDA/ACMP_O/ SWDIO/CT16B1_CAP0	16	11	B1	[4][6]	I/O	I; IA	**PIO0_3 —** General purpose digital input/output pin. High-current sink (20 mA) or standard-current sink (4 mA) programmable; true open-drain for all pin functions. Input glitch filter (50 ns) capable.
					I/O	-	**SDA —** I^2C-bus data (true open-drain) input/output. Input glitch filter (50 ns) capable.
					O	-	**ACMP_O —** Analog comparator output.
					I/O	-	**SWDIO —** Serial Wire Debug I/O (secondary for LQFP and HVQFN packages). Input glitch filter (50 ns) capable. For the WLCSP20 package only, this pin is configured to the SWDIO function by the boot loader after reset.
					I	-	**CT16B1_CAP0 —** Capture input 0 for 16-bit timer 1. Input glitch filter (50 ns) capable.
PIO0_4/R/AOUT/ CT16B0_MAT1/MOSI0	28	18	A4	[7]	I/O	I; PU	**PIO0_4 —** General purpose digital input/output pin. Input glitch filter (10 ns) capable.
					-	-	**R —** Reserved.
					O	-	**AOUT —** D/A converter output.
					O	-	**CT16B0_MAT1 —** Match output 1 for 16-bit timer 0.
					I/O	-	**MOSI0 —** Master Out Slave In for SSP0. Input glitch filter (10 ns) capable.
TCK/SWCLK/PIO0_5/ R/CT16B0_MAT2/ SCK0	29	19	-	[9]	I	I; PU	**TCK/SWCLK —** Test clock TCK for JTAG interface and primary (default) Serial Wire Debug Clock. Input glitch filter (10 ns) capable.
					I/O	-	**PIO0_5 —** General purpose digital input/output pin. Input glitch filter (10 ns) capable.
					-	-	**R —** Reserved.
					O	-	**CT16B0_MAT2 —** Match output 2 for 16-bit timer 0.
					I/O	-	**SCK0 —** Serial clock for SSP0. Input glitch filter (10 ns) capable.
TCK/SWCLK/PIO0_5/ VDDCMP/ CT16B0_MAT2/ SCK0	-	-	B3	[7][8]	I	I; PU	**TCK/SWCLK —** Test clock TCK for JTAG interface and secondary Serial Wire Debug ClocK. Use PIO0_2 for the default TCK/SWCLK function. Input glitch filter (10 ns) capable.
					I/O	-	**PIO0_5 —** General purpose digital input/output pin. Input glitch filter (10 ns) capable.
					I	-	**VDDCMP —** Analog comparator alternate reference voltage.
					O	-	**CT16B0_MAT2 —** Match output 2 for 16-bit timer 0.
					I/O	-	**SCK0 —** Serial clock for SSP0. Input glitch filter (10 ns) capable.

Table 4. LPC11Axx pin description table

Symbol	Pin/Ball				Type	Reset state [1]	Description
	LQFP48	HVQFN33	WLCSP20				
TDI/PIO0_6/AD0/ CT32B0_MAT3/MISO0	32	21	C3	[9]	I	I; PU	**TDI** — Test Data In for JTAG interface. Input glitch filter (10 ns) capable.
					I/O	-	**PIO0_6** — General purpose digital input/output pin. Input glitch filter (10 ns) capable.
					I	-	**AD0** — A/D converter input 0.
					O	-	**CT32B0_MAT3** — Match output 3 for 32-bit timer 0.
					I/O	-	**MISO0** — Master In Slave Out for SSP0. Input glitch filter (10 ns) capable.
TMS/PIO0_7/AD1/ CT32B1_CAP0/ CT16B0_MAT0	33	22	C4	[9]	I	I; PU	**TMS** — Test Mode Select for JTAG interface. Input glitch filter (10 ns) capable.
					I/O	-	**PIO0_7** — General purpose digital input/output pin. Input glitch filter (10 ns) capable.
					I	-	**AD1** — A/D converter input 1.
					I	-	**CT32B1_CAP0** — Capture input 0 for 32-bit timer 1. Input glitch filter (10 ns) capable.
					O	-	**CT16B0_MAT0** — Match output 2 for 16-bit timer 0.
TDO/PIO0_8/AD2/ CT32B1_MAT0/SCK1	34	23	C2	[9]	O	I; PU	**TDO** — Test Data Out for JTAG interface.
					I/O	-	**PIO0_8** — General purpose digital input/output pin. Input glitch filter (10 ns) capable.
					I	-	**AD2** — A/D converter input 2.
					O	-	**CT32B1_MAT0** — Match output 0 for 32-bit timer 1.
					I/O	-	**SCK1** — Serial clock for SSP1. Input glitch filter (10 ns) capable.
$\overline{\text{TRST}}$/PIO0_9/AD3/ CT32B1_MAT1/ CT16B0_MAT1/$\overline{\text{CTS}}$	35	24	D4	[9]	I	I; PU	**$\overline{\text{TRST}}$** — Test Reset for JTAG interface. Input glitch filter (10 ns) capable.
					I/O	-	**PIO0_9** — General purpose digital input/output pin. Input glitch filter (10 ns) capable.
					I	-	**AD3** — A/D converter, input 3.
					O	-	**CT32B1_MAT1** — Match output 1 for 32-bit timer 1.
					O	-	**CT16B0_MAT1** — Match output 1 for 16-bit timer 0.
					I	-	**$\overline{\text{CTS}}$** — Clear To Send input for USART. Input glitch filter (10 ns) capable.

Table 4. LPC11Axx pin description table

Symbol	Pin/Ball				Type	Reset state [1]	Description
	LQFP48	HVQFN33	WLCSP20				
SWDIO/PIO0_10/AD4/ CT32B1_MAT2/ CT16B0_MAT2/RTS	38	25	D3	[9]	I/O	I; PU	**SWDIO** — Primary (default) Serial Wire Debug I/O for the LQFP48 and HVQFN33 packages. For the WLCSP20 package, use PIO0_3. Input glitch filter (10 ns) capable.
					I/O	-	**PIO0_10** — General purpose digital input/output pin. Input glitch filter (10 ns) capable.
					I	-	**AD4** — A/D converter, input 4.
					O	-	**CT32B1_MAT2** — Match output 2 for 32-bit timer 1.
					O	-	**CT16B0_MAT2** — Match output 2 for 16-bit timer 0.
					O	-	**$\overline{\text{RTS}}$** — Request To Send output for USART.
PIO0_11/SCLK/ AD5/CT32B1_MAT3/ CT32B0_CAP0	39	26	D2	[9]	I/O	I; PU	**PIO0_11** — General purpose digital input/output pin. Input glitch filter (10 ns) capable.
					I/O	-	**SCLK** — Serial clock for USART. Input glitch filter (10 ns) capable.
					I	-	**AD5** — A/D converter, input 5.
					O	-	**CT32B1_MAT3** — Match output 3 for 32-bit timer 1.
					I	-	**CT32B0_CAP0** — Capture input 0 for 32-bit timer 0. Input glitch filter (10 ns) capable.
PIO0_12/RXD/ ACMP_O/ CT32B0_MAT0/SCL/ CLKIN	46	31	E1	[3]	I/O	I; PU	**PIO0_12** — General purpose digital input/output pin.
					I	-	**RXD** — Receiver data input for USART. This pin is used for ISP communication.
					O	-	**ACMP_O** — Analog comparator output.
					O	-	**CT32B0_MAT0** — Match output 0 for 32-bit timer 0.
					I/O	-	**SCL** — I^2C-bus clock input/output. This is not an I^2C-bus open-drain pin[10].
					I	-	**CLKIN** — External clock input.
PIO0_13/TXD/ ACMP_I2/ CT32B0_MAT1/SDA	47	32	D1	[9]	I/O	I; PU	**PIO0_13** — General purpose digital input/output pin. Input glitch filter (10 ns) capable.
					O	-	**TXD** — Transmitter data output for USART. This pin is used for ISP communication.
					I	-	**ACMP_I2** — Analog comparator input 2.
					O	-	**CT32B0_MAT1** — Match output 1 for 32-bit timer 0.
					I/O	-	**SDA** — I^2C-bus data input/output. This is not an I^2C-bus open-drain pin[10]. Input glitch filter (10 ns) capable.

Table 4. LPC11Axx pin description table

Symbol	Pin/Ball				Type	Reset state [1]	Description
	LQFP48	HVQFN33	WLCSP20				
PIO0_14/MISO1/AD6/ CT32B0_CAP1/ CT16B1_MAT1/ VDDCMP	30	20	-	[7]	I/O	I; PU	**PIO0_14 —** General purpose digital input/output pin. Input glitch filter (10 ns) capable.
					I/O	-	**MISO1 —** Master In Slave Out for SSP1. Input glitch filter (10 ns) capable.
					I	-	**AD6 —** A/D converter, input 6.
					I	-	**CT32B0_CAP1 —** Capture input 1 for 32-bit timer 0. Input glitch filter (10 ns) capable.
					O	-	**CT16B1_MAT1 —** Match output 1 for 16-bit timer 1.
					I	-	**VDDCMP —** Analog comparator alternate reference voltage.
PIO0_14/MISO1/AD6/ CT32B0_CAP1/ CT16B1_MAT1	-	-	B4	[9]	I/O	I; PU	**PIO0_14 —** General purpose digital input/output pin. Input glitch filter (10 ns) capable.
					I/O	-	**MISO1 —** Master In Slave Out for SSP1. Input glitch filter (10 ns) capable.
					I	-	**AD6 —** A/D converter, input 6.
					I	-	**CT32B0_CAP1 —** Capture input 1 for 32-bit timer 0. Input glitch filter (10 ns) capable.
					O	-	**CT16B1_MAT1 —** Match output 1 for 16-bit timer 1.
PIO0_15/TXD/AD7/ CT32B0_CAP2/SDA	41	27	E4	[9]	I/O	I; PU	**PIO0_15 —** General purpose digital input/output pin. Input glitch filter (10 ns) capable.
					O	-	**TXD —** Transmitter data output for USART.
					I	-	**AD7 —** A/D converter, input 7.
					I	-	**CT32B0_CAP2 —** Capture input 2 for 32-bit timer 0. Input glitch filter (10 ns) capable.
					I/O	-	**SDA —** I^2C-bus data input/output. This is not an I^2C-bus open-drain pin[10]. Input glitch filter (10 ns) capable.
PIO0_16/ ATRG0/ACMP_I3/ CT16B0_CAP1/SCL	18	13	A2	[9]	I/O	I; PU	**PIO0_16 —** General purpose digital input/output pin. Input glitch filter (10 ns) capable.
					I	-	**ATRG0 —** Conversion trigger 0 for ADC or DAC. Input glitch filter (10 ns) capable.
					I	-	**ACMP_I3 —** Analog comparator input 3.
					I	-	**CT16B0_CAP1 —** Capture input 1 for 16-bit timer 0. Input glitch filter (10 ns) capable.
					I/O	-	**SCL —** I^2C-bus clock input/output. This is not an I^2C-bus open-drain pin[10]. Input glitch filter (10 ns) capable.

Table 4. LPC11Axx pin description table

Symbol	Pin/Ball				Type	Reset state [1]	Description
	LQFP48	HVQFN33	WLCSP20				
PIO0_17/ ATRG1/ACMP_I4/ CT16B0_CAP2/ CT16B0_MAT0	21	14	A3	[9]	I/O	I; PU	**PIO0_17** — General purpose digital input/output pin. Input glitch filter (10 ns) capable.
					I	-	**ATRG1** — Conversion trigger 1 for ADC or DAC. Input glitch filter (10 ns) capable.
					I	-	**ACMP_I4** — Analog comparator input 4.
					I	-	**CT16B0_CAP2** — Capture input 2 for 16-bit timer 0. Input glitch filter (10 ns) capable.
					O	-	**CT16B0_MAT0** — Match output 0 for 16-bit timer 0.
PIO0_18/R/SSEL0/ CT16B0_CAP0/ CT16B1_CAP1	10	8	-	[3]	I/O	I; PU	**PIO0_18** — General purpose digital input/output pin.
					-	-	**R** — Reserved.
					I/O	-	**SSEL0** — Slave Select for SSP0.
					I	-	**CT16B0_CAP0** — Capture input 0 for 16-bit timer 0.
					I	-	**CT16B1_CAP1** — Capture input 1 for 16-bit timer 1.
PIO0_19/CLKIN/ CLKOUT/ MOSI0/CT16B1_MAT0	14	9	-	[3]	I/O	I; PU	**PIO0_19** — General purpose digital input/output pin.
					I	-	**CLKIN** — External clock input.
					O	-	**CLKOUT** — Clock output.
					I/O	-	**MOSI0** — Master Out Slave In for SSP0.
					O	-	**CT16B1_MAT0** — Match output 0 for 16-bit timer 1.
PIO0_20/R/SCK0/ CT32B1_CAP0/ CT16B1_MAT2	22	15	-	[3]	I/O	I; PU	**PIO0_20** — General purpose digital input/output pin.
					-	-	**R** — Reserved.
					I/O	-	**SCK0** — Serial clock for SSP0.
					I	-	**CT32B1_CAP0** — Capture input 0 for 32-bit timer 1.
					O	-	**CT16B1_MAT2** — Match output 2 for 16-bit timer 1.
PIO0_21/$\overline{\text{CTS}}$/ ACMP_O/ CT32B1_CAP1/SCLK	23	16	-	[3]	I/O	I; PU	**PIO0_21** — General purpose digital input/output pin. If configured as output, this pin is a high-current source output driver (20 mA).
					I	-	**$\overline{\text{CTS}}$** — Clear To Send input for USART.
					O	-	**ACMP_O** — Analog comparator output.
					I	-	**CT32B1_CAP1** — Capture input 1 for 32-bit timer 1.
					I/O	-	**SCLK** — Serial clock for USART.
PIO0_22/MISO0/ ACMP_I5/ CT32B1_MAT2/ CT32B1_CAP2	27	17	-	[9]	I/O	I; PU	**PIO0_22** — General purpose digital input/output pin. Input glitch filter (10 ns) capable.
					I/O	-	**MISO0** — Master In Slave Out for SSP0. Input glitch filter (10 ns) capable.
					I	-	**ACMP_I5** — Analog comparator input 5.
					O	-	**CT32B1_MAT2** — Match output 2 for 32-bit timer 1.
					I	-	**CT32B1_CAP2** — Capture input 2 for 32-bit timer 1. Input glitch filter (10 ns) capable.

Table 4. LPC11Axx pin description table

Symbol	Pin/Ball				Type	Reset state [1]	Description
	LQFP48	HVQFN33	WLCSP20				
PIO0_23/$\overline{\text{RTS}}$/ ACMP_O/ CT32B0_CAP0/SCLK	45	30	-	[3]	I/O	I; PU	**PIO0_23** — General purpose digital input/output pin.
					O	-	**$\overline{\text{RTS}}$** — Request To Send output for USART.
					O	-	**ACMP_O** — Analog comparator output.
					I	-	**CT32B0_CAP0** — Capture input 0 for 32-bit timer 0.
					I/O	-	**SCLK** — Serial clock for USART.
PIO0_24/SCL/CLKIN/ CT16B1_CAP0	9	7	-	[3]	I/O	I; PU	**PIO0_24** — General purpose digital input/output pin.
					I/O	-	**SCL** — I^2C-bus clock input/output. This is not an I^2C-bus open-drain pin[10].
					I	-	**CLKIN** — External clock input.
					I	-	**CT16B1_CAP0** — Capture input 0 for 16-bit timer 1.
PIO0_25/SDA/SSEL1/ CT16B1_MAT0	17	12	-	[3]	I/O	I; PU	**PIO0_25** — General purpose digital input/output pin.
					I/O	-	**SDA** — I^2C-bus data input/output. This is not an I^2C-bus open-drain pin[10].
					I/O	-	**SSEL1** — Slave Select for SSP1.
					O	-	**CT16B1_MAT0** — Match output 0 for 16-bit timer 1.
PIO0_26/TXD/MISO1/ CT16B1_CAP1/ CT32B0_CAP2	1	1	-	[3]	I/O	I; PU	**PIO0_26** — General purpose digital input/output pin.
					O	-	**TXD** — Transmitter data output for USART.
					I/O	-	**MISO1** — Master In Slave Out for SSP1.
					I	-	**CT16B1_CAP1** — Capture input 1 for 16-bit timer 1.
					I	-	**CT32B0_CAP2** — Capture input 2 for 32-bit timer 0.
PIO0_27/MOSI1/ ACMP_I1/ CT32B1_MAT1/ CT16B1_CAP2	43	28	-	[9]	I/O	I; PU	**PIO0_27** — General purpose digital input/output pin. Input glitch filter (10 ns) capable.
					I/O	-	**MOSI1** — Master Out Slave In for SSP1. Input glitch filter (10 ns) capable.
					I	-	**ACMP_I1** — Analog comparator input 1.
					O	-	**CT32B1_MAT1** — Match output 1 for 32-bit timer 1.
					I	-	**CT16B1_CAP2** — Capture input 2 for 16-bit timer 1. Input glitch filter (10 ns) capable.
PIO0_28/$\overline{\text{DTR}}$/SSEL1/ CT32B0_CAP0	2	-	-	[3]	I/O	I; PU	**PIO0_28** — General purpose digital input/output pin.
					O	-	**$\overline{\text{DTR}}$** — Data Terminal Ready output for USART.
					I/O	-	**SSEL1** — Slave Select for SSP1.
					I	-	**CT32B0_CAP0** — Capture input 0 for 32-bit timer 0.
PIO0_29/$\overline{\text{DSR}}$/SCK1/ CT32B0_CAP1	13	-	-	[3]	I/O	I; PU	**PIO0_29** — General purpose digital input/output pin.
					I	-	**$\overline{\text{DSR}}$** — Data Set Ready input for USART.
					I/O	-	**SCK1** — Serial clock for SSP1.
					I	-	**CT32B0_CAP1** — Capture input 1 for 32-bit timer 0.

Table 4. LPC11Axx pin description table

Symbol	Pin/Ball				Type	Reset state [1]	Description
	LQFP48	HVQFN33	WLCSP20				
PIO0_30/$\overline{\text{RI}}$/MOSI1/ CT32B0_MAT0/ CT16B0_CAP0	40	-	-	[3]	I/O	I; PU	**PIO0_30** — General purpose digital input/output pin.
					I	-	**$\overline{\text{RI}}$** — Ring Indicator input for USART.
					I/O	-	**MOSI1** — Master Out Slave In for SSP1.
					O	-	**CT32B0_MAT0** — Match output 0 for 32-bit timer 0.
					I	-	**CT16B0_CAP0** — Capture input 0 for 16-bit timer 0.
PIO0_31/$\overline{\text{RI}}$/MOSI1/ CT32B1_MAT0/ CT16B1_CAP1	24	-	-	[3]	I/O	I; PU	**PIO0_31** — General purpose digital input/output pin.
					I	-	**$\overline{\text{RI}}$** — Ring Indicator input for USART.
					I/O	-	**MOSI1** — Master Out Slave In for SSP1.
					O	-	**CT32B1_MAT0** — Match output 0 for 32-bit timer 1.
					I	-	**CT16B1_CAP1** — Capture input 1 for 16-bit timer 1.
PIO1_0/$\overline{\text{DCD}}$/SCK0/ CT32B1_MAT3/ CT16B0_MAT1	31	-	-	[3]	I/O	I; PU	**PIO1_0** — General purpose digital input/output pin.
					I	-	**$\overline{\text{DCD}}$** — Data Carrier Detect input for USART.
					I/O	-	**SCK0** — Serial clock for SSP0.
					O	-	**CT32B1_MAT3** — Match output 3 for 32-bit timer 1.
					O	-	**CT16B0_MAT1** — Match output 1 for 16-bit timer 0.
PIO1_1/$\overline{\text{DTR}}$/SSEL0/ CT32B1_MAT3/ CT16B1_MAT0	36	-	-	[3]	I/O	I; PU	**PIO1_1** — General purpose digital input/output pin.
					O	-	**$\overline{\text{DTR}}$** — Data Terminal Ready output for USART.
					I/O	-	**SSEL0** — Slave Select for SSP0.
					O	-	**CT32B1_MAT3** — Match output 3 for 32-bit timer 1.
					O	-	**CT16B1_MAT0** — Match output 0 for 16-bit timer 1.
PIO1_2/$\overline{\text{DSR}}$/MISO0/ CT16B1_MAT2/ CT16B1_MAT1	37	-	-	[3]	I/O	I; PU	**PIO1_2** — General purpose digital input/output pin.
					I	-	**$\overline{\text{DSR}}$** — Data Set Ready input for USART.
					I/O	-	**MISO0** — Master In Slave Out for SSP0.
					O	-	**CT16B1_MAT2** — Match output 2 for 16-bit timer 1.
					O	-	**CT16B1_MAT1** — Match output 1 for 16-bit timer 1.
PIO1_3/$\overline{\text{RI}}$/MOSI0/ CT16B1_CAP0	48	-	-	[3]	I/O	I; PU	**PIO1_3** — General purpose digital input/output pin.
					I	-	**$\overline{\text{RI}}$** — Ring Indicator input for USART.
					I/O	-	**MOSI0** — Master Out Slave In for SSP0.
					I	-	**CT16B1_CAP0** — Capture input 0 for 16-bit timer 1.
PIO1_4/RXD/SSEL1/ CT32B0_MAT1/ CT32B1_CAP0/ CT16B0_CAP1	19	-	-	[3]	I/O	I; PU	**PIO1_4** — General purpose digital input/output pin.
					I	-	**RXD** — Receiver data input for USART.
					I/O	-	**SSEL1** — Slave Select for SSP1.
					O	-	**CT32B0_MAT1** — Match output 1 for 32-bit timer 0.
					I	-	**CT32B1_CAP0** — Capture input 0 for 32-bit timer 1.
					I	-	**CT16B0_CAP1** — Capture input 1 for 16-bit timer 0.

Table 4. LPC11Axx pin description table

Symbol	Pin/Ball				Type	Reset state [1]	Description
	LQFP48	HVQFN33	WLCSP20				
PIO1_5/TXD/SCK1/ CT32B0_MAT2/ CT32B1_CAP1/ CT16B0_CAP2	20	-	-	[3]	I/O	I; PU	**PIO1_5 —** General purpose digital input/output pin.
					O	-	**TXD —** Transmitter data output for USART.
					I/O	-	**SCK1 —** Serial clock for SSP1.
					O	-	**CT32B0_MAT2 —** Match output 2 for 32-bit timer 0.
					I	-	**CT32B1_CAP1 —** Capture input 1 for 32-bit timer 1.
					I	-	**CT16B0_CAP2 —** Capture input 2 for 16-bit timer 0.
PIO1_6/$\overline{\text{RTS}}$/MOSI1/ CT32B0_MAT3/ CT32B1_CAP2/ CT16B0_MAT0	11	-	-	[3]	I/O	I; PU	**PIO1_6 —** General purpose digital input/output pin.
					O	-	**$\overline{\text{RTS}}$ —** Request To Send output for USART.
					I/O	-	**MOSI1 —** Master Out Slave In for SSP1.
					O	-	**CT32B0_MAT3 —** Match output 3 for 32-bit timer 0.
					I	-	**CT32B1_CAP2 —** Capture input 2 for 32-bit timer 1.
					O	-	**CT16B0_MAT0 —** Match output 0 for 16-bit timer 0.
PIO1_7/$\overline{\text{CTS}}$/MOSI0/ CT32B1_MAT1/ CT16B0_MAT2/ CT16B1_CAP2	25	-	-	[3]	I/O	I; PU	**PIO1_7 —** General purpose digital input/output pin.
					I	-	**$\overline{\text{CTS}}$ —** Clear To Send input for USART.
					I/O	-	**MOSI0 —** Master Out Slave In for SSP0.
					O	-	**CT32B1_MAT1 —** Match output 1 for 32-bit timer 1.
					O	-	**CT16B0_MAT2 —** Match output 2 for 16-bit timer 0.
					I	-	**CT16B1_CAP2 —** Capture input 2 for 16-bit timer 1.
PIO1_8/RXD / MISO1/ CT32B1_MAT0/ CT16B1_MAT1	26	-	-	[3]	I/O	I; PU	**PIO1_8 —** General purpose digital input/output pin.
					I	-	**RXD —** Receiver data input for USART.
					I/O	-	**MISO1 —** Master In Slave Out for SSP1.
					O	-	**CT32B1_MAT0 —** Match output 0 for 32-bit timer 1.
					O	-	**CT16B1_MAT1 —** Match output 1 for 16-bit timer 1.
PIO1_9/$\overline{\text{DCD}}$/R/ CT32B1_MAT2 / CT16B1_MAT2	12	-	-	[3]	I/O	I; PU	**PIO1_9 —** General purpose digital input/output pin.
					I	-	**$\overline{\text{DCD}}$ —** Data Carrier Detect input for USART.
					-	-	**R —** Reserved.
					O	-	**CT32B1_MAT2 —** Match output 2 for 32-bit timer 1.
					O	-	**CT16B1_MAT2 —** Match output 2 for 16-bit timer 1.
XTALIN	6	4	-	[11]	-	-	Input to the oscillator circuit and internal clock generator circuits. Input voltage must not exceed 1.8 V.
XTALOUT	7	5	-	[11]	-	-	Output from the oscillator amplifier.
$V_{DD(IO)}$	8	6	E2	[12] [13]	-	-	3.3 V input/output supply voltage.

Table 4. LPC11Axx pin description table

Symbol	Pin/Ball				Type	Reset state [1]	Description
	LQFP48	HVQFN33	WLCSP20				
$V_{SS(IO)}$	5	33	E3	[14]	-	-	Ground.
$V_{DD(3V3)}$	44	29	E2	[12] [13]	-	-	3.3 V supply voltage to the analog blocks, internal regulator, and internal clock generator circuits. Also used as the ADC reference voltage.
V_{SS}	42	33	E3	[14]	-	-	Ground.

[1] Pin state at reset for default function: I = Input; O = Output; PU = internal pull-up resistor (weak PMOS device) enabled; IA = inactive, no pull-up/down enabled.

[2] See Figure 32 for the reset configuration.

[3] 5 V tolerant pin providing standard digital I/O functions with configurable modes and configurable hysteresis (Figure 31).

[4] I^2C-bus pins compliant with the I^2C-bus specification for I^2C standard mode, I^2C Fast-mode, and I^2C Fast-mode Plus.

[5] For the SWD function, a pull-up resistor is recommended for the SWCLK pin (WLCSP20 parts only).

[6] For the SWD function, a pull-up resistor is recommended for the SWDIO pin (WLCSP20 parts only).

[7] Not a 5 V tolerant pin due to special analog functionality. Pin provides standard digital I/O functions with configurable modes, configurable hysteresis, and analog I/O. When configured as an analog I/O, the digital section of the pin is disabled (Figure 31).

[8] If this pin is configured for its VDDCMP function, it cannot be used for SWCLK when the part is on the board. The bypass filter of the power supply filters out the SWCLK clock input signal.

[9] 5 V tolerant pin providing standard digital I/O functions with configurable modes, configurable hysteresis, and analog I/O. When configured as an analog I/O, digital section of the pin is disabled, and the pin is not 5 V tolerant (Figure 31).

[10] I^2C-bus pins are standard digital I/O pins and have limited performance and electrical characteristics compared to the full I^2C-bus specification. Pins can be configured with an on-chip pull-up resistor (pMOS device) and with open-drain mode. In this mode, typical bit rates of up to 100 kbit/s with 20 pF load are supported if the internal pull-ups are enabled. Higher bit rates can be achieved with an external resistor.

[11] When the system oscillator is not used, connect XTALIN and XTALOUT as follows: XTALIN can be left floating or can be grounded (grounding is preferred to reduce susceptibility to noise). XTALOUT should be left floating. See Section 12.3 if an external clock is connected to the XTALIN pin.

[12] If separate supplies are used for $V_{DD(3V3)}$ and $V_{DD(IO)}$, ensure that the power supply pins are filtered for noise with respect to their corresponding grounds V_{SS} and $V_{SS(IO)}$ (LQFP48 package). Using separate filtered supplies reduces the noise to the analog blocks (see also Section 12.1).

[13] If separate supplies are used for $V_{DD(3V3)}$ and $V_{DD(IO)}$, ensure that the voltage difference between both supplies is smaller than or equal to 0.5 V.

[14] Thermal pad (HVQFN33 pin package). Connect to ground.

7. Functional description

7.1 ARM Cortex-M0 processor

The ARM Cortex-M0 is a general purpose, 32-bit microprocessor, which offers high performance and very low power consumption.

7.2 On-chip flash program memory

The LPC11Axx contain up to 32 kB of on-chip flash program memory.

7.3 On-chip EEPROM data memory

The LPC11Axx contain up to 4 kB of on-chip EEPROM data memory.

Remark: The top 64 bytes of the 4 kB EEPROM memory are reserved and cannot be written to. The entire EEPROM is writable for smaller EEPROM sizes.

7.4 On-chip SRAM

The LPC11Axx contain a total of 8 kB, 4 kB, or 2 kB on-chip static RAM data memory.

7.5 On-chip ROM

The on-chip ROM contains the boot loader and the following Application Programming Interfaces (API):

- In-System Programming (ISP) and In-Application Programming (IAP) support for flash programming
- Power profiles for configuring power consumption and PLL settings
- 32-bit integer division routines
- I^2C-bus driver routines

7.6 Memory map

The LPC11Axx incorporates several distinct memory regions, shown in the following figures. Figure 5 shows the overall map of the entire address space from the user program viewpoint following reset. The interrupt vector area supports address remapping.

The AHB peripheral area is 2 MB in size, and is divided to allow for up to 128 peripherals. The APB peripheral area is 512 kB in size and is divided to allow for up to 32 peripherals. Each peripheral of either type is allocated 16 kB of space. This allows simplifying the address decoding for each peripheral.

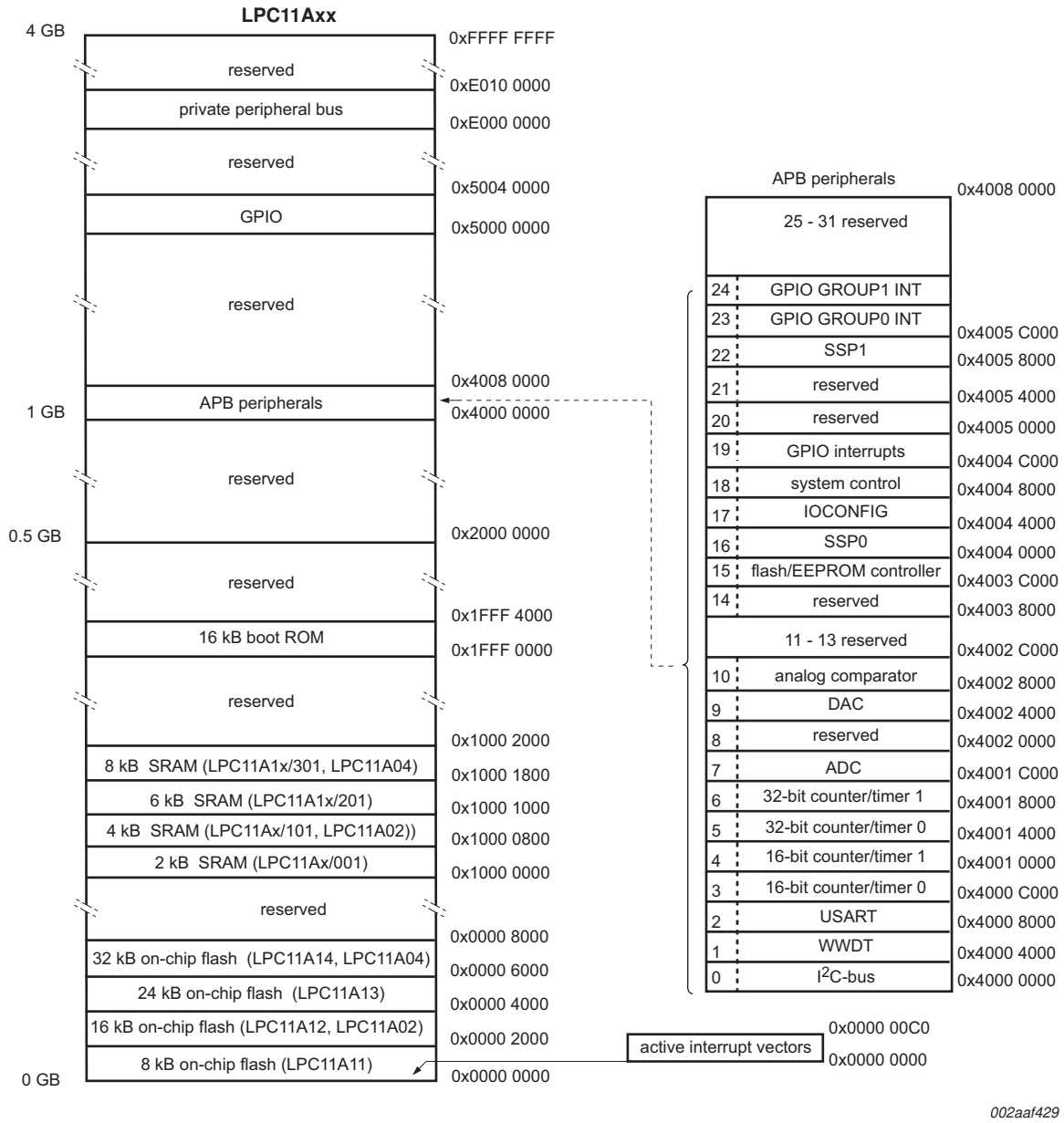


Fig 5. LPC11Axx memory map

7.7 Nested Vectored Interrupt Controller (NVIC)

The Nested Vectored Interrupt Controller (NVIC) is an integral part of the Cortex-M0. The tight coupling to the CPU allows for low interrupt latency and efficient processing of late arriving interrupts.

7.7.1 Features

- Controls system exceptions and peripheral interrupts.
- In the LPC11Axx, the NVIC supports 32 vectored interrupts including up to 8 inputs to the start logic from the individual GPIO pins.

- Four programmable interrupt priority levels with hardware priority level masking.
- Software interrupt generation.

7.7.2 Interrupt sources

Each peripheral device has one interrupt line connected to the NVIC but may have several interrupt flags. Individual interrupt flags may also represent more than one interrupt source.

Up to eight GPIO pins, regardless of the selected function, can be programmed to generate an interrupt on a level, or rising edge or falling edge, or both. The interrupt generating GPIOs can be selected from the GPIO pins with a configurable input glitch filter.

7.8 IOCON block

The IOCON block allows selected pins of the microcontroller to have more than one function. Configuration registers control the multiplexers to allow connection between the pin and the on-chip peripherals.

Peripherals should be connected to the appropriate pins prior to being activated and prior to any related interrupt(s) being enabled. Activity of any enabled peripheral function that is not mapped to a related pin should be considered undefined.

Up to 16 pins can be configured with a digital input glitch filter for removing voltage glitches with widths of 10 ns or less (see Table 3 and Table 4), two pins (PIO0_2 and PIO0_3) can be configured with a 50 ns digital input glitch filter.

7.9 Fast general purpose parallel I/O

Device pins that are not connected to a specific peripheral function are controlled by the GPIO registers. Pins may be dynamically configured as inputs or outputs. Multiple outputs can be set or cleared in one write operation.

LPC11Axx use accelerated GPIO functions:

- GPIO registers are a dedicated AHB peripheral so that the fastest possible I/O timing can be achieved.
- An entire port value can be written in one instruction.

Additionally, any GPIO pin (total of up to 42 pins) providing a digital function can be programmed to generate an interrupt on a level, a rising or falling edge, or both.

7.9.1 Features

- Bit level port registers allow a single instruction to set and clear any number of bits in one write operation.
- Direction control of individual bits.
- All I/O default to inputs with internal pull-up resistors enabled after reset - except for the I^2C-bus true open-drain pins PIO0_2 and PIO0_3.
- Pull-up/pull-down configuration, repeater, and open-drain modes can be programmed through the IOCON block for each GPIO pin (see Figure 31 and Figure 32 for functional diagrams).