Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

LPC11E3x

32-bit ARM Cortex-M0 microcontroller; up to 128 kB flash; up to 12 kB SRAM and 4 kB EEPROM; USART

Rev. 2.3 — 11 September 2014 Product data sheet

1. General description

The LPC11E3x are an ARM Cortex-M0 based, low-cost 32-bit MCU, designed for 8/16-bit microcontroller applications, offering performance, low power, simple instruction set and memory addressing together with reduced code size compared to existing 8/16-bit architectures.

The LPC11E3x operate at CPU frequencies of up to 50 MHz.

The peripheral complement of the LPC11E3x includes up to 128 kB of flash memory, up to 12 kB of SRAM data memory and 4 kB EEPROM, one Fast-mode Plus I^2C-bus interface, one RS-485/EIA-485 USART with support for synchronous mode and smart card interface, two SSP interfaces, four general purpose counter/timers, a 10-bit ADC, and up to 54 general purpose I/O pins.

The I/O Handler is a software library-supported hardware engine that can be used to add performance, connectivity and flexibility to system designs. It is available on the LPC11E37HFBD64/401. The I/O Handler can emulate serial interfaces such as UART, I^2C, and I^2S with no or very low additional CPU load and can off-load the CPU by performing processing-intensive functions like DMA transfers in hardware. Software libraries for multiple I/O Handler applications are available on http://www.LPCware.com.

2. Features and benefits

- System:
  - ARM Cortex-M0 processor, running at frequencies of up to 50 MHz.
  - ARM Cortex-M0 built-in Nested Vectored Interrupt Controller (NVIC).
  - Non Maskable Interrupt (NMI) input selectable from several input sources.
  - System tick timer.
- Memory:
  - Up to 128 kB on-chip flash program memory with sector (4 kB) and page erase (256 byte) access.
  - 4 kB on-chip EEPROM data memory; byte erasable and byte programmable; on-chip API support.
  - 12 kB SRAM data memory.
  - 16 kB boot ROM.
  - In-System Programming (ISP) and In-Application Programming (IAP) via on-chip bootloader software.
  - ROM-based 32-bit integer division routines.

- Debug options:
  - Standard JTAG (Joint Test Action Group) test interface for BSDL (Boundary Scan Description Language).
  - Serial Wire Debug.
- Digital peripherals:
  - Up to 54 General Purpose I/O (GPIO) pins with configurable pull-up/pull-down resistors, repeater mode, and open-drain mode.
  - Up to 8 GPIO pins can be selected as edge and level sensitive interrupt sources.
  - Two GPIO grouped interrupt modules enable an interrupt based on a programmable pattern of input states of a group of GPIO pins.
  - High-current source output driver (20 mA) on one pin.
  - High-current sink driver (20 mA) on true open-drain pins.
  - Four general purpose counter/timers with a total of up to 8 capture inputs and 13 match outputs.
  - Programmable Windowed WatchDog Timer (WWDT) with a dedicated, internal low-power WatchDog Oscillator (WDO).
- Analog peripherals:
  - 10-bit ADC with input multiplexing among eight pins.
- Serial interfaces:
  - USART with fractional baud rate generation, internal FIFO, a full modem control handshake interface, and support for RS-485/9-bit mode and synchronous mode. USART supports an asynchronous smart card interface (ISO 7816-3).
  - Two SSP controllers with FIFO and multi-protocol capabilities.
  - I^2C-bus interface supporting the full I^2C-bus specification and Fast-mode Plus with a data rate of up to 1 Mbit/s with multiple address recognition and monitor mode.
- I/O Handler for hardware emulation of serial interfaces and DMA; supported through software libraries.(LPC11E37HFBD64/401 only.)
- Clock generation:
  - Crystal Oscillator with an operating range of 1 MHz to 25 MHz (system oscillator).
  - 12 MHz high-frequency Internal RC oscillator (IRC) that can optionally be used as a system clock.
  - Internal low-power, low-frequency WatchDog Oscillator (WDO) with programmable frequency output.
  - PLL allows CPU operation up to the maximum CPU rate with the system oscillator or the IRC as clock sources.
  - Clock output function with divider that can reflect the crystal oscillator, the main clock, the IRC, or the watchdog oscillator.
- Power control:
  - Integrated PMU (Power Management Unit) to minimize power consumption during Sleep, Deep-sleep, Power-down, and Deep power-down modes.
  - Power profiles residing in boot ROM provide optimized performance and minimized power consumption for any given application through one simple function call.
  - Four reduced power modes: Sleep, Deep-sleep, Power-down, and Deep power-down.
  - Processor wake-up from Deep-sleep and Power-down modes via reset, selectable GPIO pins, or the watchdog interrupt.
  - Processor wake-up from Deep power-down mode using one special function pin.

- Power-On Reset (POR).
- Brownout detect with four separate thresholds for interrupt and forced reset.

- Unique device serial number for identification.
- Single 3.3 V power supply (1.8 V to 3.6 V).
- Temperature range −40 °C to +85 °C.
- Available as LQFP64, LQFP48, and HVQFN33 packages.

3. Applications

- Consumer peripherals
- Medical
- Handheld scanners
- Industrial control

4. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
LPC11E35FHI33/501	HVQFN33	plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 5 × 5 × 0.85 mm	n/a
LPC11E36FBD64/501	LQFP64	plastic low profile quad flat package; 64 leads; body 10 × 10 × 1.4 mm	SOT314-2
LPC11E36FHN33/501	HVQFN33	plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 7 × 7 × 0.85 mm	n/a
LPC11E37FBD48/501	LQFP48	plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2
LPC11E37FBD64/501	LQFP64	plastic low profile quad flat package; 64 leads; body 10 × 10 × 1.4 mm	SOT314-2
LPC11E37HFBD64/401	LQFP64	plastic low profile quad flat package; 64 leads; body 10 × 10 × 1.4 mm	SOT314-2

4.1 Ordering options

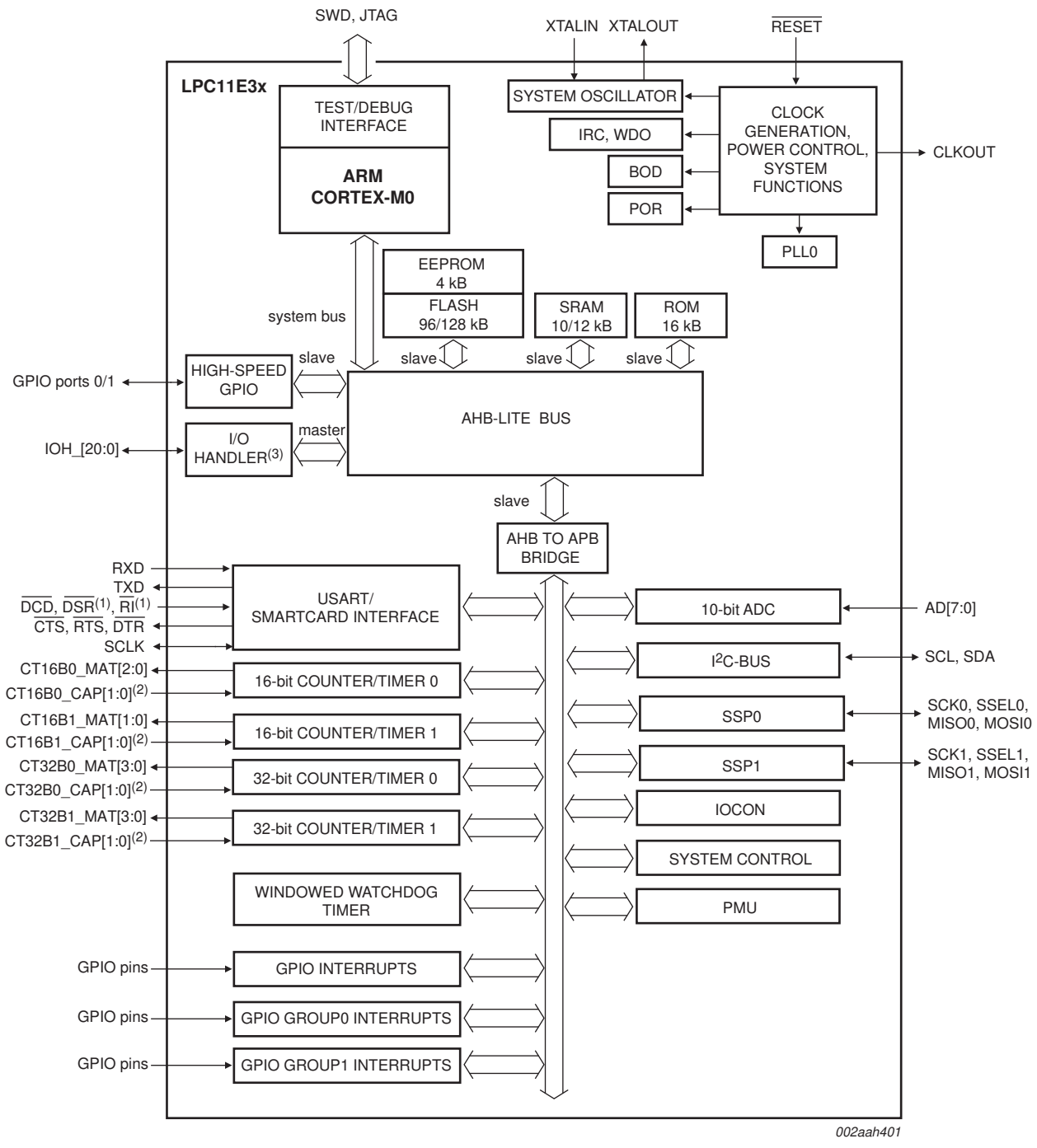
Table 2. Ordering options

Type number	Flash in kB	EEPROM in kB	SRAM0 in kB	SRAM2 in kB	SRAM1 in kB[1]	Total SRAM in kB	I/O Handler	USART	I²C-bus FM+	SSP	ADC channels	GPIO pins
LPC11E35FHI33/501	64	4	8	2	2[1]	12	no	1	1	2	8	26
LPC11E36FBD64/501	96	4	8	2	2[1]	12	no	1	1	2	8	54
LPC11E36FHN33/501	96	4	8	2	2[1]	12	no	1	1	2	8	28
LPC11E37FBD48/501	128	4	8	2	2[1]	12	no	1	1	2	8	40
LPC11E37FBD64/501	128	4	8	2	2[1]	12	no	1	1	2	8	54
LPC11E37HFBD64/401	128	4	8	2	2[2]	10	yes	1	1	2	8	54

[1] For general-purpose use.

[2] For I/O Handler use only.

5. Block diagram



(1) Not available on HVQFN33 packages.

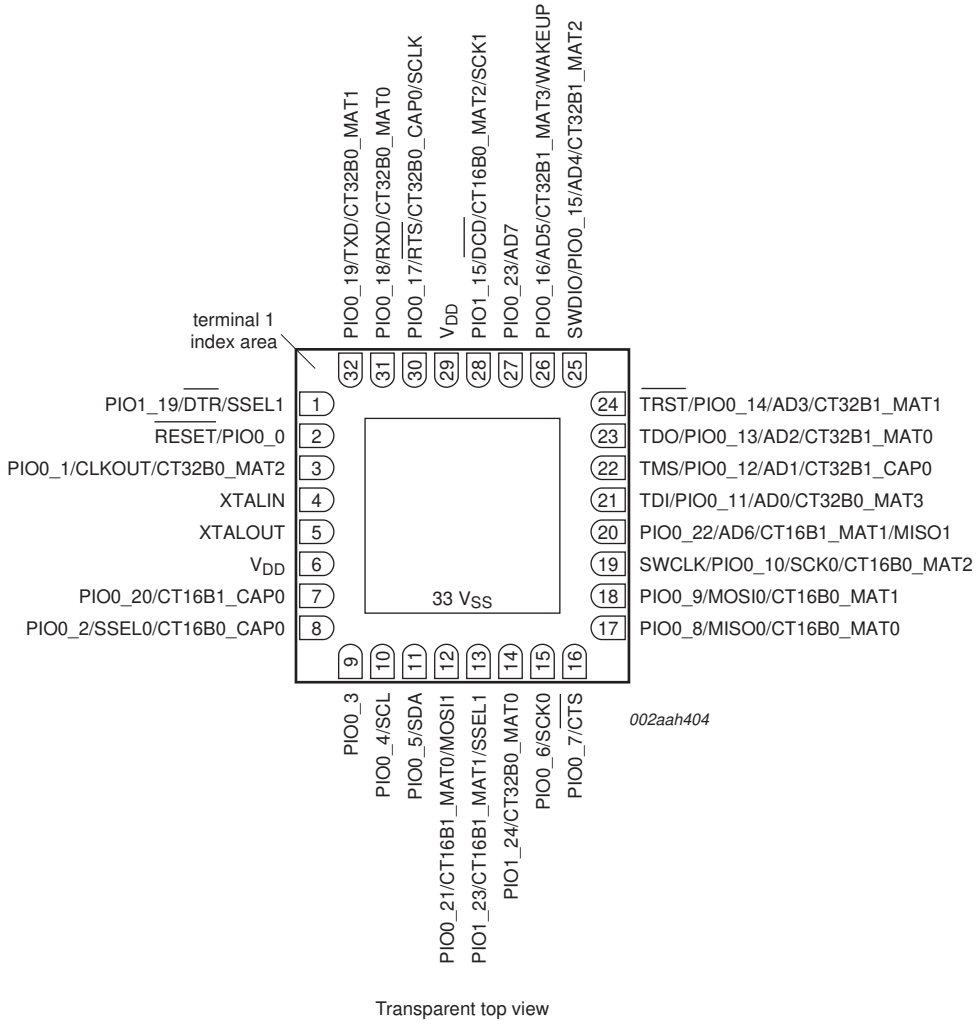
(2) CT16B0_CAP1, CT16B1_CAP1 available on LQFP64 packages only; CT32B0_CAP1 available LQFP48, and LQFP64 packages only; CT32B1_CAP1 available in LQFP64 packages only.

(3) LPC11E37HFBD64/401 only.

Fig 1. Block diagram

6. Pinning information

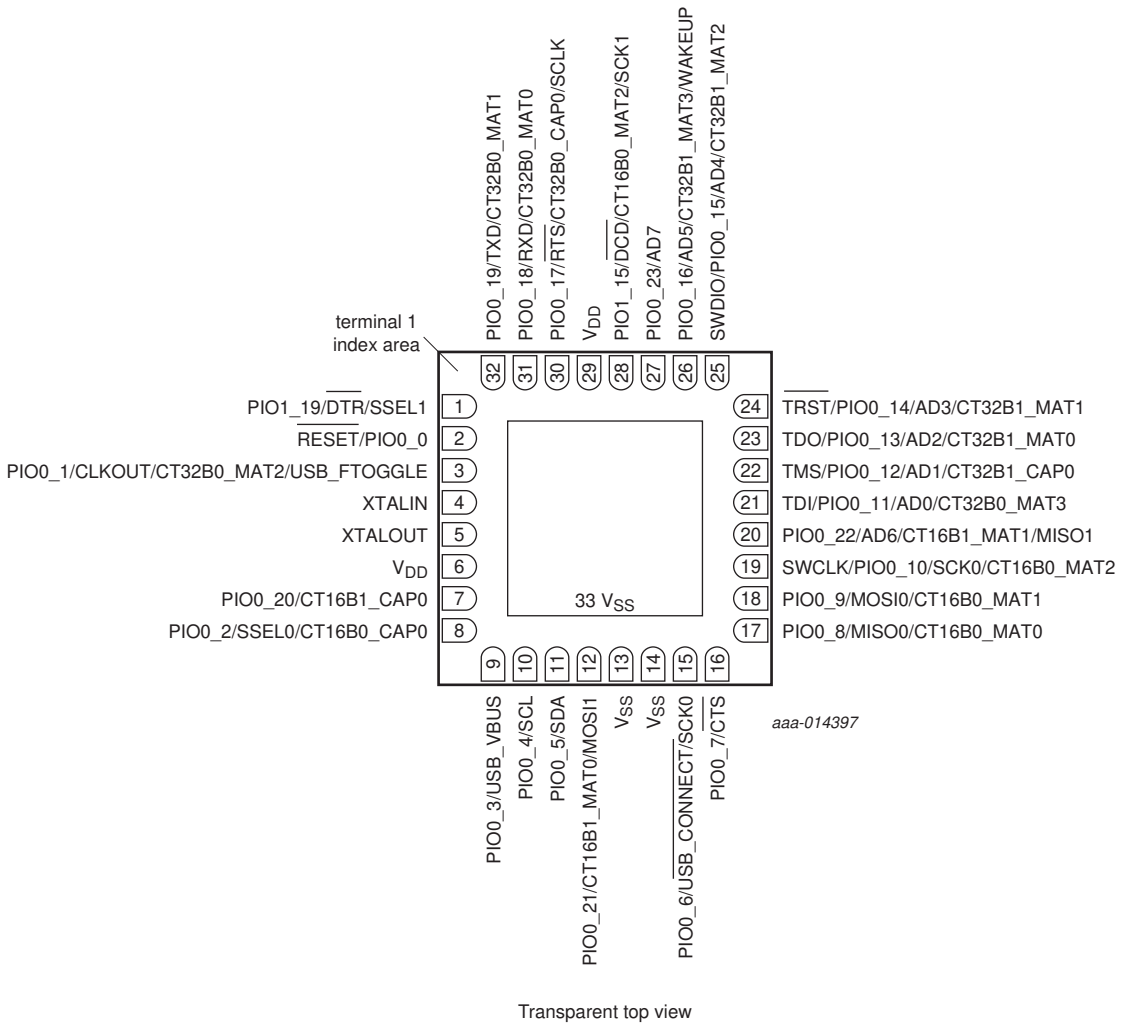
6.1 Pinning



Transparent top view

For parts LPC11E36FHN33/501

Fig 2. Pin configuration (HVQFN33, 7x7)



Transparent top view

For parts LPC11E35FHI33/501

Fig 3. Pin configuration (HVQFN33, 5x5)

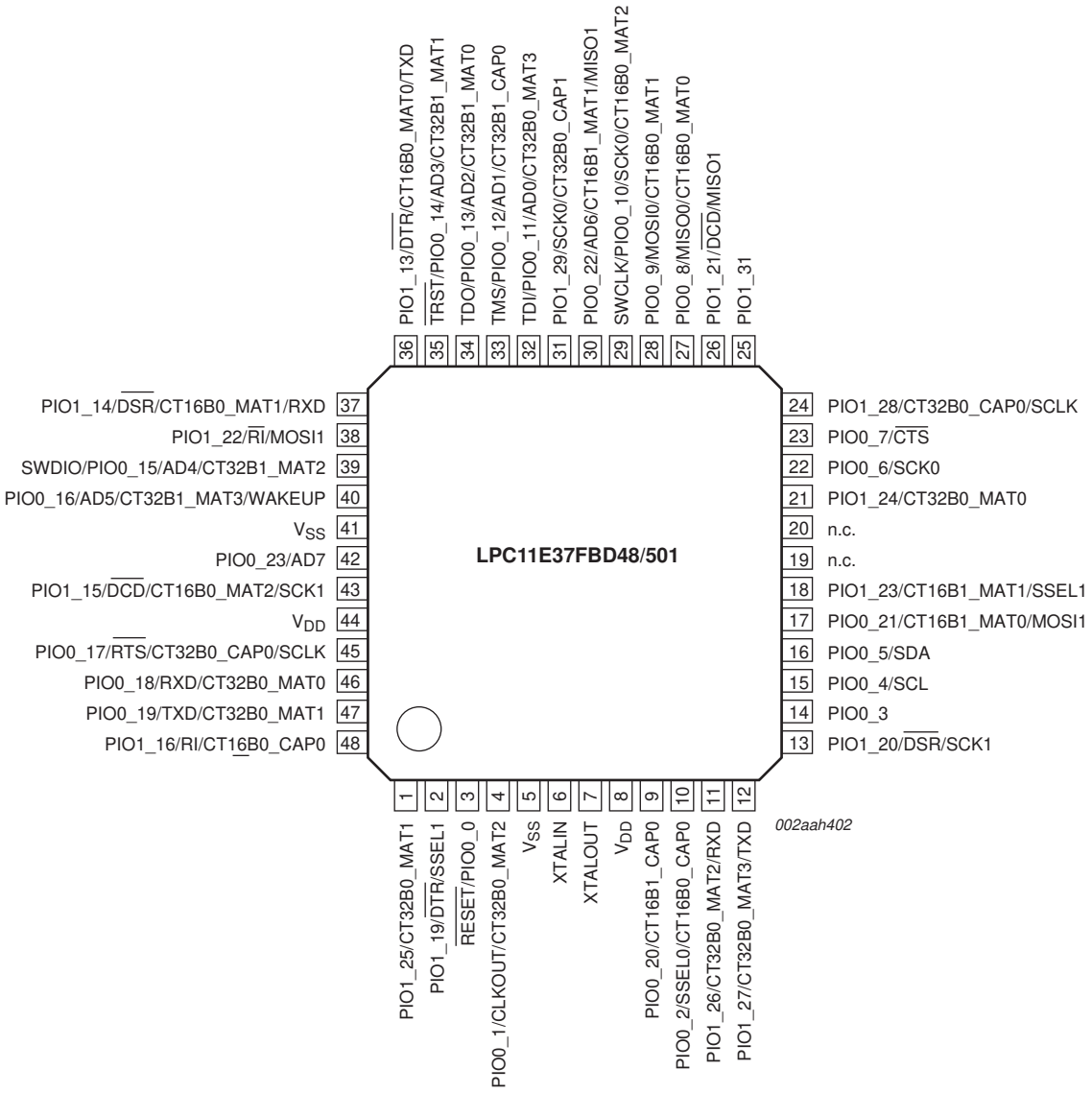
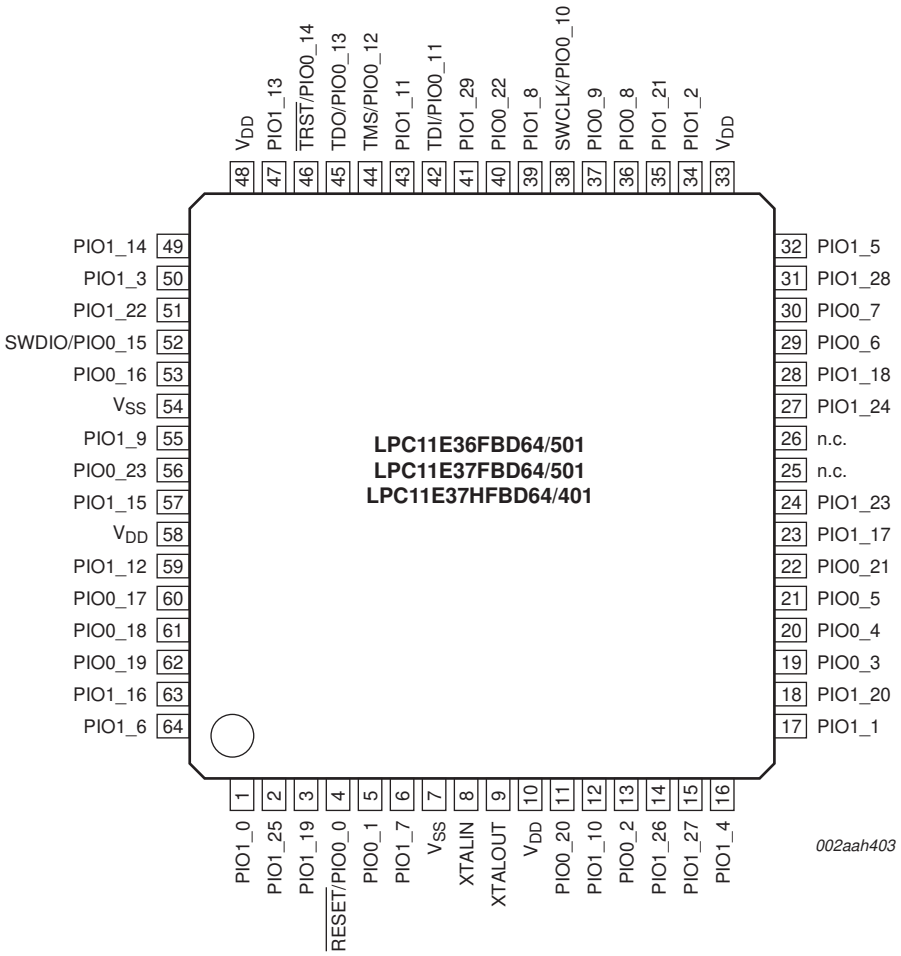


Fig 4. Pin configuration (LQFP48)



See Table 3 for the full pin name.

Fig 5. Pin configuration (LQFP64)

6.2 Pin description

Table 3 shows all pins and their assigned digital or analog functions in order of the GPIO port number. The default function after reset is listed first. All port pins have internal pull-up resistors enabled after reset except for the true open-drain pins PIO0_4 and PIO0_5.

Every port pin has a corresponding IOCON register for programming the digital or analog function, the pull-up/pull-down configuration, the repeater, and the open-drain modes.

The USART, counter/timer, and SSP functions are available on more than one port pin.

Table 3. Pin description

Symbol	Pin HVQFN33 (5x5)	Pin HVQFN33 (7x7)	Pin LQFP48	Pin LQFP64		Reset state [1]	Type	Description
$\overline{\text{RESET}}$/PIO0_0	2	2	3	4	[2]	I; PU	I	**$\overline{\text{RESET}}$ —** External reset input with 20 ns glitch filter. A LOW-going pulse as short as 50 ns on this pin resets the device, causing I/O ports and peripherals to take on their default states, and processor execution to begin at address 0. This pin also serves as the debug select input. LOW level selects the JTAG boundary scan. HIGH level selects the ARM SWD debug mode.
						-	I/O	**PIO0_0 —** General purpose digital input/output pin.
PIO0_1/CLKOUT/ CT32B0_MAT2	3	3	4	5	[3]	I; PU	I/O	**PIO0_1 —** General purpose digital input/output pin. A LOW level on this pin during reset starts the ISP command handler.
						-	O	**CLKOUT —** Clockout pin.
						-	O	**CT32B0_MAT2 —** Match output 2 for 32-bit timer 0.
PIO0_2/SSEL0/ CT16B0_CAP0/IOH_0	8	8	10	13	[3]	I; PU	I/O	**PIO0_2 —** General purpose digital input/output pin.
						-	I/O	**SSEL0 —** Slave select for SSP0.
						-	I	**CT16B0_CAP0 —** Capture input 0 for 16-bit timer 0.
						-	I/O	**IOH_0 —** I/O Handler input/output 0. LPC11E37HFBD64/401 only.
PIO0_3/R/IOH_1	9	9	14	19	[3]	I; PU	I/O	**PIO0_3 —** General purpose digital input/output pin.
						-	-	**R —** Reserved.
						-	I/O	**IOH_1 —** I/O Handler input/output 1. LPC11E37HFBD64/401 only.

Table 3. Pin description

Symbol	Pin HVQFN33 (5x5)	Pin HVQFN33 (7x7)	Pin LQFP48	Pin LQFP64		Reset state [1]	Type	Description
PIO0_4/SCL/IOH_2	10	10	15	20	[4]	I; IA	I/O	**PIO0_4 —** General purpose digital input/output pin (open-drain).
						-	I/O	**SCL —** I^2C-bus clock input/output (open-drain). High-current sink only if I^2C Fast-mode Plus is selected in the I/O configuration register.
						-	I/O	**IOH_2 —** I/O Handler input/output 2. LPC11E37HFBD64/401 only.
PIO0_5/SDA/IOH_3	11	11	16	21	[4]	I; IA	I/O	**PIO0_5 —** General purpose digital input/output pin (open-drain).
						-	I/O	**SDA —** I^2C-bus data input/output (open-drain). High-current sink only if I^2C Fast-mode Plus is selected in the I/O configuration register.
						-	I/O	**IOH_3 —** I/O Handler input/output 3. LPC11E37HFBD64/401 only.
PIO0_6/R/ SCK0/IOH_4	15	15	22	29	[3]	I; PU	I/O	**PIO0_6 —** General purpose digital input/output pin.
						-	-	**R —** Reserved.
						-	I/O	**SCK0 —** Serial clock for SSP0.
						-	I/O	**IOH_4 —** I/O Handler input/output 4. LPC11E37HFBD64/401 only.
PIO0_7/$\overline{\text{CTS}}$/IOH_5	16	16	23	30	[5]	I; PU	I/O	**PIO0_7 —** General purpose digital input/output pin (high-current output driver).
						-	I	**$\overline{\text{CTS}}$ —** Clear To Send input for USART.
						-	I/O	**IOH_5 —** I/O Handler input/output 5. LPC11E37HFBD64/401 only.
PIO0_8/MISO0/ CT16B0_MAT0/R/IOH_6	17	17	27	36	[3]	I; PU	I/O	**PIO0_8 —** General purpose digital input/output pin.
						-	I/O	**MISO0 —** Master In Slave Out for SSP0.
						-	O	**CT16B0_MAT0 —** Match output 0 for 16-bit timer 0.
						-	-	Reserved.
						-	I/O	**IOH_6 —** I/O Handler input/output 6. LPC11E37HFBD64/401 only.
PIO0_9/MOSI0/ CT16B0_MAT1/R/IOH_7	18	18	28	37	[3]	I; PU	I/O	**PIO0_9 —** General purpose digital input/output pin.
						-	I/O	**MOSI0 —** Master Out Slave In for SSP0.
						-	O	**CT16B0_MAT1 —** Match output 1 for 16-bit timer 0.
						-	-	Reserved.
						-	I/O	**IOH_7 —** I/O Handler input/output 7. LPC11E37HFBD64/401 only.

Table 3. Pin description

Symbol	Pin HVQFN33 (5x5)	Pin HVQFN33 (7x7)	Pin LQFP48	Pin LQFP64		Reset state [1]	Type	Description
SWCLK/PIO0_10/SCK0/ CT16B0_MAT2	19	19	29	38	[3]	I; PU	I	**SWCLK —** Serial wire clock and test clock TCK for JTAG interface.
						-	I/O	**PIO0_10 —** General purpose digital input/output pin.
						-	O	**SCK0 —** Serial clock for SSP0.
						-	O	**CT16B0_MAT2 —** Match output 2 for 16-bit timer 0.
TDI/PIO0_11/AD0/ CT32B0_MAT3	21	21	32	42	[6]	I; PU	I	**TDI —** Test Data In for JTAG interface.
						-	I/O	**PIO0_11 —** General purpose digital input/output pin.
						-	I	**AD0 —** A/D converter, input 0.
						-	O	**CT32B0_MAT3 —** Match output 3 for 32-bit timer 0.
TMS/PIO0_12/AD1/ CT32B1_CAP0	22	22	33	44	[6]	I; PU	I	**TMS —** Test Mode Select for JTAG interface.
						-	I/O	**PIO_12 —** General purpose digital input/output pin.
						-	I	**AD1 —** A/D converter, input 1.
						-	I	**CT32B1_CAP0 —** Capture input 0 for 32-bit timer 1.
TDO/PIO0_13/AD2/ CT32B1_MAT0	23	23	34	45	[6]	I; PU	O	**TDO —** Test Data Out for JTAG interface.
						-	I/O	**PIO0_13 —** General purpose digital input/output pin.
						-	I	**AD2 —** A/D converter, input 2.
						-	O	**CT32B1_MAT0 —** Match output 0 for 32-bit timer 1.
$\overline{\text{TRST}}$/PIO0_14/AD3/ CT32B1_MAT1	24	24	35	46	[6]	I; PU	I	**$\overline{\text{TRST}}$ —** Test Reset for JTAG interface.
						-	I/O	**PIO0_14 —** General purpose digital input/output pin.
						-	I	**AD3 —** A/D converter, input 3.
						-	O	**CT32B1_MAT1 —** Match output 1 for 32-bit timer 1.
SWDIO/PIO0_15/AD4/ CT32B1_MAT2	25	25	39	52	[6]	I; PU	I/O	**SWDIO —** Serial wire debug input/output.
						-	I/O	**PIO0_15 —** General purpose digital input/output pin.
						-	I	**AD4 —** A/D converter, input 4.
						-	O	**CT32B1_MAT2 —** Match output 2 for 32-bit timer 1.

Table 3. Pin description

Symbol	Pin HVQFN33 (5x5)	Pin HVQFN33 (7x7)	Pin LQFP48	Pin LQFP64		Reset state [1]	Type	Description
PIO0_16/AD5/ CT32B1_MAT3/IOH_8/ WAKEUP	26	26	40	53	[6]	I; PU	I/O	**PIO0_16 —** General purpose digital input/output pin.
						-	I	**AD5 —** A/D converter, input 5.
						-	O	**CT32B1_MAT3 —** Match output 3 for 32-bit timer 1.
						-	I/O	**IOH_8 —** I/O Handler input/output 8. LPC11E37HFBD64/401 only.
						-	I	**WAKEUP —** Deep power-down mode wake-up pin with 20 ns glitch filter. Pull this pin HIGH externally before entering Deep power-down mode, then pull LOW to exit Deep power-down mode. A LOW-going pulse as short as 50 ns wakes up the part.
PIO0_17/$\overline{\text{RTS}}$/ CT32B0_CAP0/SCLK	30	30	45	60	[3]	I; PU	I/O	**PIO0_17 —** General purpose digital input/output pin.
						-	O	**$\overline{\text{RTS}}$ —** Request To Send output for USART.
						-	I	**CT32B0_CAP0 —** Capture input 0 for 32-bit timer 0.
						-	I/O	**SCLK —** Serial clock input/output for USART in synchronous mode.
PIO0_18/RXD/ CT32B0_MAT0	31	31	46	61	[3]	I; PU	I/O	**PIO0_18 —** General purpose digital input/output pin.
						-	I	**RXD —** Receiver input for USART. Used in UART ISP mode.
						-	O	**CT32B0_MAT0 —** Match output 0 for 32-bit timer 0.
PIO0_19/TXD/ CT32B0_MAT1	32	32	47	62	[3]	I; PU	I/O	**PIO0_19 —** General purpose digital input/output pin.
						-	O	**TXD —** Transmitter output for USART. Used in UART ISP mode.
						-	O	**CT32B0_MAT1 —** Match output 1 for 32-bit timer 0.
PIO0_20/CT16B1_CAP0	7	7	9	11	[3]	I; PU	I/O	**PIO0_20 —** General purpose digital input/output pin.
						-	I	**CT16B1_CAP0 —** Capture input 0 for 16-bit timer 1.
PIO0_21/CT16B1_MAT0/ MOSI1	12	12	17	22	[3]	I; PU	I/O	**PIO0_21 —** General purpose digital input/output pin.
						-	O	**CT16B1_MAT0 —** Match output 0 for 16-bit timer 1.
						-	I/O	**MOSI1 —** Master Out Slave In for SSP1.

Table 3. Pin description

Symbol	Pin HVQFN33 (5x5)	Pin HVQFN33 (7x7)	Pin LQFP48	Pin LQFP64		Reset state [1]	Type	Description
PIO0_22/AD6/ CT16B1_MAT1/MISO1	20	20	30	40	[6]	I; PU	I/O	**PIO0_22 —** General purpose digital input/output pin.
						-	I	**AD6 —** A/D converter, input 6.
						-	O	**CT16B1_MAT1 —** Match output 1 for 16-bit timer 1.
						-	I/O	**MISO1 —** Master In Slave Out for SSP1.
PIO0_23/AD7/IOH_9	27	27	42	56	[6]	I; PU	I/O	**PIO0_23 —** General purpose digital input/output pin.
						-	I	**AD7 —** A/D converter, input 7.
						-	I/O	**IOH_9 —** I/O Handler input/output 9. LPC11E37HFBD64/401 only.
PIO1_0/CT32B1_MAT0/ IOH_10	-	-	-	1	[3]	I; PU	I/O	**PIO1_0 —** General purpose digital input/output pin.
						-	O	**CT32B1_MAT0 —** Match output 0 for 32-bit timer 1.
						-	I/O	**IOH_10 —** I/O Handler input/output 10. LPC11E37HFBD64/401 only.
PIO1_1/CT32B1_MAT1/ IOH_11	-	-	-	17	[3]	I; PU	I/O	**PIO1_1 —** General purpose digital input/output pin.
						-	O	**CT32B1_MAT1 —** Match output 1 for 32-bit timer 1.
						-	I/O	**IOH_11 —** I/O Handler input/output 11. LPC11E37HFBD64/401 only.
PIO1_2/CT32B1_MAT2/ IOH_12	-	-	-	34	[3]	I; PU	I/O	**PIO1_2 —** General purpose digital input/output pin.
						-	O	**CT32B1_MAT2 —** Match output 2 for 32-bit timer 1.
						-	I/O	**IOH_12 —** I/O Handler input/output 12. LPC11E37HFBD64/401 only.
PIO1_3/CT32B1_MAT3/ IOH_13	-	-	-	50	[3]	I; PU	I/O	**PIO1_3 —** General purpose digital input/output pin.
						-	O	**CT32B1_MAT3 —** Match output 3 for 32-bit timer 1.
						-	I/O	**IOH_13 —** I/O Handler input/output 13. (LPC11E37HFBD64/401 only.)
PIO1_4/CT32B1_CAP0/ IOH_14	-	-	-	16	[3]	I; PU	I/O	**PIO1_4 —** General purpose digital input/output pin.
						-	I	**CT32B1_CAP0 —** Capture input 0 for 32-bit timer 1.
						-	I/O	**IOH_14 —** I/O Handler input/output 14. (LPC11E37HFBD64/401 only.)

Table 3. Pin description

Symbol	Pin HVQFN33 (5x5)	Pin HVQFN33 (7x7)	Pin LQFP48	Pin LQFP64		Reset state [1]	Type	Description
PIO1_5/CT32B1_CAP1/ IOH_15	-	-	-	32	[3]	I; PU	I/O	**PIO1_5 —** General purpose digital input/output pin.
						-	I	**CT32B1_CAP1 —** Capture input 1 for 32-bit timer 1.
						-	I/O	**IOH_15 —** I/O Handler input/output 15. (LPC11E37HFBD64/401 only.)
PIO1_6/IOH_16	-	-	-	64	[3]	I; PU	I/O	**PIO1_6 —** General purpose digital input/output pin.
						-	I/O	**IOH_16 —** I/O Handler input/output 16. (LPC11E37HFBD64/401 only.)
PIO1_7/IOH_17	-	-	-	6	[3]	I; PU	I/O	**PIO1_7 —** General purpose digital input/output pin.
						-	I/O	**IOH_17 —** I/O Handler input/output 17. (LPC11E37HFBD64/401 only.)
PIO1_8/IOH_18	-	-	-	39	[3]	I; PU	I/O	**PIO1_8 —** General purpose digital input/output pin.
						-	I/O	**IOH_18 —** I/O Handler input/output 18. (LPC11E37HFBD64/401 only.)
PIO1_9	-	-	-	55	[3]	I; PU	I/O	**PIO1_9 —** General purpose digital input/output pin.
PIO1_10	-	-	-	12	[3]	I; PU	I/O	**PIO1_10 —** General purpose digital input/output pin.
PIO1_11	-	-	-	43	[3]	I; PU	I/O	**PIO1_11 —** General purpose digital input/output pin.
PIO1_12	-	-	-	59	[3]	I; PU	I/O	**PIO1_12 —** General purpose digital input/output pin.
PIO1_13/$\overline{\text{DTR}}$/ CT16B0_MAT0/TXD	-	-	36	47	[3]	I; PU	I/O	**PIO1_13 —** General purpose digital input/output pin.
						-	O	**$\overline{\text{DTR}}$ —** Data Terminal Ready output for USART.
						-	O	**CT16B0_MAT0 —** Match output 0 for 16-bit timer 0.
						-	O	**TXD —** Transmitter output for USART.
PIO1_14/$\overline{\text{DSR}}$/ CT16B0_MAT1/RXD	-	-	37	49	[3]	I; PU	I/O	**PIO1_14 —** General purpose digital input/output pin.
						-	I	**$\overline{\text{DSR}}$ —** Data Set Ready input for USART.
						-	O	**CT16B0_MAT1 —** Match output 1 for 16-bit timer 0.
						-	I	**RXD —** Receiver input for USART.

Table 3. Pin description

Symbol	Pin HVQFN33 (5x5)	Pin HVQFN33 (7x7)	Pin LQFP48	Pin LQFP64		Reset state [1]	Type	Description
PIO1_15/$\overline{\text{DCD}}$/ CT16B0_MAT2/SCK1	28	28	43	57	[3]	I; PU	I/O	**PIO1_15** — General purpose digital input/output pin.
							I	**$\overline{\text{DCD}}$** — Data Carrier Detect input for USART.
						-	O	**CT16B0_MAT2** — Match output 2 for 16-bit timer 0.
						-	I/O	**SCK1** — Serial clock for SSP1.
PIO1_16/$\overline{\text{RI}}$/ CT16B0_CAP0	-	-	48	63	[3]	I; PU	I/O	**PIO1_16** — General purpose digital input/output pin.
						-	I	**$\overline{\text{RI}}$** — Ring Indicator input for USART.
						-	I	**CT16B0_CAP0** — Capture input 0 for 16-bit timer 0.
PIO1_17/CT16B0_CAP1/ RXD	-	-	-	23	[3]	I; PU	I/O	**PIO1_17** — General purpose digital input/output pin.
						-	I	**CT16B0_CAP1** — Capture input 1 for 16-bit timer 0.
						-	I	**RXD** — Receiver input for USART.
PIO1_18/CT16B1_CAP1/ TXD	-	-	-	28	[3]	I; PU	I/O	**PIO1_18** — General purpose digital input/output pin.
						-	I	**CT16B1_CAP1** — Capture input 1 for 16-bit timer 1.
						-	O	**TXD** — Transmitter output for USART.
PIO1_19/$\overline{\text{DTR}}$/SSEL1	1	1	2	3	[3]	I; PU	I/O	**PIO1_19** — General purpose digital input/output pin.
						-	O	**$\overline{\text{DTR}}$** — Data Terminal Ready output for USART.
						-	I/O	**SSEL1** — Slave select for SSP1.
PIO1_20/$\overline{\text{DSR}}$/SCK1	-	-	13	18	[3]	I; PU	I/O	**PIO1_20** — General purpose digital input/output pin.
						-	I	**$\overline{\text{DSR}}$** — Data Set Ready input for USART.
						-	I/O	**SCK1** — Serial clock for SSP1.
PIO1_21/$\overline{\text{DCD}}$/MISO1	-	-	26	35	[3]	I; PU	I/O	**PIO1_21** — General purpose digital input/output pin.
						-	I	**$\overline{\text{DCD}}$** — Data Carrier Detect input for USART.
						-	I/O	**MISO1** — Master In Slave Out for SSP1.
PIO1_22/$\overline{\text{RI}}$/MOSI1	-	-	38	51	[3]	I; PU	I/O	**PIO1_22** — General purpose digital input/output pin.
						-	I	**$\overline{\text{RI}}$** — Ring Indicator input for USART.
						-	I/O	**MOSI1** — Master Out Slave In for SSP1.

Table 3. Pin description

Symbol	Pin HVQFN33 (5x5)	Pin HVQFN33 (7x7)	Pin LQFP48	Pin LQFP64		Reset state [1]	Type	Description
PIO1_23/CT16B1_MAT1/ SSEL1	-	13	18	24	[3]	I; PU	I/O	**PIO1_23 —** General purpose digital input/output pin.
						-	O	**CT16B1_MAT1 —** Match output 1 for 16-bit timer 1.
						-	I/O	**SSEL1 —** Slave select for SSP1.
PIO1_24/CT32B0_MAT0	-	14	21	27	[3]	I; PU	I/O	**PIO1_24 —** General purpose digital input/output pin.
						-	O	**CT32B0_MAT0 —** Match output 0 for 32-bit timer 0.
PIO1_25/CT32B0_MAT1	-	-	1	2	[3]	I; PU	I/O	**PIO1_25 —** General purpose digital input/output pin.
						-	O	**CT32B0_MAT1 —** Match output 1 for 32-bit timer 0.
PIO1_26/CT32B0_MAT2/ RXD/IOH_19	-	-	11	14	[3]	I; PU	I/O	**PIO1_26 —** General purpose digital input/output pin.
						-	O	**CT32B0_MAT2 —** Match output 2 for 32-bit timer 0.
						-	I	**RXD —** Receiver input for USART.
						-	I/O	**IOH_19 —** I/O Handler input/output 18. (LPC11E37HFBD64/401 only.)
PIO1_27/CT32B0_MAT3/ TXD/IOH_20	-	-	12	15	[3]	I; PU	I/O	**PIO1_27 —** General purpose digital input/output pin.
						-	O	**CT32B0_MAT3 —** Match output 3 for 32-bit timer 0.
						-	O	**TXD —** Transmitter output for USART.
						-	I/O	**IOH_20 —** I/O Handler input/output 20. (LPC11E37HFBD64/401 only.)
PIO1_28/CT32B0_CAP0/ SCLK	-	-	24	31	[3]	I; PU	I/O	**PIO1_28 —** General purpose digital input/output pin.
						-	I	**CT32B0_CAP0 —** Capture input 0 for 32-bit timer 0.
						-	I/O	**SCLK —** Serial clock input/output for USART in synchronous mode.
PIO1_29/SCK0/ CT32B0_CAP1	-	-	31	41	[3]	I; PU	I/O	**PIO1_29 —** General purpose digital input/output pin.
						-	I/O	**SCK0 —** Serial clock for SSP0.
						-	I	**CT32B0_CAP1 —** Capture input 1 for 32-bit timer 0.
PIO1_31	-	-	25	-	[3]	I; PU	I/O	**PIO1_31 —** General purpose digital input/output pin.
n.c.	-	-	19	25		-	-	Not connected.
n.c.	-	-	20	26		-	-	Not connected.

Table 3. Pin description

Symbol	Pin HVQFN33 (5x5)	Pin HVQFN33 (7x7)	Pin LQFP48	Pin LQFP64		Reset state [1]	Type	Description
XTALIN	4	4	6	8	[7]	-	-	Input to the oscillator circuit and internal clock generator circuits. Input voltage must not exceed 1.8 V.
XTALOUT	5	5	7	9	[7]	-	-	Output from the oscillator amplifier.
V_{DD}	6; 29	6; 29	8; 44	10; 33; 48; 58		-	-	Supply voltage to the internal regulator, the external rail, and the ADC. Also used as the ADC reference voltage.
V_{SS}	33; 13; 14	33	5; 41	7; 54		-	-	Ground.

[1] Pin state at reset for default function: I = Input; O = Output; PU = internal pull-up enabled; IA = inactive, no pull-up/down enabled; F = floating; If the pins are not used, tie floating pins to ground or power to minimize power consumption.

[2] 5 V tolerant pad. $\overline{\text{RESET}}$ functionality is not available in Deep power-down mode. Use the WAKEUP pin to reset the chip and wake up from Deep power-down mode. An external pull-up resistor is required on this pin for the Deep power-down mode. See Figure 29 for the reset pad configuration.

[3] 5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors and configurable hysteresis (see Figure 28).

[4] I^2C-bus pins compliant with the I^2C-bus specification for I^2C standard mode, I^2C Fast-mode, and I^2C Fast-mode Plus.

[5] 5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors and configurable hysteresis (see Figure 28); includes high-current output driver.

[6] 5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors, configurable hysteresis, and analog input. When configured as a ADC input, digital section of the pad is disabled and the pin is not 5 V tolerant (see Figure 28); includes digital input glitch filter.

[7] When the system oscillator is not used, connect XTALIN and XTALOUT as follows: XTALIN can be left floating or can be grounded (grounding is preferred to reduce susceptibility to noise). Leave XTALOUT floating.

7. Functional description

7.1 On-chip flash programming memory

The LPC11E3x contain up to 128 kB on-chip flash program memory. The flash can be programmed using In-System Programming (ISP) or In-Application Programming (IAP) via the on-chip boot loader software.

The flash memory is divided into 4 kB sectors with each sector consisting of 16 pages. Individual pages can be erased using the IAP erase page command.

7.2 EEPROM

The LPC11E3x contain 4 kB of on-chip byte-erasable and byte-programmable EEPROM data memory. The EEPROM can be programmed using In-Application Programming (IAP) via the on-chip boot loader software.

7.3 SRAM

The LPC11E3x contain a total of 10 kB (LPC11E37HFBD64/401) or 12 kB on-chip static RAM memory.

On the LPC11E37HFBD64/401, the 2 kB SRAM1 region at location 0x2000 0000 to 0x2000 07FFF is used for the I/O Handler software library. Do not use this memory location for data or other user code.

7.4 On-chip ROM

The on-chip ROM contains the boot loader and the following Application Programming Interfaces (APIs):

- In-System Programming (ISP) and In-Application Programming (IAP) support for flash including IAP erase page command.
- IAP support for EEPROM.
- Power profiles for configuring power consumption and PLL settings.
- 32-bit integer division routines.

7.5 Memory map

The LPC11E3x incorporates several distinct memory regions, shown in the following figures. Figure 6 shows the overall map of the entire address space from the user program viewpoint following reset. The interrupt vector area supports address remapping.

The AHB (Advanced High-performance Bus) peripheral area is 2 MB in size and is divided to allow for up to 128 peripherals. The APB (Advanced Peripheral Bus) peripheral area is 512 kB in size and is divided to allow for up to 32 peripherals. Each peripheral of either type is allocated 16 kB of space. This addressing scheme allows simplifying the address decoding for each peripheral.

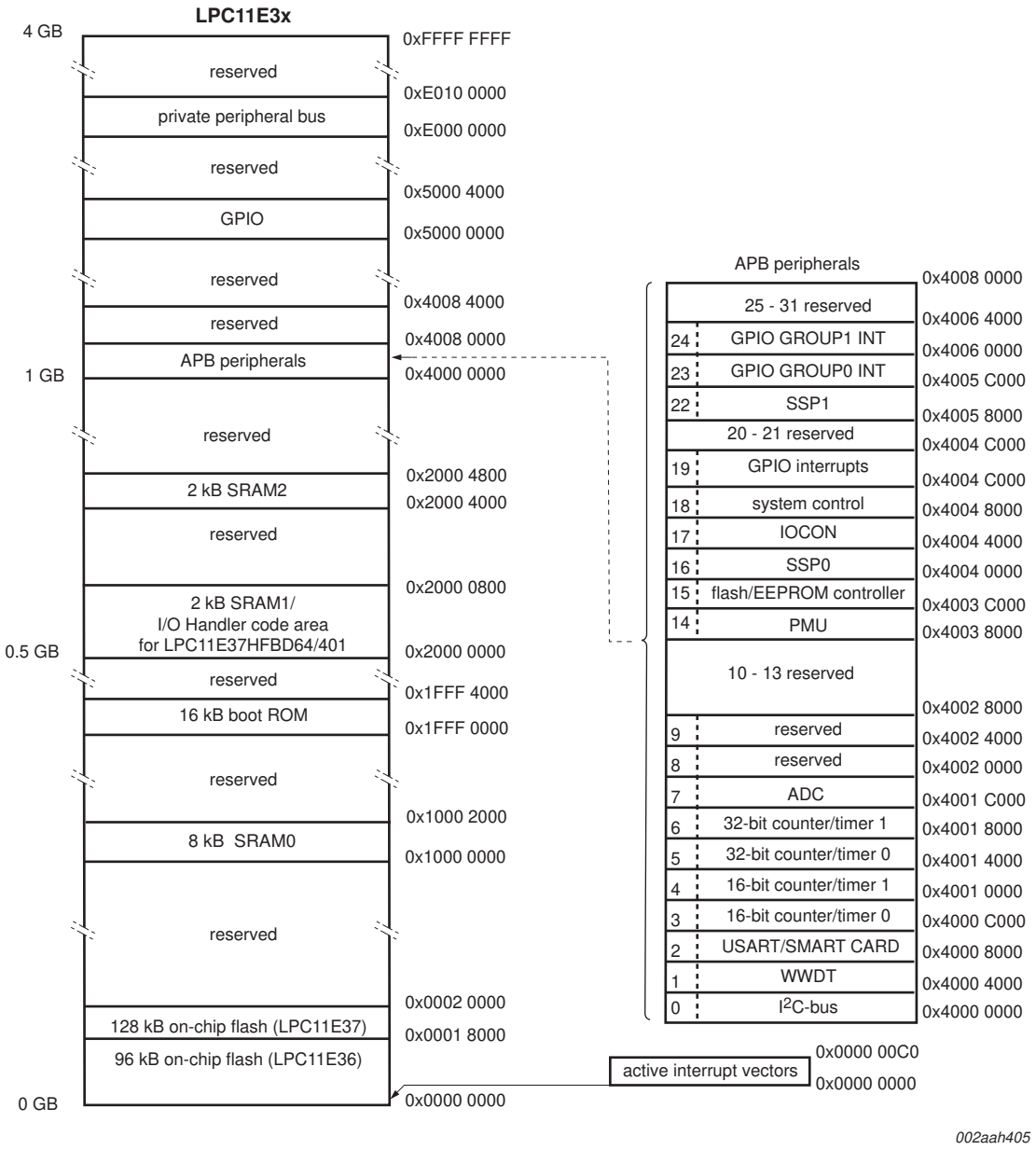


Fig 6. LPC11E3x memory map

7.6 Nested Vectored Interrupt Controller (NVIC)

The Nested Vectored Interrupt Controller (NVIC) is part of the Cortex-M0. The tight coupling to the CPU allows for low interrupt latency and efficient processing of late arriving interrupts.

7.6.1 Features

- Controls system exceptions and peripheral interrupts.
- In the LPC11E3x, the NVIC supports 24 vectored interrupts.

- Four programmable interrupt priority levels, with hardware priority level masking.
- Software interrupt generation.

7.6.2 Interrupt sources

Each peripheral device has one interrupt line connected to the NVIC but can have several interrupt flags. Individual interrupt flags can also represent more than one interrupt source.

7.7 IOCON block

The IOCON block allows selected pins of the microcontroller to have more than one function. Configuration registers control the multiplexers to allow connection between the pin and the on-chip peripherals.

Connect peripherals to the appropriate pins before activating the peripheral and before enabling any related interrupt. . Activity of any enabled peripheral function that is not mapped to a related pin is treated as undefined.

7.7.1 Features

- Programmable pull-up, pull-down, or repeater mode.
- All GPIO pins (except PIO0_4 and PIO0_5) are pulled up to 3.3 V (V_{DD} = 3.3 V) if their pull-up resistor is enabled.
- Programmable pseudo open-drain mode.
- Programmable 10 ns glitch filter on pins PIO0_22, PIO0_23, and PIO0_11 to PIO0_16. The glitch filter is turned on by default.
- Programmable hysteresis.
- Programmable input inverter.

7.8 General-Purpose Input/Output GPIO

The GPIO registers control device pin functions that are not connected to a specific peripheral function. Pins can be dynamically configured as inputs or outputs. Multiple outputs can be set or cleared in one write operation.

LPC11E3x use accelerated GPIO functions:

- GPIO registers are a dedicated AHB peripheral so that the fastest possible I/O timing can be achieved.
- Entire port value can be written in one instruction.

Any GPIO pin providing a digital function can be programmed to generate an interrupt on a level, a rising or falling edge, or both.

The GPIO block consists of three parts:

1. The GPIO ports.
2. The GPIO pin interrupt block to control eight GPIO pins selected as pin interrupts.
3. Two GPIO group interrupt blocks to control two combined interrupts from all GPIO pins.

7.8.1 Features

- GPIO pins can be configured as input or output by software.
- All GPIO pins default to inputs with interrupt disabled at reset.
- Pin registers allow pins to be sensed and set individually.
- Up to eight GPIO pins can be selected from all GPIO pins to create an edge- or level-sensitive GPIO interrupt request.
- Any pin or pins in each port can trigger a port interrupt.

7.9 I/O Handler (LPC11E37HFBD64/401 only)

The I/O Handler is a software library-supported hardware engine for emulating serial interfaces and DMA. The I/O Handler can emulate serial interfaces such as UART, I^2C, or I^2S with no or very low additional CPU load. The software libraries are available with supporting application notes from NXP (see http://www.LPCware.com.) LPCXpresso, Keil, and IAR IDEs are supported. I/O Handler library code must be executed from the memory area 0x2000 0000 to 0x2000 07FF. This memory is not available for other use.

For application examples, see Section 11.7 “I/O Handler software library applications”.

7.10 USART

The LPC11E3x contains one USART.

The USART includes full modem control, support for synchronous mode, and a smart card interface. The RS-485/9-bit mode allows both software address detection and automatic address detection using 9-bit mode.

The USART uses a fractional baud rate generator. Standard baud rates such as 115200 Bd can be achieved with any crystal frequency above 2 MHz.

7.10.1 Features

- Maximum USART data bit rate of 3.125 Mbit/s.
- 16 byte receive and transmit FIFOs.
- Register locations conform to 16C550 industry standard.
- Receiver FIFO trigger points at 1 B, 4 B, 8 B, and 14 B.
- Built-in fractional baud rate generator covering wide range of baud rates without a need for external crystals of particular values.
- Fractional divider for baud rate control, auto baud capabilities and FIFO control mechanism that enables software flow control implementation.
- Support for RS-485/9-bit mode.
- Support for modem control.
- Support for synchronous mode.
- Includes smart card interface.

7.11 SSP serial I/O controller

The SSP controllers operate on a SSP, 4-wire SSI, or Microwire bus. It can interact with multiple masters and slaves on the bus. Only a single master and a single slave can communicate on the bus during a given data transfer. The SSP supports full duplex transfers, with frames of 4 bit to 16 bit of data flowing from the master to the slave and from the slave to the master. In practice, often only one of these data flows carries meaningful data.

7.11.1 Features

- Maximum SSP speed of 25 Mbit/s (master) or 4.17 Mbit/s (slave) (in SSP mode).
- Compatible with Motorola SPI (Serial Peripheral Interface), 4-wire Texas Instruments SSI (Serial Synchronous Interface), and National Semiconductor Microwire buses.
- Synchronous serial communication.
- Master or slave operation.
- 8-frame FIFOs for both transmit and receive.
- 4-bit to 16-bit frame.

7.12 I^2C-bus serial I/O controller

The LPC11E3x contain one I^2C-bus controller.

The I^2C-bus is bidirectional for inter-IC control using only two wires: a Serial CLock line (SCL) and a Serial DAta line (SDA). Each device is recognized by a unique address and can operate as either a receiver-only device (e.g., an LCD driver) or a transmitter with the capability to both receive and send information (such as memory). Transmitters and/or receivers can operate in either master or slave mode, depending on whether the chip has to initiate a data transfer or is only addressed. The I^2C-bus is a multi-master bus, and more than one bus master connected to the interface can be controlled the bus.

7.12.1 Features

- The I^2C-interface is an I^2C-bus compliant interface with open-drain pins. The I^2C-bus interface supports Fast-mode Plus with bit rates up to 1 Mbit/s.
- Easy to configure as master, slave, or master/slave.
- Programmable clocks allow versatile rate control.
- Bidirectional data transfer between masters and slaves.
- Multi-master bus (no central master).
- Arbitration between simultaneously transmitting masters without corruption of serial data on the bus.
- Serial clock synchronization allows devices with different bit rates to communicate via one serial bus.
- Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer.
- The I^2C-bus can be used for test and diagnostic purposes.
- The I^2C-bus controller supports multiple address recognition and a bus monitor mode.

7.13 10-bit ADC

The LPC11E3x contains one ADC. It is a single 10-bit successive approximation ADC with eight channels.

7.13.1 Features

- 10-bit successive approximation ADC.
- Input multiplexing among 8 pins.
- Power-down mode.
- Measurement range 0 V to V_{DD}.
- 10-bit conversion time $\geq$ 2.44 μs (up to 400 kSamples/s).
- Burst conversion mode for single or multiple inputs.
- Optional conversion on transition of input pin or timer match signal.
- Individual result registers for each ADC channel to reduce interrupt overhead.

7.14 General purpose external event counter/timers

The LPC11E3x includes two 32-bit counter/timers and two 16-bit counter/timers. The counter/timer is designed to count cycles of the system derived clock. It can optionally generate interrupts or perform other actions at specified timer values, based on four match registers. Each counter/timer also includes one capture input to trap the timer value when an input signal transitions, optionally generating an interrupt.

7.14.1 Features

- A 32-bit/16-bit timer/counter with a programmable 32-bit/16-bit prescaler.
- Counter or timer operation.
- Up to two capture channels per timer, that can take a snapshot of the timer value when an input signal transitions. A capture event can also generate an interrupt.
- Four match registers per timer that allow:
  - Continuous operation with optional interrupt generation on match.
  - Stop timer on match with optional interrupt generation.
  - Reset timer on match with optional interrupt generation.
- Up to four external outputs corresponding to match registers, with the following capabilities:
  - Set LOW on match.
  - Set HIGH on match.
  - Toggle on match.
  - Do nothing on match.
- The timer and prescaler can be configured to be cleared on a designated capture event. This feature permits easy pulse-width measurement by clearing the timer on the leading edge of an input pulse and capturing the timer value on the trailing edge.

7.15 System tick timer

The ARM Cortex-M0 includes a system tick timer (SYSTICK) that is intended to generate a dedicated SYSTICK exception at a fixed time interval (typically 10 ms).

7.16 Windowed WatchDog Timer (WWDT)

The purpose of the WWDT is to prevent an unresponsive system state. If software fails to update the watchdog within a programmable time window, the watchdog resets the microcontroller

7.16.1 Features

- Internally resets chip if not periodically reloaded during the programmable time-out period.
- Optional windowed operation requires reload to occur between a minimum and maximum time period, both programmable.
- Optional warning interrupt can be generated at a programmable time before watchdog time-out.
- Software enables the WWDT, but a hardware reset or a watchdog reset/interrupt is required to disable the WWDT.
- Incorrect feed sequence causes reset or interrupt, if enabled.
- Flag to indicate watchdog reset.
- Programmable 24-bit timer with internal prescaler.
- Selectable time period from ($T_{cy(WDCLK)} \times 256 \times 4$) to ($T_{cy(WDCLK)} \times 2^{24} \times 4$) in multiples of $T_{cy(WDCLK)} \times 4$.
- The Watchdog Clock (WDCLK) source can be selected from the IRC or the dedicated watchdog oscillator (WDO). The clock source selection provides a wide range of potential timing choices of watchdog operation under different power conditions.

7.17 Clocking and power control

7.17.1 Integrated oscillators

The LPC11E3x include three independent oscillators: the system oscillator, the Internal RC oscillator (IRC), and the watchdog oscillator. Each oscillator can be used for more than one purpose as required in a particular application.

Following reset, the LPC11E3x operates from the internal RC oscillator until software switches to a different clock source. The IRC allows the system to operate without any external crystal and the bootloader code to operate at a known frequency.

See Figure 7 for an overview of the LPC11E3x clock generation.