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LPC11U1x

32-bit ARM Cortex-M0 microcontroller; up to 32 kB flash; 6 kB SRAM; USB device; USART

Rev. 2.2 — 11 March 2014 Product data sheet

1. General description

The LPC11U1x are an ARM Cortex-M0 based, low-cost 32-bit MCU family, designed for 8/16-bit microcontroller applications, offering performance, low power, simple instruction set and memory addressing together with reduced code size compared to existing 8/16-bit architectures.

The LPC11U1x operate at CPU frequencies of up to 50 MHz.

Equipped with a highly flexible and configurable Full Speed USB 2.0 device controller, the LPC11U1x brings unparalleled design flexibility and seamless integration to today's demanding connectivity solutions.

The peripheral complement of the LPC11U1x includes up to 32 kB of flash memory, 6 kB of SRAM data memory, one Fast-mode Plus I^2C-bus interface, one RS-485/EIA-485 USART with support for synchronous mode and smart card interface, two SSP interfaces, four general purpose counter/timers, a 10-bit ADC, and up to 40 general purpose I/O pins.

For additional documentation related to the LPC11U1x parts, see Section 15 "References".

2. Features and benefits

- System:
  - ARM Cortex-M0 processor, running at frequencies of up to 50 MHz.
  - ARM Cortex-M0 built-in Nested Vectored Interrupt Controller (NVIC).
  - Non Maskable Interrupt (NMI) input selectable from several input sources.
  - System tick timer.
- Memory:
  - Up to 32 kB on-chip flash program memory.
  - Total of 6 kB SRAM data memory (4 kB main SRAM and 2 kB USB SRAM).
  - 16 kB boot ROM includes
  - In-System Programming (ISP) and In-Application Programming (IAP) via on-chip bootloader software.
  - ROM-based 32-bit integer division routines.
- Debug options:
  - Standard JTAG test interface for BSDL.
  - Serial Wire Debug.
- Digital peripherals:

- Up to 40 General Purpose I/O (GPIO) pins with configurable pull-up/pull-down resistors, repeater mode, input inverter, and open-drain mode. Eight pins support a programmable glitch filter.
- Up to 8 GPIO pins can be selected as edge and level sensitive interrupt sources.
- Two GPIO grouped interrupt modules enable an interrupt based on a programmable pattern of input states of a group of GPIO pins.
- High-current source output driver (20 mA) on one pin (P0_7).
- High-current sink driver (20 mA) on true open-drain pins (P0_4 and P0_5).
- Four general purpose counter/timers with a total of up to 5 capture inputs and 13 match outputs.
- Programmable Windowed WatchDog Timer (WWDT) with a dedicated, internal low-power WatchDog Oscillator (WDO).

- Analog peripherals:
  - 10-bit ADC with input multiplexing among eight pins.
- Serial interfaces:
  - USB 2.0 full-speed device controller.
  - USART with fractional baud rate generation, internal FIFO, a full modem control handshake interface, and support for RS-485/9-bit mode and synchronous mode. USART supports an asynchronous smart card interface (ISO 7816-3).
  - Two SSP controllers with FIFO and multi-protocol capabilities.
  - I^2C-bus interface supporting the full I^2C-bus specification and Fast-mode Plus with a data rate of up to 1 Mbit/s with multiple address recognition and monitor mode.
- Clock generation:
  - Crystal Oscillator with an operating range of 1 MHz to 25 MHz (system oscillator).
  - 12 MHz high-frequency Internal RC oscillator (IRC) that can optionally be used as a system clock.
  - Internal low-power, low-frequency WatchDog Oscillator (WDO) with programmable frequency output.
  - PLL allows CPU operation up to the maximum CPU rate with the system oscillator or the IRC as clock sources.
  - A second, dedicated PLL is provided for USB.
  - Clock output function with divider that can reflect the crystal oscillator, the main clock, the IRC, or the watchdog oscillator.
- Power control:
  - Four reduced power modes: Sleep, Deep-sleep, Power-down, and Deep power-down.
  - Power profiles residing in boot ROM allow optimized performance and minimized power consumption for any given application through one simple function call.
  - Processor wake-up from Deep-sleep and Power-down modes via reset, selectable GPIO pins, watchdog interrupt, or USB port activity.
  - Processor wake-up from Deep power-down mode using one special function pin.
  - Integrated PMU (Power Management Unit) to minimize power consumption during Sleep, Deep-sleep, Power-down, and Deep power-down modes.
  - Power-On Reset (POR).
  - Brownout detect with four separate thresholds for interrupt and forced reset.
- Unique device serial number for identification.
- Single 3.3 V power supply (1.8 V to 3.6 V).

- Temperature range −40 °C to +85 °C.
- Available as LQFP48, TFBGA48, and HVQFN33 packages.
- Pin compatible to the LPC134x series.

3. Applications

- Consumer peripherals
- Medical
- Industrial control
- Handheld scanners
- USB audio devices

4. Ordering information

Table 1. Ordering information

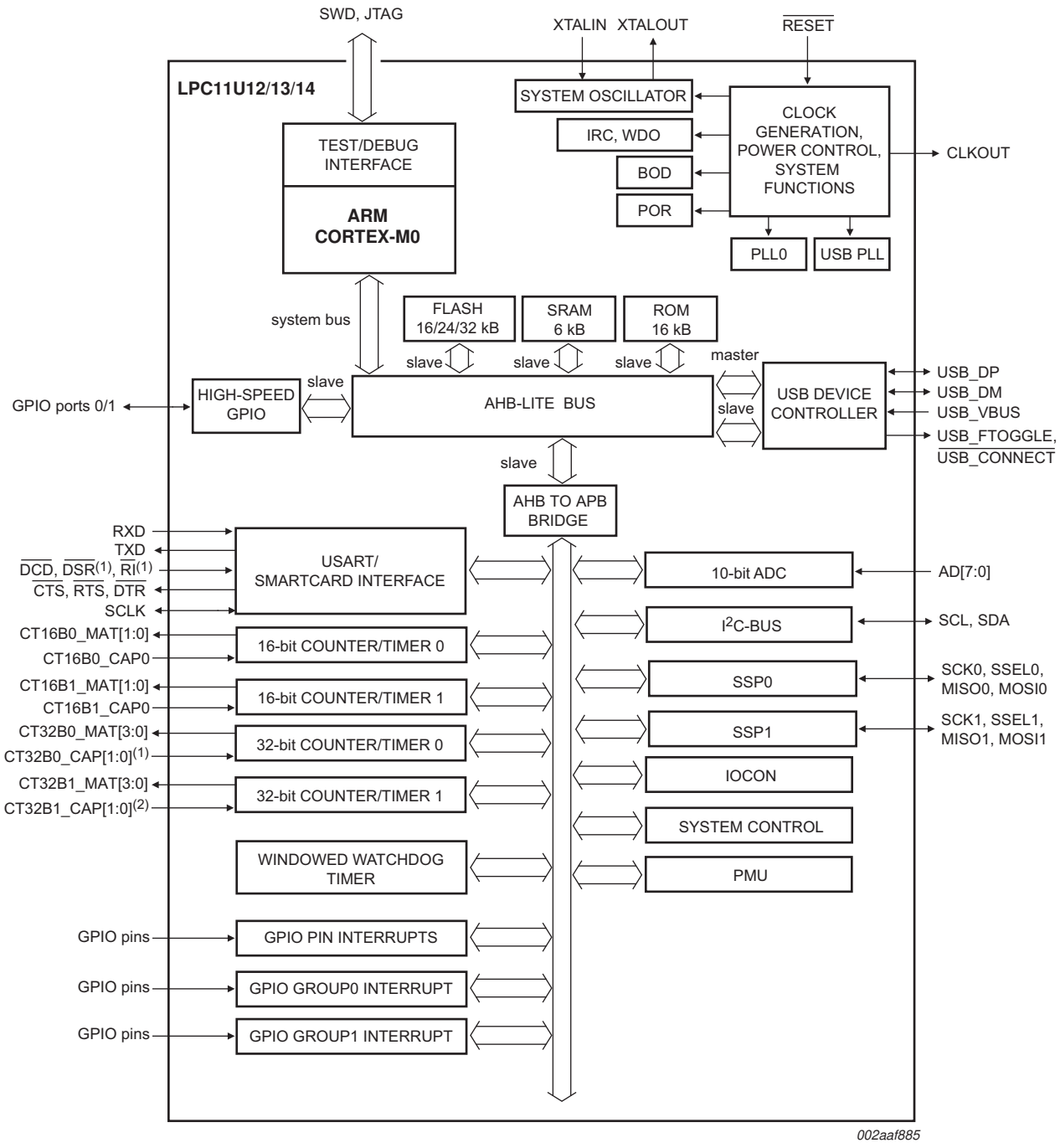
Type number	Package		
	Name	Description	Version
LPC11U12FHN33/201	HVQFN33	plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 7 × 7 × 0.85 mm	n/a
LPC11U12FBD48/201	LQFP48	plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2
LPC11U13FBD48/201	LQFP48	plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2
LPC11U14FHN33/201	HVQFN33	plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 7 × 7 × 0.85 mm	n/a
LPC11U14FHI33/201	HVQFN33	plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 5 × 5 × 0.85 mm	n/a
LPC11U14FBD48/201	LQFP48	plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2
LPC11U14FET48/201	TFBGA48	plastic thin fine-pitch ball grid array package; 48 balls; body 4.5 × 4.5 × 0.7 mm	SOT1155-2

4.1 Ordering options

Table 2. Ordering options

Type number	Flash	SRAM			USART	I^2C-bus FM+	SSP	USB device	ADC channels	GPIO pins
		CPU	USB	Total						
LPC11U12FHN33/201	16 kB	4 kB	2 kB	6 kB	1	1	2	1	8	26
LPC11U12FBD48/201	16 kB	4 kB	2 kB	6 kB	1	1	2	1	8	40
LPC11U13FBD48/201	24 kB	4 kB	2 kB	6 kB	1	1	2	1	8	40
LPC11U14FHN33/201	32 kB	4 kB	2 kB	6 kB	1	1	2	1	8	26
LPC11U14FHI33/201	32 kB	4 kB	2 kB	6 kB	1	1	2	1	8	26
LPC11U14FBD48/201	32 kB	4 kB	2 kB	6 kB	1	1	2	1	8	40
LPC11U14FET48/201	32 kB	4 kB	2 kB	6 kB	1	1	2	1	8	40

5. Block diagram



(1) DSR, RI, CT32B0_CAP1 are not available on HVQFN33 packages.

(2) CT32B1_CAP1 is available only on the TFBGA48package.

Fig 1. Block diagram

6. Pinning information

6.1 Pinning

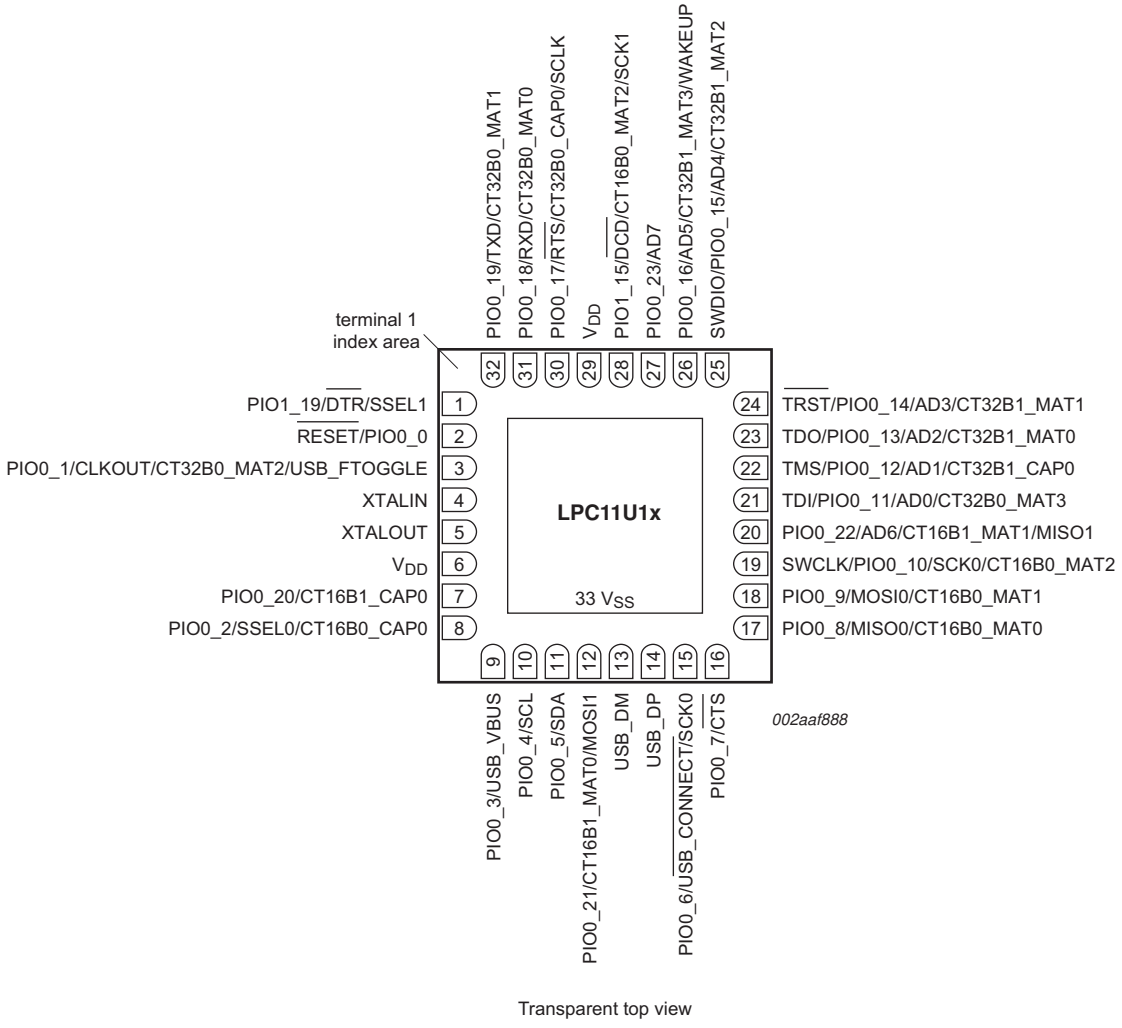


Fig 2. Pin configuration (HVQFN33)

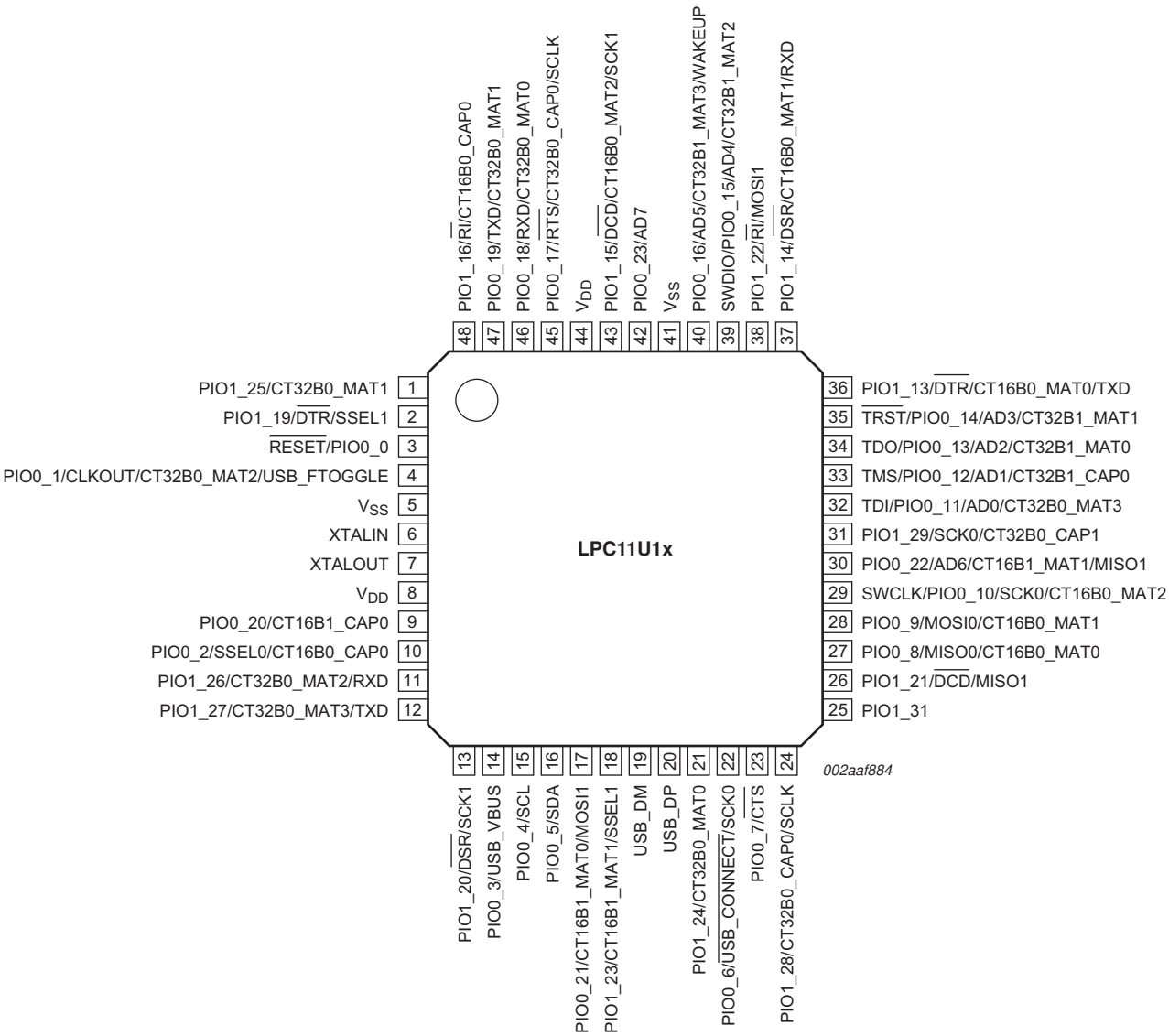


Fig 3. Pin configuration (LQFP48)

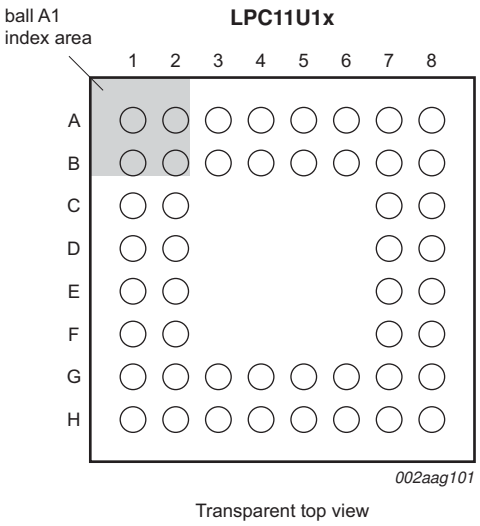


Fig 4. Pin configuration (TFBGA48)

6.2 Pin description

Table 3 shows all pins and their assigned digital or analog functions ordered by GPIO port number. The default function after reset is listed first. All port pins have internal pull-up resistors enabled after reset with the exception of the true open-drain pins PIO0_4 and PIO0_5.

Every port pin has a corresponding IOCON register for programming the digital or analog function, the pull-up/pull-down configuration, the repeater, and the open-drain modes.

The USART, counter/timer, and SSP functions are available on more than one port pin. Table 4 shows how peripheral functions are assigned to port pins.

Table 3. Pin description

Symbol	Pin HVQFN33	Pin LQFP48	Ball TFBGA48	Reset state [1]	Type	Description
$\overline{\text{RESET}}$/PIO0_0	2	3	C1 [2]	I; PU	I	**$\overline{\text{RESET}}$ —** External reset input with 20 ns glitch filter. A LOW-going pulse as short as 50 ns on this pin resets the device, causing I/O ports and peripherals to take on their default states, and processor execution to begin at address 0. This pin also serves as the debug select input. LOW level selects the JTAG boundary scan. HIGH level selects the ARM SWD debug mode. In deep power-down mode, this pin must be pulled HIGH externally. The $\overline{\text{RESET}}$ pin can be left unconnected or be used as a GPIO pin if an external $\overline{\text{RESET}}$ function is not needed and Deep power-down mode is not used.
				-	I/O	**PIO0_0 —** General purpose digital input/output pin.
PIO0_1/CLKOUT/ CT32B0_MAT2/ USB_FTOGGLE	3	4	C2 [3][4]	I; PU	I/O	**PIO0_1 —** General purpose digital input/output pin. A LOW level on this pin during reset starts the ISP command handler.
				-	O	**CLKOUT —** Clockout pin.
				-	O	**CT32B0_MAT2 —** Match output 2 for 32-bit timer 0.
				-	O	**USB_FTOGGLE —** USB 1 ms Start-of-Frame signal.
PIO0_2/SSEL0/ CT16B0_CAP0	8	10	F1 [3]	I; PU	I/O	**PIO0_2 —** General purpose digital input/output pin.
				-	I/O	**SSEL0 —** Slave select for SSP0.
				-	I	**CT16B0_CAP0 —** Capture input 0 for 16-bit timer 0.
PIO0_3/USB_VBUS	9	14	H2 [3]	I; PU	I/O	**PIO0_3 —** General purpose digital input/output pin.
				-	I	**USB_VBUS —** Monitors the presence of USB bus power.

Table 3. Pin description *...continued*

Symbol	Pin HVQFN33	Pin LQFP48	Ball TFBGA48	Reset state [1]	Type	Description
PIO0_4/SCL	10	15	G3 [5]	I; IA	I/O	**PIO0_4 —** General purpose digital input/output pin (open-drain).
				-	I/O	**SCL —** I^2C-bus clock input/output (open-drain). High-current sink only if I^2C Fast-mode Plus is selected in the I/O configuration register.
PIO0_5/SDA	11	16	H3 [5]	I; IA	I/O	**PIO0_5 —** General purpose digital input/output pin (open-drain).
				-	I/O	**SDA —** I^2C-bus data input/output (open-drain). High-current sink only if I^2C Fast-mode Plus is selected in the I/O configuration register.
PIO0_6/$\overline{\text{USB\_CONNECT}}$/SCK0	15	22	H6 [3]	I; PU	I/O	**PIO0_6 —** General purpose digital input/output pin.
				-	O	**$\overline{\text{USB\_CONNECT}}$ —** Signal used to switch an external 1.5 kΩ resistor under software control. Used with the SoftConnect USB feature.
				-	I/O	**SCK0 —** Serial clock for SSP0.
PIO0_7/$\overline{\text{CTS}}$	16	23	G7 [6]	I; PU	I/O	**PIO0_7 —** General purpose digital input/output pin (high-current output driver).
				-	I	**$\overline{\text{CTS}}$ —** Clear To Send input for USART.
PIO0_8/MISO0/CT16B0_MAT0	17	27	F8 [3]	I; PU	I/O	**PIO0_8 —** General purpose digital input/output pin.
				-	I/O	**MISO0 —** Master In Slave Out for SSP0.
				-	O	**CT16B0_MAT0 —** Match output 0 for 16-bit timer 0.
PIO0_9/MOSI0/CT16B0_MAT1	18	28	F7 [3]	I; PU	I/O	**PIO0_9 —** General purpose digital input/output pin.
				-	I/O	**MOSI0 —** Master Out Slave In for SSP0.
				-	O	**CT16B0_MAT1 —** Match output 1 for 16-bit timer 0.
SWCLK/PIO0_10/SCK0/CT16B0_MAT2	19	29	E7 [3]	I; PU	I	**SWCLK —** Serial wire clock and test clock TCK for JTAG interface.
				-	I/O	**PIO0_10 —** General purpose digital input/output pin.
				-	O	**SCK0 —** Serial clock for SSP0.
				-	O	**CT16B0_MAT2 —** Match output 2 for 16-bit timer 0.
TDI/PIO0_11/AD0/CT32B0_MAT3	21	32	D8 [7]	I; PU	I	**TDI —** Test Data In for JTAG interface.
				-	I/O	**PIO0_11 —** General purpose digital input/output pin.
				-	I	**AD0 —** A/D converter, input 0.
				-	O	**CT32B0_MAT3 —** Match output 3 for 32-bit timer 0.

Table 3. Pin description *...continued*

Symbol	Pin HVQFN33	Pin LQFP48	Ball TFBGA48	Reset state [1]	Type	Description
TMS/PIO0_12/AD1/ CT32B1_CAP0	22	33	C7 [7]	I; PU	I	**TMS** — Test Mode Select for JTAG interface.
				-	I/O	**PIO_12** — General purpose digital input/output pin.
				-	I	**AD1** — A/D converter, input 1.
				-	I	**CT32B1_CAP0** — Capture input 0 for 32-bit timer 1.
TDO/PIO0_13/AD2/ CT32B1_MAT0	23	34	C8 [7]	I; PU	O	**TDO** — Test Data Out for JTAG interface.
				-	I/O	**PIO0_13** — General purpose digital input/output pin.
				-	I	**AD2** — A/D converter, input 2.
				-	O	**CT32B1_MAT0** — Match output 0 for 32-bit timer 1.
$\overline{\text{TRST}}$/PIO0_14/AD3/ CT32B1_MAT1	24	35	B7 [7]	I; PU	I	**$\overline{\text{TRST}}$** — Test Reset for JTAG interface.
				-	I/O	**PIO0_14** — General purpose digital input/output pin.
				-	I	**AD3** — A/D converter, input 3.
				-	O	**CT32B1_MAT1** — Match output 1 for 32-bit timer 1.
SWDIO/PIO0_15/AD4/ CT32B1_MAT2	25	39	B6 [7]	I; PU	I/O	**SWDIO** — Serial wire debug input/output.
				-	I/O	**PIO0_15** — General purpose digital input/output pin.
				-	I	**AD4** — A/D converter, input 4.
				-	O	**CT32B1_MAT2** — Match output 2 for 32-bit timer 1.
PIO0_16/AD5/ CT32B1_MAT3/WAKEUP	26	40	A6 [7]	I; PU	I/O	**PIO0_16** — General purpose digital input/output pin.
				-	I	**AD5** — A/D converter, input 5.
				-	O	**CT32B1_MAT3** — Match output 3 for 32-bit timer 1.
				-	I	**WAKEUP** — Deep power-down mode wake-up pin with 20 ns glitch filter. This pin must be pulled HIGH externally to enter Deep power-down mode and pulled LOW to exit Deep power-down mode. A LOW-going pulse as short as 50 ns wakes up the part.
PIO0_17/$\overline{\text{RTS}}$/ CT32B0_CAP0/SCLK	30	45	A3 [3]	I; PU	I/O	**PIO0_17** — General purpose digital input/output pin.
				-	O	**$\overline{\text{RTS}}$** — Request To Send output for USART.
				-	I	**CT32B0_CAP0** — Capture input 0 for 32-bit timer 0.
				-	I/O	**SCLK** — Serial clock input/output for USART in synchronous mode.

Table 3. Pin description *...continued*

Symbol	Pin HVQFN33	Pin LQFP48	Ball TFBGA48	Reset state [1]	Type	Description
PIO0_18/RXD/ CT32B0_MAT0	31	46	B3 [3]	I; PU	I/O	**PIO0_18 —** General purpose digital input/output pin.
				-	I	**RXD —** Receiver input for USART.Used in UART ISP mode.
				-	O	**CT32B0_MAT0 —** Match output 0 for 32-bit timer 0.
PIO0_19/TXD/ CT32B0_MAT1	32	47	B2 [3]	I; PU	I/O	**PIO0_19 —** General purpose digital input/output pin.
				-	O	**TXD —** Transmitter output for USART. Used in UART ISP mode.
				-	O	**CT32B0_MAT1 —** Match output 1 for 32-bit timer 0.
PIO0_20/CT16B1_CAP0	7	9	F2 [3]	I; PU	I/O	**PIO0_20 —** General purpose digital input/output pin.
				-	I	**CT16B1_CAP0 —** Capture input 0 for 16-bit timer 1.
PIO0_21/CT16B1_MAT0/ MOSI1	12	17	G4 [3]	I; PU	I/O	**PIO0_21 —** General purpose digital input/output pin.
				-	O	**CT16B1_MAT0 —** Match output 0 for 16-bit timer 1.
				-	I/O	**MOSI1 —** Master Out Slave In for SSP1.
PIO0_22/AD6/ CT16B1_MAT1/MISO1	20	30	E8 [7]	I; PU	I/O	**PIO0_22 —** General purpose digital input/output pin.
				-	I	**AD6 —** A/D converter, input 6.
				-	O	**CT16B1_MAT1 —** Match output 1 for 16-bit timer 1.
				-	I/O	**MISO1 —** Master In Slave Out for SSP1.
PIO0_23/AD7	27	42	A5 [7]	I; PU	I/O	**PIO0_23 —** General purpose digital input/output pin.
				-	I	**AD7 —** A/D converter, input 7.
PIO1_5/CT32B1_CAP1	-	-	H8 [3]	I; PU	I/O	**PIO1_5 —** General purpose digital input/output pin.
				-	I	**CT32B1_CAP1 —** Capture input 1 for 32-bit timer 1.
PIO1_13/$\overline{\text{DTR}}$/ CT16B0_MAT0/TXD	-	36	B8 [3]	I; PU	I/O	**PIO1_13 —** General purpose digital input/output pin.
				-	O	**$\overline{\text{DTR}}$ —** Data Terminal Ready output for USART.
				-	O	**CT16B0_MAT0 —** Match output 0 for 16-bit timer 0.
				-	O	**TXD —** Transmitter output for USART.

Table 3. Pin description *...continued*

Symbol	Pin HVQFN33	Pin LQFP48	Ball TFBGA48		Reset state [1]	Type	Description
PIO1_14/$\overline{\text{DSR}}$/ CT16B0_MAT1/RXD	-	37	A8	[3]	I; PU	I/O	**PIO1_14 —** General purpose digital input/output pin.
					-	I	**$\overline{\text{DSR}}$ —** Data Set Ready input for USART.
					-	O	**CT16B0_MAT1 —** Match output 1 for 16-bit timer 0.
					-	I	**RXD —** Receiver input for USART.
PIO1_15/$\overline{\text{DCD}}$/ CT16B0_MAT2/SCK1	28	43	A4	[3]	I; PU	I/O	**PIO1_15 —** General purpose digital input/output pin.
						I	**$\overline{\text{DCD}}$ —** Data Carrier Detect input for USART.
					-	O	**CT16B0_MAT2 —** Match output 2 for 16-bit timer 0.
					-	I/O	**SCK1 —** Serial clock for SSP1.
PIO1_16/$\overline{\text{RI}}$/ CT16B0_CAP0	-	48	A2	[3]	I; PU	I/O	**PIO1_16 —** General purpose digital input/output pin.
					-	I	**$\overline{\text{RI}}$ —** Ring Indicator input for USART.
					-	I	**CT16B0_CAP0 —** Capture input 0 for 16-bit timer 0.
PIO1_19/$\overline{\text{DTR}}$/SSEL1	1	2	B1	[3]	I; PU	I/O	**PIO1_19 —** General purpose digital input/output pin.
					-	O	**$\overline{\text{DTR}}$ —** Data Terminal Ready output for USART.
					-	I/O	**SSEL1 —** Slave select for SSP1.
PIO1_20/$\overline{\text{DSR}}$/SCK1	-	13	H1	[3]	I; PU	I/O	**PIO1_20 —** General purpose digital input/output pin.
					-	I	**$\overline{\text{DSR}}$ —** Data Set Ready input for USART.
					-	I/O	**SCK1 —** Serial clock for SSP1.
PIO1_21/$\overline{\text{DCD}}$/MISO1	-	26	G8	[3]	I; PU	I/O	**PIO1_21 —** General purpose digital input/output pin.
					-	I	**$\overline{\text{DCD}}$ —** Data Carrier Detect input for USART.
					-	I/O	**MISO1 —** Master In Slave Out for SSP1.
PIO1_22/$\overline{\text{RI}}$/MOSI1	-	38	A7	[3]	I; PU	I/O	**PIO1_22 —** General purpose digital input/output pin.
					-	I	**$\overline{\text{RI}}$ —** Ring Indicator input for USART.
					-	I/O	**MOSI1 —** Master Out Slave In for SSP1.
PIO1_23/CT16B1_MAT1/ SSEL1	-	18	H4	[3]	I; PU	I/O	**PIO1_23 —** General purpose digital input/output pin.
					-	O	**CT16B1_MAT1 —** Match output 1 for 16-bit timer 1.
					-	I/O	**SSEL1 —** Slave select for SSP1.

Table 3. Pin description *...continued*

Symbol	Pin HVQFN33	Pin LQFP48	Ball TFBGA48	Reset state [1]	Type	Description
PIO1_24/CT32B0_MAT0	-	21	G6 [3]	I; PU	I/O	**PIO1_24 —** General purpose digital input/output pin.
				-	O	**CT32B0_MAT0 —** Match output 0 for 32-bit timer 0.
PIO1_25/CT32B0_MAT1	-	1	A1 [3]	I; PU	I/O	**PIO1_25 —** General purpose digital input/output pin.
				-	O	**CT32B0_MAT1 —** Match output 1 for 32-bit timer 0.
PIO1_26/CT32B0_MAT2/ RXD	-	11	G2 [3]	I; PU	I/O	**PIO1_26 —** General purpose digital input/output pin.
				-	O	**CT32B0_MAT2 —** Match output 2 for 32-bit timer 0.
				-	I	**RXD —** Receiver input for USART.
PIO1_27/CT32B0_MAT3/ TXD	-	12	G1 [3]	I; PU	I/O	**PIO1_27 —** General purpose digital input/output pin.
				-	O	**CT32B0_MAT3 —** Match output 3 for 32-bit timer 0.
				-	O	**TXD —** Transmitter output for USART.
PIO1_28/CT32B0_CAP0/ SCLK	-	24	H7 [3]	I; PU	I/O	**PIO1_28 —** General purpose digital input/output pin.
				-	I	**CT32B0_CAP0 —** Capture input 0 for 32-bit timer 0.
				-	I/O	**SCLK —** Serial clock input/output for USART in synchronous mode.
PIO1_29/SCK0/ CT32B0_CAP1	-	31	D7 [3]	I; PU	I/O	**PIO1_29 —** General purpose digital input/output pin.
				-	I/O	**SCK0 —** Serial clock for SSP0.
				-	I	**CT32B0_CAP1 —** Capture input 1 for 32-bit timer 0.
PIO1_31	-	25	- [3]	I; PU	I/O	**PIO1_31 —** General purpose digital input/output pin.
USB_DM	13	19	G5 [8]	F	-	**USB_DM —** USB bidirectional D− line.
USB_DP	14	20	H5 [8]	F	-	**USB_DP —** USB bidirectional D+ line.
XTALIN	4	6	D1 [9]	-	-	Input to the oscillator circuit and internal clock generator circuits. Input voltage must not exceed 1.8 V.
XTALOUT	5	7	E1 [9]	-	-	Output from the oscillator amplifier.
V_{DD}	6; 29	8; 44	B4, E2	-	-	Supply voltage to the internal regulator, the external rail, and the ADC. Also used as the ADC reference voltage.
V_{SS}	33	5; 41	B5, D2	-	-	Ground.

[1] Pin state at reset for default function: I = Input; O = Output; PU = internal pull-up enabled; IA = inactive, no pull-up/down enabled; F = floating; floating pins, if not used, should be tied to ground or power to minimize power consumption.

[2] 5 V tolerant pad. $\overline{\text{RESET}}$ functionality is not available in Deep power-down mode. Use the WAKEUP pin to reset the chip and wake up from Deep power-down mode. An external pull-up resistor is required on this pin for the Deep power-down mode. See Figure 31 for the reset pad configuration.

[3] 5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors and configurable hysteresis (see Figure 30).

[4] For parts with bootloader version 7.0, both pins (PIO0_1, PIO0_3) must be pulled LOW to enter UART ISP mode.

[5] I^2C-bus pins compliant with the I^2C-bus specification for I^2C standard mode, I^2C Fast-mode, and I^2C Fast-mode Plus. The pin requires an external pull-up to provide output functionality. When power is switched off, this pin is floating and does not disturb the I2C lines. Open-drain configuration applies to all functions on this pin.

[6] 5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors and configurable hysteresis (see Figure 30); includes high-current output driver.

[7] 5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors, configurable hysteresis, and analog input. When configured as a ADC input, digital section of the pad is disabled and the pin is not 5 V tolerant (see Figure 30); includes digital input glitch filter.

[8] Pad provides USB functions. It is designed in accordance with the USB specification, revision 2.0 (Full-speed and Low-speed mode only). This pad is not 5 V tolerant.

[9] When the system oscillator is not used, connect XTALIN and XTALOUT as follows: XTALIN can be left floating or can be grounded (grounding is preferred to reduce susceptibility to noise). XTALOUT should be left floating.

To assign a peripheral function to a port, program the FUNC bits in the port pin's IOCON register with this function. The user must ensure that the assignment of a function to a port pin is unambiguous. Only the debug functions for JTAG and SWD are selected by default in their corresponding IOCON registers. All other functions must be programmed in the IOCON block before they can be used. For details see the *LPC11Uxx user manual*.

Table 4. Multiplexing of peripheral functions

Peripheral	Function	Type	Default	Available on ports				
				HVQFN33/LQFP48/TFBGA48		LQFP48/TFBGA48		TFBGA48
USART	RXD	I	no	PIO0_18	-	PIO1_14	PIO1_26	-
	TXD	O	no	PIO0_19	-	PIO1_13	PIO1_27	-
	$\overline{\text{CTS}}$	I	no	PIO0_7	-	-	-	-
	$\overline{\text{RTS}}$	O	no	PIO0_17	-	-	-	-
	$\overline{\text{DTR}}$	O	no	PIO1_13	PIO1_19	-	-	-
	$\overline{\text{DSR}}$	I	no	-	-	PIO1_14	PIO1_20	-
	$\overline{\text{DCD}}$	I	no	PIO1_15		PIO1_21	-	-
	$\overline{\text{RI}}$	I	no	-		PIO1_16	PIO1_22	-
	SCLK	I/O	no	PIO0_17		PIO1_28	-	-
SSP0	SCK0	I/O	no	PIO0_6	PIO0_10	PIO1_29		-
	SSEL0	I/O	no	PIO0_2	-	-	-	-
	MISO0	I/O	no	PIO0_8	-	-	-	-
	MOSI0	I/O	no	PIO0_9	-	-	-	-
SSP1	SCK1	I/O	no	PIO1_15	-	PIO1_20	-	-
	SSEL1	I/O	no	PIO1_19	-	PIO1_23	-	-
	MISO1	I/O	no	PIO0_22	-	PIO1_21	-	-
	MOSI1	I/O	no	PIO0_21	-	PIO1_22	-	-

Table 4. Multiplexing of peripheral functions *…continued*

Peripheral	Function	Type	Default	Available on ports				
				HVQFN33/LQFP48/TFBGA48		LQFP48/TFBGA48		TFBGA48
CT16B0	CT16B0_CAP0	I	no	PIO0_2	-	PIO1_16	-	-
	CT16B0_MAT0	O	no	PIO0_8	-	PIO1_13	-	-
	CT16B0_MAT1	O	no	PIO0_9	-	PIO1_14	-	-
	CT16B0_MAT2	O	no	PIO0_10	PIO1_15	-	-	-
CT16B1	CT16B1_CAP0	I	no	PIO0_20	-	-	-	-
	CT16B1_MAT0	O	no	PIO0_21	-	-	-	-
	CT16B1_MAT1	O	no	PIO0_22	-	PIO1_23	-	-
CT32B0	CT32B0_CAP0	I	no	PIO0_17	-	PIO1_28	-	-
	CT32B0_CAP1	I	no	PIO1_29	-	-	-	-
	CT32B0_MAT0	O	no	PIO0_18	-	PIO1_24	-	-
	CT32B0_MAT1	O	no	PIO0_19	-	PIO1_25	-	-
	CT32B0_MAT2	O	no	PIO0_1	-	PIO1_26	-	-
	CT32B0_MAT3	O	no	PIO0_11	-	PIO1_27	-	-
CT32B1	CT32B1_CAP0	I	no	PIO0_12		-	-	-
	CT32B1_CAP1	I	no	-	-	-	-	PIO1_5
	CT32B1_MAT0	O	no	PIO0_13	-	-	-	-
	CT32B1_MAT1	O	no	PIO0_14	-	-	-	-
	CT32B1_MAT2	O	no	PIO0_15	-	-	-	-
	CT32B1_MAT3	O	no	PIO0_16	-	-	-	-
ADC	AD0	I	no	PIO0_11	-	-	-	-
	AD1	I	no	PIO0_12	-	-	-	-
	AD2	I	no	PIO0_13	-	-	-	-
	AD3	I	no	PIO0_14	-	-	-	-
	AD4	I	no	PIO0_15	-	-	-	-
	AD5	I	no	PIO0_16	-	-	-	-
	AD6	I	no	PIO0_22	-	-	-	-
	AD7	I	no	PIO0_23	-	-	-	-
USB	USB_VBUS	I	no	PIO0_3	-	-	-	-
	USB_FTOGGLE	O	no	PIO0_1	-	-	-	-
	$\overline{\text{USB\_CONNECT}}$	O	no	PIO0_6	-	-	-	-
CLKOUT	CLKOUT	O	no	PIO0_1	-	-	-	-
JTAG	TDI	I	yes	PIO0_11	-	-	-	-
	TMS	I	yes	PIO0_12	-	-	-	-
	TDO	O	yes	PIO0_13	-	-	-	-
	$\overline{\text{TRST}}$	I	yes	PIO0_14	-	-	-	-
	TCK	I	yes	PIO0_10	-	-	-	-
SWD	SWCLK	I	yes	PIO0_10	-	-	-	-
	SWDIO	I/O	yes	PIO0_15	-	-	-	-

7. Functional description

7.1 On-chip flash programming memory

The LPC11U1x contain up to 32 kB on-chip flash program memory. The flash can be programmed using In-System Programming (ISP) or In-Application Programming (IAP) via the on-chip boot loader software.

7.2 SRAM

The LPC11U1x contain a total of 6 kB on-chip static RAM memory.

7.3 On-chip ROM

The on-chip ROM contains the boot loader and the following Application Programming Interfaces (APIs):

- In-System Programming (ISP) and In-Application Programming (IAP) support for flash programming
- Power profiles for configuring power consumption and PLL settings
- 32-bit integer division routines

7.4 Memory map

The LPC11U1x incorporates several distinct memory regions, shown in the following figures. Figure 5 shows the overall map of the entire address space from the user program viewpoint following reset. The interrupt vector area supports address remapping.

The AHB peripheral area is 2 MB in size and is divided to allow for up to 128 peripherals. The APB peripheral area is 512 kB in size and is divided to allow for up to 32 peripherals. Each peripheral of either type is allocated 16 kB of space. This allows simplifying the address decoding for each peripheral.

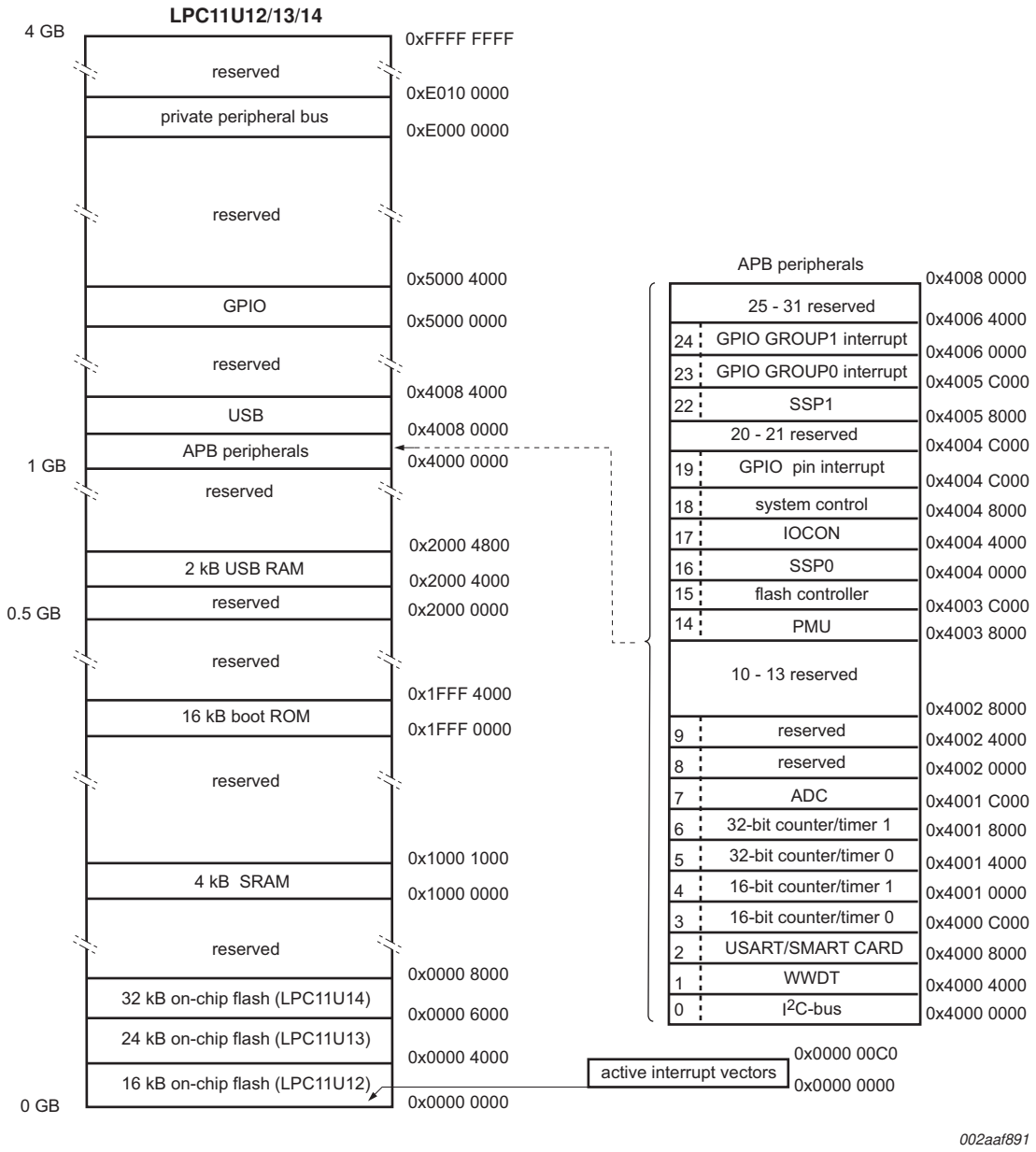


Fig 5. LPC11U1x memory map

7.5 Nested Vectored Interrupt Controller (NVIC)

The Nested Vectored Interrupt Controller (NVIC) is an integral part of the Cortex-M0. The tight coupling to the CPU allows for low interrupt latency and efficient processing of late arriving interrupts.

7.5.1 Features

- Controls system exceptions and peripheral interrupts.
- In the LPC11U1x, the NVIC supports 24 vectored interrupts.

- Four programmable interrupt priority levels, with hardware priority level masking.
- Software interrupt generation.

7.5.2 Interrupt sources

Each peripheral device has one interrupt line connected to the NVIC but may have several interrupt flags. Individual interrupt flags may also represent more than one interrupt source.

7.6 IOCON block

The IOCON block allows selected pins of the microcontroller to have more than one function. Configuration registers control the multiplexers to allow connection between the pin and the on-chip peripherals.

Peripherals should be connected to the appropriate pins prior to being activated and prior to any related interrupts being enabled. Activity of any enabled peripheral function that is not mapped to a related pin should be considered undefined.

7.6.1 Features

- Programmable pull-up, pull-down, or repeater mode.
- All GPIO pins (except PIO0_4 and PIO0_5) are pulled up to 3.3 V (V_{DD} = 3.3 V) if their pull-up resistor is enabled.
- Programmable pseudo open-drain mode.
- Programmable 10-ns glitch filter on pins PIO0_22, PIO0_23, and PIO0_11 to PIO0_16. The glitch filter is turned on by default.
- Programmable hysteresis.
- Programmable input inverter.

7.7 General Purpose Input/Output GPIO

Device pins that are not connected to a specific peripheral function are controlled by the GPIO registers. Pins may be dynamically configured as inputs or outputs. Multiple outputs can be set or cleared in one write operation.

LPC11U1x use accelerated GPIO functions:

- GPIO registers are a dedicated AHB peripheral so that the fastest possible I/O timing can be achieved.
- Entire port value can be written in one instruction.

Any GPIO pin providing a digital function can be programmed to generate an interrupt on a level, a rising or falling edge, or both.

The GPIO block consists of three parts:

1. The GPIO ports.
2. The GPIO pin interrupt block to control eight GPIO pins selected as pin interrupts.
3. Two GPIO group interrupt blocks to control two combined interrupts from all GPIO pins.

7.7.1 Features

- GPIO pins can be configured as input or output by software.
- All GPIO pins default to inputs with interrupt disabled at reset.
- Pin registers allow pins to be sensed and set individually.
- Up to eight GPIO pins can be selected from all GPIO pins to create an edge- or level-sensitive GPIO interrupt request.
- Port interrupts can be triggered by any pin or pins in each port.

7.8 USB interface

The Universal Serial Bus (USB) is a 4-wire bus that supports communication between a host and one or more (up to 127) peripherals. The host controller allocates the USB bandwidth to attached devices through a token-based protocol. The bus supports hot-plugging and dynamic configuration of the devices. All transactions are initiated by the host controller.

The LPC11U1x USB interface consists of a full-speed device controller with on-chip PHY for device functions.

Remark: Configure the LPC11U1x in default power mode with the power profiles before using the USB (see Section 7.16.5.1). Do not use the USB with the part in performance, efficiency, or low-power mode.

7.8.1 Full-speed USB device controller

The device controller enables 12 Mbit/s data exchange with a USB Host controller. It consists of a register interface, serial interface engine, and endpoint buffer memory. The serial interface engine decodes the USB data stream and writes data to the appropriate endpoint buffer. The status of a completed USB transfer or error condition is indicated via status registers. An interrupt is also generated if enabled.

7.8.1.1 Features

- Dedicated USB PLL available.
- Fully compliant with *USB 2.0 specification (full speed)*.
- Supports 10 physical (5 logical) endpoints including one control endpoint.
- Single and double buffering supported.
- Each non-control endpoint supports bulk, interrupt, or isochronous endpoint types.
- Supports wake-up from Deep-sleep mode and Power-down mode on USB activity and remote wake-up.
- Supports SoftConnect.

7.9 USART

The LPC11U1x contains one USART.

The USART includes full modem control, support for synchronous mode, and a smart card interface. The RS-485/9-bit mode allows both software address detection and automatic address detection using 9-bit mode.

The USART uses a fractional baud rate generator. Standard baud rates such as 115200 Bd can be achieved with any crystal frequency above 2 MHz.

7.9.1 Features

- Maximum USART data bit rate of 3.125 Mbit/s.
- 16-byte receive and transmit FIFOs.
- Register locations conform to 16C550 industry standard.
- Receiver FIFO trigger points at 1 B, 4 B, 8 B, and 14 B.
- Built-in fractional baud rate generator covering wide range of baud rates without a need for external crystals of particular values.
- Fractional divider for baud rate control, auto baud capabilities and FIFO control mechanism that enables software flow control implementation.
- Support for RS-485/9-bit mode.
- Support for modem control.
- Support for synchronous mode.
- Includes smart card interface.

7.10 SSP serial I/O controller

The SSP controllers are capable of operation on a SSP, 4-wire SSI, or Microwire bus. It can interact with multiple masters and slaves on the bus. Only a single master and a single slave can communicate on the bus during a given data transfer. The SSP supports full duplex transfers, with frames of 4 bits to 16 bits of data flowing from the master to the slave and from the slave to the master. In practice, often only one of these data flows carries meaningful data.

7.10.1 Features

- Maximum SSP speed of 25 Mbit/s (master) or 4.17 Mbit/s (slave) (in SSP mode)
- Compatible with Motorola SPI, 4-wire Texas Instruments SSI, and National Semiconductor Microwire buses
- Synchronous serial communication
- Master or slave operation
- 8-frame FIFOs for both transmit and receive
- 4-bit to 16-bit frame

7.11 I^2C-bus serial I/O controller

The LPC11U1x contain one I^2C-bus controller.

The I^2C-bus is bidirectional for inter-IC control using only two wires: a Serial Clock line (SCL) and a Serial Data line (SDA). Each device is recognized by a unique address and can operate as either a receiver-only device (e.g., an LCD driver) or a transmitter with the capability to both receive and send information (such as memory). Transmitters and/or receivers can operate in either master or slave mode, depending on whether the chip has to initiate a data transfer or is only addressed. The I^2C is a multi-master bus and can be controlled by more than one bus master connected to it.

7.11.1 Features

- The I^2C-interface is an I^2C-bus compliant interface with open-drain pins. The I^2C-bus interface supports Fast-mode Plus with bit rates up to 1 Mbit/s.
- Easy to configure as master, slave, or master/slave.
- Programmable clocks allow versatile rate control.
- Bidirectional data transfer between masters and slaves.
- Multi-master bus (no central master).
- Arbitration between simultaneously transmitting masters without corruption of serial data on the bus.
- Serial clock synchronization allows devices with different bit rates to communicate via one serial bus.
- Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer.
- The I^2C-bus can be used for test and diagnostic purposes.
- The I^2C-bus controller supports multiple address recognition and a bus monitor mode.

7.12 10-bit ADC

The LPC11U1x contains one ADC. It is a single 10-bit successive approximation ADC with eight channels.

7.12.1 Features

- 10-bit successive approximation ADC.
- Input multiplexing among 8 pins.
- Power-down mode.
- Measurement range 0 V to V_{DD}.
- 10-bit conversion time $\geq$ 2.44 μs (up to 400 kSamples/s).
- Burst conversion mode for single or multiple inputs.
- Optional conversion on transition of input pin or timer match signal.
- Individual result registers for each ADC channel to reduce interrupt overhead.

7.13 General purpose external event counter/timers

The LPC11U1x includes two 32-bit counter/timers and two 16-bit counter/timers. The counter/timer is designed to count cycles of the system derived clock. It can optionally generate interrupts or perform other actions at specified timer values, based on four match registers. Each counter/timer also includes one capture input to trap the timer value when an input signal transitions, optionally generating an interrupt.

7.13.1 Features

- A 32-bit/16-bit timer/counter with a programmable 32-bit/16-bit prescaler.
- Counter or timer operation.
- One capture channel per timer, that can take a snapshot of the timer value when an input signal transitions. A capture event may also generate an interrupt.

- Four match registers per timer that allow:
  - Continuous operation with optional interrupt generation on match.
  - Stop timer on match with optional interrupt generation.
  - Reset timer on match with optional interrupt generation.
- Up to four external outputs corresponding to match registers, with the following capabilities:
  - Set LOW on match.
  - Set HIGH on match.
  - Toggle on match.
  - Do nothing on match.
- The timer and prescaler may be configured to be cleared on a designated capture event. This feature permits easy pulse-width measurement by clearing the timer on the leading edge of an input pulse and capturing the timer value on the trailing edge.

7.14 System tick timer

The ARM Cortex-M0 includes a system tick timer (SYSTICK) that is intended to generate a dedicated SYSTICK exception at a fixed time interval (typically 10 ms).

7.15 Windowed WatchDog Timer (WWDT)

The purpose of the watchdog is to reset the controller if software fails to periodically service it within a programmable time window.

7.15.1 Features

- Internally resets chip if not periodically reloaded during the programmable time-out period.
- Optional windowed operation requires reload to occur between a minimum and maximum time period, both programmable.
- Optional warning interrupt can be generated at a programmable time prior to watchdog time-out.
- Enabled by software but requires a hardware reset or a watchdog reset/interrupt to be disabled.
- Incorrect feed sequence causes reset or interrupt if enabled.
- Flag to indicate watchdog reset.
- Programmable 24-bit timer with internal prescaler.
- Selectable time period from ($T_{cy(WDCLK)} \times 256 \times 4$) to ($T_{cy(WDCLK)} \times 2^{24} \times 4$) in multiples of $T_{cy(WDCLK)} \times 4$.
- The Watchdog Clock (WDCLK) source can be selected from the IRC or the dedicated watchdog oscillator (WDO). This gives a wide range of potential timing choices of watchdog operation under different power conditions.

7.16 Clocking and power control

7.16.1 Integrated oscillators

The LPC11U1x include three independent oscillators. These are the system oscillator, the Internal RC oscillator (IRC), and the watchdog oscillator. Each oscillator can be used for more than one purpose as required in a particular application.

Following reset, the LPC11U1x will operate from the internal RC oscillator until switched by software. This allows systems to operate without any external crystal and the bootloader code to operate at a known frequency.

See Figure 6 for an overview of the LPC11U1x clock generation.

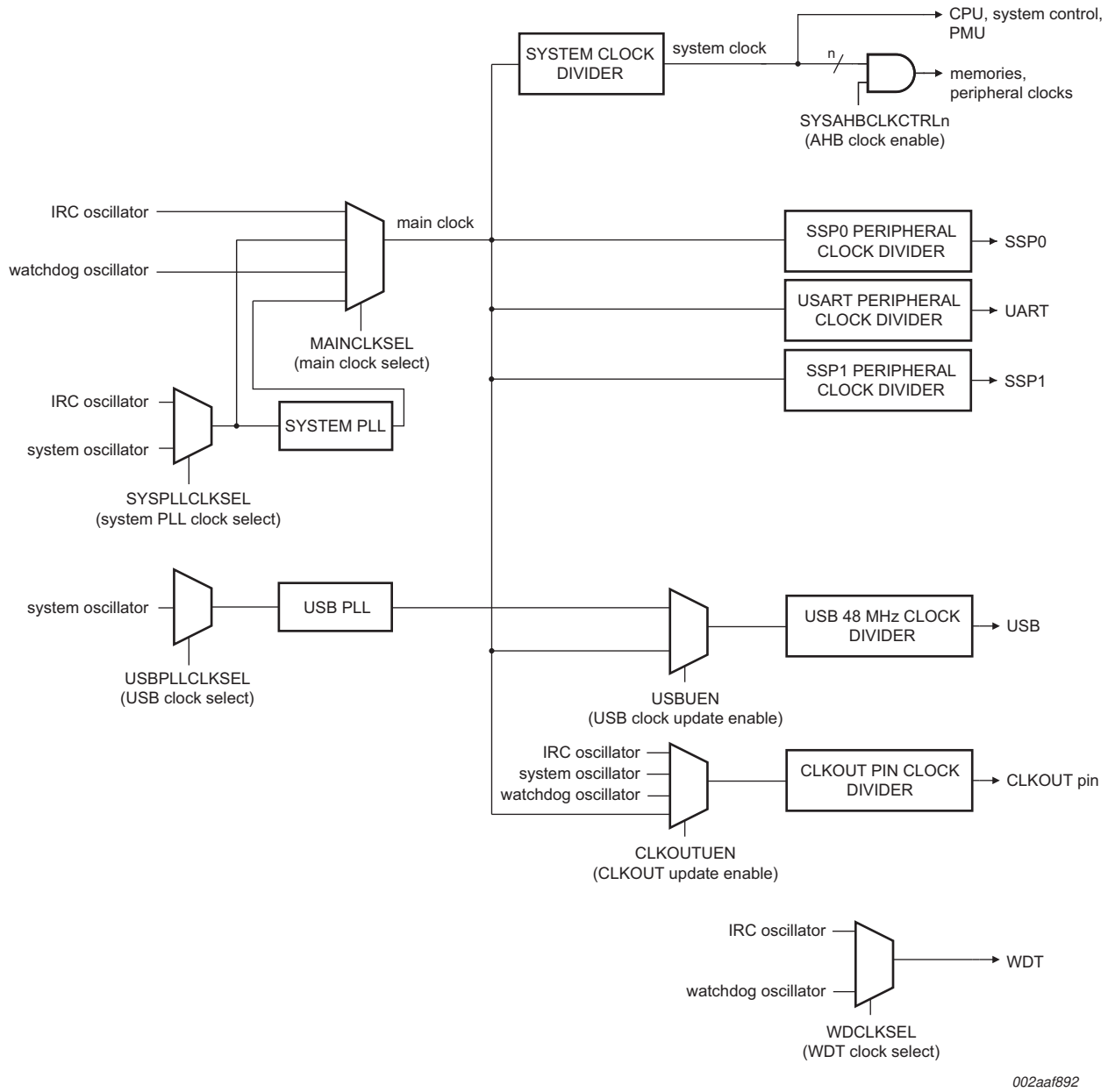


Fig 6. LPC11U1x clocking generation block diagram

7.16.1.1 Internal RC oscillator

The IRC may be used as the clock source for the WDT, and/or as the clock that drives the system PLL and subsequently the CPU. The nominal IRC frequency is 12 MHz.

Upon power-up, any chip reset, or wake-up from Deep power-down mode, the LPC11U1x use the IRC as the clock source. Software may later switch to one of the other available clock sources.

7.16.1.2 System oscillator

The system oscillator can be used as the clock source for the CPU, with or without using the PLL. On the LPC11U1x, the system oscillator must be used to provide the clock source to USB.

The system oscillator operates at frequencies of 1 MHz to 25 MHz. This frequency can be boosted to a higher frequency, up to the maximum CPU operating frequency, by the system PLL.

7.16.1.3 Watchdog oscillator

The watchdog oscillator can be used as a clock source that directly drives the CPU, the watchdog timer, or the CLKOUT pin. The watchdog oscillator nominal frequency is programmable between 7.8 kHz and 1.7 MHz. The frequency spread over processing and temperature is ±40 % (see also Table 13).

7.16.2 System PLL and USB PLL

The LPC11U1x contain a system PLL and a dedicated PLL for generating the 48 MHz USB clock. The system and USB PLLs are identical.

The PLL accepts an input clock frequency in the range of 10 MHz to 25 MHz. The input frequency is multiplied up to a high frequency with a Current Controlled Oscillator (CCO). The multiplier can be an integer value from 1 to 32. The CCO operates in the range of 156 MHz to 320 MHz, so there is an additional divider in the loop to keep the CCO within its frequency range while the PLL is providing the desired output frequency. The output divider may be set to divide by 2, 4, 8, or 16 to produce the output clock. The PLL output frequency must be lower than 100 MHz. Since the minimum output divider value is 2, it is insured that the PLL output has a 50 % duty cycle. The PLL is turned off and bypassed following a chip reset and may be enabled by software. The program must configure and activate the PLL, wait for the PLL to lock, and then connect to the PLL as a clock source. The PLL settling time is 100 μs.

7.16.3 Clock output

The LPC11U1x features a clock output function that routes the IRC oscillator, the system oscillator, the watchdog oscillator, or the main clock to an output pin.

7.16.4 Wake-up process

The LPC11U1x begin operation at power-up and when awakened from Deep power-down mode by using the 12 MHz IRC oscillator as the clock source. This allows chip operation to resume quickly. If the main oscillator or the PLL is needed by the application, software will need to enable these features and wait for them to stabilize before they are used as a clock source.

7.16.5 Power control

The LPC11U1x support a variety of power control features. There are four special modes of processor power reduction: Sleep mode, Deep-sleep mode, Power-down mode, and Deep power-down mode. The CPU clock rate may also be controlled as needed by changing clock sources, reconfiguring PLL values, and/or altering the CPU clock divider value. This allows a trade-off of power versus processing speed based on application requirements. In addition, a register is provided for shutting down the clocks to individual