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LPC1315/16/17/45/46/47

32-bit ARM Cortex-M3 microcontroller; up to 64 kB flash; up to 12 kB SRAM; USB device; USART; EEPROM

Rev. 3 — 20 September 2012 Product data sheet

1. General description

The LPC1315/16/17/45/46/47 are ARM Cortex-M3 based microcontrollers for embedded applications featuring a high level of integration and low power consumption. The ARM Cortex-M3 is a next generation core that offers system enhancements such as enhanced debug features and a higher level of support block integration.

The LPC1315/16/17/45/46/47 operate at CPU frequencies of up to 72 MHz. The ARM Cortex-M3 CPU incorporates a 3-stage pipeline and uses a Harvard architecture with separate local instruction and data buses as well as a third bus for peripherals. The ARM Cortex-M3 CPU also includes an internal prefetch unit that supports speculative branching.

Equipped with a highly flexible and configurable Full-Speed USB 2.0 device controller available on the LPC1345/46/47, this series brings unparalleled design flexibility and seamless integration to today's demanding connectivity solutions.

The peripheral complement of the LPC1315/16/17/45/46/47 includes up to 64 kB of flash memory, 8 kB or 10 kB of SRAM data memory, one Fast-mode Plus I^2C-bus interface, one RS-485/EIA-485 USART with support for synchronous mode and smart card interface, two SSP interfaces, four general purpose counter/timers, an 8-channel, 12-bit ADC, and up to 51 general purpose I/O pins.

2. Features and benefits

- System:
  - ARM Cortex-M3 r2p1 processor, running at frequencies of up to 72 MHz.
  - ARM Cortex-M3 built-in Nested Vectored Interrupt Controller (NVIC).
  - Non Maskable Interrupt (NMI) input selectable from several input sources.
  - System tick timer.
- Memory:
  - Up to 64 kB on-chip flash program memory with a 256 byte page erase function.
  - In-System Programming (ISP) and In-Application Programming (IAP) via on-chip bootloader software. Flash updates via USB supported.
  - Up to 4 kB on-chip EEPROM data memory with on-chip API support.
  - Up to 12 kB SRAM data memory.
  - 16 kB boot ROM with API support for USB API, power control, EEPROM, and flash IAP/ISP.

- Debug options:
  - Standard JTAG test interface for BSDL.
  - Serial Wire Debug.
  - Support for ETM ARM Cortex-M3 debug time stamping.
- Digital peripherals:
  - Up to 51 General Purpose I/O (GPIO) pins with configurable pull-up/pull-down resistors, repeater mode, input inverter, and pseudo open-drain mode. Eight pins support programmable glitch filter.
  - Up to 8 GPIO pins can be selected as edge and level sensitive interrupt sources.
  - Two GPIO grouped interrupt modules enable an interrupt based on a programmable pattern of input states of a group of GPIO pins.
  - High-current source output driver (20 mA) on one pin (P0_7).
  - High-current sink driver (20 mA) on true open-drain pins (P0_4 and P0_5).
  - Four general purpose counter/timers with a total of up to 8 capture inputs and 13 match outputs.
  - Programmable Windowed WatchDog Timer (WWDT) with a internal low-power WatchDog Oscillator (WDO).
  - Repetitive Interrupt Timer (RI Timer).
- Analog peripherals:
  - 12-bit ADC with eight input channels and sampling rates of up to 500 kSamples/s.
- Serial interfaces:
  - USB 2.0 full-speed device controller (LPC1345/46/47) with on-chip ROM-based USB driver library.
  - USART with fractional baud rate generation, internal FIFO, a full modem control handshake interface, and support for RS-485/9-bit mode and synchronous mode. USART supports an asynchronous smart card interface (ISO 7816-3).
  - Two SSP controllers with FIFO and multi-protocol capabilities.
  - I^2C-bus interface supporting the full I^2C-bus specification and Fast-mode Plus with a data rate of up to 1 Mbit/s with multiple address recognition and monitor mode.
- Clock generation:
  - Crystal Oscillator with an operating range of 1 MHz to 25 MHz (system oscillator) with failure detector.
  - 12 MHz high-frequency Internal RC oscillator (IRC) trimmed to 1 % accuracy over the entire voltage and temperature range. The IRC can optionally be used as a system clock.
  - Internal low-power, low-frequency WatchDog Oscillator (WDO) with programmable frequency output.
  - PLL allows CPU operation up to the maximum CPU rate with the system oscillator or the IRC as clock sources.
  - A second, dedicated PLL is provided for USB (LPC1345/46/47).
  - Clock output function with divider that can reflect the crystal oscillator, the main clock, the IRC, or the watchdog oscillator.
- Power control:
  - Four reduced power modes: Sleep, Deep-sleep, Power-down, and Deep power-down.
  - Power profiles residing in boot ROM allow optimized performance and minimized power consumption for any given application through one simple function call.

- Processor wake-up from Deep-sleep and Power-down modes via reset, selectable GPIO pins, watchdog interrupt, or USB port activity.
- Processor wake-up from Deep power-down mode using one special function pin.
- Integrated PMU (Power Management Unit) to minimize power consumption during Sleep, Deep-sleep, Power-down, and Deep power-down modes.
- Power-On Reset (POR).
- Brownout detect with up to four separate thresholds for interrupt and forced reset.

- Unique device serial number for identification.
- Single 3.3 V power supply (2.0 V to 3.6 V).
- Temperature range −40 °C to +85 °C.
- Available as LQFP64, LQFP48, and HVQFN33 package.

3. Applications

- Consumer peripherals
- Medical
- Industrial control
- Handheld scanners
- USB audio devices

4. Ordering information

Table 1. Ordering information

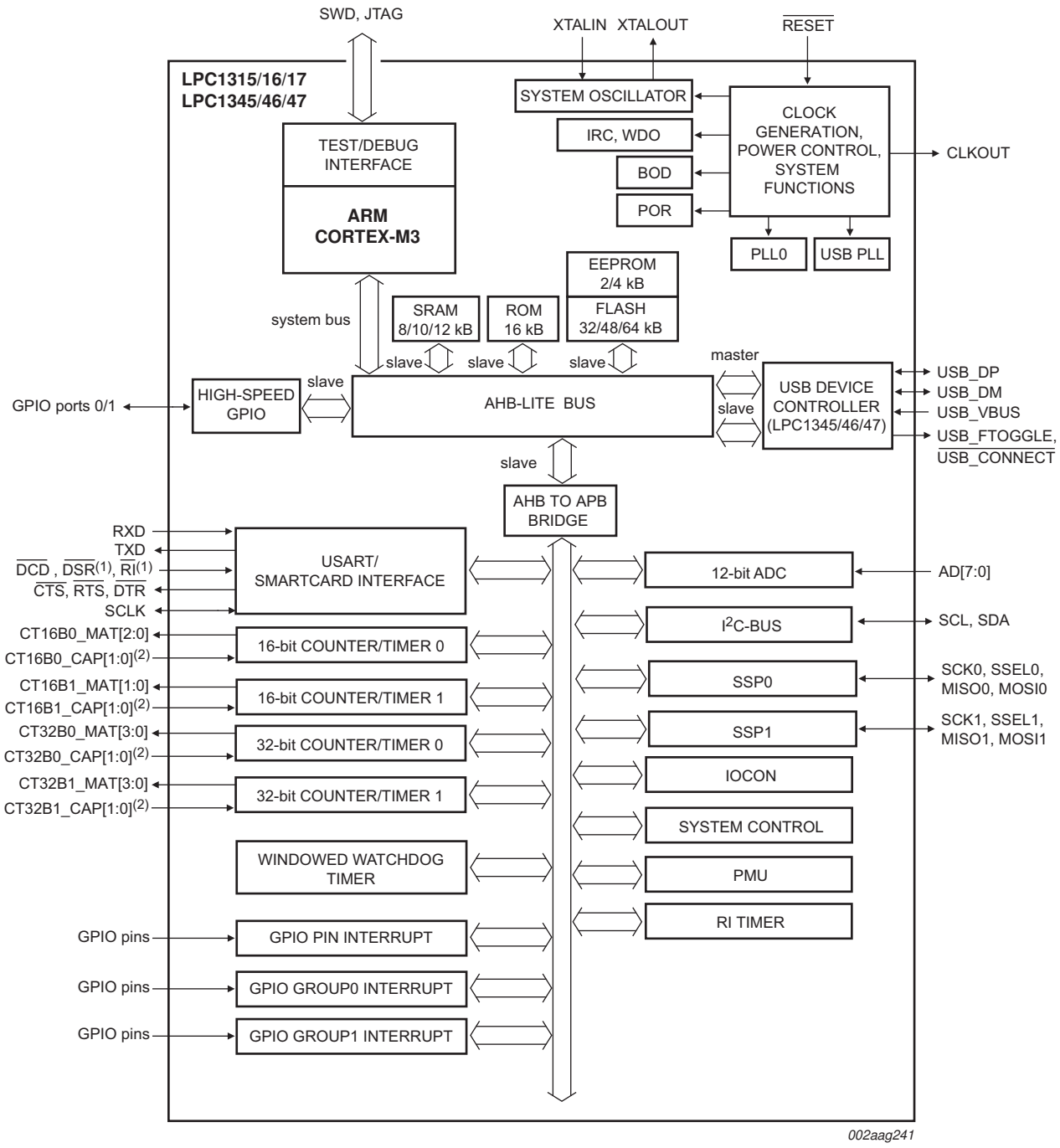
Type number	Package		
	Name	Description	Version
LPC1345FHN33	HVQFN33	plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 7 × 7 × 0.85 mm	n/a
LPC1345FBD48	LQFP48	plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2
LPC1346FHN33	HVQFN33	plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 7 × 7 × 0.85 mm	n/a
LPC1346FBD48	LQFP48	plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2
LPC1347FHN33	HVQFN33	plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 7 × 7 × 0.85 mm	n/a
LPC1347FBD48	LQFP48	plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2
LPC1347FBD64	LQFP64	LQFP64: plastic low profile quad flat package; 64 leads; body 10 × 10 × 1.4 mm	SOT314-2
LPC1315FHN33	HVQFN33	plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 7 × 7 × 0.85 mm	n/a
LPC1315FBD48	LQFP48	plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2
LPC1316FHN33	HVQFN33	plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 7 × 7 × 0.85 mm	n/a
LPC1316FBD48	LQFP48	plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2
LPC1317FHN33	HVQFN33	plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 7 × 7 × 0.85 mm	n/a
LPC1317FBD48	LQFP48	plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2
LPC1317FBD64	LQFP64	LQFP64: plastic low profile quad flat package; 64 leads; body 10 × 10 × 1.4 mm	SOT314-2

4.1 Ordering options

Table 2. Ordering options

Type number	Flash [kB]	SRAM [kB]			EEPROM [kB]	USB device	SSP	I2C/ FM+	ADC channels	GPIO pins
		SRAM0	USB SRAM	SRAM1						
LPC1345FHN33	32	8	2	-	2	yes	2	1	8	26
LPC1345FBD48	32	8	2	-	2	yes	2	1	8	40
LPC1346FHN33	48	8	2	-	4	yes	2	1	8	26
LPC1346FBD48	48	8	2	-	4	yes	2	1	8	40
LPC1347FHN33	64	8	2	2	4	yes	2	1	8	26
LPC1347FBD48	64	8	2	2	4	yes	2	1	8	40
LPC1347FBD64	64	8	2	2	4	yes	2	1	8	51
LPC1315FHN33	32	8	-	-	2	no	2	1	8	28
LPC1315FBD48	32	8	-	-	2	no	2	1	8	40
LPC1316FHN33	48	8	-	-	4	no	2	1	8	28
LPC1316FBD48	48	8	-	-	4	no	2	1	8	40
LPC1317FHN33	64	8	-	2	4	no	2	1	8	28
LPC1317FBD48	64	8	-	2	4	no	2	1	8	40
LPC1317FBD64	64	8	-	2	4	no	2	1	8	51

5. Block diagram



(1) Available on LQFP48 and LQFP64 packages only.

(2) CT16B0_CAP1, CT16B1_CAP1, CT32B1_CAP1 inputs available on LQFP64 packages only. CT32B0_CAP0 input available on LQFP48 and LQFP64 packages only.

Fig 1. Block diagram

6. Pinning information

6.1 Pinning

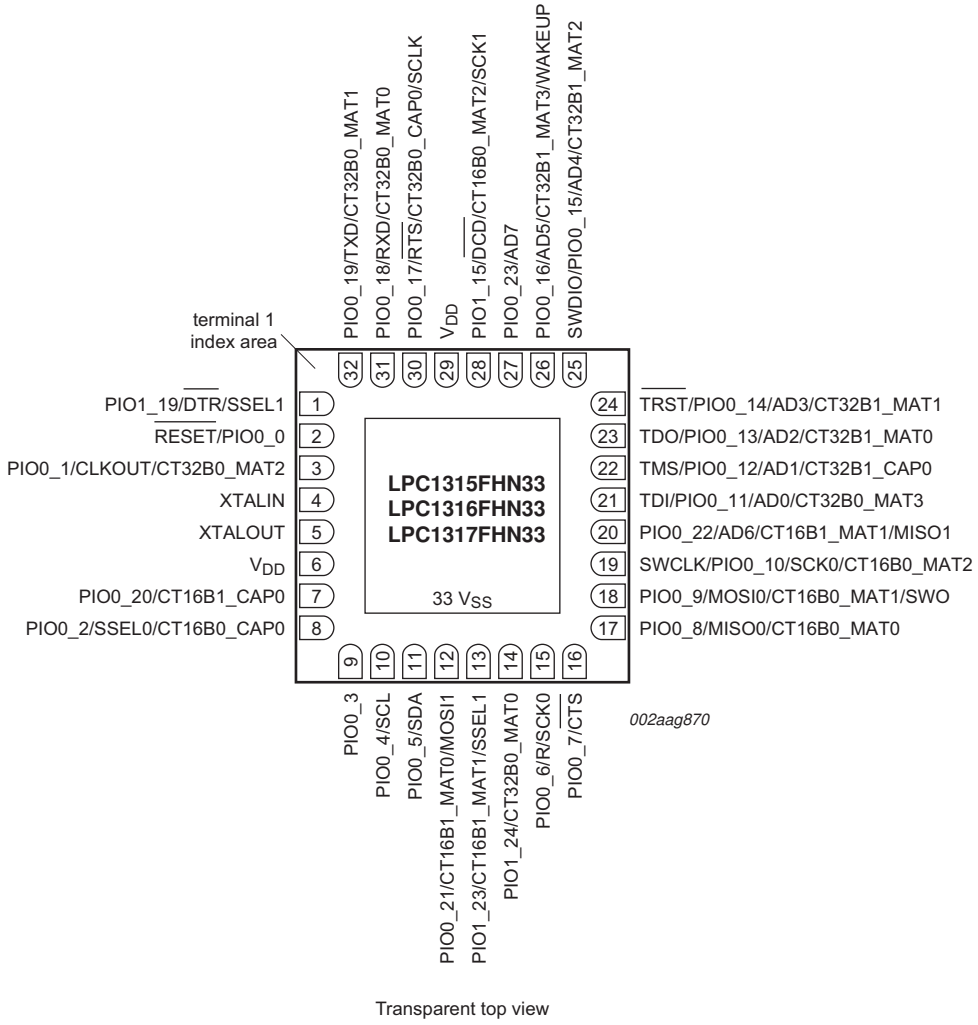


Fig 2. Pin configuration HVQFN33 package (LPC1315/16/17 - no USB)

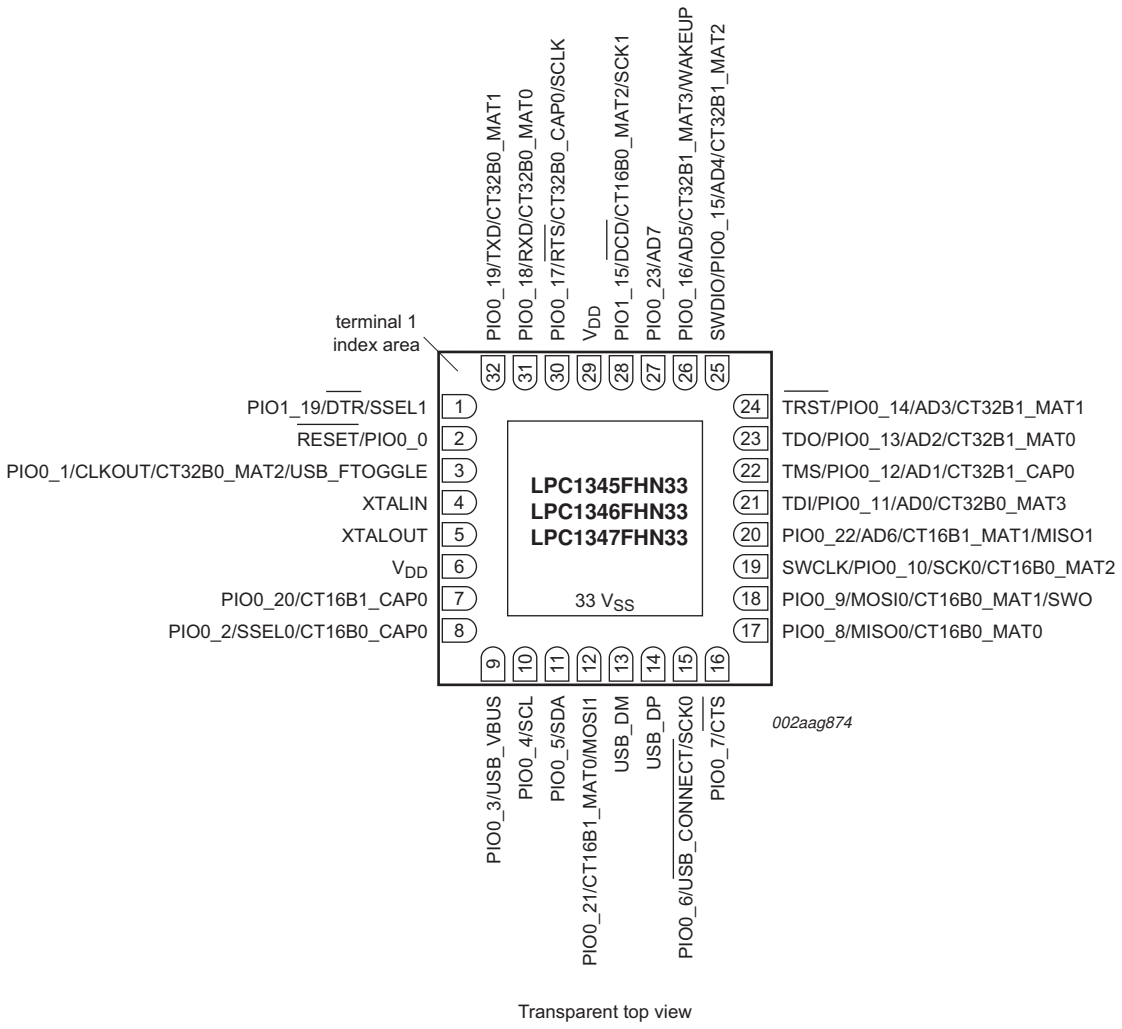


Fig 3. Pin configuration HVQFN33 package (LPC1345/46/47 - with USB)

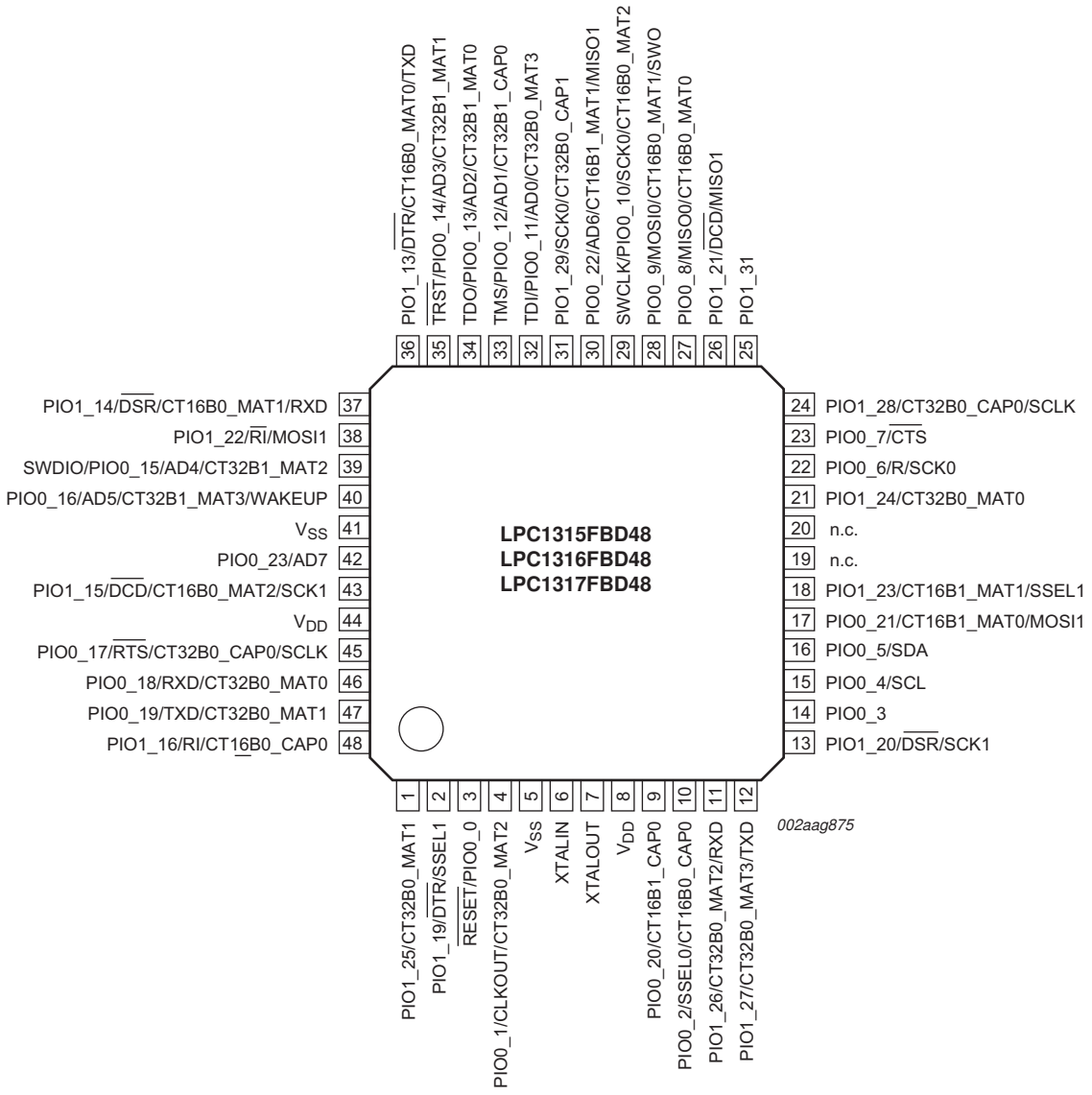


Fig 4. Pin configuration LQFP48 package (LPC1315/16/17 - no USB)

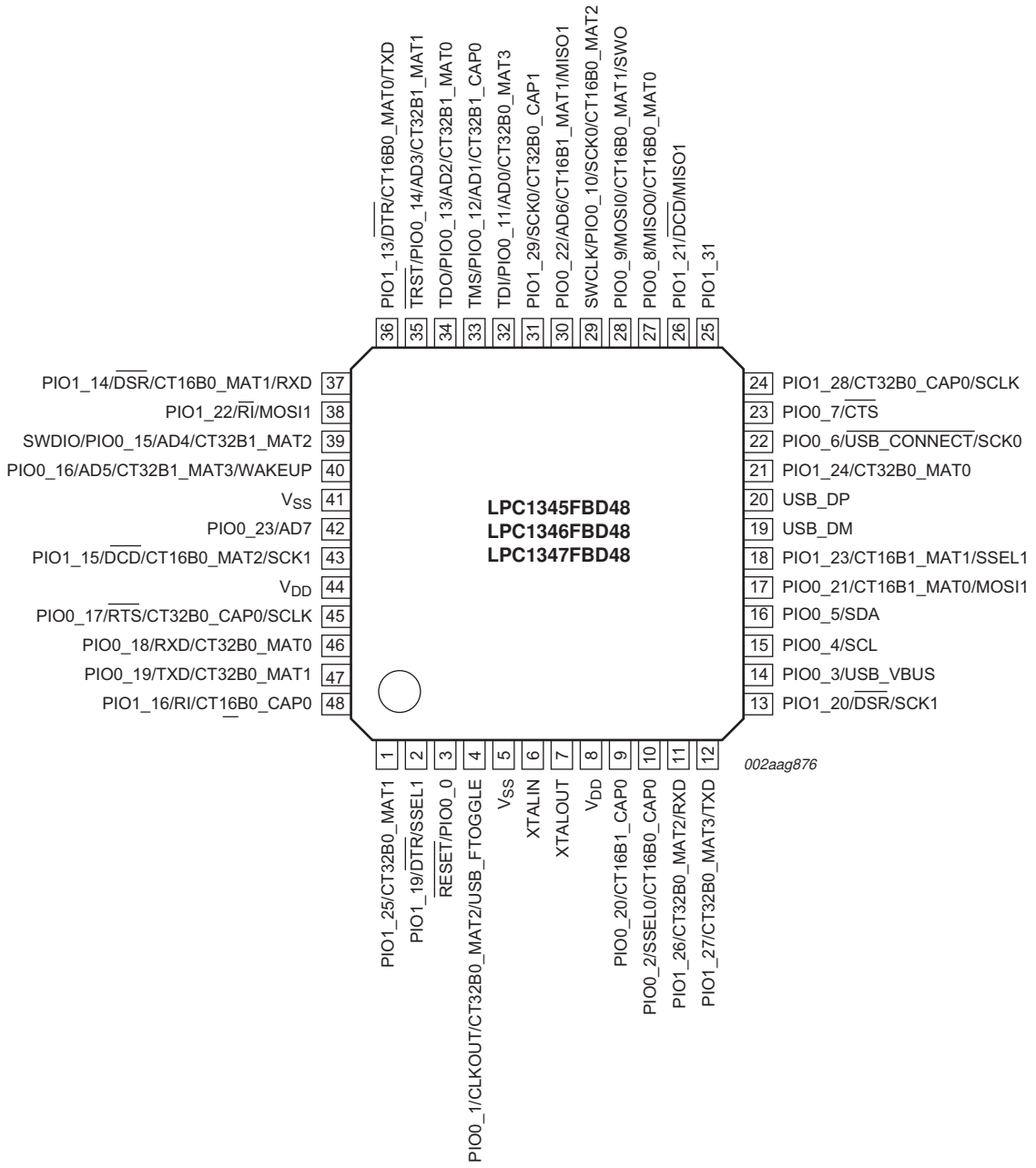
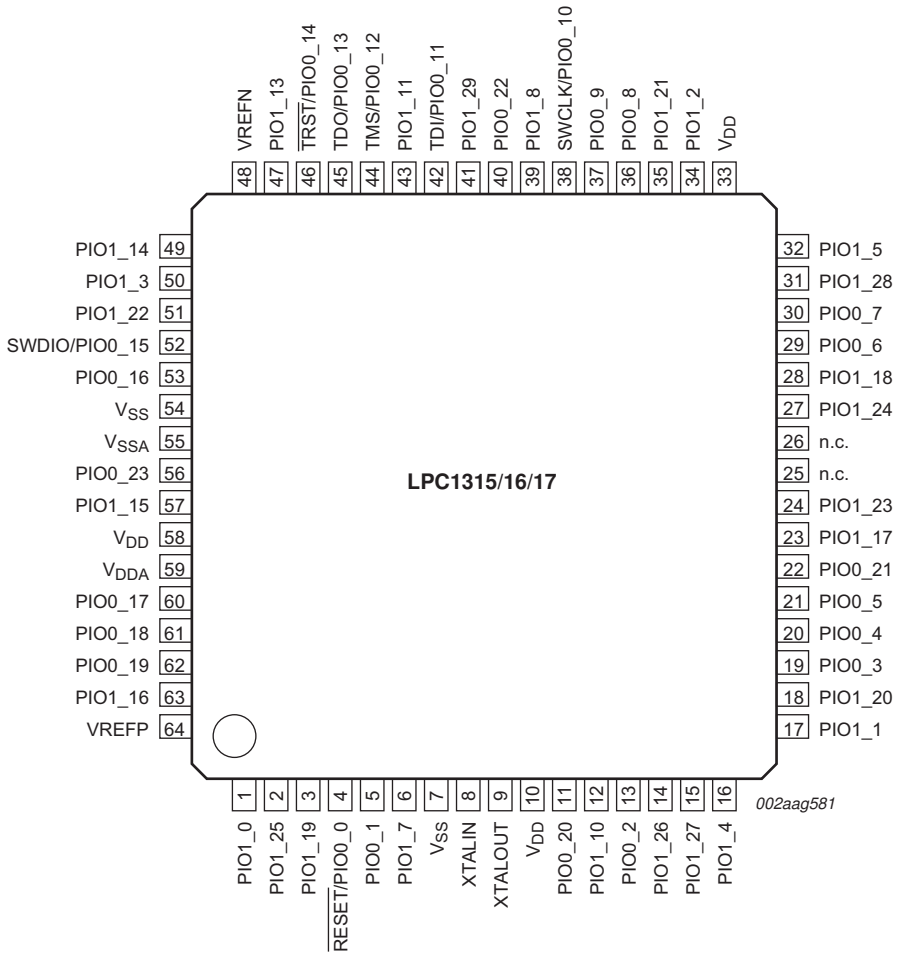


Fig 5. Pin configuration LQFP48 package (LPC1345/46/47 - with USB)



See Table 3 for the full pin name.

Fig 6. Pin configuration LQFP64 package (LPC1315/16/17 - no USB)

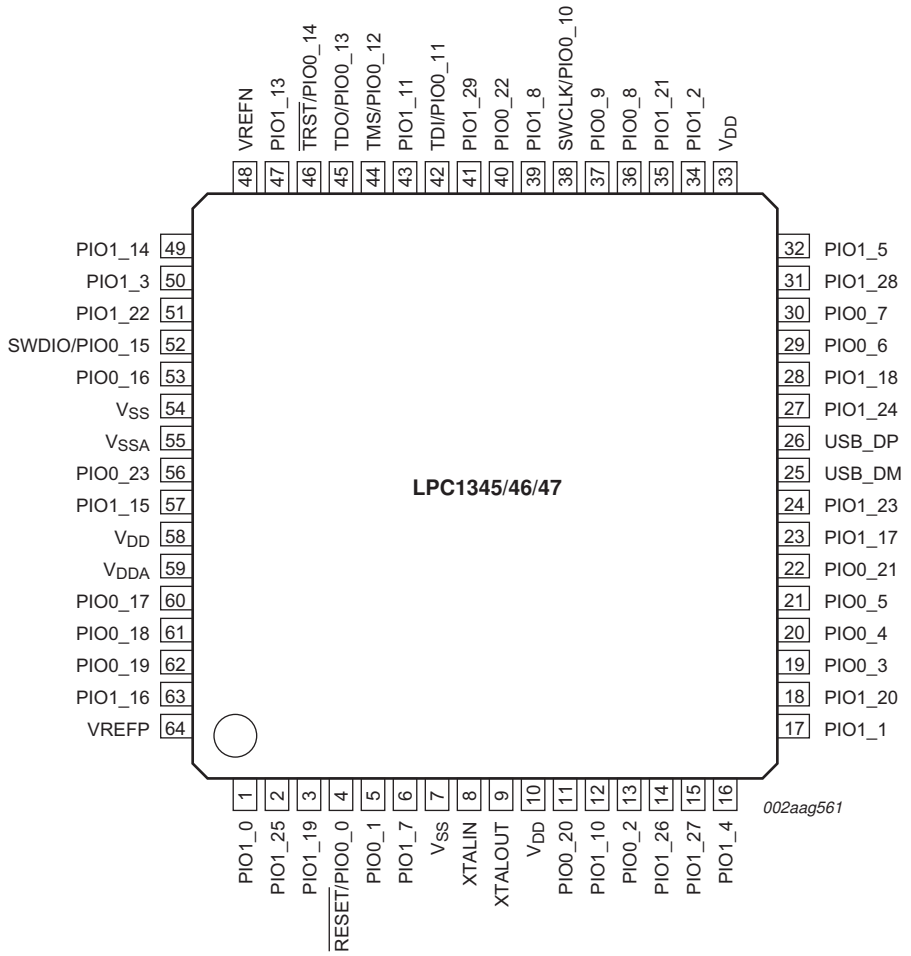


Fig 7. Pin configuration LQFP64 package (LPC1345/46/47 - with USB)

6.2 Pin description

Table 3. Pin description (LPC1315/16/17 - no USB)

Symbol	LQFP64	LQFP48	HVQFN33		Reset state[1]	Type	Description
$\overline{\text{RESET}}$/PIO0_0	4	3	2	[2]	I; PU	I	**$\overline{\text{RESET}}$ —** External reset input with 20 ns glitch filter. A LOW-going pulse as short as 50 ns on this pin resets the device, causing I/O ports and peripherals to take on their default states, and processor execution to begin at address 0. This pin also serves as the debug select input. LOW level selects the JTAG boundary scan. HIGH level selects the ARM SWD debug mode.
					-	I/O	**PIO0_0 —** General purpose digital input/output pin.
PIO0_1/CLKOUT/ CT32B0_MAT2	5	4	3	[3]	I; PU	I/O	**PIO0_1 —** General purpose digital input/output pin. A LOW level on this pin during reset starts the ISP command handler.
					-	O	**CLKOUT —** Clockout pin.
					-	O	**CT32B0_MAT2 —** Match output 2 for 32-bit timer 0.
PIO0_2/SSEL0/ CT16B0_CAP0	13	10	8	[3]	I; PU	I/O	**PIO0_2 —** General purpose digital input/output pin.
						I/O	**SSEL0 —** Slave select for SSP0.
						I	**CT16B0_CAP0 —** Capture input 0 for 16-bit timer 0.
PIO0_3	19	14	9	[3]	I; PU	I/O	**PIO0_3 —** General purpose digital input/output pin.
PIO0_4/SCL	20	15	10	[4]	IA	I/O	**PIO0_4 —** General purpose digital input/output pin (open-drain).
					-	I/O	**SCL —** I^2C-bus clock input/output (open-drain). High-current sink only if I^2C Fast-mode Plus is selected in the I/O configuration register.
PIO0_5/SDA	21	16	11	[4]	IA	I/O	**PIO0_5 —** General purpose digital input/output pin (open-drain).
					-	I/O	**SDA —** I^2C-bus data input/output (open-drain). High-current sink only if I^2C Fast-mode Plus is selected in the I/O configuration register.
PIO0_6/R/ SCK0	29	22	15	[3]	I; PU	I/O	**PIO0_6 —** General purpose digital input/output pin.
					-	-	**R —** Reserved.
					-	I/O	**SCK0 —** Serial clock for SSP0.
PIO0_7/$\overline{\text{CTS}}$	30	23	16	[5]	I; PU	I/O	**PIO0_7 —** General purpose digital input/output pin (high-current output driver).
					-	I	**$\overline{\text{CTS}}$ —** Clear To Send input for USART.
PIO0_8/MISO0/ CT16B0_MAT0	36	27	17	[3]	I; PU	I/O	**PIO0_8 —** General purpose digital input/output pin.
					-	I/O	**MISO0 —** Master In Slave Out for SSP0.
					-	O	**CT16B0_MAT0 —** Match output 0 for 16-bit timer 0.
PIO0_9/MOSI0/ CT16B0_MAT1/ SWO	37	28	18	[3]	I; PU	I/O	**PIO0_9 —** General purpose digital input/output pin.
					-	I/O	**MOSI0 —** Master Out Slave In for SSP0.
					-	O	**CT16B0_MAT1 —** Match output 1 for 16-bit timer 0.
					-	O	**SWO —** Serial wire trace output.

Table 3. Pin description (LPC1315/16/17 - no USB)

Symbol	LQFP64	LQFP48	HVQFN33		Reset state[1]	Type	Description
SWCLK/PIO0_10/SCK0/ CT16B0_MAT2	38	29	19	[3]	I; PU	I	**SWCLK —** Serial wire clock and test clock TCK for JTAG interface.
					-	I/O	**PIO0_10 —** General purpose digital input/output pin.
					-	O	**SCK0 —** Serial clock for SSP0.
					-	O	**CT16B0_MAT2 —** Match output 2 for 16-bit timer 0.
TDI/PIO0_11/AD0/ CT32B0_MAT3	42	32	21	[6]	I; PU	I	**TDI —** Test Data In for JTAG interface.
					-	I/O	**PIO0_11 —** General purpose digital input/output pin.
					-	I	**AD0 —** A/D converter, input 0.
					-	O	**CT32B0_MAT3 —** Match output 3 for 32-bit timer 0.
TMS/PIO0_12/AD1/ CT32B1_CAP0	44	33	22	[6]	I; PU	I	**TMS —** Test Mode Select for JTAG interface.
					-	I/O	**PIO_12 —** General purpose digital input/output pin.
					-	I	**AD1 —** A/D converter, input 1.
					-	I	**CT32B1_CAP0 —** Capture input 0 for 32-bit timer 1.
TDO/PIO0_13/AD2/ CT32B1_MAT0	45	34	23	[6]	I; PU	O	**TDO —** Test Data Out for JTAG interface.
					-	I/O	**PIO0_13 —** General purpose digital input/output pin.
					-	I	**AD2 —** A/D converter, input 2.
					-	O	**CT32B1_MAT0 —** Match output 0 for 32-bit timer 1.
$\overline{\text{TRST}}$/PIO0_14/AD3/ CT32B1_MAT1	46	35	24	[6]	I; PU	I	**$\overline{\text{TRST}}$ —** Test Reset for JTAG interface.
					-	I/O	**PIO0_14 —** General purpose digital input/output pin.
					-	I	**AD3 —** A/D converter, input 3.
					-	O	**CT32B1_MAT1 —** Match output 1 for 32-bit timer 1.
SWDIO/PIO0_15/AD4/ CT32B1_MAT2	52	39	25	[6]	I; PU	I/O	**SWDIO —** Serial wire debug input/output.
					-	I/O	**PIO0_15 —** General purpose digital input/output pin.
					-	I	**AD4 —** A/D converter, input 4.
					-	O	**CT32B1_MAT2 —** Match output 2 for 32-bit timer 1.
PIO0_16/AD5/ CT32B1_MAT3/WAKEUP	53	40	26	[7]	I; PU	I/O	**PIO0_16 —** General purpose digital input/output pin.
					-	I	**AD5 —** A/D converter, input 5.
					-	O	**CT32B1_MAT3 —** Match output 3 for 32-bit timer 1.
					-	I	**WAKEUP —** Deep power-down mode wake-up pin with 20 ns glitch filter. This pin must be pulled HIGH externally to enter Deep power-down mode and pulled LOW to exit Deep power-down mode. A LOW-going pulse as short as 50 ns wakes up the part.
PIO0_17/$\overline{\text{RTS}}$/ CT32B0_CAP0/SCLK	60	45	30	[3]	I; PU	I/O	**PIO0_17 —** General purpose digital input/output pin.
					-	O	**$\overline{\text{RTS}}$ —** Request To Send output for USART.
					-	I	**CT32B0_CAP0 —** Capture input 0 for 32-bit timer 0.
					-	I/O	**SCLK —** Serial clock input/output for USART in synchronous mode.

Table 3. Pin description (LPC1315/16/17 - no USB)

Symbol	LQFP64	LQFP48	HVQFN33		Reset state[1]	Type	Description
PIO0_18/RXD/ CT32B0_MAT0	61	46	31	[3]	I; PU	I/O	**PIO0_18** — General purpose digital input/output pin.
					-	I	**RXD** — Receiver input for USART. Used in UART ISP mode.
					-	O	**CT32B0_MAT0** — Match output 0 for 32-bit timer 0.
PIO0_19/TXD/ CT32B0_MAT1	62	47	32	[3]	I; PU	I/O	**PIO0_19** — General purpose digital input/output pin.
					-	O	**TXD** — Transmitter output for USART. Used in UART ISP mode.
					-	O	**CT32B0_MAT1** — Match output 1 for 32-bit timer 0.
PIO0_20/CT16B1_CAP0	11	9	7	[3]	I; PU	I/O	**PIO0_20** — General purpose digital input/output pin.
					-	I	**CT16B1_CAP0** — Capture input 0 for 16-bit timer 1.
PIO0_21/CT16B1_MAT0/ MOSI1	22	17	12	[3]	I; PU	I/O	**PIO0_21** — General purpose digital input/output pin.
					-	O	**CT16B1_MAT0** — Match output 0 for 16-bit timer 1.
					-	I/O	**MOSI1** — Master Out Slave In for SSP1.
PIO0_22/AD6/ CT16B1_MAT1/MISO1	40	30	20	[6]	I; PU	I/O	**PIO0_22** — General purpose digital input/output pin.
					-	I	**AD6** — A/D converter, input 6.
					-	O	**CT16B1_MAT1** — Match output 1 for 16-bit timer 1.
					-	I/O	**MISO1** — Master In Slave Out for SSP1.
PIO0_23/AD7	56	42	27	[6]	I; PU	I/O	**PIO0_23** — General purpose digital input/output pin.
					-	I	**AD7** — A/D converter, input 7.
PIO1_0/CT32B1_MAT0	1	-	-	[3]	I; PU	I/O	**PIO1_0** — General purpose digital input/output pin.
					-	O	**CT32B1_MAT0** — Match output 0 for 32-bit timer 1.
PIO1_1/CT32B1_MAT1	17	-	-	[3]	I; PU	I/O	**PIO1_1** — General purpose digital input/output pin.
					-	O	**CT32B1_MAT1** — Match output 1 for 32-bit timer 1.
PIO1_2/CT32B1_MAT2	34	-	-	[3]	I; PU	I/O	**PIO1_2** — General purpose digital input/output pin.
					-	O	**CT32B1_MAT2** — Match output 2 for 32-bit timer 1.
PIO1_3/CT32B1_MAT3	50	-	-	[3]	I; PU	I/O	**PIO1_3** — General purpose digital input/output pin.
					-	O	**CT32B1_MAT3** — Match output 3 for 32-bit timer 1.
PIO1_4/CT32B1_CAP0	16	-	-	[3]	I; PU	I/O	**PIO1_4** — General purpose digital input/output pin.
					-	I	**CT32B1_CAP0** — Capture input 0 for 32-bit timer 1.
PIO1_5/CT32B1_CAP1	32	-	-	[3]	I; PU	I/O	**PIO1_5** — General purpose digital input/output pin.
					-	I	**CT32B1_CAP1** — Capture input 1 for 32-bit timer 1.
PIO1_7	6	-	-	[3]	I; PU	I/O	**PIO1_7** — General purpose digital input/output pin.
PIO1_8	39	-	-	[3]	I; PU	I/O	**PIO1_8** — General purpose digital input/output pin.
PIO1_10	12	-	-	[3]	I; PU	I/O	**PIO1_10** — General purpose digital input/output pin.
PIO1_11	43	-	-	[3]	I; PU	I/O	**PIO1_11** — General purpose digital input/output pin.

Table 3. Pin description (LPC1315/16/17 - no USB)

Symbol	LQFP64	LQFP48	HVQFN33		Reset state[1]	Type	Description
PIO1_13/DTR/ CT16B0_MAT0/TXD	47	36	-	[3]	I; PU	I/O	**PIO1_13** — General purpose digital input/output pin.
					-	O	**DTR** — Data Terminal Ready output for USART.
					-	O	**CT16B0_MAT0** — Match output 0 for 16-bit timer 0.
					-	O	**TXD** — Transmitter output for USART.
PIO1_14/DSR/ CT16B0_MAT1/RXD	49	37	-	[3]	I; PU	I/O	**PIO1_14** — General purpose digital input/output pin.
					-	I	**DSR** — Data Set Ready input for USART.
					-	O	**CT16B0_MAT1** — Match output 1 for 16-bit timer 0.
					-	I	**RXD** — Receiver input for USART.
PIO1_15/DCD/ CT16B0_MAT2/SCK1	57	43	28	[3]	I; PU	I/O	**PIO1_15** — General purpose digital input/output pin.
					-	I	**DCD** — Data Carrier Detect input for USART.
					-	O	**CT16B0_MAT2** — Match output 2 for 16-bit timer 0.
					-	I/O	**SCK1** — Serial clock for SSP1.
PIO1_16/RI/CT16B0_CAP0	63	48	-	[3]	I; PU	I/O	**PIO1_16** — General purpose digital input/output pin.
					-	I	**RI** — Ring Indicator input for USART.
					-	I	**CT16B0_CAP0** — Capture input 0 for 16-bit timer 0.
PIO1_17/CT16B0_CAP1/ RXD	23	-	-	[3]	I; PU	I/O	**PIO1_17** — General purpose digital input/output pin.
					-	I	**CT16B0_CAP1** — Capture input 1 for 16-bit timer 0.
					-	I	**RXD** — Receiver input for USART.
PIO1_18/CT16B1_CAP1/ TXD	28	-	-	[3]	I; PU	I/O	**PIO1_18** — General purpose digital input/output pin.
					-	I	**CT16B1_CAP1** — Capture input 1 for 16-bit timer 1.
					-	O	**TXD** — Transmitter output for USART.
PIO1_19/DTR/SSEL1	3	2	1	[3]	I; PU	I/O	**PIO1_19** — General purpose digital input/output pin.
					-	O	**DTR** — Data Terminal Ready output for USART.
					-	I/O	**SSEL1** — Slave select for SSP1.
PIO1_20/DSR/SCK1	18	13	-	[3]	I; PU	I/O	**PIO1_20** — General purpose digital input/output pin.
					-	I	**DSR** — Data Set Ready input for USART.
					-	I/O	**SCK1** — Serial clock for SSP1.
PIO1_21/DCD/MISO1	35	26	-	[3]	I; PU	I/O	**PIO1_21** — General purpose digital input/output pin.
					-	I	**DCD** — Data Carrier Detect input for USART.
					-	I/O	**MISO1** — Master In Slave Out for SSP1.
PIO1_22/RI/MOSI1	51	38	-	[3]	I; PU	I/O	**PIO1_22** — General purpose digital input/output pin.
					-	I	**RI** — Ring Indicator input for USART.
					-	I/O	**MOSI1** — Master Out Slave In for SSP1.
PIO1_23/CT16B1_MAT1/ SSEL1	24	18	13	[3]	I; PU	I/O	**PIO1_23** — General purpose digital input/output pin.
					-	O	**CT16B1_MAT1** — Match output 1 for 16-bit timer 1.
					-	I/O	**SSEL1** — Slave select for SSP1.
PIO1_24/CT32B0_MAT0	27	21	14	[3]	I; PU	I/O	**PIO1_24** — General purpose digital input/output pin.
					-	O	**CT32B0_MAT0** — Match output 0 for 32-bit timer 0.

Table 3. Pin description (LPC1315/16/17 - no USB)

Symbol	LQFP64	LQFP48	HVQFN33		Reset state[1]	Type	Description
PIO1_25/CT32B0_MAT1	2	1	-	[3]	I; PU	I/O	**PIO1_25 —** General purpose digital input/output pin.
					-	O	**CT32B0_MAT1 —** Match output 1 for 32-bit timer 0.
PIO1_26/CT32B0_MAT2/ RXD	14	11	-	[3]	I; PU	I/O	**PIO1_26 —** General purpose digital input/output pin.
					-	O	**CT32B0_MAT2 —** Match output 2 for 32-bit timer 0.
					-	I	**RXD —** Receiver input for USART.
PIO1_27/CT32B0_MAT3/ TXD	15	12	-	[3]	I; PU	I/O	**PIO1_27 —** General purpose digital input/output pin.
					-	O	**CT32B0_MAT3 —** Match output 3 for 32-bit timer 0.
					-	O	**TXD —** Transmitter output for USART.
PIO1_28/CT32B0_CAP0/ SCLK	31	24	-	[3]	I; PU	I/O	**PIO1_28 —** General purpose digital input/output pin.
					-	I	**CT32B0_CAP0 —** Capture input 0 for 32-bit timer 0.
					-	I/O	**SCLK —** Serial clock input/output for USART in synchronous mode.
PIO1_29/SCK0/ CT32B0_CAP1	41	31	-	[3]	I; PU	I/O	**PIO1_29 —** General purpose digital input/output pin.
					-	I/O	**SCK0 —** Serial clock for SSP0.
					-	I	**CT32B0_CAP1 —** Capture input 1 for 32-bit timer 0.
PIO1_31	-	25	-	[3]	I; PU	I/O	**PIO1_31 —** General purpose digital input/output pin.
n.c.	25	19	-		-	-	Not connected.
n.c.	26	20	-		-	-	Not connected.
XTALIN	8	6	4	[8]	-	-	Input to the oscillator circuit and internal clock generator circuits. Input voltage must not exceed 1.8 V.
XTALOUT	9	7	5	[8]	-	-	Output from the oscillator amplifier.
V_{DDA}	59	-	-		-	-	Analog 3.3 V pad supply voltage: This should be nominally the same voltage as V_{DD} but should be isolated to minimize noise and error. This voltage is used to power the ADC. This pin should be tied to 3.3 V if the ADC is not used.
VREFN	48	-	-		-	-	ADC negative reference voltage: This should be nominally the same voltage as V_{SS} but should be isolated to minimize noise and error. Level on this pin is used as a reference for ADC.

Table 3. Pin description (LPC1315/16/17 - no USB)

Symbol	LQFP64	LQFP48	HVQFN33	Reset state[1]	Type	Description
VREFP	64	-	-	-	-	ADC positive reference voltage: This should be nominally the same voltage as V_{DDA} but should be isolated to minimize noise and error. Level on this pin is used as a reference for ADC. This pin should be tied to 3.3 V if the ADC is not used.
V_{SSA}	55	-	-	-	-	Analog ground: 0 V reference. This should nominally be the same voltage as V_{SS}Product data sheet but should be isolated to minimize noise and error.
V_{DD}	10; 33; 58	8; 44	6; 29	-	-	Supply voltage to the internal regulator and the external rail. On LQFP48 and HVQFN33 packages, this pin is also connected to the 3.3 V ADC supply and reference voltage.
V_{SS}	7; 54	5; 41	33	-	-	Ground.

[1] Pin state at reset for default function: I = Input; O = Output; PU = internal pull-up enabled; IA = inactive, no pull-up/down enabled; F = floating; floating pins, if not used, should be tied to ground or power to minimize power consumption.

[2] See Figure 33 for the reset pad configuration. $\overline{\text{RESET}}$ functionality is not available in Deep power-down mode. Use the WAKEUP pin to reset the chip and wake up from Deep power-down mode. An external pull-up resistor is required on this pin for the Deep power-down mode.

[3] 5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors and configurable hysteresis (see Figure 32).

[4] I^2C-bus pins compliant with the I^2C-bus specification for I^2C standard mode, I^2C Fast-mode, and I^2C Fast-mode Plus.

[5] 5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors and configurable hysteresis (see Figure 32); includes high-current output driver.

[6] 5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors, configurable hysteresis, and analog input. When configured as a ADC input, digital section of the pad is disabled and the pin is not 5 V tolerant (see Figure 32); includes programmable digital input glitch filter.

[7] WAKEUP pin. 5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors, configurable hysteresis, and analog input. When configured as a ADC input, digital section of the pad is disabled and the pin is not 5 V tolerant (see Figure 32); includes digital input glitch filter.

[8] When the system oscillator is not used, connect XTALIN and XTALOUT as follows: XTALIN can be left floating or can be grounded (grounding is preferred to reduce susceptibility to noise). XTALOUT should be left floating.

Table 4. Pin description (LPC1345/46/47 - with USB)

Symbol	LQFP64	LQFP48	HVQFN33		Reset state[1]	Type	Description
$\overline{\text{RESET}}$/PIO0_0	4	3	2	[2]	I; PU	I	**$\overline{\text{RESET}}$ —** External reset input with 20 ns glitch filter. A LOW-going pulse as short as 50 ns on this pin resets the device, causing I/O ports and peripherals to take on their default states, and processor execution to begin at address 0. This pin also serves as the debug select input. LOW level selects the JTAG boundary scan. HIGH level selects the ARM SWD debug mode.
					-	I/O	**PIO0_0 —** General purpose digital input/output pin.
PIO0_1/CLKOUT/ CT32B0_MAT2/ USB_FTOGGLE	5	4	3	[3]	I; PU	I/O	**PIO0_1 —** General purpose digital input/output pin. A LOW level on this pin during reset starts the ISP command handler or the USB device enumeration.
					-	O	**CLKOUT —** Clockout pin.
					-	O	**CT32B0_MAT2 —** Match output 2 for 32-bit timer 0.
					-	O	**USB_FTOGGLE —** USB 1 ms Start-of-Frame signal.
PIO0_2/SSEL0/ CT16B0_CAP0	13	10	8	[3]	I; PU	I/O	**PIO0_2 —** General purpose digital input/output pin.
						I/O	**SSEL0 —** Slave select for SSP0.
						I	**CT16B0_CAP0 —** Capture input 0 for 16-bit timer 0.
PIO0_3/USB_VBUS	19	14	9	[3]	I; PU	I/O	**PIO0_3 —** General purpose digital input/output pin. A LOW level on this pin during reset starts the ISP command handler. A HIGH level during reset starts the USB device enumeration.
					-	I	**USB_VBUS —** Monitors the presence of USB bus power.
PIO0_4/SCL	20	15	10	[4]	IA	I/O	**PIO0_4 —** General purpose digital input/output pin (open-drain).
					-	I/O	**SCL —** I^2C-bus clock input/output (open-drain). High-current sink only if I^2C Fast-mode Plus is selected in the I/O configuration register.
PIO0_5/SDA	21	16	11	[4]	IA	I/O	**PIO0_5 —** General purpose digital input/output pin (open-drain).
					-	I/O	**SDA —** I^2C-bus data input/output (open-drain). High-current sink only if I^2C Fast-mode Plus is selected in the I/O configuration register.
PIO0_6/$\overline{\text{USB_CONNECT}}$/ SCK0	29	22	15	[3]	I; PU	I/O	**PIO0_6 —** General purpose digital input/output pin.
					-	O	**$\overline{\text{USB_CONNECT}}$ —** Signal used to switch an external 1.5 kΩ resistor under software control. Used with the SoftConnect USB feature.
					-	I/O	**SCK0 —** Serial clock for SSP0.
PIO0_7/$\overline{\text{CTS}}$	30	23	16	[5]	I; PU	I/O	**PIO0_7 —** General purpose digital input/output pin (high-current output driver).
					-	I	**$\overline{\text{CTS}}$ —** Clear To Send input for USART.
PIO0_8/MISO0/ CT16B0_MAT0	36	27	17	[3]	I; PU	I/O	**PIO0_8 —** General purpose digital input/output pin.
					-	I/O	**MISO0 —** Master In Slave Out for SSP0.
					-	O	**CT16B0_MAT0 —** Match output 0 for 16-bit timer 0.

Table 4. Pin description (LPC1345/46/47 - with USB)

Symbol	LQFP64	LQFP48	HVQFN33		Reset state[1]	Type	Description
PIO0_9/MOSI0/ CT16B0_MAT1/ SWO	37	28	18	[3]	I; PU	I/O	**PIO0_9** — General purpose digital input/output pin.
					-	I/O	**MOSI0** — Master Out Slave In for SSP0.
					-	O	**CT16B0_MAT1** — Match output 1 for 16-bit timer 0.
					-	O	**SWO** — Serial wire trace output.
SWCLK/PIO0_10/SCK0/ CT16B0_MAT2	38	29	19	[3]	I; PU	I	**SWCLK** — Serial wire clock and test clock TCK for JTAG interface.
					-	I/O	**PIO0_10** — General purpose digital input/output pin.
					-	O	**SCK0** — Serial clock for SSP0.
					-	O	**CT16B0_MAT2** — Match output 2 for 16-bit timer 0.
TDI/PIO0_11/AD0/ CT32B0_MAT3	42	32	21	[6]	I; PU	I	**TDI** — Test Data In for JTAG interface.
					-	I/O	**PIO0_11** — General purpose digital input/output pin.
					-	I	**AD0** — A/D converter, input 0.
					-	O	**CT32B0_MAT3** — Match output 3 for 32-bit timer 0.
TMS/PIO0_12/AD1/ CT32B1_CAP0	44	33	22	[6]	I; PU	I	**TMS** — Test Mode Select for JTAG interface.
					-	I/O	**PIO_12** — General purpose digital input/output pin.
					-	I	**AD1** — A/D converter, input 1.
					-	I	**CT32B1_CAP0** — Capture input 0 for 32-bit timer 1.
TDO/PIO0_13/AD2/ CT32B1_MAT0	45	34	23	[6]	I; PU	O	**TDO** — Test Data Out for JTAG interface.
					-	I/O	**PIO0_13** — General purpose digital input/output pin.
					-	I	**AD2** — A/D converter, input 2.
					-	O	**CT32B1_MAT0** — Match output 0 for 32-bit timer 1.
$\overline{\text{TRST}}$/PIO0_14/AD3/ CT32B1_MAT1	46	35	24	[6]	I; PU	I	**$\overline{\text{TRST}}$** — Test Reset for JTAG interface.
					-	I/O	**PIO0_14** — General purpose digital input/output pin.
					-	I	**AD3** — A/D converter, input 3.
					-	O	**CT32B1_MAT1** — Match output 1 for 32-bit timer 1.
SWDIO/PIO0_15/AD4/ CT32B1_MAT2	52	39	25	[6]	I; PU	I/O	**SWDIO** — Serial wire debug input/output.
					-	I/O	**PIO0_15** — General purpose digital input/output pin.
					-	I	**AD4** — A/D converter, input 4.
					-	O	**CT32B1_MAT2** — Match output 2 for 32-bit timer 1.
PIO0_16/AD5/ CT32B1_MAT3/WAKEUP	53	40	26	[7]	I; PU	I/O	**PIO0_16** — General purpose digital input/output pin.
					-	I	**AD5** — A/D converter, input 5.
					-	O	**CT32B1_MAT3** — Match output 3 for 32-bit timer 1.
					-	I	**WAKEUP** — Deep power-down mode wake-up pin with 20 ns glitch filter. This pin must be pulled HIGH externally to enter Deep power-down mode and pulled LOW to exit Deep power-down mode. A LOW-going pulse as short as 50 ns wakes up the part.

Table 4. Pin description (LPC1345/46/47 - with USB)

Symbol	LQFP64	LQFP48	HVQFN33		Reset state[1]	Type	Description
PIO0_17/$\overline{\text{RTS}}$/ CT32B0_CAP0/SCLK	60	45	30	[3]	I; PU	I/O	**PIO0_17** — General purpose digital input/output pin.
					-	O	**$\overline{\text{RTS}}$** — Request To Send output for USART.
					-	I	**CT32B0_CAP0** — Capture input 0 for 32-bit timer 0.
					-	I/O	**SCLK** — Serial clock input/output for USART in synchronous mode.
PIO0_18/RXD/ CT32B0_MAT0	61	46	31	[3]	I; PU	I/O	**PIO0_18** — General purpose digital input/output pin.
					-	I	**RXD** — Receiver input for USART. Used in UART ISP mode.
					-	O	**CT32B0_MAT0** — Match output 0 for 32-bit timer 0.
PIO0_19/TXD/ CT32B0_MAT1	62	47	32	[3]	I; PU	I/O	**PIO0_19** — General purpose digital input/output pin.
					-	O	**TXD** — Transmitter output for USART. Used in UART ISP mode.
					-	O	**CT32B0_MAT1** — Match output 1 for 32-bit timer 0.
PIO0_20/CT16B1_CAP0	11	9	7	[3]	I; PU	I/O	**PIO0_20** — General purpose digital input/output pin.
					-	I	**CT16B1_CAP0** — Capture input 0 for 16-bit timer 1.
PIO0_21/CT16B1_MAT0/ MOSI1	22	17	12	[3]	I; PU	I/O	**PIO0_21** — General purpose digital input/output pin.
					-	O	**CT16B1_MAT0** — Match output 0 for 16-bit timer 1.
					-	I/O	**MOSI1** — Master Out Slave In for SSP1.
PIO0_22/AD6/ CT16B1_MAT1/MISO1	40	30	20	[6]	I; PU	I/O	**PIO0_22** — General purpose digital input/output pin.
					-	I	**AD6** — A/D converter, input 6.
					-	O	**CT16B1_MAT1** — Match output 1 for 16-bit timer 1.
					-	I/O	**MISO1** — Master In Slave Out for SSP1.
PIO0_23/AD7	56	42	27	[6]	I; PU	I/O	**PIO0_23** — General purpose digital input/output pin.
					-	I	**AD7** — A/D converter, input 7.
PIO1_0/CT32B1_MAT0	1	-	-	[3]	I; PU	I/O	**PIO1_0** — General purpose digital input/output pin.
					-	O	**CT32B1_MAT0** — Match output 0 for 32-bit timer 1.
PIO1_1/CT32B1_MAT1	17	-	-	[3]	I; PU	I/O	**PIO1_1** — General purpose digital input/output pin.
					-	O	**CT32B1_MAT1** — Match output 1 for 32-bit timer 1.
PIO1_2/CT32B1_MAT2	34	-	-	[3]	I; PU	I/O	**PIO1_2** — General purpose digital input/output pin.
					-	O	**CT32B1_MAT2** — Match output 2 for 32-bit timer 1.
PIO1_3/CT32B1_MAT3	50	-	-	[3]	I; PU	I/O	**PIO1_3** — General purpose digital input/output pin.
					-	O	**CT32B1_MAT3** — Match output 3 for 32-bit timer 1.
PIO1_4/CT32B1_CAP0	16	-	-	[3]	I; PU	I/O	**PIO1_4** — General purpose digital input/output pin.
					-	I	**CT32B1_CAP0** — Capture input 0 for 32-bit timer 1.
PIO1_5/CT32B1_CAP1	32	-	-	[3]	I; PU	I/O	**PIO1_5** — General purpose digital input/output pin.
					-	I	**CT32B1_CAP1** — Capture input 1 for 32-bit timer 1.
PIO1_7	6	-	-	[3]	I; PU	I/O	**PIO1_7** — General purpose digital input/output pin.
PIO1_8	39	-	-	[3]	I; PU	I/O	**PIO1_8** — General purpose digital input/output pin.

Table 4. Pin description (LPC1345/46/47 - with USB)

Symbol	LQFP64	LQFP48	HVQFN33		Reset state[1]	Type	Description
PIO1_10	12	-	-	[3]	I; PU	I/O	**PIO1_10** — General purpose digital input/output pin.
PIO1_11	43	-	-	[3]	I; PU	I/O	**PIO1_11** — General purpose digital input/output pin.
PIO1_13/$\overline{\text{DTR}}$/ CT16B0_MAT0/TXD	47	36	-	[3]	I; PU	I/O	**PIO1_13** — General purpose digital input/output pin.
					-	O	**$\overline{\text{DTR}}$** — Data Terminal Ready output for USART.
					-	O	**CT16B0_MAT0** — Match output 0 for 16-bit timer 0.
					-	O	**TXD** — Transmitter output for USART.
PIO1_14/$\overline{\text{DSR}}$/ CT16B0_MAT1/RXD	49	37	-	[3]	I; PU	I/O	**PIO1_14** — General purpose digital input/output pin.
					-	I	**$\overline{\text{DSR}}$** — Data Set Ready input for USART.
					-	O	**CT16B0_MAT1** — Match output 1 for 16-bit timer 0.
					-	I	**RXD** — Receiver input for USART.
PIO1_15/$\overline{\text{DCD}}$/ CT16B0_MAT2/SCK1	57	43	28	[3]	I; PU	I/O	**PIO1_15** — General purpose digital input/output pin.
					-	I	**$\overline{\text{DCD}}$** — Data Carrier Detect input for USART.
					-	O	**CT16B0_MAT2** — Match output 2 for 16-bit timer 0.
					-	I/O	**SCK1** — Serial clock for SSP1.
PIO1_16/$\overline{\text{RI}}$/CT16B0_CAP0	63	48	-	[3]	I; PU	I/O	**PIO1_16** — General purpose digital input/output pin.
					-	I	**$\overline{\text{RI}}$** — Ring Indicator input for USART.
					-	I	**CT16B0_CAP0** — Capture input 0 for 16-bit timer 0.
PIO1_17/CT16B0_CAP1/ RXD	23	-	-	[3]	I; PU	I/O	**PIO1_17** — General purpose digital input/output pin.
					-	I	**CT16B0_CAP1** — Capture input 1 for 16-bit timer 0.
					-	I	**RXD** — Receiver input for USART.
PIO1_18/CT16B1_CAP1/ TXD	28	-	-	[3]	I; PU	I/O	**PIO1_18** — General purpose digital input/output pin.
					-	I	**CT16B1_CAP1** — Capture input 1 for 16-bit timer 1.
					-	O	**TXD** — Transmitter output for USART.
PIO1_19/$\overline{\text{DTR}}$/SSEL1	3	2	1	[3]	I; PU	I/O	**PIO1_19** — General purpose digital input/output pin.
					-	O	**$\overline{\text{DTR}}$** — Data Terminal Ready output for USART.
					-	I/O	**SSEL1** — Slave select for SSP1.
PIO1_20/$\overline{\text{DSR}}$/SCK1	18	13	-	[3]	I; PU	I/O	**PIO1_20** — General purpose digital input/output pin.
					-	I	**$\overline{\text{DSR}}$** — Data Set Ready input for USART.
					-	I/O	**SCK1** — Serial clock for SSP1.
PIO1_21/$\overline{\text{DCD}}$/MISO1	35	26	-	[3]	I; PU	I/O	**PIO1_21** — General purpose digital input/output pin.
					-	I	**$\overline{\text{DCD}}$** — Data Carrier Detect input for USART.
					-	I/O	**MISO1** — Master In Slave Out for SSP1.
PIO1_22/$\overline{\text{RI}}$/MOSI1	51	38	-	[3]	I; PU	I/O	**PIO1_22** — General purpose digital input/output pin.
					-	I	**$\overline{\text{RI}}$** — Ring Indicator input for USART.
					-	I/O	**MOSI1** — Master Out Slave In for SSP1.
PIO1_23/CT16B1_MAT1/ SSEL1	24	18	-	[3]	I; PU	I/O	**PIO1_23** — General purpose digital input/output pin.
					-	O	**CT16B1_MAT1** — Match output 1 for 16-bit timer 1.
					-	I/O	**SSEL1** — Slave select for SSP1.

Table 4. Pin description (LPC1345/46/47 - with USB)

Symbol	LQFP64	LQFP48	HVQFN33		Reset state[1]	Type	Description
PIO1_24/CT32B0_MAT0	27	21	-	[3]	I; PU	I/O	**PIO1_24 —** General purpose digital input/output pin.
					-	O	**CT32B0_MAT0 —** Match output 0 for 32-bit timer 0.
PIO1_25/CT32B0_MAT1	2	1	-	[3]	I; PU	I/O	**PIO1_25 —** General purpose digital input/output pin.
					-	O	**CT32B0_MAT1 —** Match output 1 for 32-bit timer 0.
PIO1_26/CT32B0_MAT2/ RXD	14	11	-	[3]	I; PU	I/O	**PIO1_26 —** General purpose digital input/output pin.
					-	O	**CT32B0_MAT2 —** Match output 2 for 32-bit timer 0.
					-	I	**RXD —** Receiver input for USART.
PIO1_27/CT32B0_MAT3/ TXD	15	12	-	[3]	I; PU	I/O	**PIO1_27 —** General purpose digital input/output pin.
					-	O	**CT32B0_MAT3 —** Match output 3 for 32-bit timer 0.
					-	O	**TXD —** Transmitter output for USART.
PIO1_28/CT32B0_CAP0/ SCLK	31	24	-	[3]	I; PU	I/O	**PIO1_28 —** General purpose digital input/output pin.
					-	I	**CT32B0_CAP0 —** Capture input 0 for 32-bit timer 0.
					-	I/O	**SCLK —** Serial clock input/output for USART in synchronous mode.
PIO1_29/SCK0/ CT32B0_CAP1	41	31	-	[3]	I; PU	I/O	**PIO1_29 —** General purpose digital input/output pin.
					-	I/O	**SCK0 —** Serial clock for SSP0.
					-	I	**CT32B0_CAP1 —** Capture input 1 for 32-bit timer 0.
PIO1_31	-	25	-	[3]	I; PU	I/O	**PIO1_31 —** General purpose digital input/output pin.
USB_DM	25	19	13	[8]	F	-	**USB_DM —** USB bidirectional D− line. (LPC1345/46/46 only.)
USB_DP	26	20	14	[8]	F	-	**USB_DP —** USB bidirectional D+ line. (LPC1345/46/46 only.)
XTALIN	8	6	4	[9]	-	-	Input to the oscillator circuit and internal clock generator circuits. Input voltage must not exceed 1.8 V.
XTALOUT	9	7	5	[9]	-	-	Output from the oscillator amplifier.
V_{DDA}	59	-	-		-	-	Analog 3.3 V pad supply voltage: This should be nominally the same voltage as V_{DD} but should be isolated to minimize noise and error. This voltage is used to power the ADC. This pin should be tied to 3.3 V if the ADC are not used.
VREFN	48	-	-		-	-	ADC negative reference voltage: This should be nominally the same voltage as V_{SS} but should be isolated to minimize noise and error. Level on this pin is used as a reference for ADC.

Table 4. Pin description (LPC1345/46/47 - with USB)

Symbol	LQFP64	LQFP48	HVQFN33	Reset state[1]	Type	Description
VREFP	64	-	-	-	-	ADC positive reference voltage: This should be nominally the same voltage as V_{DDA} but should be isolated to minimize noise and error. Level on this pin is used as a reference for ADC. This pin should be tied to 3.3 V if the ADC is not used.
V_{SSA}	55	-	-	-	-	analog ground: 0 V reference. This should nominally be the same voltage as V_{SS}, but should be isolated to minimize noise and error.
V_{DD}	10; 33; 58	8; 44	6; 29	-	-	Supply voltage to the internal regulator and the external rail. On LQFP48 and HVQFN33 packages, this pin is also connected to the 3.3 V ADC supply and reference voltage.
V_{SS}	7; 54	5; 41	33	-	-	Ground.

[1] Pin state at reset for default function: I = Input; O = Output; PU = internal pull-up enabled; IA = inactive, no pull-up/down enabled; F = floating; floating pins, if not used, should be tied to ground or power to minimize power consumption.

[2] See Figure 33 for the reset pad configuration. $\overline{\text{RESET}}$ functionality is not available in Deep power-down mode. Use the WAKEUP pin to reset the chip and wake up from Deep power-down mode. An external pull-up resistor is required on this pin for the Deep power-down mode.

[3] 5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors and configurable hysteresis (see Figure 32).

[4] I^2C-bus pins compliant with the I^2C-bus specification for I^2C standard mode, I^2C Fast-mode, and I^2C Fast-mode Plus.

[5] 5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors and configurable hysteresis (see Figure 32); includes high-current output driver.

[6] 5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors, configurable hysteresis, and analog input. When configured as a ADC input, digital section of the pad is disabled and the pin is not 5 V tolerant (see Figure 32); includes programmable digital input glitch filter.

[7] WAKEUP pin. 5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors, configurable hysteresis, and analog input. When configured as a ADC input, digital section of the pad is disabled and the pin is not 5 V tolerant (see Figure 32); includes digital input glitch filter.

[8] Pad provides USB functions. It is designed in accordance with the USB specification, revision 2.0 (Full-speed and Low-speed mode only). This pad is not 5 V tolerant.

[9] When the system oscillator is not used, connect XTALIN and XTALOUT as follows: XTALIN can be left floating or can be grounded (grounding is preferred to reduce susceptibility to noise). XTALOUT should be left floating.15

7. Functional description

7.1 On-chip flash programming memory

The LPC1315/16/17/45/46/47 contain up to 64 kB on-chip flash program memory. The flash can be programmed using In-System Programming (ISP) or In-Application Programming (IAP) via the on-chip boot loader software. Flash updates via USB are supported as well.

The flash memory is divided into 4 kB sectors with each sector consisting of 16 pages. Individual pages of 256 byte each can be erased using the IAP erase page command.

7.2 EEPROM

The LPC1315/16/17/45/46/47 contain 2 kB or 4 kB of on-chip byte-erasable and byte-programmable EEPROM data memory. The EEPROM can be programmed using In-Application Programming (IAP) via the on-chip boot loader software.

7.3 SRAM

The LPC1315/16/17/45/46/47 contain a total of 8 kB, 10 kB, or 12 kB on-chip static RAM memory.

7.4 On-chip ROM

The on-chip ROM contains the boot loader and the following Application Programming Interfaces (APIs):

- In-System Programming (ISP) and In-Application Programming (IAP) support for flash including IAP erase page command.
- IAP support for EEPROM
- USB API (HID, CDC, and MSC drivers) (LPC1345/46/47 only)
- Power profiles for configuring power consumption and PLL settings
- Flash updates via USB supported (LPC1345/46/47 only)

7.5 Memory map

The LPC1315/16/17/45/46/47 incorporates several distinct memory regions, shown in the following figures. Figure 8 shows the overall map of the entire address space from the user program viewpoint following reset. The interrupt vector area supports address remapping.

The AHB peripheral area is 2 MB in size and is divided to allow for up to 128 peripherals. The APB peripheral area is 512 kB in size and is divided to allow for up to 32 peripherals. Each peripheral of either type is allocated 16 kB of space. This allows simplifying the address decoding for each peripheral.

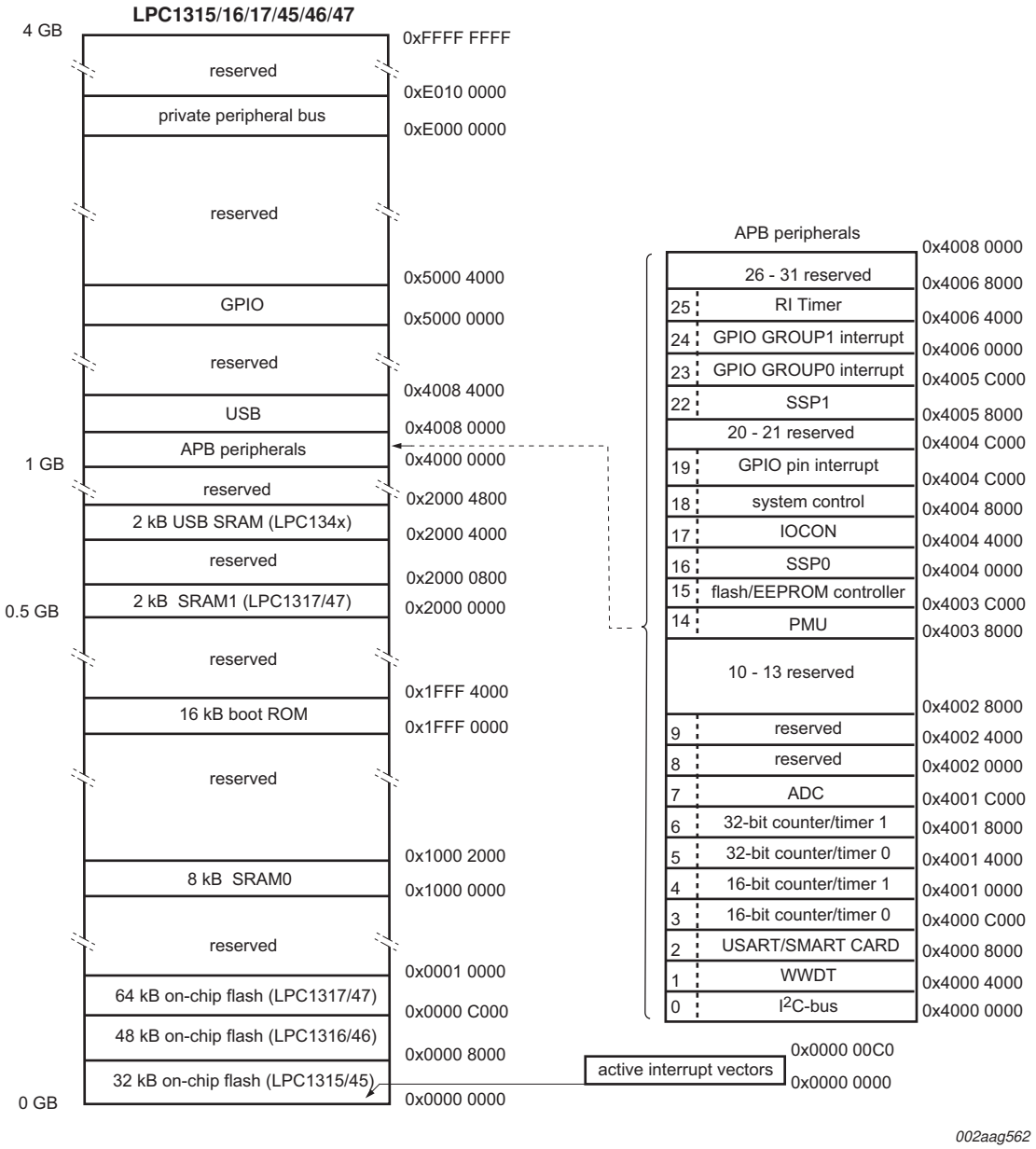


Fig 8. LPC1315/16/17/45/46/47 memory map

7.6 Nested Vectored Interrupt Controller (NVIC)

The Nested Vectored Interrupt Controller (NVIC) is an integral part of the Cortex-M3. The tight coupling to the CPU allows for low interrupt latency and efficient processing of late arriving interrupts.

7.6.1 Features

- Controls system exceptions and peripheral interrupts.
- In the LPC1315/16/17/45/46/47, the NVIC supports up to 32 vectored interrupts.
- Eight programmable interrupt priority levels with hardware priority level masking.