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LPC15xx

32-bit ARM Cortex-M3 microcontroller; up to 256 kB flash and 36 kB SRAM; FS USB, CAN, RTC, SPI, USART, I2C

Rev. 1.1 — 29 April 2015 Product data sheet

1. General description

The LPC15xx are ARM Cortex-M3 based microcontrollers for embedded applications featuring a rich peripheral set with very low power consumption. The ARM Cortex-M3 is a next generation core that offers system enhancements such as enhanced debug features and a higher level of support block integration.

The LPC15xx operate at CPU frequencies of up to 72 MHz. The ARM Cortex-M3 CPU incorporates a 3-stage pipeline and uses a Harvard architecture with separate local instruction and data buses as well as a third bus for peripherals. The ARM Cortex-M3 CPU also includes an internal prefetch unit that supports speculative branching.

The LPC15xx includes up to 256 kB of flash memory, 32 kB of ROM, a 4 kB EEPROM, and up to 36 kB of SRAM. The peripheral complement includes one full-speed USB 2.0 device, two SPI interfaces, three USARTs, one Fast-mode Plus I^2C-bus interface, one C_CAN module, PWM/timer subsystem with four configurable, multi-purpose State Configurable Timers (SCTimer/PWM) with input pre-processing unit, a Real-time clock module with independent power supply and a dedicated oscillator, two 12-channel/12-bit, 2 Msamples/s ADCs, one 12-bit, 500 kSamples/s DAC, four voltage comparators with internal voltage reference, and a temperature sensor. A DMA engine can service most peripherals.

For additional documentation related to the LPC15xx parts, see Section 17 “References”.

2. Features and benefits

- System:
  - ARM Cortex-M3 processor (version r2p1), running at frequencies of up to 72 MHz.
  - ARM Cortex-M3 built-in Nested Vectored Interrupt Controller (NVIC).
  - System tick timer.
  - Serial Wire Debug (SWD) with four breakpoints and two watchpoints.
  - Single-cycle multiplier supported.
  - Memory Protection Unit (MPU) included.
- Memory:
  - Up to 256 kB on-chip flash programming memory with 256 Byte page write and erase.
  - Up to 36 kB SRAM.
  - 4 kB EEPROM.

- ROM API support:
  - Boot loader with boot options from flash or external source via USART, C_CAN, or USB
  - USB drivers
  - ADC drivers
  - SPI drivers
  - USART drivers
  - I2C drivers
  - Power profiles and power mode configuration with low-power mode configuration option
  - DMA drivers
  - C_CAN drivers
  - Flash In-Application Programming (IAP) and In-System Programming (ISP).
- Digital peripherals:
  - Simple DMA engine with 18 channels and 20 programmable input triggers.
  - High-speed GPIO interface with up to 76 General-Purpose I/O (GPIO) pins with configurable pull-up/pull-down resistors, open-drain mode, input inverter, and programmable digital glitch filter.
  - GPIO interrupt generation capability with boolean pattern-matching feature on eight external inputs.
  - Two GPIO grouped port interrupts.
  - Switch matrix for flexible configuration of each I/O pin function.
  - CRC engine.
  - Quadrature Encoder Interface (QEI).
- Configurable PWM/timer/motor control subsystem:
  - Up to four 32-bit counter/timers or up to eight 16-bit counter/timers or combinations of 16-bit and 32-bit timers.
  - Up to 28 match outputs and 22 configurable capture inputs with input multiplexer.
  - Up to 28 PWM outputs total.
  - Dither engine for improved average resolution of pulse edges.
  - Four State Configurable Timers (SCTimers) for highly flexible, event-driven timing and PWM applications.
  - SCT Input Pre-processor Unit (SCTIPU) for processing timer inputs and immediate handling of abort situations.
  - Integrated with ADC threshold compare interrupts, temperature sensor, and analog comparator outputs for motor control feedback using analog signals.
- Special-application and simple timers:
  - 24-bit, four-channel, multi-rate timer (MRT) for repetitive interrupt generation at up to four programmable, fixed rates.
  - Repetitive interrupt timer for general purpose use.
  - Windowed Watchdog timer (WWDT).
  - High-resolution 32-bit Real-time clock (RTC) with selectable 1 s or 1 ms time resolution running in the always-on power domain. RTC can be used for wake-up from all low power modes including Deep power-down.

- Analog peripherals:
  - Two 12-bit ADC with up to 12 input channels per ADC and with multiple internal and external trigger inputs and sample rates of up to 2 Msamples/s. Each ADC supports two independent conversion sequences. ADC conversion clock can be the system clock or an asynchronous clock derived from one of the three PLLs.
  - One 12-bit DAC.
  - Integrated temperature sensor and band gap internal reference voltage.
  - Four comparators with external and internal voltage references (ACMP0 to 3). Comparator outputs are internally connected to the SCTimer/PWMs and ADCs and externally to pins. Each comparator output contains a programmable glitch filter.
- Serial interfaces:
  - Three USART interfaces with DMA, RS-485 support, autobaud, and with synchronous mode and 32 kHz mode for wake-up from Deep-sleep and Power-down modes. The USARTs share a fractional baud-rate generator.
  - Two SPI controllers.
  - One I^2C-bus interface supporting fast mode and Fast-mode Plus with data rates of up to 1Mbit/s and with multiple address recognition and monitor mode.
  - One C_CAN controller.
  - One USB 2.0 full-speed device controller with on-chip PHY.
- Clock generation:
  - 12 MHz internal RC oscillator trimmed to 1 % accuracy for $-25\ °C \leq T_{amb} \leq +85\ °C$ that can optionally be used as a system clock.
  - Crystal oscillator with an operating range of 1 MHz to 25 MHz.
  - Watchdog oscillator with a frequency range of 503 kHz.
  - 32 kHz low-power RTC oscillator with 32 kHz, 1 kHz, and 1 Hz outputs.
  - System PLL allows CPU operation up to the maximum CPU rate without the need for a high-frequency crystal. May be run from the system oscillator or the internal RC oscillator.
  - Two additional PLLs for generating the USB and SCTimer/PWM clocks.
  - Clock output function with divider that can reflect the crystal oscillator, the main clock, the IRC, or the watchdog oscillator.
- Power control:
  - Integrated PMU (Power Management Unit) to minimize power consumption.
  - Reduced power modes: Sleep mode, Deep-sleep mode, Power-down mode, and Deep power-down mode.
  - APIs provided for optimizing power consumption in active and sleep modes and for configuring Deep-sleep, Power-down, and Deep power-down modes.
  - Wake-up from Deep-sleep and Power-down modes on activity on USB, USART, SPI, and I2C peripherals.
  - Wake-up from Sleep, Deep-sleep, Power-down, and Deep power-down modes from the RTC alarm or wake-up interrupts.
  - Timer-controlled self wake-up from Deep power-down mode using the RTC high-resolution/wake-up 1 kHz timer.
  - Power-On Reset (POR).
  - BrownOut Detect BOD).
- JTAG boundary scan modes supported.
- Unique device serial number for identification.

- Single power supply 2.4 V to 3.6 V.
- Temperature range −40 °C to +105 °C.
- Available as LQFP100, LQFP64, and LQFP48 packages.

3. Applications

- Motor control
- Motion drives
- Digital power supplies
- Industrial and medical
- Solar inverters
- Home appliances
- Building and factory automation

4. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
LPC1549JBD100	LQFP100	plastic low profile quad flat package; 100 leads; body 14 × 14 × 1.4 mm	SOT407-1
LPC1549JBD64	LQFP64	plastic low profile quad flat package; 64 leads; body 10 × 10 × 1.4 mm	SOT314-2
LPC1549JBD48	LQFP48	plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2
LPC1548JBD100	LQFP100	plastic low profile quad flat package; 100 leads; body 14 × 14 × 1.4 mm	SOT407-1
LPC1548JBD64	LQFP64	plastic low profile quad flat package; 64 leads; body 10 × 10 × 1.4 mm	SOT314-2
LPC1547JBD64	LQFP64	plastic low profile quad flat package; 64 leads; body 10 × 10 × 1.4 mm	SOT314-2
LPC1547JBD48	LQFP48	plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2
LPC1519JBD100	LQFP100	plastic low profile quad flat package; 100 leads; body 14 × 14 × 1.4 mm	SOT407-1
LPC1519JBD64	LQFP64	plastic low profile quad flat package; 64 leads; body 10 × 10 × 1.4 mm	SOT314-2
LPC1518JBD100	LQFP100	plastic low profile quad flat package; 100 leads; body 14 × 14 × 1.4 mm	SOT407-1
LPC1518JBD64	LQFP64	plastic low profile quad flat package; 64 leads; body 10 × 10 × 1.4 mm	SOT314-2
LPC1517JBD64	LQFP64	plastic low profile quad flat package; 64 leads; body 10 × 10 × 1.4 mm	SOT314-2
LPC1517JBD48	LQFP48	plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2

4.1 Ordering options

Table 2. Ordering options for LPC15xx

Type number	Flash/ kB	EEPROM/ kB	Total SRAM/ kB	USB	USART	I^2C	SPI	C_CAN	SCTimer/ PWM	12-bit ADC0/1 channels	DAC	GPIO
LPC1549JBD100	256	4	36	yes	3	1	2	1	4	12/12	1	76
LPC1549JBD64	256	4	36	yes	3	1	2	1	4	12/12	1	44
LPC1549JBD48	256	4	36	yes	3	1	2	1	4	9/7	1	30
LPC1548JBD100	128	4	20	yes	3	1	2	1	4	12/12	1	76
LPC1548JBD64	128	4	20	yes	3	1	2	1	4	12/12	1	44
LPC1547JBD64	64	4	12	yes	3	1	2	1	4	12/12	1	44
LPC1547JBD48	64	4	12	yes	3	1	2	1	4	9/7	1	30
LPC1519JBD100	256	4	36	no	3	1	2	1	4	12/12	1	78
LPC1519JBD64	256	4	36	no	3	1	2	1	4	12/12	1	46
LPC1518JBD100	128	4	20	no	3	1	2	1	4	12/12	1	78
LPC1518JBD64	128	4	20	no	3	1	2	1	4	12/12	1	46
LPC1517JBD64	64	4	12	no	3	1	2	1	4	12/12	1	46
LPC1517JBD48	64	4	12	no	3	1	2	1	4	9/7	1	32

5. Marking

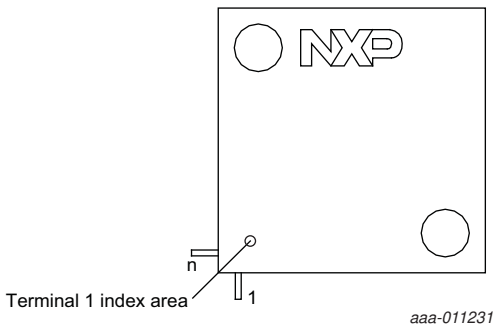


Fig 1. LQFP64/100 package marking

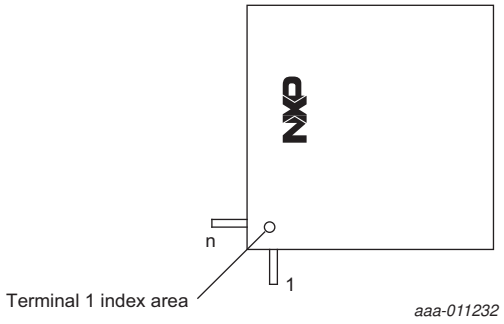


Fig 2. LQFP48 package marking

The LPC15xx devices typically have the following top-side marking for LQFP100 packages:

LPC15xxJxxx
Xxxxxx xx
xxxyywwxxx

The LPC15xx devices typically have the following top-side marking for LQFP64 packages:

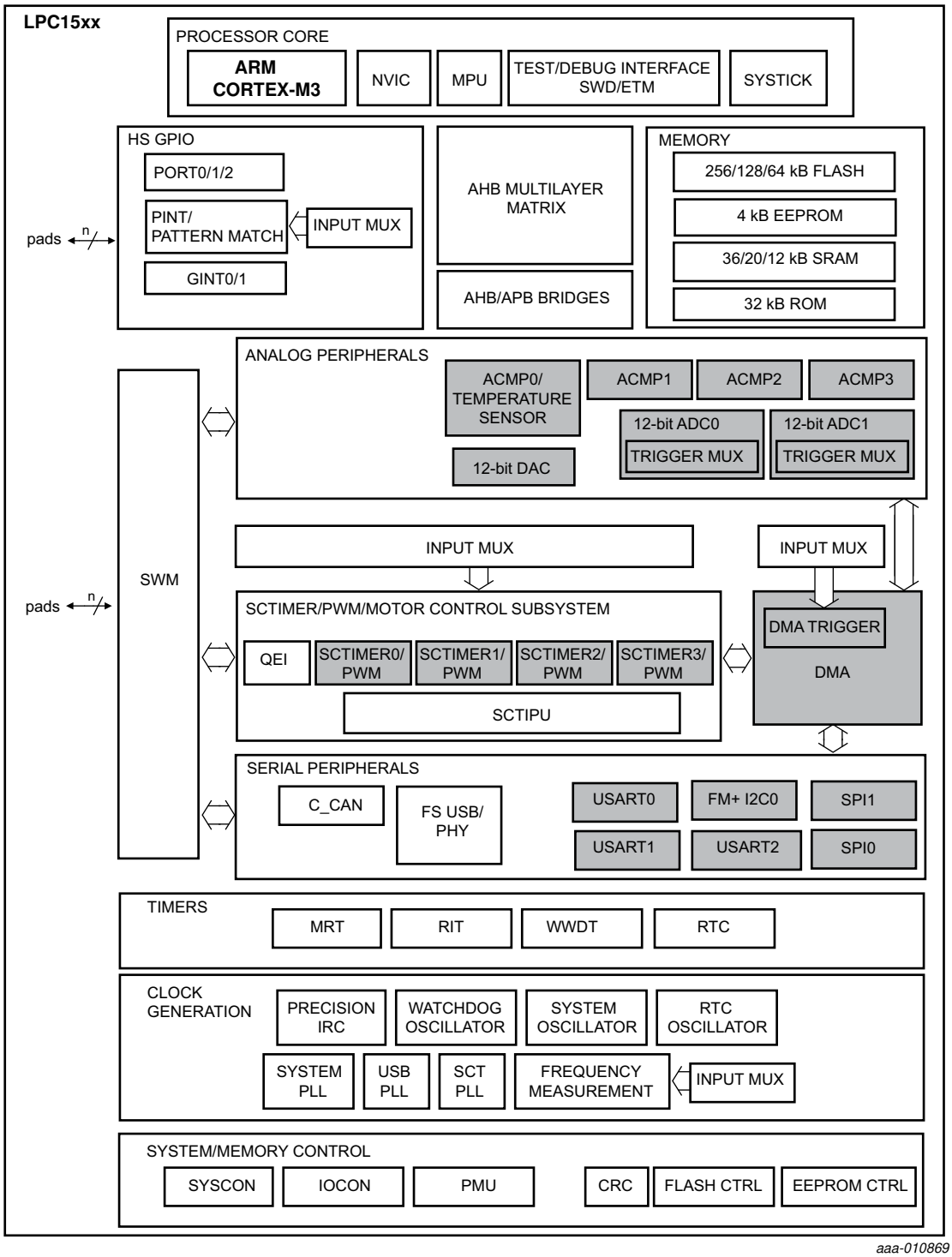
LPC15xxJ
Xxxxxx xx
xxxyywwxxx

The LPC15xx devices typically have the following top-side marking for LQFP48 packages:

LPC15xxJ
Xxxxxx
Xxxyy
wwxxx

Field ‘yy’ states the year the device was manufactured. Field ‘ww’ states the week the device was manufactured during that year.

6. Block diagram



Grey-shaded blocks show peripherals that can provide hardware triggers for DMA transfers or have DMA request lines.

Fig 3. LPC15xx Block diagram

7. Pinning information

7.1 Pinning

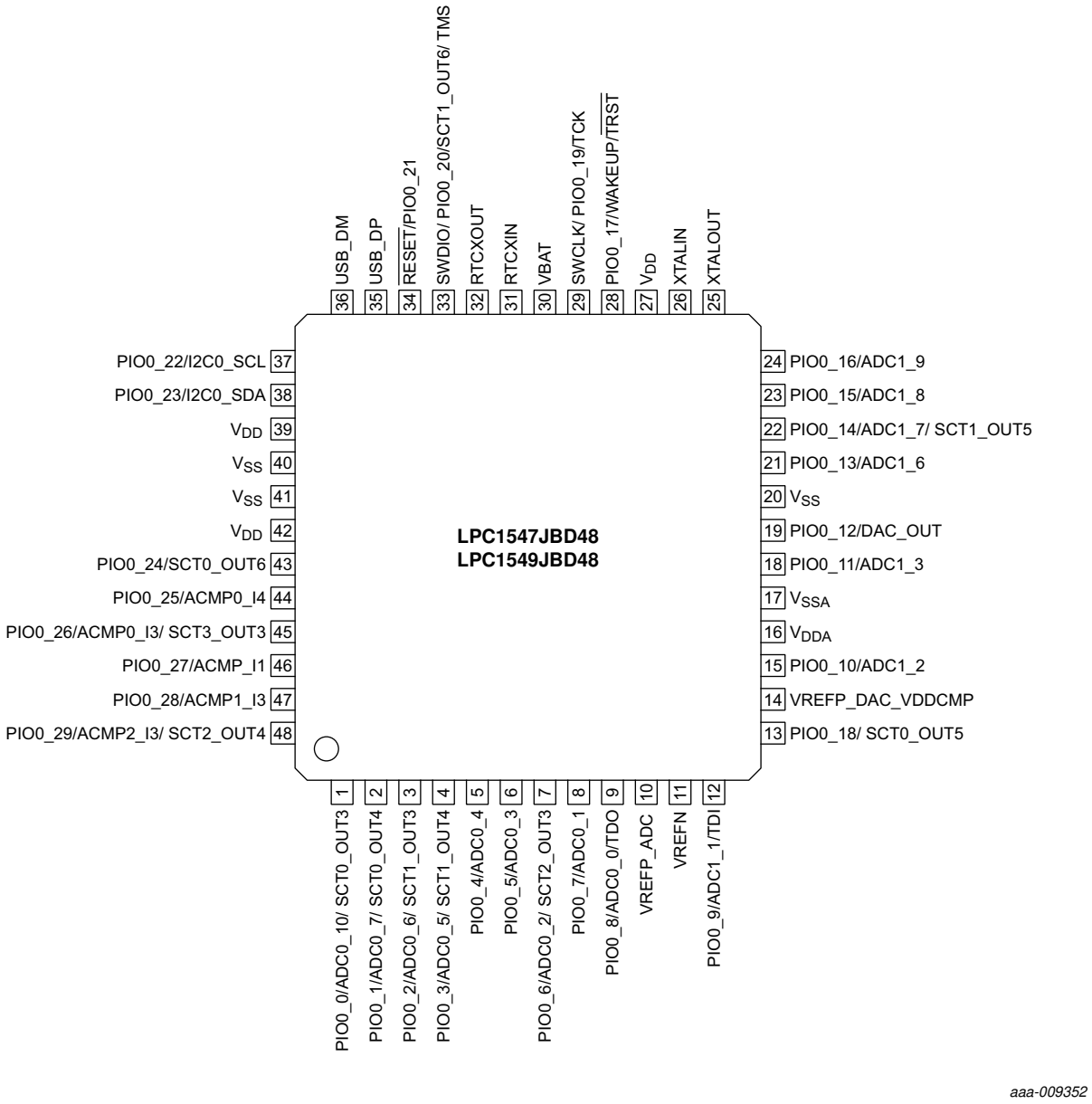


Fig 4. LQFP48 pin configuration (with USB)

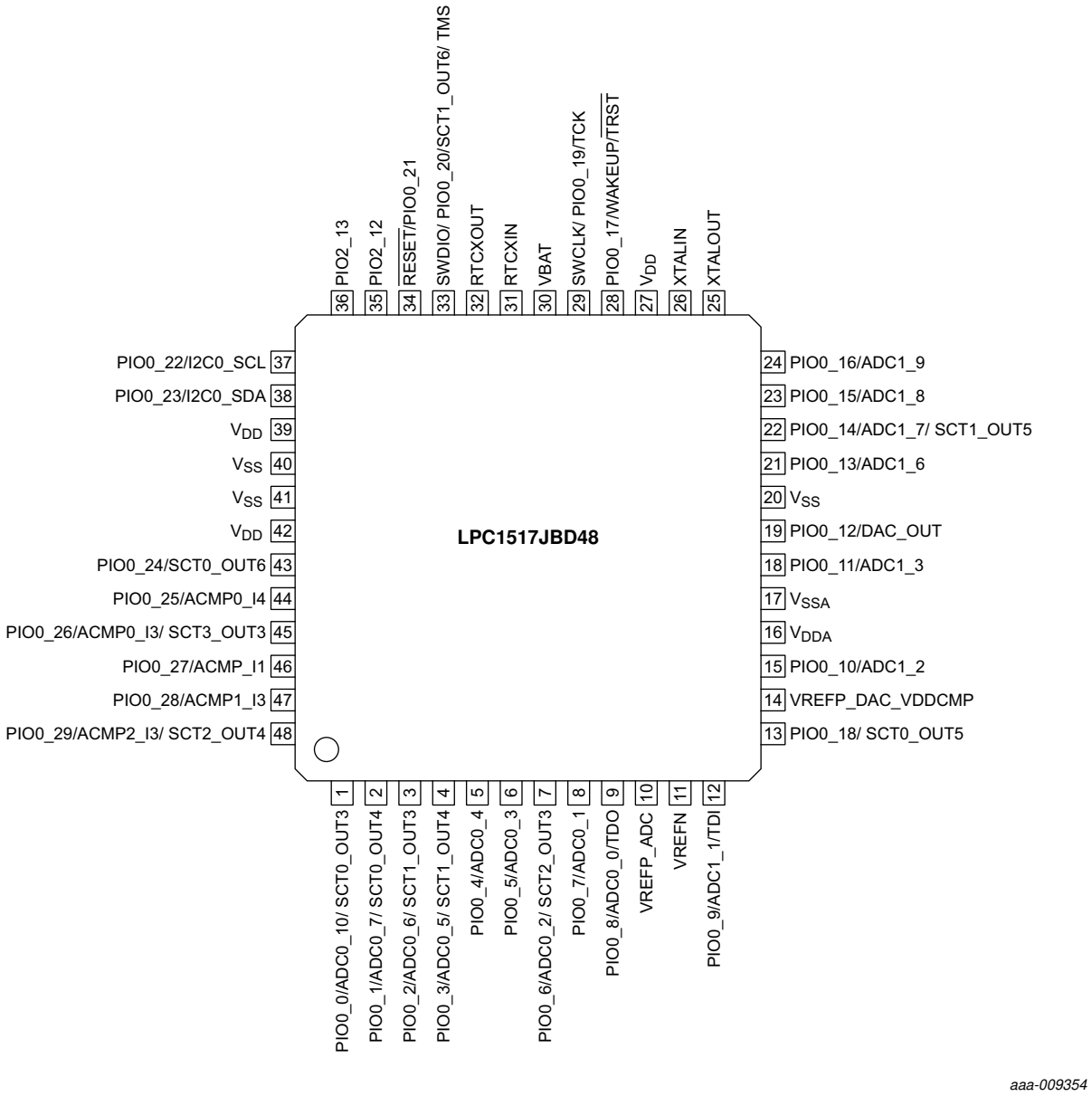
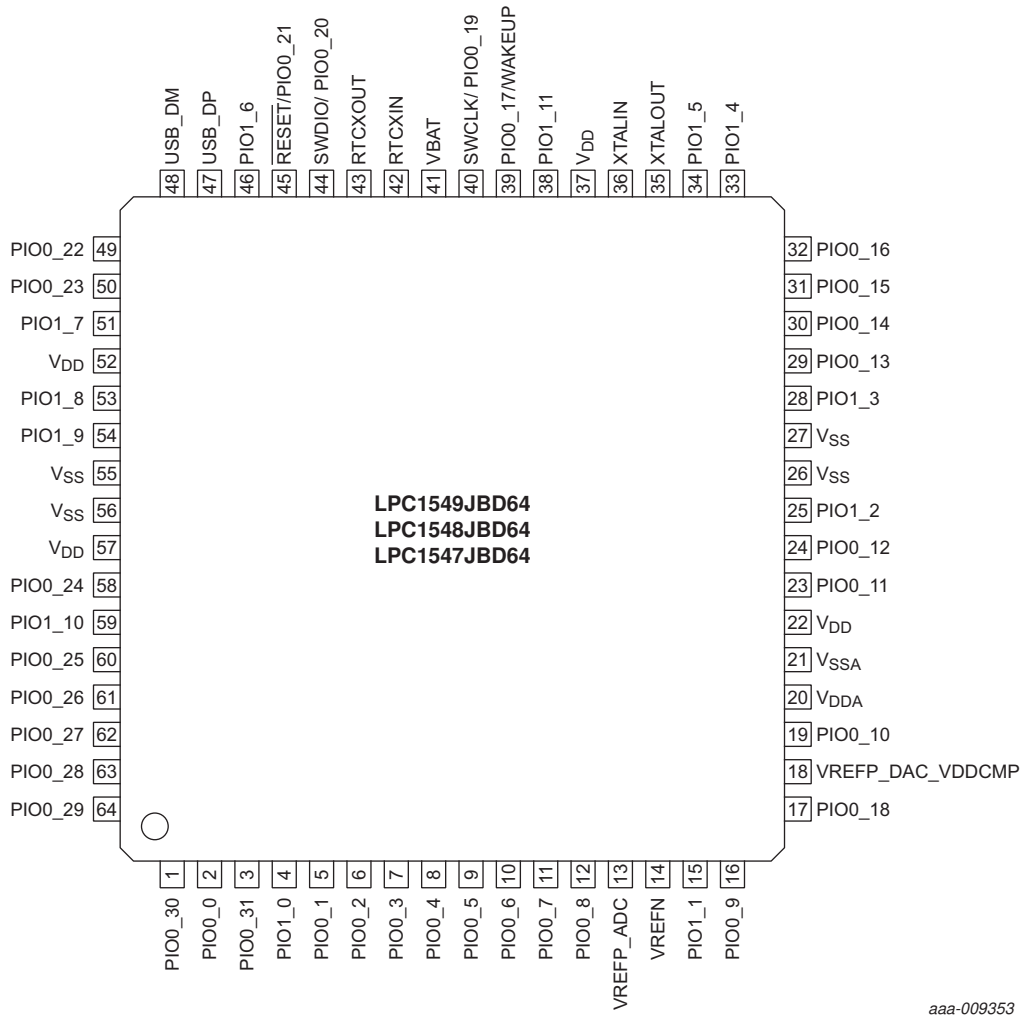


Fig 5. LQFP48 pin configuration (without USB)



See Table 3 for the full pin name.

Fig 6. LQFP64 pin configuration (with USB)

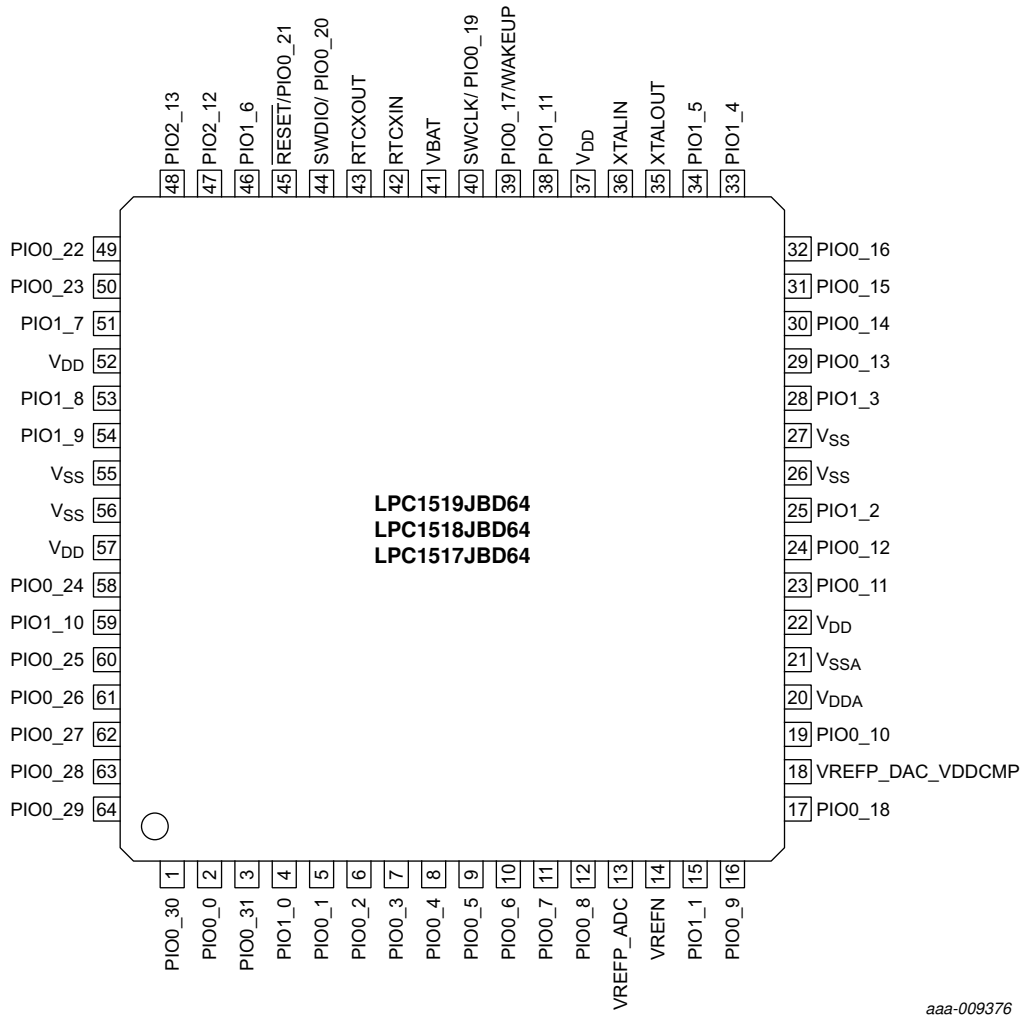


Fig 7. LQFP64 pin configuration (without USB)

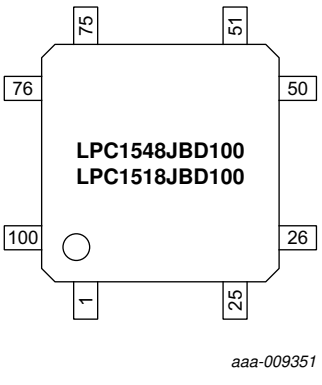


Fig 8. LQFP100 pin configuration

7.2 Pin description

Most pins are configurable for multiple functions, which can be analog or digital. Digital inputs can be connected to several peripherals at once, however only one digital output or one analog function can be assigned to any on pin. The pin's connections to internal peripheral blocks are configured by the switch matrix (SWM), the input multiplexer (INPUT MUX), and the SCT Input Pre-processor Unit (SCTIPU).

The switch matrix enables certain fixed-pin functions that can only reside on specific pins (see Table 3) and assigns all other pin functions (movable functions) to any available pin (see Table 4), so that the pinout can be optimized for a given application.

The input multiplexer provides many choices (pins and internal signals) for selecting the inputs of the SCTimer/PWMs and the frequency measure block. Pins that are connected to the input multiplexer are listed in Table 5. If a pin is selected in the input multiplexer, it is directly connected to the peripheral input without being routed through the switch matrix. Independently of being selected in the input multiplexer, the same pin can also be assigned by the switch matrix to another peripheral input.

Four pins can also be connected directly to the SCTIPU and at the same time be inputs to the input multiplexer and the switch matrix (see Table 5).

Table 3. Pin description with fixed-pin functions

Symbol	LQFP48	LQFP64	LQFP100		Reset state[1]	Type	Description
PIO0_0/ADC0_10/ SCT0_OUT3	1	2	2	[2]	I; PU	IO	**PIO0_0 —** General purpose port 0 input/output 0.
						A	**ADC0_10 —** ADC0 input 10.
						O	**SCT0_OUT3 —** SCTimer0/PWM output 3.
PIO0_1/ADC0_7/ SCT0_OUT4	2	5	6	[2]	I; PU	IO	**PIO0_1 —** General purpose port 0 input/output 1.
						A	**ADC0_7 —** ADC0 input 7.
						O	**SCT0_OUT4 —** SCTimer0/PWM output 4.
PIO0_2/ADC0_6/ SCT1_OUT3	3	6	8	[2]	I; PU	IO	**PIO0_2 —** General purpose port 0 input/output 2.
							ADC0_6 — ADC0 input 6.
						O	**SCT1_OUT3 —** SCTimer1/PWM output 3.
PIO0_3/ADC0_5/ SCT1_OUT4	4	7	10	[2]	I; PU	IO	**PIO0_3 —** General purpose port 0 input/output 3.
						A	**ADC0_5 —** ADC0 input 5.
						O	**SCT1_OUT4 —** SCTimer1/PWM output 4.
PIO0_4/ADC0_4	5	8	13	[2]	I; PU	IO	**PIO0_4 —** General purpose port 0 input/output 4. This is the ISP_0 boot pin for the LQFP48 package.
						A	**ADC0_4 —** ADC0 input 4.
PIO0_5/ADC0_3	6	9	14	[2]	I; PU	IO	**PIO0_5 —** General purpose port 0 input/output 5.
						A	**ADC0_3 —** ADC0 input 3.
PIO0_6/ADC0_2/ SCT2_OUT3	7	10	16	[2]	I; PU	IO	**PIO0_6 —** General purpose port 0 input/output 6.
						A	**ADC0_2 —** ADC0 input 2.
						O	**SCT2_OUT3 —** SCTimer2/PWM output 3.
PIO0_7/ADC0_1	8	11	17	[2]	I; PU	IO	**PIO0_7 —** General purpose port 0 input/output 7.
						A	**ADC0_1 —** ADC0 input 1.

Table 3. Pin description with fixed-pin functions

Symbol	LQFP48	LQFP64	LQFP100		Reset state[1]	Type	Description
PIO0_8/ADC0_0/TDO	9	12	19	[2]	I; PU	IO	**PIO0_8 —** General purpose port 0 input/output 8. In boundary scan mode: TDO (Test Data Out).
						A	**ADC0_0 —** ADC0 input 0.
PIO0_9/ADC1_1/TDI	12	16	24	[2]	I; PU	IO	**PIO0_9 —** General purpose port 0 input/output 9. In boundary scan mode: TDI (Test Data In).
						A	**ADC1_1 —** ADC1 input 1.
PIO0_10/ADC1_2	15	19	28	[2]	I; PU	IO	**PIO0_10 —** General purpose port 0 input/output 10.
						A	**ADC1_2 —** ADC1 input 2.
PIO0_11/ADC1_3	18	23	33	[2]	I; PU	IO	**PIO0_11 —** General purpose port 0 input/output 11. On the LQFP64 package, this pin is assigned to CAN0_RD in ISP C_CAN mode.
						A	**ADC1_3 —** ADC1 input 3.
PIO0_12/DAC_OUT	19	24	35	[3]	I; PU	IO	**PIO0_12 —** General purpose port 0 input/output 12. If this pin is configured as a digital input, the input voltage level must not be higher than V_{DDA}.
						A	**DAC_OUT —** DAC analog output.
PIO0_13/ADC1_6	21	29	43	[2]	I; PU	IO	**PIO0_13 —** General purpose port 0 input/output 13. On the LQFP64 package, this pin is assigned to U0_RXD in ISP USART mode. On the LQFP48 package, this pin is assigned to CAN0_RD in ISP C_CAN mode.
						A	**ADC1_6 —** ADC1 input 6.
PIO0_14/ADC1_7/ SCT1_OUT5	22	30	45	[2]	I; PU	IO	**PIO0_14 —** General purpose port 0 input/output 14. On the LQFP48 package, this pin is assigned to U0_RXD in ISP USART mode.
						A	**ADC1_7 —** ADC1 input 7.
						O	**SCT1_OUT5 —** SCTimer1/PWM output 5.
PIO0_15/ADC1_8	23	31	47	[2]	I; PU	IO	**PIO0_15 —** General purpose port 0 input/output 15. On the LQFP48 package, this pin is assigned to U0_TXD in ISP USART mode.
						A	**ADC1_8 —** ADC1 input 8.
PIO0_16/ADC1_9	24	32	49	[2]	I; PU	IO	**PIO0_16 —** General purpose port 0 input/output 16. On the LQFP48 package, this is the ISP_1 boot pin.
						A	**ADC1_9 —** ADC1 input 9.
PIO0_17/WAKEUP/ $\overline{\text{TRST}}$	28	39	61	[4]	I; PU	IO	**PIO0_17 —** General purpose port 0 input/output 17. In boundary scan mode: $\overline{\text{TRST}}$ (Test Reset). This pin triggers a wake-up from Deep power-down mode. For wake up from Deep power-down mode via an external pin, do not assign any movable function to this pin. Pull this pin HIGH externally while in Deep power-down mode. Pull this pin LOW to exit Deep power-down mode. A LOW-going pulse as short as 50 ns wakes up the part.

Table 3. Pin description with fixed-pin functions

Symbol	LQFP48	LQFP64	LQFP100		Reset state[1]	Type	Description
PIO0_18/ SCT0_OUT5	13	17	26	[5]	I; PU	IO	**PIO0_18 —** General purpose port 0 input/output 18. On the LQFP64 package, this pin is assigned to U0_TXD in ISP USART mode. On the LQFP48 package, this pin is assigned to CAN0_TD in ISP C_CAN mode.
						O	**SCT0_OUT5 —** SCTimer0/PWM output 5.
SWCLK/ PIO0_19/TCK	29	40	63	[5]	I; PU	I	**SWCLK —** Serial Wire Clock. SWCLK is enabled by default on this pin. In boundary scan mode: TCK (Test Clock).
						IO	**PIO0_19 —** General purpose port 0 input/output 19.
SWDIO/ PIO0_20/SCT1_OUT6/ TMS	33	44	69	[5]	I; PU	I/O	**SWDIO —** Serial Wire Debug I/O. SWDIO is enabled by default on this pin. In boundary scan mode: TMS (Test Mode Select).
						I/O	**PIO0_20 —** General purpose port 0 input/output 20.
						O	**SCT1_OUT6 —** SCTimer1/PWM output 6.
$\overline{\text{RESET}}$/PIO0_21	34	45	71	[6]	I; PU	I	**$\overline{\text{RESET}}$ —** External reset input: A LOW-going pulse as short as 50 ns on this pin resets the device, causing I/O ports and peripherals to take on their default states, and processor execution to begin at address 0. In deep power-down mode, this pin must be pulled HIGH externally. The $\overline{\text{RESET}}$ pin can be left unconnected or be used as a GPIO or for any movable function if an external $\overline{\text{RESET}}$ function is not needed and the Deep power-down mode is not used.
						I/O	**PIO0_21 —** General purpose port 0 input/output 21.
PIO0_22/I2C0_SCL	37	49	78	[7]	IA	IO	**PIO0_22 —** General purpose port 0 input/output 22 (open-drain)
						I/O	**I2C0_SCL —** Open-drain I^2C-bus clock input/output. High-current sink if I^2C Fast-mode Plus is selected in the I/O configuration register.
PIO0_23/I2C0_SDA	38	50	79	[7]	IA	IO	**PIO0_23 —** General purpose port 0 input/output 23 (open-drain).
						I/O	**I2C0_SDA —** I^2C-bus data input/output. High-current sink if I^2C Fast-mode Plus is selected in the I/O configuration register.
PIO0_24/SCT0_OUT6	43	58	90	[8]	I; PU	IO	**PIO0_24 —** General purpose port 0 input/output 24. High-current output driver.
						O	**SCT0_OUT6 —** SCTimer0/PWM output 6.
PIO0_25/ACMP0_I4	44	60	93	[2]	I; PU	IO	**PIO0_25 —** General purpose port 0 input/output 25.
						A	**ACMP0_I4 —** Analog comparator 0 input 4.
PIO0_26/ACMP0_I3/ SCT3_OUT3	45	61	95	[2]	I; PU	IO	**PIO0_26 —** General purpose port 0 input/output 26.
						A	**ACMP0_I3 —** Analog comparator 0 input 3.
						O	**SCT3_OUT3 —** SCTimer3/PWM output 3.

Table 3. Pin description with fixed-pin functions

Symbol	LQFP48	LQFP64	LQFP100		Reset state[1]	Type	Description
PIO0_27/ACMP_I1	46	62	97	[2]	I; PU	IO	**PIO0_27 —** General purpose port 0 input/output 27.
						A	**ACMP_I1 —** Analog comparator common input 1.
PIO0_28/ACMP1_I3	47	63	98	[2]	I; PU	IO	**PIO0_28 —** General purpose port 0 input/output 28.
						A	**ACMP1_I3 —** Analog comparator 1 input 3.
PIO0_29/ACMP2_I3/ SCT2_OUT4	48	64	100	[2]	I; PU	IO	**PIO0_29 —** General purpose port 0 input/output 29.
						A	**ACMP2_I3 —** Analog comparator 2 input 3.
						O	**SCT2_OUT4 —** SCTimer2/PWM output 4.
PIO0_30/ADC0_11	-	1	1	[2]	I; PU	IO	**PIO0_30 —** General purpose port 0 input/output 30.
						A	**ADC0_11 —** ADC0 input 11.
PIO0_31/ADC0_9	-	3	3	[2]	I; PU	IO	**PIO0_31 —** General purpose port 0 input/output 31. On the LQFP64 package, this pin is assigned to CAN0_TD in ISP C_CAN mode.
						A	**ADC0_9 —** ADC0 input 9.
PIO1_0/ADC0_8	-	4	5	[2]	I; PU	IO	**PIO1_0 —** General purpose port 1 input/output 0.
						A	**ADC0_8 —** ADC0 input 8.
PIO1_1/ADC1_0	-	15	23	[2]	I; PU	IO	**PIO1_1 —** General purpose port 1 input/output 1.
						A	**ADC1_0 —** ADC1 input 0.
PIO1_2/ADC1_4	-	25	36	[2]	I; PU	IO	**PIO1_2 —** General purpose port 1 input/output 2.
						A	**ADC1_4 —** ADC1 input 4.
PIO1_3/ADC1_5	-	28	41	[2]	I; PU	IO	**PIO1_3 —** General purpose port 1 input/output 3.
						A	**ADC1_5 —** ADC1 input 5.
PIO1_4/ADC1_10	-	33	51	[2]	I; PU	IO	**PIO1_4 —** General purpose port 1 input/output 4.
						A	**ADC1_10 —** ADC1 input 10.
PIO1_5/ADC1_11	-	34	52	[2]	I; PU	IO	**PIO1_5 —** General purpose port 1 input/output 5.
						A	**ADC1_11 —** ADC1 input 11.
PIO1_6/ACMP_I2	-	46	73	[2]	I; PU	IO	**PIO1_6 —** General purpose port 1 input/output 6.
						A	**ACMP_I2 —** Analog comparator common input 2.
PIO1_7/ACMP3_I4	-	51	81	[2]	I; PU	IO	**PIO1_7 —** General purpose port 1 input/output 7.
						A	**ACMP3_I4 —** Analog comparator 3 input 4.
PIO1_8/ACMP3_I3/ SCT3_OUT4	-	53	84	[2]	I; PU	IO	**PIO1_8 —** General purpose port 1 input/output 8.
						A	**ACMP3_I3 —** Analog comparator 3 input 3.
						O	**SCT3_OUT4 —** SCTimer3/PWM output 4.
PIO1_9/ACMP2_I4	-	54	85	[2]	I; PU	IO	**PIO1_9 —** General purpose port 1 input/output 9. On the LQFP64 package, this is the ISP_0 boot pin.
						A	**ACMP2_I4 —** Analog comparator 2 input 4.
PIO1_10/ACMP1_I4	-	59	91	[2]	I; PU	IO	**PIO1_10 —** General purpose port 1 input/output 10.
						A	**ACMP1_I4 —** Analog comparator 1 input 4.
PIO1_11	-	38	58	[5]	I; PU	IO	**PIO1_11 —** General purpose port 1 input/output 11. On the LQFP64 package, this is the ISP_1 boot pin.

Table 3. Pin description with fixed-pin functions

Symbol	LQFP48	LQFP64	LQFP100		Reset state[1]	Type	Description
PIO1_12	-	-	9	[5]	I; PU	IO	**PIO1_12 —** General purpose port 1 input/output 12.
PIO1_13	-	-	11	[5]	I; PU	IO	**PIO1_13 —** General purpose port 1 input/output 13.
PIO1_14/SCT0_OUT7	-	-	12	[5]	I; PU	IO	**PIO1_14 —** General purpose port 1 input/output 14.
						O	**SCT0_OUT7 —** SCTimer0/PWM output 7.
PIO1_15	-	-	15	[5]	I; PU	IO	**PIO1_15 —** General purpose port 1 input/output 15.
PIO1_16	-	-	18	[5]	I; PU	IO	**PIO1_16 —** General purpose port 1 input/output 16.
PIO1_17/SCT1_OUT7	-	-	20	[5]	I; PU	IO	**PIO1_17 —** General purpose port 1 input/output 17.
						O	**SCT1_OUT7 —** SCTimer1/PWM output 7.
PIO1_18	-	-	25	[5]	I; PU	IO	**PIO1_18 —** General purpose port 1 input/output 18.
PIO1_19	-	-	29	[5]	I; PU	IO	**PIO1_19 —** General purpose port 1 input/output 19.
PIO1_20/SCT2_OUT5	-	-	34	[5]	I; PU	IO	**PIO1_20 —** General purpose port 1 input/output 20.
						O	**SCT2_OUT5 —** SCTimer2/PWM output 5.
PIO1_21	-	-	37	[5]	I; PU	IO	**PIO1_21 —** General purpose port 1 input/output 21.
PIO1_22	-	-	38	[5]	I; PU	IO	**PIO1_22 —** General purpose port 1 input/output 22.
PIO1_23	-	-	42	[5]	I; PU	IO	**PIO1_23 —** General purpose port 1 input/output 23.
PIO1_24/SCT3_OUT5	-	-	44	[5]	I; PU	IO	**PIO1_24 —** General purpose port 1 input/output 24.
						O	**SCT3_OUT5 —** SCTimer3/PWM output 5.
PIO1_25	-	-	46	[5]	I; PU	IO	**PIO1_25 —** General purpose port 1 input/output 25.
PIO1_26	-	-	48	[5]	I; PU	IO	**PIO1_26 —** General purpose port 1 input/output 26.
PIO1_27	-	-	50	[5]	I; PU	IO	**PIO1_27 —** General purpose port 1 input/output 27.
PIO1_28	-	-	55	[5]	I; PU	IO	**PIO1_28 —** General purpose port 1 input/output 28.
PIO1_29	-	-	56	[5]	I; PU	IO	**PIO1_29 —** General purpose port 1 input/output 29.
PIO1_30	-	-	59	[5]	I; PU	IO	**PIO1_30 —** General purpose port 1 input/output 30.
PIO1_31	-	-	60	[5]	I; PU	IO	**PIO1_31 —** General purpose port 1 input/output 31.
PIO2_0	-	-	62	[5]	I; PU	IO	**PIO2_0 —** General purpose port 2 input/output 0.
PIO2_1	-	-	64	[5]	I; PU	IO	**PIO2_1 —** General purpose port 2 input/output 1.
PIO2_2	-	-	72	[5]	I; PU	IO	**PIO2_2 —** General purpose port 2 input/output 2.
PIO2_3	-	-	76	[5]	I; PU	IO	**PIO2_3 —** General purpose port 2 input/output 3.
PIO2_4	-	-	77	[5]	I; PU	IO	**PIO2_4 —** General purpose port 2 input/output 4. On the LQFP100 package, this is the ISP_1 boot pin.
PIO2_5	-	-	80	[5]	I; PU	IO	**PIO2_5 —** General purpose port 2 input/output 5. On the LQFP100 package, this is the ISP_0 boot pin.
PIO2_6	-	-	82	[5]	I; PU	IO	**PIO2_6 —** General purpose port 2 input/output 6. On the LQFP100 package, this pin is assigned to U0_TXD in ISP USART mode.
PIO2_7	-	-	86	[5]	I; PU	IO	**PIO2_7 —** General purpose port 2 input/output 7. On the LQFP100 package, this pin is assigned to U0_RXD in ISP USART mode.

Table 3. Pin description with fixed-pin functions

Symbol	LQFP48	LQFP64	LQFP100		Reset state[1]	Type	Description
PIO2_8	-	-	92	[5]	I; PU	IO	**PIO2_8 —** General purpose port 2 input/output 8. On the LQFP100 package, this pin is assigned to CAN0_TD in ISP C_CAN mode.
PIO2_9	-	-	94	[5]	I; PU	IO	**PIO2_9 —** General purpose port 2 input/output 9. On the LQFP100 package, this pin is assigned to CAN0_RD in ISP C_CAN mode.
PIO2_10	-	-	96	[5]	I; PU	IO	**PIO2_10 —** General purpose port 2 input/output 10.
PIO2_11	-	-	99	[5]	I; PU	IO	**PIO2_11 —** General purpose port 2 input/output 11.
PIO2_12	35	47	74	[5]	I; PU	IO	**PIO2_12 —** General purpose port 2 input/output 12. On parts LPC1519/17/18 only.
PIO2_13	36	48	75	[5]	I; PU	IO	**PIO2_13 —** General purpose port 2 input/output 13. On parts LPC1519/17/18 only.
USB_DP	35	47	74	[10]	-	IO	USB bidirectional D+ line. Pad includes internal 33 Ω series termination resistor. On parts LPC1549/48/47 only.
USB_DM	36	48	75	[10]	-	IO	USB bidirectional D− line. Pad includes internal 33 Ω series termination resistor. On parts LPC1549/48/47 only.
RTCXIN	31	42	66	[9]	-		RTC oscillator input. This input should be grounded if the RTC is not used.
RTCXOUT	32	43	67	[9]	-		RTC oscillator output.
XTALIN	26	36	54	[9] [11]	-		Input to the oscillator circuit and internal clock generator circuits. Input voltage must not exceed 1.8 V.
XTALOUT	25	35	53	[9] [11]	-		Output from the oscillator amplifier.
VBAT	30	41	65		-		Battery supply voltage. Supplies power to the RTC. If no battery is used, tie VBAT to VDD or to ground.
V_{DDA}	16	20	30		-		Analog supply voltage. V_{DD} and the analog reference voltages VREFP_ADC and VREFP_DAC_VDDCMP must not exceed the voltage level on V_{DDA}. V_{DDA}should typically be the same voltages as V_{DD} but should be isolated to minimize noise and error. V_{DDA} should be tied to V_{DD} if the ADC is not used.
V_{DD}	39, 27, 42	22, 52, 37, 57	4, 32, 70, 83, 57, 89		-		3.3 V supply voltage (2.4 V to 3.6 V). The voltage level on V_{DD} must be equal or lower than the analog supply voltage V_{DDA}.
VREFP_DAC_VDDCMP	14	18	27	[9]	-		DAC positive reference voltage and analog comparator reference voltage. The voltage level on VREFP_DAC_VDDCMP must be equal to or lower than the voltage applied to V_{DDA}.
VREFN	11	14	22		-		ADC and DAC negative voltage reference. If the ADC is not used, tie VREFN to V_{SS}.

Table 3. Pin description with fixed-pin functions

Symbol	LQFP48	LQFP64	LQFP100		Reset state[1]	Type	Description
VREFP_ADC	10	13	21		-		ADC positive reference voltage. The voltage level on VREFP_ADC must be equal to or lower than the voltage applied to V_{DDA}. If the ADC is not used, tie VREFP_ADC to V_{DD}.
V_{SSA}	17	21	31		-		Analog ground. V_{SSA}should typically be the same voltage as V_{SS} but should be isolated to minimize noise and error. V_{SSA} should be tied to V_{SS} if the ADC is not used.
V_{SS}	41, 20, 40	56, 26, 27, 55	88, 7, 39, 40, 68, 87		-		Ground.

[1] Pin state at reset for default function: I = Input; O = Output; PU = internal pull-up enabled; IA = inactive, no pull-up/down enabled; F = floating; If the pins are not used, tie floating pins to ground or power to minimize power consumption.

[2] 5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors, configurable hysteresis, and analog input. When configured as analog input, digital section of the pad is disabled and the pin is not 5 V tolerant. This pin includes a 10 ns on/off glitch filter. By default, the glitch filter is turned on.

[3] This pin is not 5 V tolerant due to special analog functionality. When configured for a digital function, this pin is 3 V tolerant and provides standard digital I/O functions with configurable internal pull-up and pull-down resistors and hysteresis. When configured for DAC_OUT, the digital section of the pin is disabled and this pin is a 3 V tolerant analog output. This pin includes a 10 ns on/off glitch filter. By default, the glitch filter is turned on.

[4] 5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors, and configurable hysteresis. This pin includes a 10 ns on/off glitch filter. By default, the glitch filter is turned on. This pin is powered in deep power-down mode and can wake up the part. The wake-up pin function can be disabled and the pin can be used for other purposes, if the RTC is enabled for waking up the part from Deep power-down mode.

[5] 5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors and configurable hysteresis.

[6] 5 V tolerant pad. $\overline{\text{RESET}}$ functionality is not available in Deep power-down mode. Use the WAKEUP pin to reset the chip and wake up from Deep power-down mode. An external pull-up resistor is required on this pin for the Deep power-down mode.

[7] I^2C-bus pin compliant with the I^2C-bus specification for I^2C standard mode, I^2C Fast-mode, and I^2C Fast-mode Plus. The pin requires an external pull-up to provide output functionality. When power is switched off, this pin is floating and does not disturb the I2C lines. Open-drain configuration applies to all functions on this pin.

[8] 5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors and configurable hysteresis; includes high-current output driver.

[9] Special analog pin.

[10] Pad provides USB functions. It is designed in accordance with the USB specification, revision 2.0 (Full-speed and Low-speed mode only). This pad is not 5 V tolerant.

[11] When the main oscillator is not used, connect XTALIN and XTALOUT as follows: XTALIN can be left floating or can be grounded (grounding is preferred to reduce susceptibility to noise). XTALOUT should be left floating.

Table 4. Movable functions

Function name	Type	Description
U0_TXD	O	Transmitter output for USART0.
U0_RXD	I	Receiver input for USART0.
$\overline{\text{U0\_RTS}}$	O	Request To Send output for USART0.
$\overline{\text{U0\_CTS}}$	I	Clear To Send input for USART0.
U0_SCLK	I/O	Serial clock input/output for USART0 in synchronous mode.

Table 4. Movable functions *…continued*

Function name	Type	Description
U1_TXD	O	Transmitter output for USART1.
U1_RXD	I	Receiver input for USART1.
$\overline{\text{U1\_RTS}}$	O	Request To Send output for USART1.
$\overline{\text{U1\_CTS}}$	I	Clear To Send input for USART1.
U1_SCLK	I/O	Serial clock input/output for USART1 in synchronous mode.
U2_TXD	O	Transmitter output for USART2.
U2_RXD	I	Receiver input for USART2.
U2_SCLK	I/O	Serial clock input/output for USART1 in synchronous mode.
SPI0_SCK	I/O	Serial clock for SPI0.
SPI0_MOSI	I/O	Master Out Slave In for SPI0.
SPI0_MISO	I/O	Master In Slave Out for SPI0.
SPI0_SSEL0	I/O	Slave select 0 for SPI0.
SPI0_SSEL1	I/O	Slave select 1 for SPI0.
SPI0_SSEL2	I/O	Slave select 2 for SPI0.
SPI0_SSEL3	I/O	Slave select 3 for SPI0.
SPI1_SCK	I/O	Serial clock for SPI1.
SPI1_MOSI	I/O	Master Out Slave In for SPI1.
SPI1_MISO	I/O	Master In Slave Out for SPI1.
SPI1_SSEL0	I/O	Slave select 0 for SPI1.
SPI1_SSEL1	I/O	Slave select 1 for SPI1.
CAN0_TD	O	CAN0 transmit.
CAN0_RD	I	CAN0 receive.
USB_VBUS	I	USB VBUS.
SCT0_OUT0	O	SCTimer0/PWM output 0.
SCT0_OUT1	O	SCTimer0/PWM output 1.
SCT0_OUT2	O	SCTimer0/PWM output 2.
SCT1_OUT0	O	SCTimer1/PWM output 0.
SCT1_OUT1	O	SCTimer1/PWM output 1.
SCT1_OUT2	O	SCTimer1/PWM output 2.
SCT2_OUT0	O	SCTimer2/PWM output 0.
SCT2_OUT1	O	SCTimer2/PWM output 1.
SCT2_OUT2	O	SCTimer2/PWM output 2.
SCT3_OUT0	O	SCTimer3/PWM output 0.
SCT3_OUT1	O	SCTimer3/PWM output 1.
SCT3_OUT2	O	SCTimer3/PWM output 2.
SCT_ABORT0	I	SCT abort 0.
SCT_ABORT1	I	SCT abort 1.
ADC0_PINTRIG0	I	ADC0 external pin trigger input 0.
ADC0_PINTRIG1	I	ADC0 external pin trigger input 1.
ADC1_PINTRIG0	I	ADC1 external pin trigger input 0.
ADC1_PINTRIG1	I	ADC1 external pin trigger input 1.

Table 4. Movable functions *…continued*

Function name	Type	Description
DAC_PINTRIG	I	DAC external pin trigger input.
DAC_SHUTOFF	I	DAC shut-off external input.
ACMP0_O	O	Analog comparator 0 output.
ACMP1_O	O	Analog comparator 1 output.
ACMP2_O	O	Analog comparator 2 output.
ACMP3_O	O	Analog comparator 3 output.
CLKOUT	O	Clock output.
ROSC	O	Analog comparator ring oscillator output.
ROSC_RESET	I	Analog comparator ring oscillator reset.
USB_FTOGGLE	O	USB frame toggle. Do not assign this function to a pin until a USB device is connected and the first SOF interrupt has been received by the device.
QEI_PHA	I	QEI phase A input.
QEI_PHB	I	QEI phase B input.
QEI_IDX	I	QEI index input.
GPIO_INT_BMAT	O	Output of the pattern match engine.
SWO	O	Serial wire output.

Table 5. Pins connected to the INPUT multiplexer and SCT IPU

Symbol	LQFP48	LQFP64	LQFP100	Description
PIO0_2/ADC0_6/SCT1_OUT3	3	6	8	SCT0 input multiplexer
PIO0_3/ADC0_5/SCT1_OUT4	4	7	10	SCT0 input multiplexer
PIO0_4/ADC0_4	5	8	13	SCT2 input multiplexer
PIO0_5/ADC0_3	6	9	14	FREQMEAS
PIO0_7/ADC0_1	8	11	17	SCT3 input multiplexer
PIO0_14/ADC1_7/SCT1_OUT5	22	30	45	SCTIPU input SAMPLE_IN_A0
PIO0_15/ADC1_8	23	31	47	SCT1 input multiplexer
PIO0_16/ADC1_9	24	32	49	SCT1 input multiplexer
PIO0_17/WAKEUP/$\overline{\text{TRST}}$	28	39	61	SCT0 input multiplexer
SWCLK/PIO0_19/TCK	29	40	63	FREQMEAS
$\overline{\text{RESET}}$/PIO0_21	34	45	71	SCT1 input multiplexer
PIO0_25/ACMP0_I4	44	60	93	SCTIPU input SAMPLE_IN_A1
PIO0_27/ACMP_I1	46	62	97	SCT2 input multiplexer
PIO0_30/ADC0_11	-	1	1	FREQMEAS
				SCT0 input multiplexer
PIO0_31/ADC0_9	-	3	3	SCT1 input multiplexer
PIO1_4/ADC1_10	-	33	51	SCT1 input multiplexer
PIO1_5/ADC1_11	-	34	52	SCT1 input multiplexer
PIO1_6/ACMP_I2	-	46	73	SCT0 input multiplexer

Table 5. Pins connected to the INPUT multiplexer and SCT IPU

Symbol	LQFP48	LQFP64	LQFP100	Description
PIO1_7/ACMP3_I4	-	51	81	SCT0 input multiplexer
PIO1_11	-	38	58	SCT3 input multiplexer
				SCTIPU input SAMPLE_IN_A2
PIO1_12	-	-	9	SCT0 input multiplexer
PIO1_13	-	-	11	SCT0 input multiplexer
PIO1_15	-	-	12	SCT1 input multiplexer
PIO1_16	-	-	18	SCT1 input multiplexer
PIO1_18	-	-	25	SCT2 input multiplexer
PIO1_19	-	-	29	SCT2 input multiplexer
PIO1_21	-	-	37	SCT3 input multiplexer
PIO1_22	-	-	38	SCT3 input multiplexer
PIO1_26	-	-	48	SCTIPU input SAMPLE_IN_A3
PIO1_27	-	-	50	FREQMEAS

8. Functional description

8.1 ARM Cortex-M3 processor

The ARM Cortex-M3 is a general purpose, 32-bit microprocessor, which offers high performance and very low power consumption. The ARM Cortex-M3 offers many new features, including a Thumb-2 instruction set, low interrupt latency, hardware division, hardware single-cycle multiply, interruptible/continuable multiple load and store instructions, automatic state save and restore for interrupts, tightly integrated interrupt controller, and multiple core buses capable of simultaneous accesses.

Pipeline techniques are employed so that all parts of the processing and memory systems can operate continuously. Typically, while one instruction is being executed, its successor is being decoded, and a third instruction is being fetched from memory.

The ARM Cortex-M3 processor is described in detail in the *Cortex-M3 Technical Reference Manual*, which is available on the official ARM website.

8.2 Memory Protection Unit (MPU)

The LPC15xx have a Memory Protection Unit (MPU) which can be used to improve the reliability of an embedded system by protecting critical data within the user application.

The MPU allows separating processing tasks by disallowing access to each other's data, disabling access to memory regions, allowing memory regions to be defined as read-only and detecting unexpected memory accesses that could potentially break the system.

The MPU separates the memory into distinct regions and implements protection by preventing disallowed accesses. The MPU supports up to eight regions each of which can be divided into eight subregions. Accesses to memory locations that are not defined in the MPU regions, or not permitted by the region setting, will cause the Memory Management Fault exception to take place.

8.3 On-chip flash programming memory

The LPC15xx contain up to 256 kB on-chip flash program memory. The flash can be programmed using In-System Programming (ISP) or In-Application Programming (IAP) via the on-chip boot loader software. Flash updates via USB are supported as well.

The flash memory is divided into 4 kB sectors with each sector consisting of 16 pages. Individual pages of 256 byte each can be erased using the IAP erase page command.

8.3.1 ISP pin configuration

The LPC15xx supports ISP via the USART0, C_CAN, or USB interfaces. The ISP mode is determined by the state of two pins (ISP_0 and ISP_1) at boot time:

Table 6. ISP modes

Boot mode	ISP_0	ISP_1	Description
No ISP	HIGH	HIGH	ISP bypassed. Part attempts to boot from flash. If the user code in flash is not valid, then enters ISP via USB.
C_CAN	HIGH	LOW	Part enters ISP via C_CAN.
USB	LOW	HIGH	Part enters ISP via USB.
USART0	LOW	LOW	Part enters ISP via USART0.

The ISP pin assignment is different for each package, so that the fewest functions possible are blocked. No more than four pins must be set aside for entering ISP in any ISP mode. The boot code assigns two ISP pins for each package, which are probed when the part boots to determine whether or not to enter ISP mode. Once the ISP mode has been determined, the boot loader configures the necessary serial pins for each package.

Pins which are not configured by the boot loader for the selected boot mode (for example CAN0_RD and CAN0_TD in USART mode) can be assigned to any function through the switch matrix.

Table 7. Pin assignments for ISP modes

Boot pin	LQFP48	LQFP64	LQFP100
ISP_0	PIO0_4	PIO1_9	PIO2_5
ISP_1	PIO0_16	PIO1_11	PIO2_4
USART mode			
U0_TXD	PIO0_15	PIO0_18	PIO2_6
U0_RXD	PIO0_14	PIO0_13	PIO2_7
C_CAN mode			
CAN0_TD	PIO0_18	PIO0_31	PIO2_8
CAN0_RD	PIO0_13	PIO0_11	PIO2_9
USB mode			
USB_VBUS (same as ISP_1)	PIO0_16	PIO1_11	PIO2_4

8.4 EEPROM

The LPC15xx contain 4 kB of on-chip byte-erasable and byte-programmable EEPROM data memory. The EEPROM can be programmed using In-Application Programming (IAP) via the on-chip boot loader software.

8.5 SRAM

The LPC15xx contain a total 36 kB, 20 kB or 12 kB of contiguous, on-chip static RAM memory. For each SRAM configuration, the SRAM is divided into three blocks: 2 x 16 kB + 4 kB for 36 kB SRAM, 2 x 8 kB + 4 kB for 20 kB SRAM, and 2 x 4 kB + 4 kB for 12 kB SRAM. The bottom 16 kB, 8 kB, or 4 kB are enabled by the bootloader and cannot be disabled. The next two SRAM blocks in each configuration can be disabled or enabled individually in the SYSCON block to save power.

Table 8. LPC15xx SRAM configurations

	SRAM0	SRAM1	SRAM2
LPC1549/19 (total SRAM = 36 kB)			
address range	0x0200 0000 to 0x0200 3FFF	0x0200 4000 to 0x0200 7FFF	0x0200 8000 to 0x0200 8FFF
size	16 kB	16 kB	4 kB
control	cannot be disabled	disable/enable	disable/enable
default	enabled	enabled	enabled
LPC1548/18 (total SRAM = 20 kB)			
address range	0x0200 0000 to 0x0200 1FFF	0x0200 2000 to 0x0200 3FFF	0x0200 4000 to 0x0200 4FFF
size	8 kB	8 kB	4 kB
control	cannot be disabled	disable/enable	disable/enable
default	enabled	enabled	enabled
LPC1547/17 (total SRAM = 12 kB)			
address range	0x0200 0000 to 0x0200 0FFF	0x0200 1000 to 0x0200 1FFF	0x0200 2000 to 0x0200 2FFF
size	4 kB	4 kB	4 kB
control	cannot be disabled	disable/enable	disable/enable
default	enabled	enabled	enabled

8.6 On-chip ROM

The on-chip ROM contains the boot loader and the following Application Programming Interfaces (APIs):

- In-System Programming (ISP) and In-Application Programming (IAP) support for flash including IAP erase page command.
- IAP support for EEPROM.
- Flash updates via USB and C_CAN supported.
- USB API (HID, CDC, and MSC drivers).
- DMA, I2C, USART, SPI, and C_CAN drivers.
- Power profiles for configuring power consumption and PLL settings.

- Power mode configuration for configuring deep-sleep, power-down, and deep power-down modes.
- ADC drivers for analog-to-digital conversion and ADC calibration.

8.7 AHB multilayer matrix

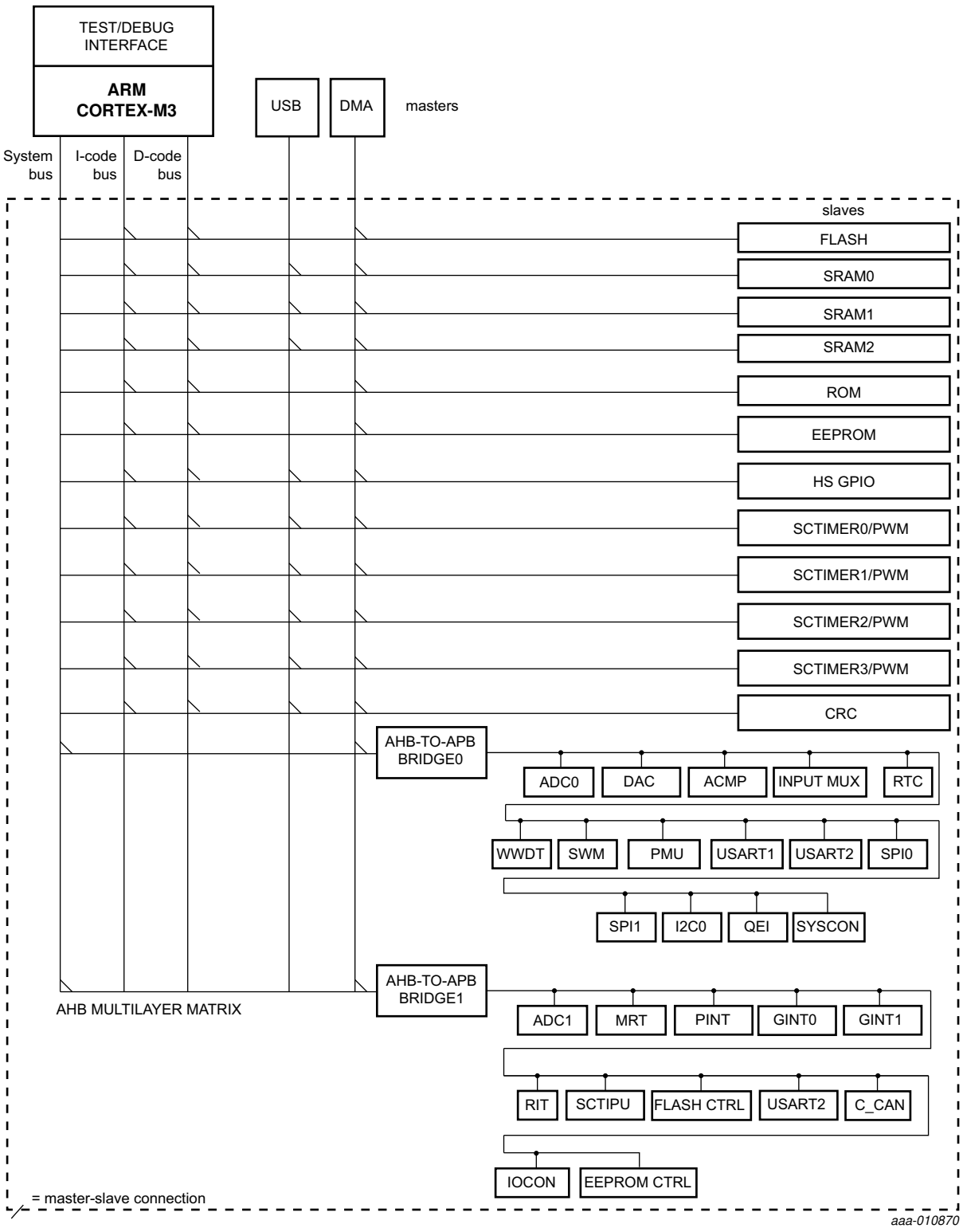


Fig 9. AHB multilayer matrix