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Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

LPC185x/3x/2x/1x

32-bit ARM Cortex-M3 MCU; up to 1 MB flash and 136 kB SRAM; Ethernet, two High-speed USB, LCD, EMC

Rev. 5.2 — 8 March 2016 Product data sheet

1. General description

The LPC185x/3x/2x/1x are ARM Cortex-M3 based microcontrollers for embedded applications. The ARM Cortex-M3 is a next generation core that offers system enhancements such as low power consumption, enhanced debug features, and a high level of support block integration.

The LPC185x/3x/2x/1x operate at CPU frequencies of up to 180 MHz. The ARM Cortex-M3 CPU incorporates a 3-stage pipeline and uses a Harvard architecture with separate local instruction and data buses as well as a third bus for peripherals. The ARM Cortex-M3 CPU also includes an internal prefetch unit that supports speculative branching.

The LPC185x/3x/2x/1x include up to 1 MB of flash and 136 kB of on-chip SRAM, 16 kB of EEPROM memory, a quad SPI Flash Interface (SPIFI), a State-configurable Timer/PWM (SCTimer/PWM) subsystem, two High-speed USB controllers, Ethernet, LCD, an external memory controller, and multiple digital and analog peripherals.

For additional documentation related to the LPC18xx parts, see Section 17 “References”.

2. Features and benefits

- Processor core
  - ARM Cortex-M3 processor (version r2p1), running at CPU frequencies of up to 180 MHz.
  - ARM Cortex-M3 built-in Memory Protection Unit (MPU) supporting eight regions.
  - ARM Cortex-M3 built-in Nested Vectored Interrupt Controller (NVIC).
  - Non-maskable Interrupt (NMI) input.
  - JTAG and Serial Wire Debug, serial trace, eight breakpoints, and four watch points.
  - Enhanced Trace Module (ETM) and Enhanced Trace Buffer (ETB) support.
  - System tick timer.
- On-chip memory
  - Up to 1 MB on-chip dual bank flash memory with flash accelerator.
  - 16 kB on-chip EEPROM data memory.
  - 136 kB SRAM for code and data use.
  - Multiple SRAM blocks with separate bus access.
  - 64 kB ROM containing boot code and on-chip software drivers.
  - 64 bit+ 256 bit of One-Time Programmable (OTP) memory for general-purpose use.
- Clock generation unit

- Crystal oscillator with an operating range of 1 MHz to 25 MHz.
- 12 MHz internal RC oscillator trimmed to 3 % accuracy over temperature and voltage (1.5 % accuracy for T_{amb} = 0 °C to 85 °C).
- Ultra-low power RTC crystal oscillator.
- Three PLLs allow CPU operation up to the maximum CPU rate without the need for a high-frequency crystal. The second PLL can be used with the High-speed USB, the third PLL can be used as audio PLL.
- Clock output.

- Configurable digital peripherals:
  - State Configurable Timer/PWM (SCTimer/PWM) subsystem on AHB.
  - Global Input Multiplexer Array (GIMA) allows to cross-connect multiple inputs and outputs to event driven peripherals like timers, SCTimer/PWM, and ADC0/1.
- Serial interfaces:
  - Quad SPI Flash Interface (SPIFI) with 1-, 2-, or 4-bit data at rates of up to 52 MB per second.
  - 10/100T Ethernet MAC with RMII and MII interfaces and DMA support for high throughput at low CPU load. Support for IEEE 1588 time stamping/advanced time stamping (IEEE 1588-2008 v2).
  - One High-speed USB 2.0 Host/Device/OTG interface with DMA support and on-chip high-speed PHY (USB0).
  - One High-speed USB 2.0 Host/Device interface with DMA support, on-chip full-speed PHY and ULPI interface to an external high-speed PHY (USB1).
  - USB interface electrical test software included in ROM USB stack.
  - Four 550 UARTs with DMA support: one UART with full modem interface; one UART with IrDA interface; three USARTs support UART synchronous mode and a smart card interface conforming to ISO7816 specification.
  - Up to two C_CAN 2.0B controllers with one channel each.
  - Two SSP controllers with FIFO and multi-protocol support. Both SSPs with DMA support.
  - One Fast-mode Plus I^2C-bus interface with monitor mode and with open-drain I/O pins conforming to the full I^2C-bus specification. Supports data rates of up to 1 Mbit/s.
  - One standard I^2C-bus interface with monitor mode and standard I/O pins.
  - Two I^2S interfaces with DMA support, each with one input and one output.
- Digital peripherals:
  - External Memory Controller (EMC) supporting external SRAM, ROM, NOR flash, and SDRAM devices.
  - LCD controller with DMA support and a programmable display resolution of up to 1024H × 768V. Supports monochrome and color STN panels and TFT color panels; supports 1/2/4/8 bpp Color Look-Up Table (CLUT) and 16/24-bit direct pixel mapping.
  - SD/MMC card interface.
  - Eight-channel General-Purpose DMA controller can access all memories on the AHB and all DMA-capable AHB slaves.
  - Up to 164 General-Purpose Input/Output (GPIO) pins with configurable pull-up/pull-down resistors.

- GPIO registers are located on the AHB for fast access. GPIO ports have DMA support.
- Up to eight GPIO pins can be selected from all GPIO pins as edge and level sensitive interrupt sources.
- Two GPIO group interrupt modules enable an interrupt based on a programmable pattern of input states of a group of GPIO pins.
- Four general-purpose timer/counters with capture and match capabilities.
- One motor control PWM for three-phase motor control.
- One Quadrature Encoder Interface (QEI).
- Repetitive Interrupt timer (RI timer).
- Windowed watchdog timer.
- Ultra-low power Real-Time Clock (RTC) on separate power domain with 256 bytes of battery powered backup registers.
- Event recorder with three inputs to record event identification and event time; can be battery powered.
- Alarm timer; can be battery powered.

- Analog peripherals:
  - One 10-bit DAC with DMA support and a data conversion rate of 400 kSamples/s.
  - Two 10-bit ADCs with DMA support and a data conversion rate of 400 kSamples/s. Up to eight analog channels total. Each analog input is connected to both ADCs.
- Unique ID for each device.
- Power:
  - Single 3.3 V (2.4 V to 3.6 V) power supply with on-chip internal voltage regulator for the core supply and the RTC power domain.
  - RTC power domain can be powered separately by a 3 V battery supply.
  - Four reduced power modes: Sleep, Deep-sleep, Power-down, and Deep power-down.
  - Processor wake-up from Sleep mode via wake-up interrupts from various peripherals.
  - Wake-up from Deep-sleep, Power-down, and Deep power-down modes via external interrupts and interrupts generated by battery powered blocks in the RTC power domain.
  - Brownout detect with four separate thresholds for interrupt and forced reset.
  - Power-On Reset (POR).
- Available in LQFP208, LBGA256, LQFP144, and TFBGA100 packages.

3. Applications

- Industrial
- Consumer
- White goods
- RFID readers
- e-Metering

4. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
LPC1857FET256	LBGA256	Plastic low profile ball grid array package; 256 balls; body 17 × 17 × 1 mm	SOT740-2
LPC1857JET256	LBGA256	Plastic low profile ball grid array package; 256 balls; body 17 × 17 × 1 mm	SOT740-2
LPC1857JBD208	LQFP208	Plastic low profile quad flat package; 208 leads; body 28 × 28 × 1.4 mm	SOT459-1
LPC1853FET256	LBGA256	Plastic low profile ball grid array package; 256 balls; body 17 × 17 × 1 mm	SOT740-2
LPC1853JET256	LBGA256	Plastic low profile ball grid array package; 256 balls; body 17 × 17 × 1 mm	SOT740-2
LPC1853JBD208	LQFP208	Plastic low profile quad flat package; 208 leads; body 28 × 28 × 1.4 mm	SOT459-1
LPC1837FET256	LBGA256	Plastic low profile ball grid array package; 256 balls; body 17 × 17 × 1 mm	SOT740-2
LPC1837JET256	LBGA256	Plastic low profile ball grid array package; 256 balls; body 17 × 17 × 1 mm	SOT740-2
LPC1837JBD144	LQFP144	Plastic low profile quad flat package; 144 leads; body 20 × 20 × 1.4 mm	SOT486-1
LPC1837JET100	TFBGA100	Plastic thin fine-pitch ball grid array package; 100 balls; body 9 × 9 × 0.7 mm	SOT926-1
LPC1833FET256	LBGA256	Plastic low profile ball grid array package; 256 balls; body 17 × 17 × 1 mm	SOT740-2
LPC1833JET256	LBGA256	Plastic low profile ball grid array package; 256 balls; body 17 × 17 × 1 mm	SOT740-2
LPC1833JBD144	LQFP144	Plastic low profile quad flat package; 144 leads; body 20 × 20 × 1.4 mm	SOT486-1
LPC1833JET100	TFBGA100	Plastic thin fine-pitch ball grid array package; 100 balls; body 9 × 9 × 0.7 mm	SOT926-1
LPC1827JBD144	LQFP144	Plastic low profile quad flat package; 144 leads; body 20 × 20 × 1.4 mm	SOT486-1
LPC1827JET100	TFBGA100	Plastic thin fine-pitch ball grid array package; 100 balls; body 9 × 9 × 0.7 mm	SOT926-1
LPC1825JBD144	LQFP144	Plastic low profile quad flat package; 144 leads; body 20 × 20 × 1.4 mm	SOT486-1
LPC1825JET100	TFBGA100	Plastic thin fine-pitch ball grid array package; 100 balls; body 9 × 9 × 0.7 mm	SOT926-1
LPC1823JBD144	LQFP144	Plastic low profile quad flat package; 144 leads; body 20 × 20 × 1.4 mm	SOT486-1
LPC1823JET100	TFBGA100	Plastic thin fine-pitch ball grid array package; 100 balls; body 9 × 9 × 0.7 mm	SOT926-1
LPC1822JBD144	LQFP144	Plastic low profile quad flat package; 144 leads; body 20 × 20 × 1.4 mm	SOT486-1
LPC1822JET100	TFBGA100	Plastic thin fine-pitch ball grid array package; 100 balls; body 9 × 9 × 0.7 mm	SOT926-1
LPC1817JBD144	LQFP144	Plastic low profile quad flat package; 144 leads; body 20 × 20 × 1.4 mm	SOT486-1
LPC1817JET100	TFBGA100	Plastic thin fine-pitch ball grid array package; 100 balls; body 9 × 9 × 0.7 mm	SOT926-1
LPC1815JBD144	LQFP144	Plastic low profile quad flat package; 144 leads; body 20 × 20 × 1.4 mm	SOT486-1
LPC1815JET100	TFBGA100	Plastic thin fine-pitch ball grid array package; 100 balls; body 9 × 9 × 0.7 mm	SOT926-1
LPC1813JBD144	LQFP144	Plastic low profile quad flat package; 144 leads; body 20 × 20 × 1.4 mm	SOT486-1
LPC1813JET100	TFBGA100	Plastic thin fine-pitch ball grid array package; 100 balls; body 9 × 9 × 0.7 mm	SOT926-1
LPC1812JBD144	LQFP144	Plastic low profile quad flat package; 144 leads; body 20 × 20 × 1.4 mm	SOT486-1
LPC1812JET100	TFBGA100	Plastic thin fine-pitch ball grid array package; 100 balls; body 9 × 9 × 0.7 mm	SOT926-1

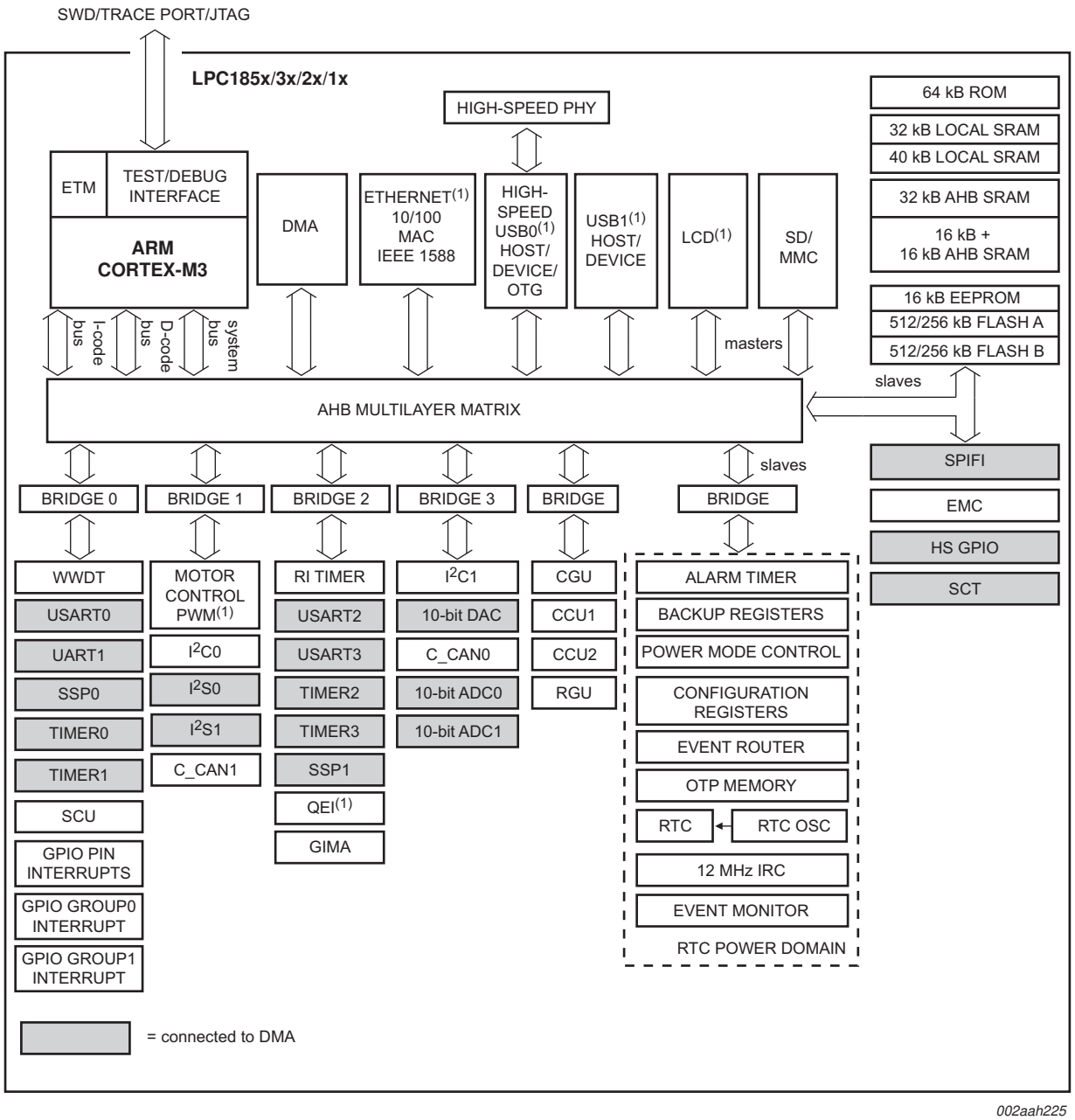
4.1 Ordering options

Table 2. Ordering options

Type number	Flash total	Flash bank A	Flash bank B	Total SRAM	LCD	Ethernet	USB0 (Host, Device, OTG)	USB1 (Host, Device)/ ULPI interface	Motor control PWM	QEI	ADC channels	Temperature range[1]	GPIO
LPC1857FET256	1 MB	512 kB	512 kB	136 kB	yes	yes	yes	yes/yes	yes	yes	8	F	164
LPC1857JET256	1 MB	512 kB	512 kB	136 kB	yes	yes	yes	yes/yes	yes	yes	8	J	164
LPC1857JBD208	1 MB	512 kB	512 kB	136 kB	yes	yes	yes	yes/yes	yes	yes	8	J	142
LPC1853FET256	512 kB	256 kB	256 kB	136 kB	yes	yes	yes	yes/yes	yes	yes	8	F	164
LPC1853JET256	512 kB	256 kB	256 kB	136 kB	yes	yes	yes	yes/yes	yes	yes	8	J	164
LPC1853JBD208	512 kB	256 kB	256 kB	136 kB	yes	yes	yes	yes/yes	yes	yes	8	J	142
LPC1837FET256	1 MB	512 kB	512 kB	136 kB	no	yes	yes	yes/yes	yes	yes	8	F	164
LPC1837JET256	1 MB	512 kB	512 kB	136 kB	no	yes	yes	yes/yes	yes	yes	8	J	164
LPC1837JBD144	1 MB	512 kB	512 kB	136 kB	no	yes	yes	yes/yes	yes	no	8	J	83
LPC1837JET100	1 MB	512 kB	512 kB	136 kB	no	yes	yes	yes/no	no	no	4	J	49
LPC1833FET256	512 kB	256 kB	256 kB	136 kB	no	yes	yes	yes/yes	yes	yes	8	F	164
LPC1833JET256	512 kB	256 kB	256 kB	136 kB	no	yes	yes	yes/yes	yes	yes	8	J	164
LPC1833JBD144	512 kB	256 kB	256 kB	136 kB	no	yes	yes	yes/yes	yes	no	8	J	83
LPC1833JET100	512 kB	256 kB	256 kB	136 kB	no	yes	yes	yes/no	no	no	4	J	49
LPC1827JBD144	1 MB	512 kB	512 kB	136 kB	no	no	yes	no/no	yes	no	8	J	83
LPC1827JET100	1 MB	512 kB	512 kB	136 kB	no	no	yes	no/no	no	no	4	J	49
LPC1825JBD144	768 kB	384 kB	384 kB	136 kB	no	no	yes	no/no	yes	no	8	J	83
LPC1825JET100	768 kB	384 kB	384 kB	136 kB	no	no	yes	no/no	no	no	4	J	49
LPC1823JBD144	512 kB	256 kB	256 kB	104 kB	no	no	yes	no/no	yes	no	8	J	83
LPC1823JET100	512 kB	256 kB	256 kB	104 kB	no	no	yes	no/no	no	no	4	J	49
LPC1822JBD144	512 kB	512 kB	0 kB	104 kB	no	no	yes	no/no	yes	no	8	J	83
LPC1822JET100	512 kB	512 kB	0 kB	104 kB	no	no	yes	no/no	no	no	4	J	49
LPC1817JBD144	1 MB	512 kB	512 kB	136 kB	no	no	no	no/no	yes	no	8	J	83
LPC1817JET100	1 MB	512 kB	512 kB	136 kB	no	no	no	no/no	no	no	4	J	49
LPC1815JBD144	768 kB	384 kB	384 kB	136 kB	no	no	no	no/no	yes	no	8	J	83
LPC1815JET100	768 kB	384 kB	384 kB	136 kB	no	no	no	no/no	no	no	4	J	49
LPC1813JBD144	512 kB	256 kB	256 kB	104 kB	no	no	no	no/no	yes	no	8	J	83
LPC1813JET100	512 kB	256 kB	256 kB	104 kB	no	no	no	no/no	no	no	4	J	49
LPC1812JBD144	512 kB	512 kB	0 kB	104 kB	no	no	no	no/no	yes	no	8	J	83
LPC1812JET100	512 kB	512 kB	0 kB	104 kB	no	no	no	no/no	no	no	4	J	49

[1] J = -40 °C to +105 °C; F = -40 °C to +85 °C.

5. Block diagram



(1) Not available on all parts. See Table 2.

Fig 1. LPC185x/3x/2x/1x block diagram

6. Pinning information

6.1 Pinning

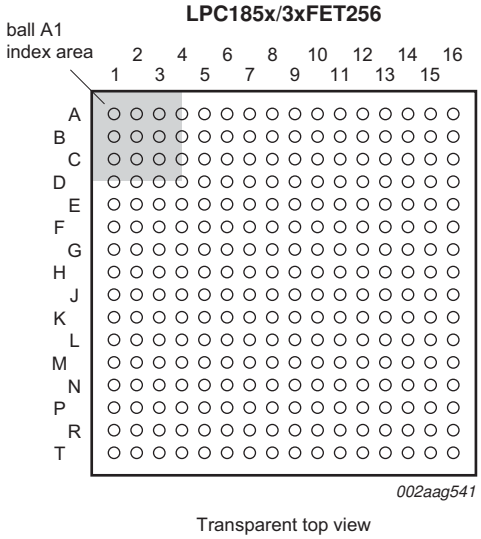


Fig 2. Pin configuration LBGA256 package

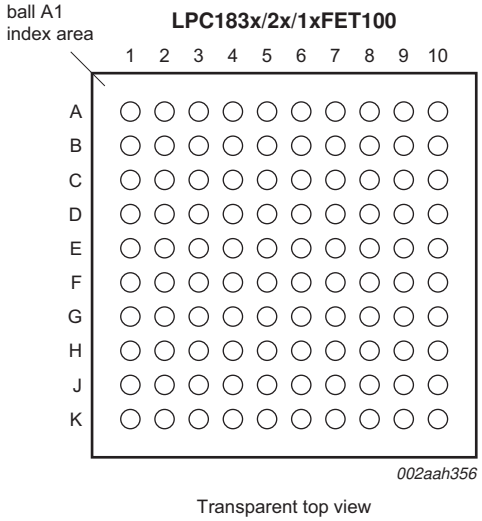


Fig 3. Pin configuration TFBGA100 package

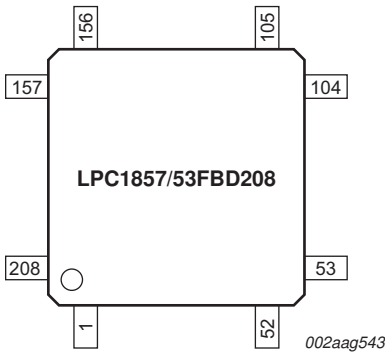


Fig 4. Pin configuration LQFP208 package

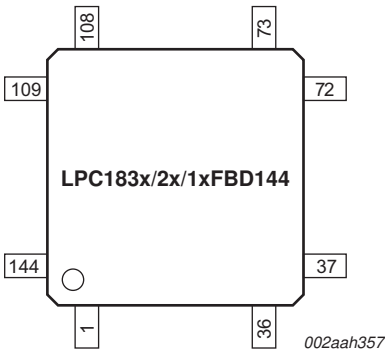


Fig 5. Pin configuration LQFP144 package

6.2 Pin description

On the LPC185x/3x/2x/1x, digital pins are grouped into 16 ports, named P0 to P9 and PA to PF, with up to 20 pins used per port. Each digital pin can support up to eight different digital functions, including General-Purpose I/O (GPIO), selectable through the SCU registers.

The pin name is not indicative of the GPIO port assigned to it.

The parts contain two 10-bit ADCs (ADC0 and ADC1). The input channels of ADC0 and ADC1 on dedicated pins and multiplexed pins are combined in such a way that all channel 0 inputs (named ADC0_0 and ADC1_0) are tied together and connected to both, channel

0 on ADC0 and channel 0 on ADC1, channel 1 inputs (named ADC0_1 and ADC1_1) are tied together and connected to channel 1 on ADC0 and ADC1, and so forth. There are eight ADC channels total for the two ADCs.

Table 3. Pin description

Pin name	LBGA256	TFBGA100	LQFP144	LQFP208		Reset state [1]	Type	Description
Multiplexed digital pins								
P0_0	L3	G2	32	47	[2]	N; PU	I/O	**GPIO0[0] —** General purpose digital input/output pin.
							I/O	**SSP1_MISO —** Master In Slave Out for SSP1.
							I	**ENET_RXD1 —** Ethernet receive data 1 (RMII/MII interface).
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							I/O	**I2S0_TX_WS —** Transmit Word Select. It is driven by the master and received by the slave. Corresponds to the signal WS in the *I²S-bus specification*.
							I/O	**I2S1_TX_WS —** Transmit Word Select. It is driven by the master and received by the slave. Corresponds to the signal WS in the *I²S-bus specification*.
P0_1	M2	G1	34	50	[2]	N; PU	I/O	**GPIO0[1] —** General purpose digital input/output pin.
							I/O	**SSP1_MOSI —** Master Out Slave in for SSP1.
							I	**ENET_COL —** Ethernet Collision detect (MII interface).
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
								ENET_TX_EN — Ethernet transmit enable (RMII/MII interface).
							I/O	**I2S1_TX_SDA —** I²S1 transmit data. It is driven by the transmitter and read by the receiver. Corresponds to the signal SD in the *I²S-bus specification*.
P1_0	P2	H1	38	54	[2]	N; PU	I/O	**GPIO0[4] —** General purpose digital input/output pin.
							I	**CTIN_3 —** SCTimer/PWM input 3. Capture input 1 of timer 1.
							I/O	**EMC_A5 —** External memory address line 5.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							I/O	**SSP0_SSEL —** Slave Select for SSP0.
							-	**R —** Function reserved.
							I/O	**EMC_D12 —** External memory data line 12.

Table 3. Pin description *...continued*

Pin name	LBGA256	TFBGA100	LQFP144	LQFP208		Reset state [1]	Type	Description
P1_1	R2	K2	42	58	[2]	N; PU	I/O	**GPIO0[8] —** General purpose digital input/output pin. External boot pin (see Table 5).
							O	**CTOUT_7 —** SCTimer/PWM output 7. Match output 3 of timer 1.
							I/O	**EMC_A6 —** External memory address line 6.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							I/O	**SSP0_MISO —** Master In Slave Out for SSP0.
							-	**R —** Function reserved.
							I/O	**EMC_D13 —** External memory data line 13.
P1_2	R3	K1	43	60	[2]	N; PU	I/O	**GPIO0[9] —** General purpose digital input/output pin. External boot pin (see Table 5).
							O	**CTOUT_6 —** SCTimer/PWM output 6. Match output 2 of timer 1.
							I/O	**EMC_A7 —** External memory address line 7.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							I/O	**SSP0_MOSI —** Master Out Slave in for SSP0.
							-	**R —** Function reserved.
							I/O	**EMC_D14 —** External memory data line 14.
P1_3	P5	J1	44	61	[2]	N; PU	I/O	**GPIO0[10] —** General purpose digital input/output pin.
							O	**CTOUT_8 —** SCTimer/PWM output 8. Match output 0 of timer 2.
							-	**R —** Function reserved.
							O	**$\overline{\text{EMC\_OE}}$ —** LOW active Output Enable signal.
							O	**USB0_IND1 —** USB0 port indicator LED control output 1.
							I/O	**SSP1_MISO —** Master In Slave Out for SSP1.
							-	**R —** Function reserved.
							O	**SD_RST —** SD/MMC reset signal for MMC4.4 card.
P1_4	T3	J2	47	64	[2]	N; PU	I/O	**GPIO0[11] —** General purpose digital input/output pin.
							O	**CTOUT_9 —** SCTimer/PWM output 9. Match output 3 of timer 3.
							-	**R —** Function reserved.
							O	**$\overline{\text{EMC\_BLS0}}$ —** LOW active Byte Lane select signal 0.
							O	**USB0_IND0 —** USB0 port indicator LED control output 0.
							I/O	**SSP1_MOSI —** Master Out Slave in for SSP1.
							I/O	**EMC_D15 —** External memory data line 15.
							O	**SD_VOLT1 —** SD/MMC bus voltage select output 1.

Table 3. Pin description *...continued*

Pin name	LBGA256	TFBGA100	LQFP144	LQFP208		Reset state [1]	Type	Description
P1_5	R5	J4	48	65	[2]	N; PU	I/O	**GPIO1[8] —** General purpose digital input/output pin.
							O	**CTOUT_10 —** SCTimer/PWM output 10. Match output 3 of timer 3.
							-	**R —** Function reserved.
							O	**EMC_CS0 —** LOW active Chip Select 0 signal.
							I	**USB0_PWR_FAULT —** Port power fault signal indicating overcurrent condition; this signal monitors over-current on the USB bus (external circuitry required to detect over-current condition).
							I/O	**SSP1_SSEL —** Slave Select for SSP1.
							-	**R —** Function reserved.
							O	**SD_POW —** SD/MMC card power monitor output.
P1_6	T4	K4	49	67	[2]	N; PU	I/O	**GPIO1[9] —** General purpose digital input/output pin.
							I	**CTIN_5 —** SCTimer/PWM input 5. Capture input 2 of timer 2.
							-	**R —** Function reserved.
							O	**EMC_WE —** LOW active Write Enable signal.
							-	**R —** Function reserved.
							O	**EMC_BLS0 —** LOW active Byte Lane select signal 0.
							-	**R —** Function reserved.
							I/O	**SD_CMD —** SD/MMC command signal.
P1_7	T5	G4	50	69	[2]	N; PU	I/O	**GPIO1[0] —** General purpose digital input/output pin.
							I	**U1_DSR —** Data Set Ready input for UART1.
							O	**CTOUT_13 —** SCTimer/PWM output 13. Match output 3 of timer 3.
							I/O	**EMC_D0 —** External memory data line 0.
							O	**USB0_PPWR —** VBUS drive signal (towards external charge pump or power management unit); indicates that VBUS must be driven (active HIGH). Add a pull-down resistor to disable the power switch at reset. This signal has opposite polarity compared to the USB_PPWR used on other NXP LPC parts.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.

Table 3. Pin description *...continued*

Pin name	LBGA256	TFBGA100	LQFP144	LQFP208		Reset state [1]	Type	Description
P1_8	R7	H5	51	71	[2]	N; PU	I/O	**GPIO1[1] —** General purpose digital input/output pin.
							O	**U1_DTR —** Data Terminal Ready output for UART1.
							O	**CTOUT_12 —** SCTimer/PWM output 12. Match output 3 of timer 3.
							I/O	**EMC_D1 —** External memory data line 1.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							O	**SD_VOLT0 —** SD/MMC bus voltage select output 0.
P1_9	T7	J5	52	73	[2]	N; PU	I/O	**GPIO1[2] —** General purpose digital input/output pin.
							O	**U1_RTS —** Request to Send output for UART1.
							O	**CTOUT_11 —** SCTimer/PWM output 11. Match output 3 of timer 2.
							I/O	**EMC_D2 —** External memory data line 2.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							I/O	**SD_DAT0 —** SD/MMC data bus line 0.
P1_10	R8	H6	53	75	[2]	N; PU	I/O	**GPIO1[3] —** General purpose digital input/output pin.
							I	**U1_RI —** Ring Indicator input for UART1.
							O	**CTOUT_14 —** SCTimer/PWM output 14. Match output 2 of timer 3.
							I/O	**EMC_D3 —** External memory data line 3.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							I/O	**SD_DAT1 —** SD/MMC data bus line 1.
P1_11	T9	J7	55	77	[2]	N; PU	I/O	**GPIO1[4] —** General purpose digital input/output pin.
							I	**U1_CTS —** Clear to Send input for UART1.
							O	**CTOUT_15 —** SCTimer/PWM output 15. Match output 3 of timer 3.
							I/O	**EMC_D4 —** External memory data line 4.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							I/O	**SD_DAT2 —** SD/MMC data bus line 2.

Table 3. Pin description *...continued*

Pin name	LBGA256	TFBGA100	LQFP144	LQFP208		Reset state [1]	Type	Description
P1_12	R9	K7	56	78	[2]	N; PU	I/O	**GPIO1[5]** — General purpose digital input/output pin.
							I	**U1_DCD** — Data Carrier Detect input for UART1.
							-	**R** — Function reserved.
							I/O	**EMC_D5** — External memory data line 5.
							I	**T0_CAP1** — Capture input 1 of timer 0.
							-	**R** — Function reserved.
							-	**R** — Function reserved.
							I/O	**SD_DAT3** — SD/MMC data bus line 3.
P1_13	R10	H8	60	83	[2]	N; PU	I/O	**GPIO1[6]** — General purpose digital input/output pin.
							O	**U1_TXD** — Transmitter output for UART1.
							-	**R** — Function reserved.
							I/O	**EMC_D6** — External memory data line 6.
							I	**T0_CAP0** — Capture input 0 of timer 0.
							-	**R** — Function reserved.
							-	**R** — Function reserved.
							I	**SD_CD** — SD/MMC card detect input.
P1_14	R11	J8	61	85	[2]	N; PU	I/O	**GPIO1[7]** — General purpose digital input/output pin.
							I	**U1_RXD** — Receiver input for UART1.
							-	**R** — Function reserved.
							I/O	**EMC_D7** — External memory data line 7.
							O	**T0_MAT2** — Match output 2 of timer 0.
							-	**R** — Function reserved.
							-	**R** — Function reserved.
							-	**R** — Function reserved.
P1_15	T12	K8	62	87	[2]	N; PU	I/O	**GPIO0[2]** — General purpose digital input/output pin.
							O	**U2_TXD** — Transmitter output for USART2.
							-	**R** — Function reserved.
							I	**ENET_RXD0** — Ethernet receive data 0 (RMII/MII interface).
							O	**T0_MAT1** — Match output 1 of timer 0.
							-	**R** — Function reserved.
							I/O	**EMC_D8** — External memory data line 8.
							-	**R** — Function reserved.

Table 3. Pin description *...continued*

Pin name	LBGA256	TFBGA100	LQFP144	LQFP208		Reset state [1]	Type	Description
P1_16	M7	H9	64	90	[2]	N; PU	I/O	**GPIO0[3] —** General purpose digital input/output pin.
							I	**U2_RXD —** Receiver input for USART2.
							-	**R —** Function reserved.
							I	**ENET_CRS —** Ethernet Carrier Sense (MII interface).
							O	**T0_MAT0 —** Match output 0 of timer 0.
							-	**R —** Function reserved.
							I/O	**EMC_D9 —** External memory data line 9.
							I	**ENET_RX_DV —** Ethernet Receive Data Valid (RMII/MII interface).
P1_17	M8	H10	66	93	[3]	N; PU	I/O	**GPIO0[12] —** General purpose digital input/output pin.
							I/O	**U2_UCLK —** Serial clock input/output for USART2 in synchronous mode.
							-	**R —** Function reserved.
							I/O	**ENET_MDIO —** Ethernet MIIM data input and output.
							I	**T0_CAP3 —** Capture input 3 of timer 0.
							O	**CAN1_TD —** CAN1 transmitter output.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
P1_18	N12	J10	67	95	[2]	N; PU	I/O	**GPIO0[13] —** General purpose digital input/output pin.
							I/O	**U2_DIR —** RS-485/EIA-485 output enable/direction control for USART2.
							-	**R —** Function reserved.
							O	**ENET_TXD0 —** Ethernet transmit data 0 (RMII/MII interface).
							O	**T0_MAT3 —** Match output 3 of timer 0.
							I	**CAN1_RD —** CAN1 receiver input.
							-	**R —** Function reserved.
							I/O	**EMC_D10 —** External memory data line 10.
P1_19	M11	K9	68	96	[2]	N; PU	I	**ENET_TX_CLK (ENET_REF_CLK) —** Ethernet Transmit Clock (MII interface) or Ethernet Reference Clock (RMII interface).
							I/O	**SSP1_SCK —** Serial clock for SSP1.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							O	**CLKOUT —** Clock output pin.
							-	**R —** Function reserved.
							O	**I2S0_RX_MCLK —** I^2S receive master clock.
							I/O	**I2S1_TX_SCK —** Transmit Clock. It is driven by the master and received by the slave. Corresponds to the signal SCK in the *I^2S-bus specification*.

Table 3. Pin description *...continued*

Pin name	LBGA256	TFBGA100	LQFP144	LQFP208		Reset state [1]	Type	Description
P1_20	M10	K10	70	100	[2]	N; PU	I/O	**GPIO0[15] —** General purpose digital input/output pin.
							I/O	**SSP1_SSEL —** Slave Select for SSP1.
							-	**R —** Function reserved.
							O	**ENET_TXD1 —** Ethernet transmit data 1 (RMII/MII interface).
							I	**T0_CAP2 —** Capture input 2 of timer 0.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							I/O	**EMC_D11 —** External memory data line 11.
P2_0	T16	G10	75	108	[2]	N; PU	-	**R —** Function reserved.
							O	**U0_TXD —** Transmitter output for USART0. See Table 4 for ISP mode.
							I/O	**EMC_A13 —** External memory address line 13.
							O	**USB0_PPWR —** VBUS drive signal (towards external charge pump or power management unit); indicates that VBUS must be driven (active HIGH). Add a pull-down resistor to disable the power switch at reset. This signal has opposite polarity compared to the $\overline{\text{USB\_PPWR}}$ used on other NXP LPC parts.
							I/O	**GPIO5[0] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							I	**T3_CAP0 —** Capture input 0 of timer 3.
							O	**ENET_MDC —** Ethernet MIIM clock.
P2_1	N15	G7	81	116	[2]	N; PU	-	**R —** Function reserved.
							I	**U0_RXD —** Receiver input for USART0. See Table 4 for ISP mode.
							I/O	**EMC_A12 —** External memory address line 12.
							I	**USB0_PWR_FAULT —** Port power fault signal indicating overcurrent condition; this signal monitors over-current on the USB bus (external circuitry required to detect over-current condition).
							I/O	**GPIO5[1] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							I	**T3_CAP1 —** Capture input 1 of timer 3.
							-	**R —** Function reserved.

Table 3. Pin description *...continued*

Pin name	LBGA256	TFBGA100	LQFP144	LQFP208		Reset state [1]	Type	Description
P2_2	M15	F5	84	121	[2]	N; PU	-	**R —** Function reserved.
							I/O	**U0_UCLK —** Serial clock input/output for USART0 in synchronous mode.
							I/O	**EMC_A11 —** External memory address line 11.
							O	**USB0_IND1 —** USB0 port indicator LED control output 1.
							I/O	**GPIO5[2] —** General purpose digital input/output pin.
							I	**CTIN_6 —** SCTimer/PWM input 6. Capture input 1 of timer 3.
							I	**T3_CAP2 —** Capture input 2 of timer 3.
							O	**$\overline{\text{EMC\_CS1}}$ —** LOW active Chip Select 1 signal.
P2_3	J12	D8	87	127	[3]	N; PU	-	**R —** Function reserved.
							I/O	**I2C1_SDA —** I^2C1 data input/output (this pin does not use a specialized I^2C pad).
							O	**U3_TXD —** Transmitter output for USART3. See Table 4 for ISP mode.
							I	**CTIN_1 —** SCTimer/PWM input 1. Capture input 1 of timer 0. Capture input 1 of timer 2.
							I/O	**GPIO5[3] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							O	**T3_MAT0 —** Match output 0 of timer 3.
							O	**USB0_PPWR —** VBUS drive signal (towards external charge pump or power management unit); indicates that VBUS must be driven (active HIGH). Add a pull-down resistor to disable the power switch at reset. This signal has opposite polarity compared to the $\overline{\text{USB\_PPWR}}$ used on other NXP LPC parts.
P2_4	K11	D9	88	128	[3]	N; PU	-	**R —** Function reserved.
							I/O	**I2C1_SCL —** I^2C1 clock input/output (this pin does not use a specialized I^2C pad).
							I	**U3_RXD —** Receiver input for USART3. See Table 4 for ISP mode.
							I	**CTIN_0 —** SCTimer/PWM input 0. Capture input 0 of timer 0, 1, 2, 3.
							I/O	**GPIO5[4] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							O	**T3_MAT1 —** Match output 1 of timer 3.
							I	**USB0_PWR_FAULT —** Port power fault signal indicating overcurrent condition; this signal monitors over-current on the USB bus (external circuitry required to detect over-current condition).

Table 3. Pin description *...continued*

Pin name	LBGA256	TFBGA100	LQFP144	LQFP208		Reset state [1]	Type	Description
P2_5	K14	D10	91	131	[3]	N; PU	-	**R —** Function reserved.
							I	**CTIN_2 —** SCTimer/PWM input 2. Capture input 2 of timer 0.
							I	**USB1_VBUS —** Monitors the presence of USB1 bus power. **Note:** This signal must be HIGH for USB reset to occur.
							I	**ADCTRIG1 —** ADC trigger input 1.
							I/O	**GPIO5[5] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							O	**T3_MAT2 —** Match output 2 of timer 3.
							O	**USB0_IND0 —** USB0 port indicator LED control output 0.
P2_6	K16	G9	95	137	[2]	N; PU	-	**R —** Function reserved.
							I/O	**U0_DIR —** RS-485/EIA-485 output enable/direction control for USART0.
							I/O	**EMC_A10 —** External memory address line 10.
							O	**USB0_IND0 —** USB0 port indicator LED control output 0.
							I/O	**GPIO5[6] —** General purpose digital input/output pin.
							I	**CTIN_7 —** SCTimer/PWM input 7.
							I	**T3_CAP3 —** Capture input 3 of timer 3.
							O	**$\overline{\text{EMC\_BLS1}}$ —** LOW active Byte Lane select signal 1.
P2_7	H14	C10	96	138	[2]	N; PU	I/O	**GPIO0[7] —** General purpose digital input/output pin. ISP entry pin. If this pin is pulled LOW at reset, the part enters ISP mode or boots from an external source (see Table 4 and Table 5).
							O	**CTOUT_1 —** SCTimer/PWM output 1. Match output 3 of timer 3.
							I/O	**U3_UCLK —** Serial clock input/output for USART3 in synchronous mode.
							I/O	**EMC_A9 —** External memory address line 9.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							O	**T3_MAT3 —** Match output 3 of timer 3.
							-	**R —** Function reserved.

Table 3. Pin description *...continued*

Pin name	LBGA256	TFBGA100	LQFP144	LQFP208		Reset state [1]	Type	Description
P2_8	J16	C6	98	140	[2]	N; PU	-	**R —** Function reserved. External boot pin (see Table 5)
							O	**CTOUT_0 —** SCTimer/PWM output 0. Match output 0 of timer 0.
							I/O	**U3_DIR —** RS-485/EIA-485 output enable/direction control for USART3.
							I/O	**EMC_A8 —** External memory address line 8.
							I/O	**GPIO5[7] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
P2_9	H16	B10	102	144	[2]	N; PU	I/O	**GPIO1[10] —** General purpose digital input/output pin. External boot pin (see Table 5).
							O	**CTOUT_3 —** SCTimer/PWM output 3. Match output 3 of timer 0.
							I/O	**U3_BAUD —** Baud pin for USART3.
							I/O	**EMC_A0 —** External memory address line 0.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
P2_10	G16	E8	104	146	[2]	N; PU	I/O	**GPIO0[14] —** General purpose digital input/output pin.
							O	**CTOUT_2 —** SCTimer/PWM output 2. Match output 2 of timer 0.
							O	**U2_TXD —** Transmitter output for USART2.
							I/O	**EMC_A1 —** External memory address line 1.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
P2_11	F16	A9	105	148	[2]	N; PU	I/O	**GPIO1[11] —** General purpose digital input/output pin.
							O	**CTOUT_5 —** SCTimer/PWM output 5. Match output 3 of timer 3.
							I	**U2_RXD —** Receiver input for USART2.
							I/O	**EMC_A2 —** External memory address line 2.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.

Table 3. Pin description *...continued*

Pin name	LBGA256	TFBGA100	LQFP144	LQFP208		Reset state [1]	Type	Description
P2_12	E15	B9	106	153	[2]	N; PU	I/O	**GPIO1[12] —** General purpose digital input/output pin.
							O	**CTOUT_4 —** SCTimer/PWM output 4. Match output 3 of timer 3.
							-	**R —** Function reserved.
							I/O	**EMC_A3 —** External memory address line 3.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							I/O	**U2_UCLK —** Serial clock input/output for USART2 in synchronous mode.
P2_13	C16	A10	108	156	[2]	N; PU	I/O	**GPIO1[13] —** General purpose digital input/output pin.
							I	**CTIN_4 —** SCTimer/PWM input 4. Capture input 2 of timer 1.
							-	**R —** Function reserved.
							I/O	**EMC_A4 —** External memory address line 4.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							I/O	**U2_DIR —** RS-485/EIA-485 output enable/direction control for USART2.
P3_0	F13	A8	112	161	[2]	N; PU	I/O	**I2S0_RX_SCK —** I^2S receive clock. It is driven by the master and received by the slave. Corresponds to the signal SCK in the *I^2S-bus specification*.
							O	**I2S0_RX_MCLK —** I^2S receive master clock.
							I/O	**I2S0_TX_SCK —** Transmit Clock. It is driven by the master and received by the slave. Corresponds to the signal SCK in the *I^2S-bus specification*.
							O	**I2S0_TX_MCLK —** I^2S transmit master clock.
							I/O	**SSP0_SCK —** Serial clock for SSP0.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.

Table 3. Pin description *...continued*

Pin name	LBGA256	TFBGA100	LQFP144	LQFP208		Reset state [1]	Type	Description
P3_1	G11	F7	114	163	[2]	N; PU	I/O	**I2S0_TX_WS —** Transmit Word Select. It is driven by the master and received by the slave. Corresponds to the signal WS in the *I²S-bus specification*.
							I/O	**I2S0_RX_WS —** Receive Word Select. It is driven by the master and received by the slave. Corresponds to the signal WS in the *I²S-bus specification*.
							I	**CAN0_RD —** CAN receiver input.
							O	**USB1_IND1 —** USB1 Port indicator LED control output 1.
							I/O	**GPIO5[8] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							O	**LCD_VD15 —** LCD data.
							-	**R —** Function reserved.
P3_2	F11	G6	116	166	[2]	OL; PU	I/O	**I2S0_TX_SDA —** I²S transmit data. It is driven by the transmitter and read by the receiver. Corresponds to the signal SD in the *I²S-bus specification*.
							I/O	**I2S0_RX_SDA —** I²S Receive data. It is driven by the transmitter and read by the receiver. Corresponds to the signal SD in the *I²S-bus specification*.
							O	**CAN0_TD —** CAN transmitter output.
							O	**USB1_IND0 —** USB1 Port indicator LED control output 0.
							I/O	**GPIO5[9] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							O	**LCD_VD14 —** LCD data.
							-	**R —** Function reserved.
P3_3	B14	A7	118	169	[4]	N; PU	-	**R —** Function reserved.
							-	**R —** Function reserved.
							I/O	**SSP0_SCK —** Serial clock for SSP0.
							O	**SPIFI_SCK —** Serial clock for SPIFI.
							O	**CGU_OUT1 —** CGU spare clock output 1.
							-	**R —** Function reserved.
							O	**I2S0_TX_MCLK —** I²S transmit master clock.
							I/O	**I2S1_TX_SCK —** Transmit Clock. It is driven by the master and received by the slave. Corresponds to the signal SCK in the *I²S-bus specification*.

Table 3. Pin description *...continued*

Pin name	LBGA256	TFBGA100	LQFP144	LQFP208		Reset state [1]	Type	Description
P3_4	A15	B8	119	171	[2]	N; PU	I/O	**GPIO1[14] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							I/O	**SPIFI_SIO3 —** I/O lane 3 for SPIFI.
							O	**U1_TXD —** Transmitter output for UART1.
							I/O	**I2S0_TX_WS —** Transmit Word Select. It is driven by the master and received by the slave. Corresponds to the signal WS in the *I²S-bus specification*.
							I/O	**I2S1_RX_SDA —** I²S1 Receive data. It is driven by the transmitter and read by the receiver. Corresponds to the signal SD in the *I²S-bus specification*.
							O	**LCD_VD13 —** LCD data.
P3_5	C12	B7	121	173	[2]	N; PU	I/O	**GPIO1[15] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							I/O	**SPIFI_SIO2 —** I/O lane 2 for SPIFI.
							I	**U1_RXD —** Receiver input for UART1.
							I/O	**I2S0_TX_SDA —** I²S transmit data. It is driven by the transmitter and read by the receiver. Corresponds to the signal SD in the *I²S-bus specification*.
							I/O	**I2S1_RX_WS —** Receive Word Select. It is driven by the master and received by the slave. Corresponds to the signal WS in the *I²S-bus specification*.
							O	**LCD_VD12 —** LCD data.
P3_6	B13	C7	122	174	[2]	N; PU	I/O	**GPIO0[6] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							I/O	**SSP0_SSEL —** Slave Select for SSP0.
							I/O	**SPIFI_MISO —** Input 1 in SPIFI quad mode; SPIFI output IO1.
							-	**R —** Function reserved.
							I/O	**SSP0_MISO —** Master In Slave Out for SSP0.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
P3_7	C11	D7	123	176	[2]	N; PU	-	**R —** Function reserved.
							-	**R —** Function reserved.
							I/O	**SSP0_MISO —** Master In Slave Out for SSP0.
							I/O	**SPIFI_MOSI —** Input 0 in SPIFI quad mode; SPIFI output IO0.
							I/O	**GPIO5[10] —** General purpose digital input/output pin.
							I/O	**SSP0_MOSI —** Master Out Slave in for SSP0.
							-	**R —** Function reserved.
							-	**R —** Function reserved.

Table 3. Pin description *...continued*

Pin name	LBGA256	TFBGA100	LQFP144	LQFP208		Reset state [1]	Type	Description
P3_8	C10	E7	124	179	[2]	N; PU	-	**R —** Function reserved.
							-	**R —** Function reserved.
							I/O	**SSP0_MOSI —** Master Out Slave in for SSP0.
							I/O	**SPIFI_CS —** SPIFI serial flash chip select.
							I/O	**GPIO5[11] —** General purpose digital input/output pin.
							I/O	**SSP0_SSEL —** Slave Select for SSP0.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
P4_0	D5	-	1	1	[2]	N; PU	I/O	**GPIO2[0] —** General purpose digital input/output pin.
							O	**MCOA0 —** Motor control PWM channel 0, output A.
							I	**NMI —** External interrupt input to NMI.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							O	**LCD_VD13 —** LCD data.
							I/O	**U3_UCLK —** Serial clock input/output for USART3 in synchronous mode.
							-	**R —** Function reserved.
P4_1	A1	-	3	3	[5]	N; PU	I/O	**GPIO2[1] —** General purpose digital input/output pin.
							O	**CTOUT_1 —** SCTimer/PWM output 1. Match output 3 of timer 3.
							O	**LCD_VD0 —** LCD data.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							O	**LCD_VD19 —** LCD data.
							O	**U3_TXD —** Transmitter output for USART3.
							I	**ENET_COL —** Ethernet Collision detect (MII interface).
							AI	**ADC0_1 —** ADC0 and ADC1, input channel 1. Configure the pin as GPIO input and use the ADC function select register in the SCU to select the ADC.
P4_2	D3	-	8	12	[2]	N; PU	I/O	**GPIO2[2] —** General purpose digital input/output pin.
							O	**CTOUT_0 —** SCTimer/PWM output 0. Match output 0 of timer 0.
							O	**LCD_VD3 —** LCD data.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							O	**LCD_VD12 —** LCD data.
							I	**U3_RXD —** Receiver input for USART3.
							-	**R —** Function reserved.

Table 3. Pin description *...continued*

Pin name	LBGA256	TFBGA100	LQFP144	LQFP208		Reset state [1]	Type	Description
P4_3	C2	-	7	10	[5]	N; PU	I/O	**GPIO2[3] —** General purpose digital input/output pin.
							O	**CTOUT_3 —** SCTimer/PWM output 3. Match output 3 of timer 0.
							O	**LCD_VD2 —** LCD data.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							O	**LCD_VD21 —** LCD data.
							I/O	**U3_BAUD —** Baud pin for USART3.
							-	**R —** Function reserved.
							AI	**ADC0_0 —** ADC0 and ADC1, input channel 0. Configure the pin as GPIO input and use the ADC function select register in the SCU to select the ADC.
P4_4	B1	-	9	14	[5]	N; PU	I/O	**GPIO2[4] —** General purpose digital input/output pin.
							O	**CTOUT_2 —** SCTimer/PWM output 2. Match output 2 of timer 0.
							O	**LCD_VD1 —** LCD data.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							O	**LCD_VD20 —** LCD data.
							I/O	**U3_DIR —** RS-485/EIA-485 output enable/direction control for USART3.
							-	**R —** Function reserved.
							AO	**DAC —** DAC output. Configure the pin as GPIO input and use the analog function select register in the SCU to select the DAC.
P4_5	D2	-	10	15	[2]	N; PU	I/O	**GPIO2[5] —** General purpose digital input/output pin.
							O	**CTOUT_5 —** SCTimer/PWM output 5. Match output 3 of timer 3.
							O	**LCD_FP —** Frame pulse (STN). Vertical synchronization pulse (TFT).
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.

Table 3. Pin description *...continued*

Pin name	LBGA256	TFBGA100	LQFP144	LQFP208		Reset state [1]	Type	Description
P4_6	C1	-	11	17	[2]	N; PU	I/O	**GPIO2[6] —** General purpose digital input/output pin.
							O	**CTOUT_4 —** SCTimer/PWM output 4. Match output 3 of timer 3.
							O	**LCD_ENAB/LCDM —** STN AC bias drive or TFT data enable input.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
P4_7	H4	-	14	21	[2]	O; PU	O	**LCD_DCLK —** LCD panel clock.
							I	**GP_CLKIN —** General-purpose clock input to the CGU.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							I/O	**I2S1_TX_SCK —** Transmit Clock. It is driven by the master and received by the slave. Corresponds to the signal SCK in the *I^2S-bus specification*.
							I/O	**I2S0_TX_SCK —** Transmit Clock. It is driven by the master and received by the slave. Corresponds to the signal SCK in the *I^2S-bus specification*.
P4_8	E2	-	15	23	[2]	N; PU	-	**R —** Function reserved.
							I	**CTIN_5 —** SCTimer/PWM input 5. Capture input 2 of timer 2.
							O	**LCD_VD9 —** LCD data.
							-	**R —** Function reserved.
							I/O	**GPIO5[12] —** General purpose digital input/output pin.
							O	**LCD_VD22 —** LCD data.
							O	**CAN1_TD —** CAN1 transmitter output.
							-	**R —** Function reserved.
P4_9	L2	-	33	48	[2]	N; PU	-	**R —** Function reserved.
							I	**CTIN_6 —** SCTimer/PWM input 6. Capture input 1 of timer 3.
							O	**LCD_VD11 —** LCD data.
							-	**R —** Function reserved.
							I/O	**GPIO5[13] —** General purpose digital input/output pin.
							O	**LCD_VD15 —** LCD data.
							I	**CAN1_RD —** CAN1 receiver input.
							-	**R —** Function reserved.

Table 3. Pin description *...continued*

Pin name	LBGA256	TFBGA100	LQFP144	LQFP208		Reset state [1]	Type	Description
P4_10	M3	-	35	51	[2]	N; PU	-	**R** — Function reserved.
							I	**CTIN_2** — SCTimer/PWM input 2. Capture input 2 of timer 0.
							O	**LCD_VD10** — LCD data.
							-	**R** — Function reserved.
							I/O	**GPIO5[14]** — General purpose digital input/output pin.
							O	**LCD_VD14** — LCD data.
							-	**R** — Function reserved.
							-	**R** — Function reserved.
P5_0	N3	-	37	53	[2]	N; PU	I/O	**GPIO2[9]** — General purpose digital input/output pin.
							O	**MCOB2** — Motor control PWM channel 2, output B.
							I/O	**EMC_D12** — External memory data line 12.
							-	**R** — Function reserved.
							I	**U1_DSR** — Data Set Ready input for UART1.
							I	**T1_CAP0** — Capture input 0 of timer 1.
							-	**R** — Function reserved.
							-	**R** — Function reserved.
P5_1	P3	-	39	55	[2]	N; PU	I/O	**GPIO2[10]** — General purpose digital input/output pin.
							I	**MCI2** — Motor control PWM channel 2, input.
							I/O	**EMC_D13** — External memory data line 13.
							-	**R** — Function reserved.
							O	**U1_DTR** — Data Terminal Ready output for UART1. Can also be configured to be an RS-485/EIA-485 output enable signal for UART1.
							I	**T1_CAP1** — Capture input 1 of timer 1.
							-	**R** — Function reserved.
							-	**R** — Function reserved.
P5_2	R4	-	46	63	[2]	N; PU	I/O	**GPIO2[11]** — General purpose digital input/output pin.
							I	**MCI1** — Motor control PWM channel 1, input.
							I/O	**EMC_D14** — External memory data line 14.
							-	**R** — Function reserved.
							O	**U1_RTS** — Request to Send output for UART1. Can also be configured to be an RS-485/EIA-485 output enable signal for UART1.
							I	**T1_CAP2** — Capture input 2 of timer 1.
							-	**R** — Function reserved.
							-	**R** — Function reserved.

Table 3. Pin description *...continued*

Pin name	LBGA256	TFBGA100	LQFP144	LQFP208		Reset state [1]	Type	Description
P5_3	T8	-	54	76	[2]	N; PU	I/O	**GPIO2[12]** — General purpose digital input/output pin.
							I	**MCI0** — Motor control PWM channel 0, input.
							I/O	**EMC_D15** — External memory data line 15.
							-	**R** — Function reserved.
							I	**U1_RI** — Ring Indicator input for UART1.
							I	**T1_CAP3** — Capture input 3 of timer 1.
							-	**R** — Function reserved.
							-	**R** — Function reserved.
P5_4	P9	-	57	80	[2]	N; PU	I/O	**GPIO2[13]** — General purpose digital input/output pin.
							O	**MCOB0** — Motor control PWM channel 0, output B.
							I/O	**EMC_D8** — External memory data line 8.
							-	**R** — Function reserved.
							I	**U1_CTS** — Clear to Send input for UART1.
							O	**T1_MAT0** — Match output 0 of timer 1.
							-	**R** — Function reserved.
							-	**R** — Function reserved.
P5_5	P10	-	58	81	[2]	N; PU	I/O	**GPIO2[14]** — General purpose digital input/output pin.
							O	**MCOA1** — Motor control PWM channel 1, output A.
							I/O	**EMC_D9** — External memory data line 9.
							-	**R** — Function reserved.
							I	**U1_DCD** — Data Carrier Detect input for UART1.
							O	**T1_MAT1** — Match output 1 of timer 1.
							-	**R** — Function reserved.
							-	**R** — Function reserved.
P5_6	T13	-	63	89	[2]	N; PU	I/O	**GPIO2[15]** — General purpose digital input/output pin.
							O	**MCOB1** — Motor control PWM channel 1, output B.
							I/O	**EMC_D10** — External memory data line 10.
							-	**R** — Function reserved.
							O	**U1_TXD** — Transmitter output for UART1.
							O	**T1_MAT2** — Match output 2 of timer 1.
							-	**R** — Function reserved.
							-	**R** — Function reserved.