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LPC2292/2294

16/32-bit ARM microcontrollers; 256 kB ISP/IAP flash with
CAN, 10-bit ADC and external memory interface

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Product data sheet

1. General description

The LPC2292/2294 microcontrollers are based on a 16/32-bit ARM7TDMI-S CPU with real-time emulation and embedded trace support, together with 256 kB of embedded high-speed flash memory. A 128-bit wide memory interface and a unique accelerator architecture enable 32-bit code execution at the maximum clock rate. For critical code size applications, the alternative 16-bit Thumb mode reduces code by more than 30 % with minimal performance penalty.

With their 144-pin package, low power consumption, various 32-bit timers, 8-channel 10-bit ADC, 2/4 (LPC2294) advanced CAN channels, PWM channels and up to nine external interrupt pins these microcontrollers are particularly suitable for automotive and industrial control applications as well as medical systems and fault-tolerant maintenance buses. The number of available GPIOs ranges from 76 (with external memory) through 112 (single-chip). With a wide range of additional serial communications interfaces, they are also suited for communication gateways and protocol converters as well as many other general-purpose applications.

Remark: Throughout the data sheet, the term LPC2292/2294 will apply to devices with and without the /00 or /01 suffix. The suffixes /00 and /01 will be used to differentiate from other devices only when necessary.

2. Features and benefits

2.1 Key features brought by LPC2292/2294/01 devices

- Fast GPIO ports enable port pin toggling up to 3.5 times faster than the original device. They also allow for a port pin to be read at any time regardless of its function.
- Dedicated result registers for ADC(s) reduce interrupt overhead. The ADC pads are 5 V tolerant when configured for digital I/O function(s).
- UART0/1 include fractional baud rate generator, auto-bauding capabilities and handshake flow-control fully implemented in hardware.
- Buffered SSP serial controller supporting SPI, 4-wire SSI, and Microwire formats.
- SPI programmable data length and master mode enhancement.
- Diversified Code Read Protection (CRP) enables different security levels to be implemented. This feature is available in LPC2292/2294/00 devices as well.
- General purpose timers can operate as external event counters.

2.2 Key features common for all devices

- 16/32-bit ARM7TDMI-S microcontroller in a LQFP144 package.



- 16 kB on-chip static RAM and 256 kB on-chip flash program memory. 128-bit wide interface/accelerator enables high-speed 60 MHz operation.
- In-System Programming/In-Application Programming (ISP/IAP) via on-chip bootloader software. Single flash sector or full chip erase in 400 ms and programming of 256 B in 1 ms.
- EmbeddedICE-RT and Embedded Trace interfaces offer real-time debugging with the on-chip RealMonitor software as well as high-speed real-time tracing of instruction execution.
- Two/four (LPC2292/2294) interconnected CAN interfaces with advanced acceptance filters. Additional serial interfaces include two UARTs (16C550), Fast I²C-bus (400 kbit/s) and two SPIs.
- Eight channel 10-bit ADC with conversion time as low as 2.44 μ s.
- Two 32-bit timers (with four capture and four compare channels), PWM unit (six outputs), Real-Time Clock (RTC), and watchdog.
- Vectored Interrupt Controller (VIC) with configurable priorities and vector addresses.
- Configurable external memory interface with up to four banks, each up to 16 MB and 8/16/32-bit data width.
- Up to 112 general purpose I/O pins (5 V tolerant). Up to nine edge/level sensitive external interrupt pins available.
- 60 MHz maximum CPU clock available from programmable on-chip PLL with settling time of 100 μ s.
- The on-chip crystal oscillator should have an operating range of 1 MHz to 25 MHz.
- Power saving modes include Idle and Power-down.
- Processor wake-up from Power-down mode via external interrupt.
- Individual enable/disable of peripheral functions for power optimization.
- Dual power supply:
 - ◆ CPU operating voltage range of 1.65 V to 1.95 V (1.8 V \pm 0.15 V).
 - ◆ I/O power supply range of 3.0 V to 3.6 V (3.3 V \pm 10 %) with 5 V tolerant I/O pads.

3. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
LPC2292FBD144/01	LQFP144	plastic low profile quad flat package; 144 leads; body 20 \times 20 \times 1.4 mm	SOT486-1
LPC2292FET144/00	TFBGA144	plastic thin fine-pitch ball grid array package; 144 balls; body 12 \times 12 \times 0.8 mm	SOT569-2
LPC2292FET144/01	TFBGA144	plastic thin fine-pitch ball grid array package; 144 balls; body 12 \times 12 \times 0.8 mm	SOT569-2
LPC2292FET144/G	TFBGA144	plastic thin fine-pitch ball grid array package; 144 balls; body 12 \times 12 \times 0.8 mm	SOT569-2

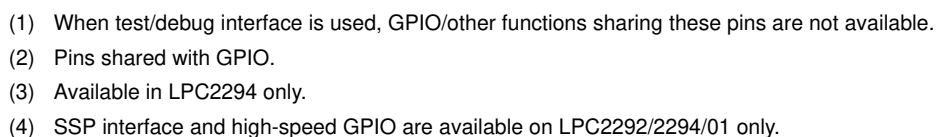
Table 1. Ordering information ...continued

Type number	Package		
	Name	Description	Version
LPC2294HBD144	LQFP144	plastic low profile quad flat package; 144 leads; body 20 × 20 × 1.4 mm	SOT486-1
LPC2294HBD144/00	LQFP144	plastic low profile quad flat package; 144 leads; body 20 × 20 × 1.4 mm	SOT486-1
LPC2294HBD144/01	LQFP144	plastic low profile quad flat package; 144 leads; body 20 × 20 × 1.4 mm	SOT486-1

3.1 Ordering options

Table 2. Ordering options

Type number	Flash memory	RAM	CAN	Fast GPIO/ SSP/ Enhanced UART, ADC, Timer	Temperature range
LPC2292FBD144/01	256 kB	16 kB	2 channels	yes	−40 °C to +85 °C
LPC2292FET144/00	256 kB	16 kB	2 channels	no	−40 °C to +85 °C
LPC2292FET144/01	256 kB	16 kB	2 channels	yes	−40 °C to +85 °C
LPC2292FET144/G	256 kB	16 kB	2 channels	no	−40 °C to +85 °C
LPC2294HBD144	256 kB	16 kB	4 channels	no	−40 °C to +125 °C
LPC2294HBD144/00	256 kB	16 kB	4 channels	no	−40 °C to +125 °C
LPC2294HBD144/01	256 kB	16 kB	4 channels	yes	−40 °C to +125 °C



LPG2292 2294

5. Pinning information

5.1 Pinning

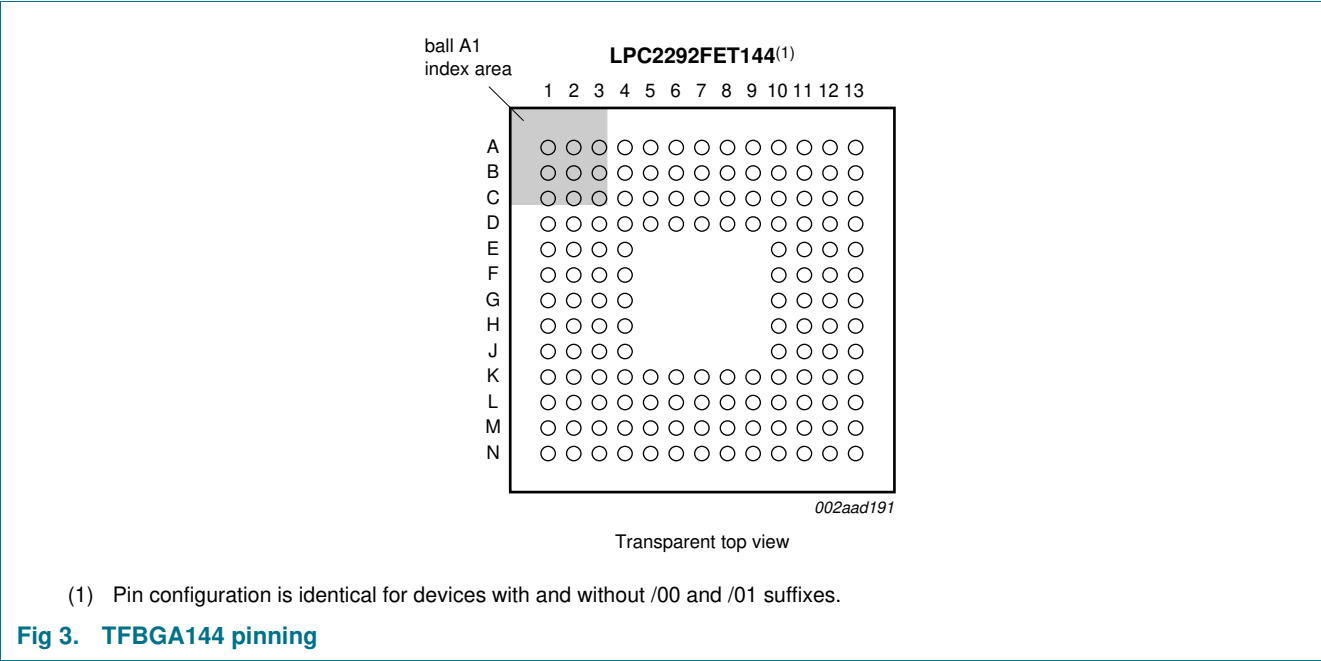
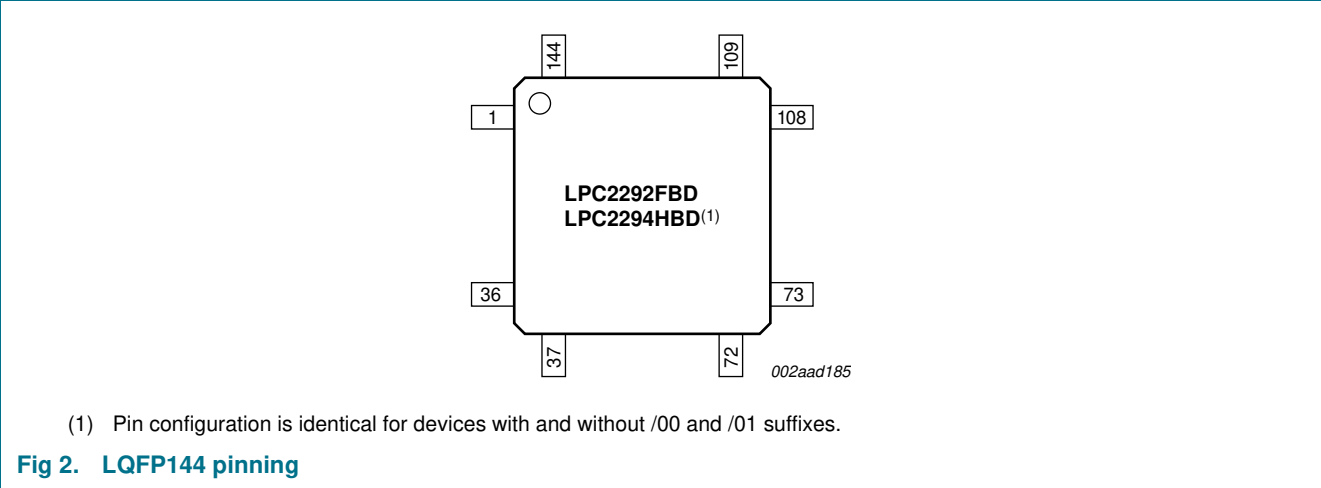


Table 3. Ball allocation

Row	Column	1	2	3	4	5	6	7	8	9	10	11	12	13
A	P2[22]/D22	V _{DDA} (1V8)	P1[28]/TDI	P2[21]/D21	P2[18]/D18	P2[14]/D14	P1[29]/TCK	P2[11]/D11	P2[10]/D10	P2[7]/D7	V _{DD} (3V3)	V _{DD} (1V8)	P2[4]/D4	
B	V _{DD} (3V3)	P1[27]/TDO	XTAL2	V _{SSA} (PLL)	P2[19]/D19	P2[15]/D15	P2[12]/D12	P0[20]/MAT1[3]/SSEL1/EINT3	V _{DD} (3V3)	P2[6]/D6	V _{SS}	P2[3]/D3	V _{SS}	
C	P0[21]/PWM5/CAP1[3]	V _{SS}	XTAL1	V _{SSA}	RESET	P2[16]/D16	P2[13]/D13	P0[19]/MAT1[2]/MOSI1/CAP1[2]	P2[9]/D9	P2[5]/D5	P2[2]/D2	P2[1]/D1	V _{DD} (3V3)	
D	P0[24]/TD2	P1[19]/TRACE PKT3	P0[23]/RD2	P0[22]/CAP0[0]/MAT0[0]	P2[20]/D20	P2[17]/D17	V _{SS}	P0[18]/CAP1[3]/MISO1/MAT1[3]	P2[8]/D8	P1[30]/TMS	V _{SS}	P1[20]/TRACE SYNC	P0[17]/CAP1[2]/SCK1/MAT1[2]	
E	P2[25]/D25	P2[24]/D24	P2[23]	V _{SS}						P0[16]/EINT0/MAT0[2]/CAP0[2]	P0[15]/RI1/EINT2	P2[0]/D0	P3[30]/BLS1	
F	P2[27]/D27/BOOT1	P1[18]/TRACE PKT2	V _{DDA} (3V3)	P2[26]/D26/BOOT0						P3[31]/BLS0	P1[21]/PIPE STAT0	V _{DD} (3V3)	V _{SS}	
G	P2[29]/D29	P2[28]/D28	P2[30]/D30/AIN4	P2[31]/D31/AIN5						P0[14]/DCD1/EINT1	P1[0]/CS0	P3[0]/A0	P1[1]/OE	
H	P0[25]/RD1	TD1	P0[27]/AIN0/CAP0[1]/MAT0[1]	P1[17]/TRACE PKT1						P0[13]/DTR1/MAT1[1]	P1[22]/PIPE STAT1	P3[2]/A2	P3[1]/A1	
J	P0[28]/AIN1/CAP0[2]/MAT0[2]	V _{SS}	P3[29]/BLS2/AIN6	P3[28]/BLS3/AIN7						P3[3]/A3	P1[23]/PIPE STAT2	P0[11]/CTS1/CAP1[1]	P0[12]/DSR1/MAT1[0]	
K	P3[27]/WE	P3[26]/CS1	V _{DD} (3V3)	P3[22]/A22	P3[20]/A20	P0[1]/RXD0/PWM3/EINT0	P3[14]/A14	P1[25]/EXTIN0	P3[11]/A11	V _{DD} (3V3)	P0[10]/RTS1/CAP1[0]	V _{SS}	P3[4]/A4	

Table 3. Ball allocation ...continued

Row	Column	1	2	3	4	5	6	7	8	9	10	11	12	13
L		P0[29]/ AIN2/ CAP0[3]/ MAT0[3]	P0[30]/ AIN3/ EINT3/ CAP0[0]	P1[16]/ TRACE PKT0	P0[0]/ TXD0/ PWM1	P3[19]/ A19	P0[2]/ SCL/ CAP0[0]	P3[15]/ A15	P0[4]/ SCK0/ CAP0[1]	P3[12]/ A12	V _{SS}	P1[24]/ TRACE CLK	P0[8]/ TXD1/ PWM4	P0[9]/ RXD1/ PWM6/ EINT3
M		P3[25]/ CS2	P3[24]/ CS3	V _{DD(3V3)}	P1[31]/ TRST	P3[18]/ A18	V _{DD(3V3)}	P3[16]/ A16	P0[3]/ SDA/ MAT0[0]/ EINT1	P3[13]/ A13	P3[9]/A9	P0[7]/ SSEL0/ PWM2/ EINT2	P3[7]/A7	P3[5]/A5
N		V _{DD(1V8)}	V _{SS}	P3[23]/ A23/ XCLK	P3[21]/ A21	P3[17]/ A17	P1[26]/ RTCK	V _{SS}	V _{DD(3V3)}	P0[5]/ MISO0/ MAT0[1]	P3[10]/ A10	P0[6]/ MOSI0/ CAP0[2]	P3[8]/A8	P3[6]/A6

5.2 Pin description

Table 4. Pin description

Symbol	Pin (LQFP)	Pin (TFBGA) ^[1]	Type	Description
P0[0] to P0[31]			I/O	<p>Port 0: Port 0 is a 32-bit bidirectional I/O port with individual direction controls for each bit. The operation of port 0 pins depends upon the pin function selected via the Pin Connect Block.</p> <p>Pins 26 and 31 of port 0 are not available.</p>
P0[0]/TXD0/ PWM1	42 ^[2]	L4 ^[2]	O	TXD0 — Transmitter output for UART0.
			O	PWM1 — Pulse Width Modulator output 1.
P0[1]/RXD0/ PWM3/EINT0	49 ^[4]	K6 ^[4]	I	RXD0 — Receiver input for UART0.
			O	PWM3 — Pulse Width Modulator output 3.
			I	EINT0 — External interrupt 0 input
P0[2]/SCL/ CAP0[0]	50 ^[5]	L6 ^[5]	I/O	SCL — I ² C-bus clock input/output. Open-drain output (for I ² C-bus compliance).
			I	CAP0[0] — Capture input for Timer 0, channel 0.
P0[3]/SDA/ MAT0[0]/EINT1	58 ^[5]	M8 ^[5]	I/O	SDA — I ² C-bus data input/output. Open-drain output (for I ² C-bus compliance).
			O	MAT0[0] — Match output for Timer 0, channel 0.
			I	EINT1 — External interrupt 1 input.
P0[4]/SCK0/ CAP0[1]	59 ^[2]	L8 ^[2]	I/O	SCK0 — Serial clock for SPI0. SPI clock output from master or input to slave.
			I	CAP0[1] — Capture input for Timer 0, channel 1.
P0[5]/MISO0/ MAT0[1]	61 ^[2]	N9 ^[2]	I/O	MISO0 — Master In Slave OUT for SPI0. Data input to SPI master or data output from SPI slave.
			O	MAT0[1] — Match output for Timer 0, channel 1.
P0[6]/MOSI0/ CAP0[2]	68 ^[2]	N11 ^[2]	I/O	MOSI0 — Master Out Slave In for SPI0. Data output from SPI master or data input to SPI slave.
			I	CAP0[2] — Capture input for Timer 0, channel 2.
P0[7]/SSEL0/ PWM2/EINT2	69 ^[4]	M11 ^[4]	I	SSEL0 — Slave Select for SPI0. Selects the SPI interface as a slave.
			O	PWM2 — Pulse Width Modulator output 2.
			I	EINT2 — External interrupt 2 input.
P0[8]/TXD1/ PWM4	75 ^[2]	L12 ^[2]	O	TXD1 — Transmitter output for UART1.
			O	PWM4 — Pulse Width Modulator output 4.
P0[9]/RXD1/ PWM6/EINT3	76 ^[4]	L13 ^[4]	I	RXD1 — Receiver input for UART1.
			O	PWM6 — Pulse Width Modulator output 6.
			I	EINT3 — External interrupt 3 input.
P0[10]/RTS1/ CAP1[0]	78 ^[2]	K11 ^[2]	O	RTS1 — Request to Send output for UART1.
			I	CAP1[0] — Capture input for Timer 1, channel 0.
P0[11]/CTS1/ CAP1[1]	83 ^[2]	J12 ^[2]	I	CTS1 — Clear to Send input for UART1.
			I	CAP1[1] — Capture input for Timer 1, channel 1.

Table 4. Pin description ...continued

Symbol	Pin (LQFP)	Pin (TFBGA) ^[1]	Type	Description
P0[12]/DSR1/ MAT1[0]/RD4	84 ^[2]	J13 ^[2]	I	DSR1 — Data Set Ready input for UART1.
			O	MAT1[0] — Match output for Timer 1, channel 0.
			I	RD4 — CAN4 receiver input (LPC2294 only).
P0[13]/DTR1/ MAT1[1]/TD4	85 ^[2]	H10 ^[2]	O	DTR1 — Data Terminal Ready output for UART1.
			O	MAT1[1] — Match output for Timer 1, channel 1.
			O	TD4 — CAN4 transmitter output (LPC2294 only).
P0[14]/DCD1/ EINT1	92 ^[4]	G10 ^[4]	I	DCD1 — Data Carrier Detect input for UART1.
			I	EINT1 — External interrupt 1 input. Note: LOW on this pin while RESET is LOW forces on-chip bootloader to take over control of the part after reset.
P0[15]/RI1/ EINT2	99 ^[4]	E11 ^[4]	I	RI1 — Ring Indicator input for UART1.
			I	EINT2 — External interrupt 2 input.
P0[16]/EINT0/ MAT0[2]/ CAP0[2]	100 ^[4]	E10 ^[4]	I	EINT0 — External interrupt 0 input.
			O	MAT0[2] — Match output for Timer 0, channel 2.
			I	CAP0[2] — Capture input for Timer 0, channel 2.
P0[17]/CAP1[2]/ SCK1/MAT1[2]	101 ^[2]	D13 ^[2]	I	CAP1[2] — Capture input for Timer 1, channel 2.
			I/O	SCK1 — Serial Clock for SPI1/SSP ^[3] . SPI clock output from master or input to slave.
			O	MAT1[2] — Match output for Timer 1, channel 2.
P0[18]/CAP1[3]/ MISO1/MAT1[3]	121 ^[2]	D8 ^[2]	I	CAP1[3] — Capture input for Timer 1, channel 3.
			I/O	MISO1 — Master In Slave Out for SPI1/SSP ^[3] . Data input to SPI master or data output from SPI slave.
			O	MAT1[3] — Match output for Timer 1, channel 3.
P0[19]/MAT1[2]/ MOSI1/CAP1[2]	122 ^[2]	C8 ^[2]	O	MAT1[2] — Match output for Timer 1, channel 2.
			I/O	MOSI1 — Master Out Slave In for SPI1/SSP ^[3] . Data output from SPI master or data input to SPI slave.
			I	CAP1[2] — Capture input for Timer 1, channel 2.
P0[20]/MAT1[3]/ SSEL1/EINT3	123 ^[4]	B8 ^[4]	O	MAT1[3] — Match output for Timer 1, channel 3.
			I	SSEL1 — Slave Select for SPI1/SSP ^[3] . Selects the SPI interface as a slave.
			I	EINT3 — External interrupt 3 input.
P0[21]/PWM5/ RD3/CAP1[3]	4 ^[2]	C1 ^[2]	O	PWM5 — Pulse Width Modulator output 5.
			I	RD3 — CAN3 receiver input (LPC2294 only).
			I	CAP1[3] — Capture input for Timer 1, channel 3.
P0[22]/TD3/ CAP0[0]/ MAT0[0]	5 ^[2]	D4 ^[2]	O	TD3 — CAN3 transmitter output (LPC2294 only).
			I	CAP0[0] — Capture input for Timer 0, channel 0.
			O	MAT0[0] — Match output for Timer 0, channel 0.
P0[23]/RD2	6 ^[2]	D3 ^[2]	I	RD2 — CAN2 receiver input.
P0[24]/TD2	8 ^[2]	D1 ^[2]	O	TD2 — CAN2 transmitter output.
P0[25]/RD1	21 ^[2]	H1 ^[2]	I	RD1 — CAN1 receiver input.

Table 4. Pin description ...continued

Symbol	Pin (LQFP)	Pin (TFBGA) ^[1]	Type	Description
P0[27]/AIN0/ CAP0[1]/ MAT0[1]	23 ^[6]	H3 ^[6]	I	AIN0 — ADC, input 0. This analog input is always connected to its pin.
			I	CAP0[1] — Capture input for Timer 0, channel 1.
			O	MAT0[1] — Match output for Timer 0, channel 1.
P0[28]/AIN1/ CAP0[2]/ MAT0[2]	25 ^[6]	J1 ^[6]	I	AIN1 — ADC, input 1. This analog input is always connected to its pin.
			I	CAP0[2] — Capture input for Timer 0, channel 2.
			O	MAT0[2] — Match output for Timer 0, channel 2.
P0[29]/AIN2/ CAP0[3]/ MAT0[3]	32 ^[6]	L1 ^[6]	I	AIN2 — ADC, input 2. This analog input is always connected to its pin.
			I	CAP0[3] — Capture input for Timer 0, Channel 3.
			O	MAT0[3] — Match output for Timer 0, channel 3.
P0[30]/AIN3/ EINT3/CAP0[0]	33 ^[6]	L2 ^[6]	I	AIN3 — ADC, input 3. This analog input is always connected to its pin.
			I	EINT3 — External interrupt 3 input.
			I	CAP0[0] — Capture input for Timer 0, channel 0.
P1[0] to P1[31]			I/O	Port 1: Port 1 is a 32-bit bidirectional I/O port with individual direction controls for each bit. The operation of port 1 pins depends upon the pin function selected via the Pin Connect Block. Pins 2 through 15 of port 1 are not available.
P1[0]/ $\overline{\text{CS0}}$	91 ^[7]	G11 ^[7]	O	CS0 — LOW-active Chip Select 0 signal. (Bank 0 addresses range 0x8000 0000 to 0x80FF FFFF)
P1[1]/ $\overline{\text{OE}}$	90 ^[7]	G13 ^[7]	O	OE — LOW-active Output Enable signal.
P1[16]/ TRACEPKT0	34 ^[7]	L3 ^[7]	O	TRACEPKT0 — Trace Packet, bit 0. Standard I/O port with internal pull-up.
P1[17]/ TRACEPKT1	24 ^[7]	H4 ^[7]	O	TRACEPKT1 — Trace Packet, bit 1. Standard I/O port with internal pull-up.
P1[18]/ TRACEPKT2	15 ^[7]	F2 ^[7]	O	TRACEPKT2 — Trace Packet, bit 2. Standard I/O port with internal pull-up.
P1[19]/ TRACEPKT3	7 ^[7]	D2 ^[7]	O	TRACEPKT3 — Trace Packet, bit 3. Standard I/O port with internal pull-up.
P1[20]/ TRACESYNC	102 ^[7]	D12 ^[7]	O	TRACESYNC — Trace Synchronization. Standard I/O port with internal pull-up. Note: LOW on this pin while $\overline{\text{RESET}}$ is LOW, enables pins P1[25:16] to operate as Trace port after reset.
P1[21]/ PIPESTAT0	95 ^[7]	F11 ^[7]	O	PIPESTAT0 — Pipeline Status, bit 0. Standard I/O port with internal pull-up.
P1[22]/ PIPESTAT1	86 ^[7]	H11 ^[7]	O	PIPESTAT1 — Pipeline Status, bit 1. Standard I/O port with internal pull-up.
P1[23]/ PIPESTAT2	82 ^[7]	J11 ^[7]	O	PIPESTAT2 — Pipeline Status, bit 2. Standard I/O port with internal pull-up.
P1[24]/ TRACECLK	70 ^[7]	L11 ^[7]	O	TRACECLK — Trace Clock. Standard I/O port with internal pull-up.

Table 4. Pin description ...continued

Symbol	Pin (LQFP)	Pin (TFBGA) ¹	Type	Description
P1[25]/EXTIN0	60 ²	K8 ²	I	EXTIN0 — External Trigger Input. Standard I/O with internal pull-up.
P1[26]/RTCK	52 ²	N6 ²	I/O	RTCK — Returned Test Clock output. Extra signal added to the JTAG port. Assists debugger synchronization when processor frequency varies. Bidirectional pin with internal pull-up. Note: LOW on this pin while $\overline{\text{RESET}}$ is LOW, enables pins P1[31:26] to operate as Debug port after reset.
P1[27]/TDO	144 ²	B2 ²	O	TDO — Test Data out for JTAG interface.
P1[28]/TDI	140 ²	A3 ²	I	TDI — Test Data in for JTAG interface.
P1[29]/TCK	126 ²	A7 ²	I	TCK — Test Clock for JTAG interface. This clock must be slower than $\frac{1}{6}$ of the CPU clock (CCLK) for the JTAG interface to operate.
P1[30]/TMS	113 ²	D10 ²	I	TMS — Test Mode Select for JTAG interface.
P1[31]/ $\overline{\text{TRST}}$	43 ²	M4 ²	I	$\overline{\text{TRST}}$ — Test Reset for JTAG interface.
P2[0] to P2[31]			I/O	Port 2 — Port 2 is a 32-bit bidirectional I/O port with individual direction controls for each bit. The operation of port 2 pins depends upon the pin function selected via the Pin Connect Block.
P2[0]/D0	98 ²	E12 ²	I/O	D0 — External memory data line 0.
P2[1]/D1	105 ²	C12 ²	I/O	D1 — External memory data line 1.
P2[2]/D2	106 ²	C11 ²	I/O	D2 — External memory data line 2.
P2[3]/D3	108 ²	B12 ²	I/O	D3 — External memory data line 3.
P2[4]/D4	109 ²	A13 ²	I/O	D4 — External memory data line 4.
P2[5]/D5	114 ²	C10 ²	I/O	D5 — External memory data line 5.
P2[6]/D6	115 ²	B10 ²	I/O	D6 — External memory data line 6.
P2[7]/D7	116 ²	A10 ²	I/O	D7 — External memory data line 7.
P2[8]/D8	117 ²	D9 ²	I/O	D8 — External memory data line 8.
P2[9]/D9	118 ²	C9 ²	I/O	D9 — External memory data line 9.
P2[10]/D10	120 ²	A9 ²	I/O	D10 — External memory data line 10.
P2[11]/D11	124 ²	A8 ²	I/O	D11 — External memory data line 11.
P2[12]/D12	125 ²	B7 ²	I/O	D12 — External memory data line 12.
P2[13]/D13	127 ²	C7 ²	I/O	D13 — External memory data line 13.
P2[14]/D14	129 ²	A6 ²	I/O	D14 — External memory data line 14.
P2[15]/D15	130 ²	B6 ²	I/O	D15 — External memory data line 15.
P2[16]/D16	131 ²	C6 ²	I/O	D16 — External memory data line 16.
P2[17]/D17	132 ²	D6 ²	I/O	D17 — External memory data line 17.
P2[18]/D18	133 ²	A5 ²	I/O	D18 — External memory data line 18.
P2[19]/D19	134 ²	B5 ²	I/O	D19 — External memory data line 19.
P2[20]/D20	136 ²	D5 ²	I/O	D20 — External memory data line 20.
P2[21]/D21	137 ²	A4 ²	I/O	D21 — External memory data line 21.
P2[22]/D22	1 ²	A1 ²	I/O	D22 — External memory data line 22.
P2[23]/D23	10 ²	E3 ²	I/O	D23 — External memory data line 23.

Table 4. Pin description ...continued

Symbol	Pin (LQFP)	Pin (TFBGA) ^[1]	Type	Description
P2[24]/D24	11 ^[7]	E2 ^[7]	I/O	D24 — External memory data line 24.
P2[25]/D25	12 ^[7]	E1 ^[7]	I/O	D25 — External memory data line 25.
P2[26]/D26/ BOOT0	13 ^[7]	F4 ^[7]	I/O I	D26 — External memory data line 26. BOOT0 — While $\overline{\text{RESET}}$ is low, together with BOOT1 controls booting and internal operation. Internal pull-up ensures high state if pin is left unconnected.
P2[27]/D27/ BOOT1	16 ^[7]	F1 ^[7]	I/O I	D27 — External memory data line 27. BOOT1 — While $\overline{\text{RESET}}$ is low, together with BOOT0 controls booting and internal operation. Internal pull-up ensures high state if pin is left unconnected. BOOT1:0 = 00 selects 8-bit memory on $\overline{\text{CS0}}$ for boot. BOOT1:0 = 01 selects 16-bit memory on $\overline{\text{CS0}}$ for boot. BOOT1:0 = 10 selects 32-bit memory on $\overline{\text{CS0}}$ for boot. BOOT1:0 = 11 selects internal flash memory.
P2[28]/D28	17 ^[7]	G2 ^[7]	I/O	D28 — External memory data line 28.
P2[29]/D29	18 ^[7]	G1 ^[7]	I/O	D29 — External memory data line 29.
P2[30]/D30/ AIN4	19 ^[6]	G3 ^[6]	I/O I	D30 — External memory data line 30. AIN4 — ADC, input 4. This analog input is always connected to its pin.
P2[31]/D31/ AIN5	20 ^[6]	G4 ^[6]	I/O I	D31 — External memory data line 31. AIN5 — ADC, input 5. This analog input is always connected to its pin.
P3[0] to P3[31]			I/O	Port 3 — Port 3 is a 32-bit bidirectional I/O port with individual direction controls for each bit. The operation of port 3 pins depends upon the pin function selected via the Pin Connect Block.
P3[0]/A0	89 ^[7]	G12 ^[7]	O	A0 — External memory address line 0.
P3[1]/A1	88 ^[7]	H13 ^[7]	O	A1 — External memory address line 1.
P3[2]/A2	87 ^[7]	H12 ^[7]	O	A2 — External memory address line 2.
P3[3]/A3	81 ^[7]	J10 ^[7]	O	A3 — External memory address line 3.
P3[4]/A4	80 ^[7]	K13 ^[7]	O	A4 — External memory address line 4.
P3[5]/A5	74 ^[7]	M13 ^[7]	O	A5 — External memory address line 5.
P3[6]/A6	73 ^[7]	N13 ^[7]	O	A6 — External memory address line 6.
P3[7]/A7	72 ^[7]	M12 ^[7]	O	A7 — External memory address line 7.
P3[8]/A8	71 ^[7]	N12 ^[7]	O	A8 — External memory address line 8.
P3[9]/A9	66 ^[7]	M10 ^[7]	O	A9 — External memory address line 9.
P3[10]/A10	65 ^[7]	N10 ^[7]	O	A10 — External memory address line 10.
P3[11]/A11	64 ^[7]	K9 ^[7]	O	A11 — External memory address line 11.
P3[12]/A12	63 ^[7]	L9 ^[7]	O	A12 — External memory address line 12.
P3[13]/A13	62 ^[7]	M9 ^[7]	O	A13 — External memory address line 13.
P3[14]/A14	56 ^[7]	K7 ^[7]	O	A14 — External memory address line 14.
P3[15]/A15	55 ^[7]	L7 ^[7]	O	A15 — External memory address line 15.
P3[16]/A16	53 ^[7]	M7 ^[7]	O	A16 — External memory address line 16.

Table 4. Pin description ...continued

Symbol	Pin (LQFP)	Pin (TFBGA) ^[1]	Type	Description
P3[17]/A17	48 ^[7]	N5 ^[7]	O	A17 — External memory address line 17.
P3[18]/A18	47 ^[7]	M5 ^[7]	O	A18 — External memory address line 18.
P3[19]/A19	46 ^[7]	L5 ^[7]	O	A19 — External memory address line 19.
P3[20]/A20	45 ^[7]	K5 ^[7]	O	A20 — External memory address line 20.
P3[21]/A21	44 ^[7]	N4 ^[7]	O	A21 — External memory address line 21.
P3[22]/A22	41 ^[7]	K4 ^[7]	O	A22 — External memory address line 22.
P3[23]/A23/ XCLK	40 ^[7]	N3 ^[7]	I/O	A23 — External memory address line 23.
			O	XCLK — Clock output.
P3[24]/ $\overline{\text{CS3}}$	36 ^[7]	M2 ^[7]	O	CS3 — LOW-active Chip Select 3 signal. (Bank 3 addresses range 0x8300 0000 to 0x83FF FFFF)
P3[25]/ $\overline{\text{CS2}}$	35 ^[7]	M1 ^[7]	O	CS2 — LOW-active Chip Select 2 signal. (Bank 2 addresses range 0x8200 0000 to 0x82FF FFFF)
P3[26]/ $\overline{\text{CS1}}$	30 ^[7]	K2 ^[7]	O	CS1 — LOW-active Chip Select 1 signal. (Bank 1 addresses range 0x8100 0000 to 0x81FF FFFF)
P3[27]/ $\overline{\text{WE}}$	29 ^[7]	K1 ^[7]	O	WE — LOW-active Write enable signal.
P3[28]/ $\overline{\text{BLS3}}$ / AIN7	28 ^[6]	J4 ^[6]	O	BLS3 — LOW-active Byte Lane Select signal (Bank 3).
			I	AIN7 — ADC, input 7. This analog input is always connected to its pin.
P3[29]/ $\overline{\text{BLS2}}$ / AIN6	27 ^[6]	J3 ^[6]	O	BLS2 — LOW-active Byte Lane Select signal (Bank 2).
			I	AIN6 — ADC, input 6. This analog input is always connected to its pin.
P3[30]/ $\overline{\text{BLS1}}$	97 ^[7]	E13 ^[7]	O	BLS1 — LOW-active Byte Lane Select signal (Bank 1).
P3[31]/ $\overline{\text{BLS0}}$	96 ^[7]	F10 ^[7]	O	BLS0 — LOW-active Byte Lane Select signal (Bank 0).
TD1	22 ^[7]	H2 ^[7]	O	TD1 : CAN1 transmitter output.
$\overline{\text{RESET}}$	135 ^[8]	C5 ^[8]	I	External Reset input : A LOW on this pin resets the device, causing I/O ports and peripherals to take on their default states, and processor execution to begin at address 0. TTL with hysteresis, 5 V tolerant.
XTAL1	142 ^[9]	C3 ^[9]	I	Input to the oscillator circuit and internal clock generator circuits.
XTAL2	141 ^[9]	B3 ^[9]	O	Output from the oscillator amplifier.
V _{SS}	3, 9, 26, 38, 54, 67, 79, 93, 103, 107, 111, 128	C2, E4, J2, N2, N7, L10, K12, F13, D11, B13, B11, D7	I	Ground : 0 V reference.
V _{SSA}	139	C4	I	Analog ground : 0 V reference. This should nominally be the same voltage as V _{SS} , but should be isolated to minimize noise and error.
V _{SSA(PLL)}	138	B4	I	PLL analog ground : 0 V reference. This should nominally be the same voltage as V _{SS} , but should be isolated to minimize noise and error.
V _{DD(1V8)}	37, 110	N1, A12	I	1.8 V core power supply : This is the power supply voltage for internal circuitry.

Table 4. Pin description ...continued

Symbol	Pin (LQFP)	Pin (TFBGA) ^[1]	Type	Description
V _{DDA(1V8)}	143	A2	I	Analog 1.8 V core power supply: This is the power supply voltage for internal circuitry. This should be nominally the same voltage as V _{DD(1V8)} but should be isolated to minimize noise and error.
V _{DD(3V3)}	2, 31, 39, 51, 57, 77, 94, 104, 112, 119	B1, K3, M3, M6, N8, K10, F12, C13, A11, B9	I	3.3 V pad power supply: This is the power supply voltage for the I/O ports.
V _{DDA(3V3)}	14	F3	I	Analog 3.3 V pad power supply: This should be nominally the same voltage as V _{DD(3V3)} but should be isolated to minimize noise and error.

[1] LPC2294 only.

[2] 5 V tolerant pad providing digital I/O functions with TTL levels and hysteresis and 10 ns slew rate control.

[3] SSP interface available on LPC2292/2294/01 only.

[4] 5 V tolerant pad providing digital I/O functions with TTL levels and hysteresis and 10 ns slew rate control. If configured for an input function, this pad utilizes built-in glitch filter that blocks pulses shorter than 3 ns.

[5] Open-drain 5 V tolerant digital I/O I²C-bus 400 kHz specification compatible pad. It requires external pull-up to provide an output functionality. Open-drain configuration applies to all output functions on this pin.

[6] 5 V tolerant pad providing digital I/O (with TTL levels and hysteresis and 10 ns slew rate control) and analog input function. If configured for a digital input function, this pad utilizes built-in glitch filter that blocks pulses shorter than 3 ns. When configured as an ADC input, digital section of the pad is disabled.

[7] 5 V tolerant pad with built-in pull-up resistor providing digital I/O functions with TTL levels and hysteresis and 10 ns slew rate control. The pull-up resistor's value ranges from 60 kΩ to 300 kΩ.

[8] 5 V tolerant pad providing digital input (with TTL levels and hysteresis) function only.

[9] Pad provides special analog functionality.

6. Functional description

6.1 Architectural overview

The ARM7TDMI-S is a general purpose 32-bit microprocessor, which offers high performance and very low power consumption. The ARM architecture is based on RISC principles, and the instruction set and related decode mechanism are much simpler than those of microprogrammed CISC. This simplicity results in a high instruction throughput and impressive real-time interrupt response from a small and cost-effective processor core.

Pipeline techniques are employed so that all parts of the processing and memory systems can operate continuously. Typically, while one instruction is being executed, its successor is being decoded, and a third instruction is being fetched from memory.

The ARM7TDMI-S processor also employs a unique architectural strategy known as Thumb, which makes it ideally suited to high-volume applications with memory restrictions, or applications where code density is an issue.

The key idea behind Thumb is that of a super-reduced instruction set. Essentially, the ARM7TDMI-S processor has two instruction sets:

- The standard 32-bit ARM set
- A 16-bit Thumb set

The Thumb set's 16-bit instruction length allows it to approach twice the density of standard ARM code while retaining most of the ARM's performance advantage over a traditional 16-bit processor using 16-bit registers. This is possible because Thumb code operates on the same 32-bit register set as ARM code.

Thumb code is able to provide up to 65 % of the code size of ARM, and 160 % of the performance of an equivalent ARM processor connected to a 16-bit memory system.

6.2 On-chip flash program memory

The LPC2292/2294 incorporate a 256 kB flash memory system respectively. This memory may be used for both code and data storage. Programming of the flash memory may be accomplished in several ways. It may be programmed In System via the serial port. The application program may also erase and/or program the flash while the application is running, allowing a great degree of flexibility for data storage field firmware upgrades, etc. When the on-chip bootloader is used, 248 kB of flash memory is available for user code.

The LPC2292/2294 flash memory provides a minimum of 100000 erase/write cycles and 20 years of data retention.

On-chip bootloader (as of revision 1.64) provides Code Read Protection (CRP) for the LPC2292/2294 on-chip flash memory. When the CRP is enabled, the JTAG debug port, external memory boot and ISP commands accessing either the on-chip RAM or flash memory are disabled. However, the ISP flash erase command can be executed at any time (no matter whether the CRP is on or off). Removal of CRP is achieved by erasure of full on-chip user flash. With the CRP off, full access to the chip via the JTAG and/or ISP is restored.

6.3 On-chip SRAM

On-chip SRAM may be used for code and/or data storage. The SRAM may be accessed as 8-bit, 16-bit, and 32-bit. The LPC2292/2294 provide 16 kB of SRAM.

6.4 Memory map

The LPC2292/2294 memory maps incorporate several distinct regions, as shown in [Figure 4](#).

In addition, the CPU interrupt vectors may be re-mapped to allow them to reside in either flash memory (the default) or on-chip static RAM. This is described in [Section 6.19](#) “System control”.

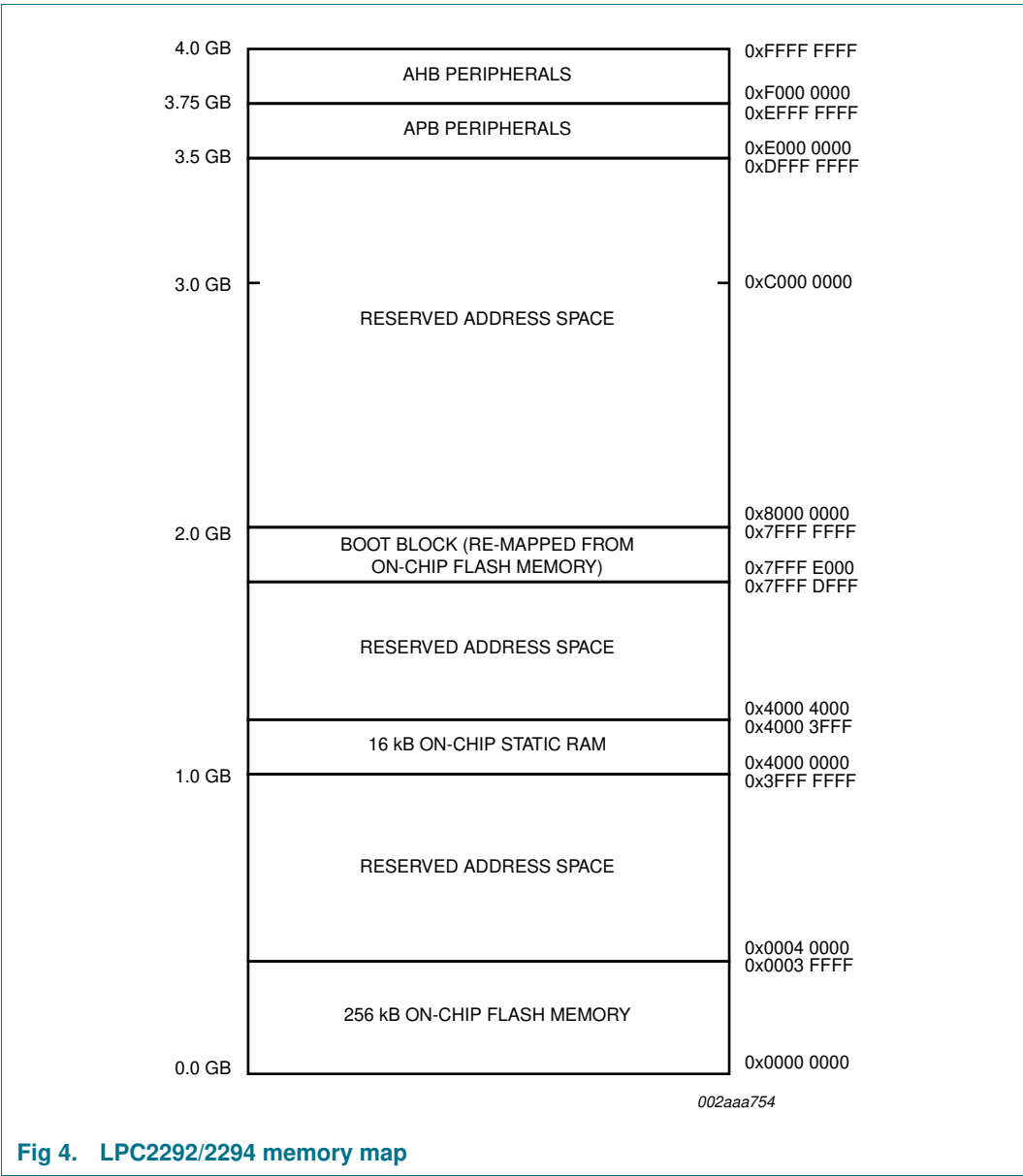


Fig 4. LPC2292/2294 memory map

6.5 Interrupt controller

The VIC accepts all of the interrupt request inputs and categorizes them as Fast Interrupt Request (FIQ), vectored Interrupt Request (IRQ), and non-vectored IRQ as defined by programmable settings. The programmable assignment scheme means that priorities of interrupts from the various peripherals can be dynamically assigned and adjusted.

FIQ has the highest priority. If more than one request is assigned to FIQ, the VIC combines the requests to produce the FIQ signal to the ARM processor. The fastest possible FIQ latency is achieved when only one request is classified as FIQ, because then the FIQ service routine can simply start dealing with that device. But if more than one request is assigned to the FIQ class, the FIQ service routine can read a word from the VIC that identifies which FIQ source(s) is (are) requesting an interrupt.

Vectored IRQs have the middle priority. Sixteen of the interrupt requests can be assigned to this category. Any of the interrupt requests can be assigned to any of the 16 vectored IRQ slots, among which slot 0 has the highest priority and slot 15 has the lowest.

Non-vectored IRQs have the lowest priority.

The VIC combines the requests from all the vectored and non-vectored IRQs to produce the IRQ signal to the ARM processor. The IRQ service routine can start by reading a register from the VIC and jumping there. If any of the vectored IRQs are requesting, the VIC provides the address of the highest-priority requesting IRQs service routine, otherwise it provides the address of a default routine that is shared by all the non-vectored IRQs. The default routine can read another VIC register to see what IRQs are active.

6.5.1 Interrupt sources

[Table 5](#) lists the interrupt sources for each peripheral function. Each peripheral device has one interrupt line connected to the VIC, but may have several internal interrupt flags. Individual interrupt flags may also represent more than one interrupt source.

Table 5. Interrupt sources

Block	Flag(s)	VIC channel #
WDT	Watchdog Interrupt (WDINT)	0
-	Reserved for software interrupts only	1
ARM Core	EmbeddedICE, DbgCommRx	2
ARM Core	EmbeddedICE, DbgCommTx	3
Timer 0	Match 0 to 3 (MR0, MR1, MR2, MR3) Capture 0 to 3 (CR0, CR1, CR2, CR3)	4
Timer 1	Match 0 to 3 (MR0, MR1, MR2, MR3) Capture 0 to 3 (CR0, CR1, CR2, CR3)	5
UART0	RX Line Status (RLS) Transmit Holding Register Empty (THRE) RX Data Available (RDA) Character Time-out Indicator (CTI) Auto-baud time-out (ABTO) [1] End of auto-baud (ABEO) [1]	6

Table 5. Interrupt sources ...continued

Block	Flag(s)	VIC channel #
UART1	RX Line Status (RLS)	7
	Transmit Holding Register empty (THRE)	
	RX Data Available (RDA)	
	Character Time-out Indicator (CTI)	
	Modem Status Interrupt (MSI)	
	Auto-baud time-out (ABTO) ^[1] End of auto-baud (ABEO) ^[1]	
PWM0	Match 0 to 6 (MR0, MR1, MR2, MR3, MR4, MR5, MR6)	8
I2C	SI (state change)	9
SPI0	SPIF, MODF	10
SPI1 and SSP ^[1]	SPIF, MODF and TXRIS, RXRIS, RTRIS, RORRIS	11
PLL	PLL Lock (PLOCK)	12
RTC	RTCCIF (Counter Increment), RTCALF (Alarm)	13
System Control	External Interrupt 0 (EINT0)	14
	External Interrupt 1 (EINT1)	15
	External Interrupt 2 (EINT2)	16
	External Interrupt 3 (EINT3)	17
ADC	ADC	18
CAN	1 ORed CAN Acceptance Filter	19
	CAN1/2 Tx	20, 21
	CAN2/3 Tx (LPC2294 only)	22, 23
	reserved	24, 25
	CAN1/2 Rx	26, 27
	CAN3/4 Rx (LPC2294 only)	28,29

[1] SSP interface and UART0/1 auto-baud control are available on LPC2292/2294/01 only.

6.6 Pin connect block

The pin connect block allows selected pins of the microcontroller to have more than one function. Configuration registers control the multiplexers to allow connection between the pin and the on chip peripherals. Peripherals should be connected to the appropriate pins prior to being activated, and prior to any related interrupt(s) being enabled. Activity of any enabled peripheral function that is not mapped to a related pin should be considered undefined.

6.7 External memory controller

The external Static Memory Controller is a module which provides an interface between the system bus and external (off-chip) memory devices. It provides support for up to four independently configurable memory banks (16 MB each with byte lane enable control) simultaneously. Each memory bank is capable of supporting SRAM, ROM, flash EPROM, burst ROM memory, or some external I/O devices.

Each memory bank may be 8-bit, 16-bit, or 32-bit wide.

6.8 General purpose parallel I/O (GPIO) and Fast I/O

Device pins that are not connected to a specific peripheral function are controlled by the parallel I/O registers. Pins may be dynamically configured as inputs or outputs. Separate registers allow setting or clearing any number of outputs simultaneously. The value of the output register may be read back, as well as the current state of the port pins.

6.8.1 Features

- Bit-level set and clear registers allow a single instruction set or clear of any number of bits in one port.
- Direction control of individual bits.
- Separate control of output set and clear.
- All I/O default to inputs after reset.

6.8.2 Features added with the Fast GPIO set of registers available on LPC2292/2294/01 only

- Fast GPIO registers are relocated to the ARM local bus for the fastest possible I/O timing, enabling port pin toggling up to 3.5 times faster than earlier LPC2000 devices.
- Mask registers allow treating sets of port bits as a group, leaving other bits unchanged.
- All Fast GPIO registers are byte addressable.
- Entire port value can be written in one instruction.
- Ports are accessible via either the legacy group of registers (GPIOs) or the group of registers providing accelerated port access (Fast GPIOs).

6.9 10-bit ADC

The LPC2292/2294 each contain a single 10-bit successive approximation ADC with four multiplexed channels.

6.9.1 Features

- Measurement range of 0 V to 3 V.
- Capable of performing more than 400000 10-bit samples per second.
- Burst conversion mode for single or multiple inputs.
- Optional conversion on transition on input pin or Timer Match signal.

6.9.2 ADC features available in LPC2292/2294/01 only

- Every analog input has a dedicated result register to reduce interrupt overhead.
- Every analog input can generate an interrupt once the conversion is completed.
- The ADC pads are 5 V tolerant when configured for digital I/O function(s).

6.10 CAN controllers and acceptance filter

The LPC2292/2294 each contain two/four CAN controllers. The CAN is a serial communications protocol which efficiently supports distributed real-time control with a very high level of security. Its domain of application ranges from high-speed networks to low cost multiplex wiring.

6.10.1 Features

- Data rates up to 1 Mbit/s on each bus.
- 32-bit register and RAM access.
- Compatible with CAN specification 2.0B, ISO 11898-1.
- Global Acceptance Filter recognizes 11-bit and 29-bit RX identifiers for all CAN buses.
- Acceptance Filter can provide FullCAN-style automatic reception for selected Standard identifiers.

6.11 UARTs

The LPC2292/2294 each contain two UARTs. In addition to standard transmit and receive data lines, the UART1 also provides a full modem control handshake interface.

6.11.1 Features

- 16 B Receive and Transmit FIFOs.
- Register locations conform to 16C550 industry standard.
- Receiver FIFO trigger points at 1 B, 4 B, 8 B, and 14 B
- Built-in fractional baud rate generator covering wide range of baud rates without a need for external crystals of particular values.
- Transmission FIFO control enables implementation of software (XON/XOFF) flow control on both UARTs.
- UART1 is equipped with standard modem interface signals. This module also provides full support for hardware flow control (auto-CTS/RTS).

6.11.2 UART features available in LPC2292/2294/01 only

Compared to previous LPC2000 microcontrollers, UARTs in LPC2292/2294/01 introduce a fractional baud rate generator for both UARTs, enabling these microcontrollers to achieve standard baud rates such as 115200 Bd with any crystal frequency above 2 MHz. In addition, auto-CTS/RTS flow-control functions are fully implemented in hardware.

- Fractional baud rate generator enables standard baud rates such as 115200 Bd to be achieved with any crystal frequency above 2 MHz.
- Auto-bauding.
- Auto-CTS/RTS flow-control fully implemented in hardware.

6.12 I²C-bus serial I/O controller

The I²C-bus is bidirectional, for inter-IC control using only two wires: a serial clock line (SCL), and a serial data line (SDA). Each device is recognized by a unique address and can operate as either a receiver-only device (e.g., an LCD driver or a transmitter with the capability to both receive and send information (such as memory). Transmitters and/or

receivers can operate in either master or slave mode, depending on whether the chip has to initiate a data transfer or is only addressed. The I²C-bus is a multi-master bus, it can be controlled by more than one bus master connected to it.

The I²C-bus implemented in LPC2292/2294 supports bit rate up to 400 kbit/s (Fast I²C-bus).

6.12.1 Features

- Compliant with standard I²C-bus interface.
- Easy to configure as master, slave, or master/slave.
- Programmable clocks allow versatile rate control.
- Bidirectional data transfer between masters and slaves.
- Multi-master bus (no central master).
- Arbitration between simultaneously transmitting masters without corruption of serial data on the bus.
- Serial clock synchronization allows devices with different bit rates to communicate via one serial bus.
- Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer.
- The I²C-bus may be used for test and diagnostic purposes.

6.13 SPI serial I/O controller

The LPC2292/2294 each contain two SPIs. The SPI is a full duplex serial interface, designed to be able to handle multiple masters and slaves connected to a given bus. Only a single master and a single slave can communicate on the interface during a given data transfer. During a data transfer the master always sends a byte of data to the slave, and the slave always sends a byte of data to the master.

6.13.1 Features

- Compliant with Serial Peripheral Interface (SPI) specification.
- Synchronous, Serial, Full Duplex communication.
- Combined SPI master and slave.
- Maximum data bit rate of $\frac{1}{8}$ of the input clock rate.

6.13.2 Features available in LPC2292/2294/01 only

- Eight to 16 bits per frame.
- When the SPI interface is used in Master mode, the SSELn pin is not needed (can be used for a different function).

6.14 SSP controller (LPC2292/94/01 only)

The SSP is a controller capable of operation on a SPI, 4-wire SSI, or Microwire bus. It can interact with multiple masters and slaves on the bus. Only a single master and a single slave can communicate on the bus during a given data transfer. Data transfers are in principle full duplex, with frames of four to 16 bits of data flowing from the master to the slave and from the slave to the master.

While the SSP and SPI1 peripherals share the same physical pins, it is not possible to have both of these two peripherals active at the same time. Application can switch on the fly from SPI1 to SSP and back.

6.14.1 Features

- Compatible with Motorola's SPI, Texas Instrument's 4-wire SSI, and National Semiconductor's Microwire buses.
- Synchronous serial communication.
- Master or slave operation.
- 8-frame FIFOs for both transmit and receive.
- Four to 16 bits per frame.

6.15 General purpose timers

The Timer/Counter is designed to count cycles of the peripheral clock (PCLK) or an externally supplied clock and optionally generate interrupts or perform other actions at specified timer values, based on four match registers. It also includes four capture inputs to trap the timer value when an input signal transitions, optionally generating an interrupt. Multiple pins can be selected to perform a single capture or match function, providing an application with 'or' and 'and', as well as 'broadcast' functions among them.

6.15.1 Features

- A 32-bit Timer/Counter with a programmable 32-bit Prescaler.
- Timer or external event counter operation
- Four 32-bit capture channels per timer that can take a snapshot of the timer value when an input signal transitions. A capture event may also optionally generate an interrupt.
- Four 32-bit match registers that allow:
 - Continuous operation with optional interrupt generation on match.
 - Stop timer on match with optional interrupt generation.
 - Reset timer on match with optional interrupt generation.
- Four external outputs per timer corresponding to match registers, with the following capabilities:
 - Set LOW on match.
 - Set HIGH on match.
 - Toggle on match.
 - Do nothing on match.

6.15.2 Features available in LPC2292/2294/01 only

The LPC2292/2294/01 can count external events on one of the capture inputs if the external pulse lasts at least one half of the period of the PCLK. In this configuration, unused capture lines can be selected as regular timer capture inputs, or used as external interrupts.

- Timer can count cycles of either the peripheral clock (PCLK) or an externally supplied clock.
- When counting cycles of an externally supplied clock, only one of the timer's capture inputs can be selected as the timer's clock. The rate of such a clock is limited to $PCLK / 4$. Duration of HIGH/LOW levels on the selected CAP input cannot be shorter than $1 / (2PCLK)$.

6.16 Watchdog timer

The purpose of the watchdog is to reset the microcontroller within a reasonable amount of time if it enters an erroneous state. When enabled, the watchdog will generate a system reset if the user program fails to 'feed' (or reload) the watchdog within a predetermined amount of time.

6.16.1 Features

- Internally resets chip if not periodically reloaded.
- Debug mode.
- Enabled by software but requires a hardware reset or a watchdog reset/interrupt to be disabled.
- Incorrect/incomplete feed sequence causes reset/interrupt if enabled.
- Flag to indicate watchdog reset.
- Programmable 32-bit timer with internal prescaler.
- Selectable time period from $(T_{cy(PCLK)} \times 256 \times 4)$ to $(T_{cy(PCLK)} \times 2^{32} \times 4)$ in multiples of $T_{cy(PCLK)} \times 4$.

6.17 Real-time clock

The Real-Time Clock (RTC) is designed to provide a set of counters to measure time when normal or idle operating mode is selected. The RTC has been designed to use little power, making it suitable for battery powered systems where the CPU is not running continuously (Idle mode).

6.17.1 Features

- Measures the passage of time to maintain a calendar and clock.
- Ultra-low power design to support battery powered systems.
- Provides Seconds, Minutes, Hours, Day of Month, Month, Year, Day of Week, and Day of Year.
- Programmable Reference Clock Divider allows adjustment of the RTC to match various crystal frequencies.

6.18 Pulse width modulator

The PWM is based on the standard Timer block and inherits all of its features, although only the PWM function is pinned out on the LPC2292/2294. The Timer is designed to count cycles of the peripheral clock (PCLK) and optionally generate interrupts or perform other actions when specified timer values occur, based on seven match registers. The PWM function is also based on match register events.

The ability to separately control rising and falling edge locations allows the PWM to be used for more applications. For instance, multi-phase motor control typically requires three non-overlapping PWM outputs with individual control of all three pulse widths and positions.

Two match registers can be used to provide a single edge controlled PWM output. One match register (MR0) controls the PWM cycle rate, by resetting the count upon match. The other match register controls the PWM edge position. Additional single edge controlled PWM outputs require only one match register each, since the repetition rate is the same for all PWM outputs. Multiple single edge controlled PWM outputs will all have a rising edge at the beginning of each PWM cycle, when an MR0 match occurs.

Three match registers can be used to provide a PWM output with both edges controlled. Again, the MR0 match register controls the PWM cycle rate. The other match registers control the two PWM edge positions. Additional double edge controlled PWM outputs require only two match registers each, since the repetition rate is the same for all PWM outputs.

With double edge controlled PWM outputs, specific match registers control the rising and falling edge of the output. This allows both positive going PWM pulses (when the rising edge occurs prior to the falling edge), and negative going PWM pulses (when the falling edge occurs prior to the rising edge).

6.18.1 Features

- Seven match registers allow up to six single edge controlled or three double edge controlled PWM outputs, or a mix of both types.
- The match registers also allow:
 - Continuous operation with optional interrupt generation on match.
 - Stop timer on match with optional interrupt generation.
 - Reset timer on match with optional interrupt generation.
- Supports single edge controlled and/or double edge controlled PWM outputs. Single edge controlled PWM outputs all go HIGH at the beginning of each cycle unless the output is a constant LOW. Double edge controlled PWM outputs can have either edge occur at any position within a cycle. This allows for both positive going and negative going pulses.
- Pulse period and width can be any number of timer counts. This allows complete flexibility in the trade-off between resolution and repetition rate. All PWM outputs will occur at the same repetition rate.
- Double edge controlled PWM outputs can be programmed to be either positive going or negative going pulses.

- Match register updates are synchronized with pulse outputs to prevent generation of erroneous pulses. Software must 'release' new match values before they can become effective.
- May be used as a standard timer if the PWM mode is not enabled.
- A 32-bit Timer/Counter with a programmable 32-bit prescaler.

6.19 System control

6.19.1 Crystal oscillator

The oscillator supports crystals in the range of 1 MHz to 25 MHz. The oscillator output frequency is called f_{osc} and the ARM processor clock frequency is referred to as CCLK for purposes of rate equations, etc. f_{osc} and CCLK are the same value unless the PLL is running and connected. Refer to [Section 6.19.2 "PLL"](#) for additional information.

6.19.2 PLL

The PLL accepts an input clock frequency in the range of 10 MHz to 25 MHz. The input frequency is multiplied up into the range of 10 MHz to 60 MHz with a Current Controlled Oscillator (CCO). The multiplier can be an integer value from 1 to 32 (in practice, the multiplier value cannot be higher than 6 on this family of microcontrollers due to the upper frequency limit of the CPU). The CCO operates in the range of 156 MHz to 320 MHz, so there is an additional divider in the loop to keep the CCO within its frequency range while the PLL is providing the desired output frequency. The output divider may be set to divide by 2, 4, 8, or 16 to produce the output clock. Since the minimum output divider value is 2, it is insured that the PLL output has a 50 % duty cycle. The PLL is turned off and bypassed following a chip reset and may be enabled by software. The program must configure and activate the PLL, wait for the PLL to Lock, then connect to the PLL as a clock source. The PLL settling time is 100 μ s.

6.19.3 Reset and wake-up timer

Reset has two sources on the LPC2292/2294: the $\overline{\text{RESET}}$ pin and watchdog reset. The $\overline{\text{RESET}}$ pin is a Schmitt trigger input pin with an additional glitch filter. Assertion of chip reset by any source starts the Wake-up Timer (see Wake-up Timer description below), causing the internal chip reset to remain asserted until the external reset is de-asserted, the oscillator is running, a fixed number of clocks have passed, and the on-chip flash controller has completed its initialization.

When the internal reset is removed, the processor begins executing at address 0, which is the reset vector. At that point, all of the processor and peripheral registers have been initialized to predetermined values.

The Wake-up Timer ensures that the oscillator and other analog functions required for chip operation are fully functional before the processor is allowed to execute instructions. This is important at power-on, all types of reset, and whenever any of the aforementioned functions are turned off for any reason. Since the oscillator and other functions are turned off during Power-down mode, any wake-up of the processor from Power-down mode makes use of the Wake-up Timer.