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LPC2364/65/66/67/68

Single-chip 16-bit/32-bit microcontrollers; up to 512 kB flash with ISP/IAP, Ethernet, USB 2.0, CAN, and 10-bit ADC/DAC

Rev. 7.1 — 16 October 2013 Product data sheet

1. General description

The LPC2364/65/66/67/68 microcontrollers are based on a 16-bit/32-bit ARM7TDMI-S CPU with real-time emulation that combines the microcontroller with up to 512 kB of embedded high-speed flash memory. A 128-bit wide memory interface and a unique accelerator architecture enable 32-bit code execution at the maximum clock rate. For critical performance in interrupt service routines and DSP algorithms, this increases performance up to 30 % over Thumb mode. For critical code size applications, the alternative 16-bit Thumb mode reduces code by more than 30 % with minimal performance penalty.

The LPC2364/65/66/67/68 are ideal for multi-purpose serial communication applications. They incorporate a 10/100 Ethernet Media Access Controller (MAC), USB full speed device with 4 kB of endpoint RAM (LPC2364/66/68 only), four UARTs, two CAN channels (LPC2364/66/68 only), an SPI interface, two Synchronous Serial Ports (SSP), three I^2C-bus interfaces, and an I^2S-bus interface. This blend of serial communications interfaces combined with an on-chip 4 MHz internal oscillator, SRAM of up to 32 kB, 16 kB SRAM for Ethernet, 8 kB SRAM for USB and general purpose use, together with 2 kB battery powered SRAM make these devices very well suited for communication gateways and protocol converters. Various 32-bit timers, an improved 10-bit ADC, 10-bit DAC, one PWM unit, a CAN control unit (LPC2364/66/68 only), and up to 70 fast GPIO lines with up to 12 edge or level sensitive external interrupt pins make these microcontrollers particularly suitable for industrial control and medical systems.

2. Features and benefits

- ARM7TDMI-S processor, running at up to 72 MHz
- Up to 512 kB on-chip flash program memory with In-System Programming (ISP) and In-Application Programming (IAP) capabilities. Flash program memory is on the ARM local bus for high performance CPU access.
- 8 kB/32 kB of SRAM on the ARM local bus for high performance CPU access.
- 16 kB SRAM for Ethernet interface. Can also be used as general purpose SRAM.
- 8 kB SRAM for general purpose DMA use also accessible by the USB.
- Dual Advanced High-performance Bus (AHB) system that provides for simultaneous Ethernet DMA, USB DMA, and program execution from on-chip flash with no contention between those functions. A bus bridge allows the Ethernet DMA to access the other AHB subsystem.
- Advanced Vectored Interrupt Controller (VIC), supporting up to 32 vectored interrupts.
- General Purpose DMA controller (GPDMA) on AHB that can be used with the SSP serial interfaces, the I^2S port, and the Secure Digital/MultiMediaCard (SD/MMC) card port, as well as for memory-to-memory transfers.

- Serial interfaces:
  - Ethernet MAC with associated DMA controller. These functions reside on an independent AHB.
  - USB 2.0 full-speed device with on-chip PHY and associated DMA controller (LPC2364/66/68 only).
  - Four UARTs with fractional baud rate generation, one with modem control I/O, one with IrDA support, all with FIFO.
  - CAN controller with two channels (LPC2364/66/68 only).
  - SPI controller.
  - Two SSP controllers, with FIFO and multi-protocol capabilities. One is an alternate for the SPI port, sharing its interrupt and pins. These can be used with the GPDMA controller.
  - Three I^2C-bus interfaces (one with open-drain and two with standard port pins).
  - I^2S (Inter-IC Sound) interface for digital audio input or output. It can be used with the GPDMA.
- Other peripherals:
  - SD/MMC memory card interface (LPC2367/68 only).
  - 70 general purpose I/O pins with configurable pull-up/down resistors.
  - 10-bit ADC with input multiplexing among 6 pins.
  - 10-bit DAC.
  - Four general purpose timers/counters with a total of 8 capture inputs and 10 compare outputs. Each timer block has an external count input.
  - One PWM/timer block with support for three-phase motor control. The PWM has two external count inputs.
  - Real-Time Clock (RTC) with separate power pin, clock source can be the RTC oscillator or the APB clock.
  - 2 kB SRAM powered from the RTC power pin, allowing data to be stored when the rest of the chip is powered off.
  - WatchDog Timer (WDT). The WDT can be clocked from the internal RC oscillator, the RTC oscillator, or the APB clock.
- Standard ARM test/debug interface for compatibility with existing tools.
- Emulation trace module supports real-time trace.
- Single 3.3 V power supply (3.0 V to 3.6 V).
- Four reduced power modes: idle, sleep, power-down, and deep power-down.
- Four external interrupt inputs configurable as edge/level sensitive. All pins on Port 0 and Port 2 can be used as edge sensitive interrupt sources.
- Processor wake-up from Power-down mode via any interrupt able to operate during Power-down mode (includes external interrupts, RTC interrupt, USB activity, Ethernet wake-up interrupt).
- Two independent power domains allow fine tuning of power consumption based on needed features.
- Each peripheral has its own clock divider for further power saving.
- Brownout detect with separate thresholds for interrupt and forced reset.
- On-chip power-on reset.
- On-chip crystal oscillator with an operating range of 1 MHz to 24 MHz.
- 4 MHz internal RC oscillator trimmed to 1 % accuracy that can optionally be used as the system clock. When used as the CPU clock, does not allow CAN and USB to run.

- On-chip PLL allows CPU operation up to the maximum CPU rate without the need for a high frequency crystal. May be run from the main oscillator, the internal RC oscillator, or the RTC oscillator.
- Boundary scan for simplified board testing is available in LPC2364FET100 and LPC2368FET100 (TFBGA package).
- Versatile pin function selections allow more possibilities for using on-chip peripheral functions.

3. Applications

- Industrial control
- Medical systems
- Protocol converter
- Communications

4. Ordering information

Table 1. Ordering information

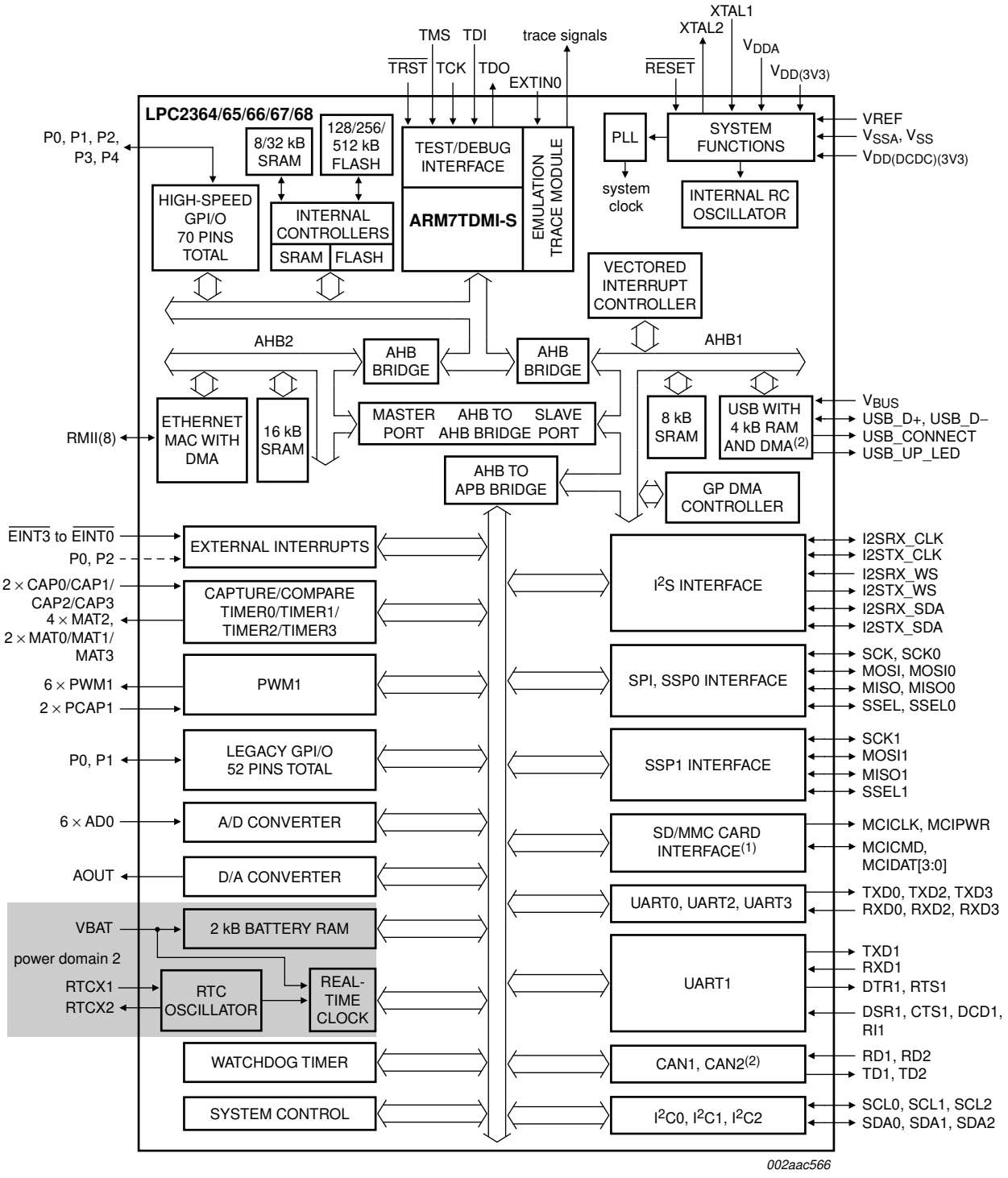
Type number	Package		
	Name	Description	Version
LPC2364FBD100	LQFP100	plastic low profile quad flat package; 100 leads; body 14 × 14 × 1.4 mm	SOT407-1
LPC2364HBD100	LQFP100	plastic low profile quad flat package; 100 leads; body 14 × 14 × 1.4 mm	SOT407-1
LPC2364FET100	TFBGA100	plastic thin fine-pitch ball grid array package; 100 balls; body 9 × 9 × 0.7 mm	SOT926-1
LPC2365FBD100	LQFP100	plastic low profile quad flat package; 100 leads; body 14 × 14 × 1.4 mm	SOT407-1
LPC2366FBD100	LQFP100	plastic low profile quad flat package; 100 leads; body 14 × 14 × 1.4 mm	SOT407-1
LPC2367FBD100	LQFP100	plastic low profile quad flat package; 100 leads; body 14 × 14 × 1.4 mm	SOT407-1
LPC2368FBD100	LQFP100	plastic low profile quad flat package; 100 leads; body 14 × 14 × 1.4 mm	SOT407-1
LPC2368FET100	TFBGA100	plastic thin fine-pitch ball grid array package; 100 balls; body 9 × 9 × 0.7 mm	SOT926-1

4.1 Ordering options

Table 2. Ordering options

Type number	Flash (kB)	SRAM (kB)					Ethernet	USB device + 4 kB FIFO	SD/MMC	GP DMA	Channels			Temp range
		Local bus	Ethernet buffers	GP/USB	RTC	Total					CAN	ADC	DAC	
LPC2364FBD100	128	8	16	8	2	34	RMII	yes	no	yes	2	6	1	–40 °C to +85 °C
LPC2364HBD100	128	8	16	8	2	34	RMII	yes	no	yes	2	6	1	–40 °C to +125 °C
LPC2364FET100	128	8	16	8	2	34	RMII	yes	no	yes	2	6	1	–40 °C to +85 °C
LPC2365FBD100	256	32	16	8	2	58	RMII	no	no	yes	-	6	1	–40 °C to +85 °C
LPC2366FBD100	256	32	16	8	2	58	RMII	yes	no	yes	2	6	1	–40 °C to +85 °C
LPC2367FBD100	512	32	16	8	2	58	RMII	no	yes	yes	-	6	1	–40 °C to +85 °C
LPC2368FBD100	512	32	16	8	2	58	RMII	yes	yes	yes	2	6	1	–40 °C to +85 °C
LPC2368FET100	512	32	16	8	2	58	RMII	yes	yes	yes	2	6	1	–40 °C to +85 °C

5. Block diagram



(1) LPC2367/68 only.

(2) LPC2364/66/68 only.

Fig 1. LPC2364/65/66/67/68 block diagram

6. Pinning information

6.1 Pinning

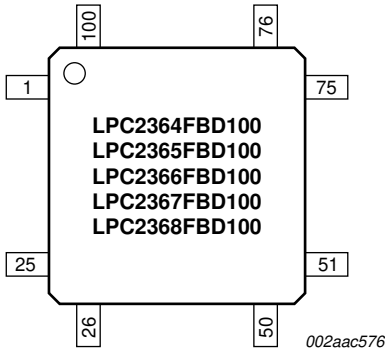


Fig 2. LPC2364/65/66/67/68 pinning

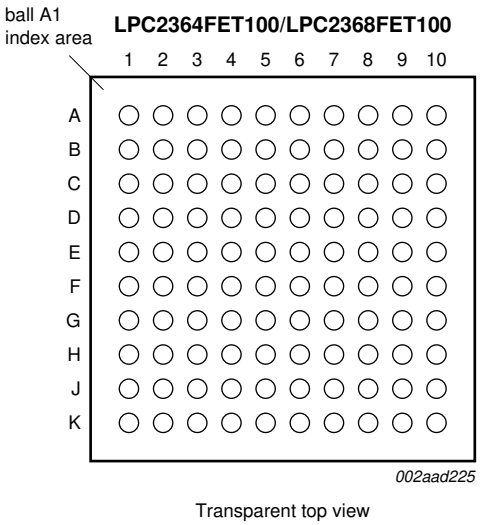


Fig 3. LPC2364/68 pinning TFBGA100 package

Table 3. Pin allocation table

Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
Row A							
1	TDO	2	P0[3]/RXD0	3	$V_{DD(3V3)}$	4	P1[4]/ENET_TX_EN
5	P1[10]/ENET_RXD1	6	P1[16]/ENET_MDC	7	$V_{DD(DCDC)(3V3)}$	8	P0[4]/I2SRX_CLK/ RD2/CAP2[0]
9	P0[7]/I2STX_CLK/ SCK1/MAT2[1]	10	P0[9]/I2STX_SDA/ MOSI1/MAT2[3]	11	-	12	-
Row B							
1	TMS	2	RTCK	3	V_{SS}	4	P1[1]/ENET_TXD1
5	P1[9]/ENET_RXD0	6	P1[17]/ ENET_MDIO	7	V_{SS}	8	P0[6]/I2SRX_SDA/ SSEL1/MAT2[0]
9	P2[0]/PWM1[1]/ TXD1/TRACECLK	10	P2[1]/PWM1[2]/ RXD1/PIPESTAT0	11	-	12	-
Row C							
1	TCK	2	$\overline{\text{TRST}}$	3	TDI	4	P0[2]/TXD0
5	P1[8]/ENET_CRS	6	P1[15]/ ENET_REF_CLK	7	P4[28]/MAT2[0]/ TXD3	8	P0[8]/I2STX_WS/ MISO1/MAT2[2]
9	V_{SS}	10	$V_{DD(3V3)}$	11	-	12	-
Row D							
1	P0[24]/AD0[1]/ I2SRX_WS/CAP3[1]	2	P0[25]/AD0[2]/ I2SRX_SDA/TXD3	3	P0[26]/AD0[3]/ AOUT/RXD3	4	DBGEN
5	P1[0]/ENET_TXD0	6	P1[14]/ENET_RX_ER	7	P0[5]/I2SRX_WS/ TD2/CAP2[1]	8	P2[2]/PWM1[3]/ CTS1/PIPESTAT1
9	P2[4]/PWM1[5]/ DSR1/TRACESYNC	10	P2[5]/PWM1[6]/ DTR1/TRACEPKT0	11	-	12	-
Row E							
1	V_{SSA}	2	V_{DDA}	3	VREF	4	$V_{DD(DCDC)(3V3)}$
5	P0[23]/AD0[0]/ I2SRX_CLK/CAP3[0]	6	P4[29]/MAT2[1]/ RXD3	7	P2[3]/PWM1[4]/ DCD1/PIPESTAT2	8	P2[6]/PCAP1[0]/RI1/ TRACEPKT1
9	P2[7]/RD2/ RTS1/TRACEPKT2	10	P2[8]/TD2/ TXD2/TRACEPKT3	11	-	12	-
Row F							
1	V_{SS}	2	RTCX1	3	$\overline{\text{RESET}}$	4	P1[31]/SCK1/ AD0[5]
5	P1[21]/PWM1[3]/ SSEL0	6	P0[18]/DCD1/ MOSI0/MOSI	7	P2[9]/USB_CONNECT/ RXD2/EXTIN0	8	P0[16]/RXD1/ SSEL0/SSEL
9	P0[17]/CTS1/ MISO0/MISO	10	P0[15]/TXD1/ SCK0/SCK	11	-	12	-
Row G							
1	RTCX2	2	VBAT	3	XTAL2	4	P0[30]/USB_D−
5	P1[25]/MAT1[1]	6	P1[29]/PCAP1[1]/ MAT0[1]	7	V_{SS}	8	P0[21]/RI1/ MCIPWR/RD1
9	P0[20]/DTR1/ MCICMD/SCL1	10	P0[19]/DSR1/ MCICLK/SDA1	11	-	12	-
Row H							

Table 3. Pin allocation table *…continued*

Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	P1[30]/V_{BUS}/ AD0[4]	2	XTAL1	3	P3[25]/MAT0[0]/ PWM1[2]	4	P1[18]/USB_UP_LED/ PWM1[1]/CAP1[0]
5	P1[24]/PWM1[5]/ MOSI0	6	$V_{DD(DCDC)(3V3)}$	7	P0[10]/TXD2/ SDA2/MAT3[0]	8	P2[11]/$\overline{\text{EINT1}}$/ MCIDAT1/I2STX_CLK
9	$V_{DD(3V3)}$	10	P0[22]/RTS1/ MCIDAT0/TD1	11	-	12	-

Table 3. Pin allocation table *…continued*

Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
Row J							
1	P0[28]/SCL0	2	P0[27]/SDA0	3	P0[29]/USB_D+	4	P1[19]/CAP1[1]
5	P1[22]/MAT1[0]	6	V_{SS}	7	P1[28]/PCAP1[0]/ MAT0[0]	8	P0[1]/TD1/RXD3/SCL1
9	P2[13]/$\overline{\text{EINT3}}$/ MCIDAT3/I2STX_SDA	10	P2[10]/$\overline{\text{EINT0}}$	11	-	12	-
Row K							
1	P3[26]/MAT0[1]/ PWM1[3]	2	$V_{DD(3V3)}$	3	V_{SS}	4	P1[20]/PWM1[2]/ SCK0
5	P1[23]/PWM1[4]/ MISO0	6	P1[26]/PWM1[6]/ CAP0[0]	7	P1[27]/CAP0[1]	8	P0[0]/RD1/TXD3/SDA1
9	P0[11]/RXD2/ SCL2/MAT3[1]	10	P2[12]/$\overline{\text{EINT2}}$/ MCIDAT2/I2STX_WS	11	-	12	-

6.2 Pin description

Table 4. Pin description

Symbol	Pin	Ball	Type	Description
P0[0] to P0[31]			I/O	**Port 0:** Port 0 is a 32-bit I/O port with individual direction controls for each bit. The operation of Port 0 pins depends upon the pin function selected via the pin connect block. Pins 12, 13, 14, and 31 of this port are not available.
P0[0]/RD1/TXD3/ SDA1	46[1]	K8[1]	I/O	**P0[0] —** General purpose digital input/output pin.
			I	**RD1 —** CAN1 receiver input. (LPC2364/66/68 only)
			O	**TXD3 —** Transmitter output for UART3.
			I/O	**SDA1 —** I^2C1 data input/output (this is not an open-drain pin).
P0[1]/TD1/RXD3/ SCL1	47[1]	J8[1]	I/O	**P0[1] —** General purpose digital input/output pin.
			O	**TD1 —** CAN1 transmitter output. (LPC2364/66/68 only)
			I	**RXD3 —** Receiver input for UART3.
			I/O	**SCL1 —** I^2C1 clock input/output (this is not an open-drain pin).
P0[2]/TXD0	98[1]	C4[1]	I/O	**P0[2] —** General purpose digital input/output pin.
			O	**TXD0 —** Transmitter output for UART0.
P0[3]/RXD0	99[1]	A2[1]	I/O	**P0[3] —** General purpose digital input/output pin.
			I	**RXD0 —** Receiver input for UART0.
P0[4]/ I2SRX_CLK/ RD2/CAP2[0]	81[1]	A8[1]	I/O	**P0[4] —** General purpose digital input/output pin.
			I/O	**I2SRX_CLK —** Receive Clock. It is driven by the master and received by the slave. Corresponds to the signal SCK in the *I^2S-bus specification*.
			I	**RD2 —** CAN2 receiver input. (LPC2364/66/68 only)
			I	**CAP2[0] —** Capture input for Timer 2, channel 0.
P0[5]/ I2SRX_WS/ TD2/CAP2[1]	80[1]	D7[1]	I/O	**P0[5] —** General purpose digital input/output pin.
			I/O	**I2SRX_WS —** Receive Word Select. It is driven by the master and received by the slave. Corresponds to the signal WS in the *I^2S-bus specification*.
			O	**TD2 —** CAN2 transmitter output. (LPC2364/66/68 only)
			I	**CAP2[1] —** Capture input for Timer 2, channel 1.
P0[6]/ I2SRX_SDA/ SSEL1/MAT2[0]	79[1]	B8[1]	I/O	**P0[6] —** General purpose digital input/output pin.
			I/O	**I2SRX_SDA —** Receive data. It is driven by the transmitter and read by the receiver. Corresponds to the signal SD in the *I^2S-bus specification*.
			I/O	**SSEL1 —** Slave Select for SSP1.
			O	**MAT2[0] —** Match output for Timer 2, channel 0.
P0[7]/ I2STX_CLK/ SCK1/MAT2[1]	78[1]	A9[1]	I/O	**P0[7] —** General purpose digital input/output pin.
			I/O	**I2STX_CLK —** Transmit Clock. It is driven by the master and received by the slave. Corresponds to the signal SCK in the *I^2S-bus specification*.
			I/O	**SCK1 —** Serial Clock for SSP1.
			O	**MAT2[1] —** Match output for Timer 2, channel 1.
P0[8]/ I2STX_WS/ MISO1/MAT2[2]	77[1]	C8[1]	I/O	**P0[8] —** General purpose digital input/output pin.
			I/O	**I2STX_WS —** Transmit Word Select. It is driven by the master and received by the slave. Corresponds to the signal WS in the *I^2S-bus specification*.
			I/O	**MISO1 —** Master In Slave Out for SSP1.
			O	**MAT2[2] —** Match output for Timer 2, channel 2.

Table 4. Pin description *...continued*

Symbol	Pin	Ball	Type	Description
P0[9]/ I2STX_SDA/ MOSI1/MAT2[3]	76[1]	A10[1]	I/O	**P0[9] —** General purpose digital input/output pin.
			I/O	**I2STX_SDA —** Transmit data. It is driven by the transmitter and read by the receiver. Corresponds to the signal SD in the *I²S-bus specification*.
			I/O	**MOSI1 —** Master Out Slave In for SSP1.
			O	**MAT2[3] —** Match output for Timer 2, channel 3.
P0[10]/TXD2/ SDA2/MAT3[0]	48[1]	H7[1]	I/O	**P0[10] —** General purpose digital input/output pin.
			O	**TXD2 —** Transmitter output for UART2.
			I/O	**SDA2 —** I²C2 data input/output (this is not an open-drain pin).
			O	**MAT3[0] —** Match output for Timer 3, channel 0.
P0[11]/RXD2/ SCL2/MAT3[1]	49[1]	K9[1]	I/O	**P0[11] —** General purpose digital input/output pin.
			I	**RXD2 —** Receiver input for UART2.
			I/O	**SCL2 —** I²C2 clock input/output (this is not an open-drain pin).
			O	**MAT3[1] —** Match output for Timer 3, channel 1.
P0[15]/TXD1/ SCK0/SCK	62[1]	F10[1]	I/O	**P0[15] —** General purpose digital input/output pin.
			O	**TXD1 —** Transmitter output for UART1.
			I/O	**SCK0 —** Serial clock for SSP0.
			I/O	**SCK —** Serial clock for SPI.
P0[16]/RXD1/ SSEL0/SSEL	63[1]	F8[1]	I/O	**P0[16] —** General purpose digital input/output pin.
			I	**RXD1 —** Receiver input for UART1.
			I/O	**SSEL0 —** Slave Select for SSP0.
			I/O	**SSEL —** Slave Select for SPI.
P0[17]/CTS1/ MISO0/MISO	61[1]	F9[1]	I/O	**P0[17] —** General purpose digital input/output pin.
			I	**CTS1 —** Clear to Send input for UART1.
			I/O	**MISO0 —** Master In Slave Out for SSP0.
			I/O	**MISO —** Master In Slave Out for SPI.
P0[18]/DCD1/ MOSI0/MOSI	60[1]	F6[1]	I/O	**P0[18] —** General purpose digital input/output pin.
			I	**DCD1 —** Data Carrier Detect input for UART1.
			I/O	**MOSI0 —** Master Out Slave In for SSP0.
			I/O	**MOSI —** Master Out Slave In for SPI.
P0[19]/DSR1/ MCICLK/SDA1	59[1]	G10[1]	I/O	**P0[19] —** General purpose digital input/output pin.
			I	**DSR1 —** Data Set Ready input for UART1.
			O	**MCICLK —** Clock output line for SD/MMC interface. (LPC2367/68 only)
			I/O	**SDA1 —** I²C1 data input/output (this is not an open-drain pin).
P0[20]/DTR1/ MCICMD/SCL1	58[1]	G9[1]	I/O	**P0[20] —** General purpose digital input/output pin.
			O	**DTR1 —** Data Terminal Ready output for UART1.
			I	**MCICMD —** Command line for SD/MMC interface. (LPC2367/68 only)
			I/O	**SCL1 —** I²C1 clock input/output (this is not an open-drain pin).

Table 4. Pin description *...continued*

Symbol	Pin	Ball	Type	Description
P0[21]/RI1/ MCIPWR/RD1	57[1]	G8[1]	I/O	**P0[21]** — General purpose digital input/output pin.
			I	**RI1** — Ring Indicator input for UART1.
			O	**MCIPWR** — Power Supply Enable for external SD/MMC power supply. (LPC2367/68 only)
			I	**RD1** — CAN1 receiver input. (LPC2364/66/68 only)
P0[22]/RTS1/ MCIDAT0/TD1	56[1]	H10[1]	I/O	**P0[22]** — General purpose digital input/output pin.
			O	**RTS1** — Request to Send output for UART1.
			O	**MCIDAT0** — Data line for SD/MMC interface. (LPC2367/68 only)
			O	**TD1** — CAN1 transmitter output. (LPC2364/66/68 only)
P0[23]/AD0[0]/ I2SRX_CLK/ CAP3[0]	9[2]	E5[2]	I/O	**P0[23]** — General purpose digital input/output pin.
			I	**AD0[0]** — A/D converter 0, input 0.
			I/O	**I2SRX_CLK** — Receive Clock. It is driven by the master and received by the slave. Corresponds to the signal SCK in the *I^2S-bus specification*.
			I	**CAP3[0]** — Capture input for Timer 3, channel 0.
P0[24]/AD0[1]/ I2SRX_WS/ CAP3[1]	8[2]	D1[2]	I/O	**P0[24]** — General purpose digital input/output pin.
			I	**AD0[1]** — A/D converter 0, input 1.
			I/O	**I2SRX_WS** — Receive Word Select. It is driven by the master and received by the slave. Corresponds to the signal WS in the *I^2S-bus specification*.
			I	**CAP3[1]** — Capture input for Timer 3, channel 1.
P0[25]/AD0[2]/ I2SRX_SDA/ TXD3	7[2]	D2[2]	I/O	**P0[25]** — General purpose digital input/output pin.
			I	**AD0[2]** — A/D converter 0, input 2.
			I/O	**I2SRX_SDA** — Receive data. It is driven by the transmitter and read by the receiver. Corresponds to the signal SD in the *I^2S-bus specification*.
			O	**TXD3** — Transmitter output for UART3.
P0[26]/AD0[3]/ AOUT/RXD3	6[3]	D3[3]	I/O	**P0[26]** — General purpose digital input/output pin.
			I	**AD0[3]** — A/D converter 0, input 3.
			O	**AOUT** — D/A converter output.
			I	**RXD3** — Receiver input for UART3.
P0[27]/SDA0	25[4]	J2[4]	I/O	**P0[27]** — General purpose digital input/output pin. Output is open-drain.
			I/O	**SDA0** — I^2C0 data input/output. Open-drain output (for I^2C-bus compliance).
P0[28]/SCL0	24[4]	J1[4]	I/O	**P0[28]** — General purpose digital input/output pin. Output is open-drain.
			I/O	**SCL0** — I^2C0 clock input/output. Open-drain output (for I^2C-bus compliance).
P0[29]/USB_D+	29[5]	J3[5]	I/O	**P0[29]** — General purpose digital input/output pin.
			I/O	**USB_D+** — USB bidirectional D+ line. (LPC2364/66/68 only)
P0[30]/USB_D−	30[5]	G4[5]	I/O	**P0[30]** — General purpose digital input/output pin.
			I/O	**USB_D−** — USB bidirectional D− line. (LPC2364/66/68 only)
P1[0] to P1[31]			I/O	**Port 1:** Port 1 is a 32-bit I/O port with individual direction controls for each bit. The operation of Port 1 pins depends upon the pin function selected via the pin connect block. Pins 2, 3, 5, 6, 7, 11, 12, and 13 of this port are not available.

Table 4. Pin description *...continued*

Symbol	Pin	Ball	Type	Description
P1[0]/ ENET_TXD0	95[1]	D5[1]	I/O	**P1[0] —** General purpose digital input/output pin.
			O	**ENET_TXD0 —** Ethernet transmit data 0.
P1[1]/ ENET_TXD1	94[1]	B4[1]	I/O	**P1[1] —** General purpose digital input/output pin.
			O	**ENET_TXD1 —** Ethernet transmit data 1.
P1[4]/ ENET_TX_EN	93[1]	A4[1]	I/O	**P1[4] —** General purpose digital input/output pin.
			O	**ENET_TX_EN —** Ethernet transmit data enable.
P1[8]/ ENET_CRS	92[1]	C5[1]	I/O	**P1[8] —** General purpose digital input/output pin.
			I	**ENET_CRS —** Ethernet carrier sense.
P1[9]/ ENET_RXD0	91[1]	B5[1]	I/O	**P1[9] —** General purpose digital input/output pin.
			I	**ENET_RXD0 —** Ethernet receive data.
P1[10]/ ENET_RXD1	90[1]	A5[1]	I/O	**P1[10] —** General purpose digital input/output pin.
			I	**ENET_RXD1 —** Ethernet receive data.
P1[14]/ ENET_RX_ER	89[1]	D6[1]	I/O	**P1[14] —** General purpose digital input/output pin.
			I	**ENET_RX_ER —** Ethernet receive error.
P1[15]/ ENET_REF_CLK	88[1]	C6[1]	I/O	**P1[15] —** General purpose digital input/output pin.
			I	**ENET_REF_CLK —** Ethernet reference clock.
P1[16]/ ENET_MDC	87[1]	A6[1]	I/O	**P1[16] —** General purpose digital input/output pin.
			O	**ENET_MDC —** Ethernet MIIM clock.
P1[17]/ ENET_MDIO	86[1]	B6[1]	I/O	**P1[17] —** General purpose digital input/output pin.
			I/O	**ENET_MDIO —** Ethernet MIIM data input and output.
P1[18]/ USB_UP_LED/ PWM1[1]/ CAP1[0]	32[1]	H4[1]	I/O	**P1[18] —** General purpose digital input/output pin.
			O	**USB_UP_LED —** USB GoodLink LED indicator. It is LOW when device is configured (non-control endpoints enabled), or when host is enabled and has detected a device on the bus. It is HIGH when the device is not configured, or when host is enabled and has not detected a device on the bus, or during global suspend. It transitions between LOW and HIGH (flashes) when host is enabled and detects activity on the bus. (LPC2364/66/68 only)
			O	**PWM1[1] —** Pulse Width Modulator 1, channel 1 output.
			I	**CAP1[0] —** Capture input for Timer 1, channel 0.
P1[19]/CAP1[1]	33[1]	J4[1]	I/O	**P1[19] —** General purpose digital input/output pin.
			I	**CAP1[1] —** Capture input for Timer 1, channel 1.
P1[20]/PWM1[2]/ SCK0	34[1]	K4[1]	I/O	**P1[20] —** General purpose digital input/output pin.
			O	**PWM1[2] —** Pulse Width Modulator 1, channel 2 output.
			I/O	**SCK0 —** Serial clock for SSP0.
P1[21]/PWM1[3]/ SSEL0	35[1]	F5[1]	I/O	**P1[21] —** General purpose digital input/output pin.
			O	**PWM1[3] —** Pulse Width Modulator 1, channel 3 output.
			I/O	**SSEL0 —** Slave Select for SSP0.
P1[22]/MAT1[0]	36[1]	J5[1]	I/O	**P1[22] —** General purpose digital input/output pin.
			O	**MAT1[0] —** Match output for Timer 1, channel 0.

Table 4. Pin description *...continued*

Symbol	Pin	Ball	Type	Description
P1[23]/PWM1[4]/ MISO0	37[1]	K5[1]	I/O	**P1[23]** — General purpose digital input/output pin.
			O	**PWM1[4]** — Pulse Width Modulator 1, channel 4 output.
			I/O	**MISO0** — Master In Slave Out for SSP0.
P1[24]/PWM1[5]/ MOSI0	38[1]	H5[1]	I/O	**P1[24]** — General purpose digital input/output pin.
			O	**PWM1[5]** — Pulse Width Modulator 1, channel 5 output.
			I/O	**MOSI0** — Master Out Slave in for SSP0.
P1[25]/MAT1[1]	39[1]	G5[1]	I/O	**P1[25]** — General purpose digital input/output pin.
			O	**MAT1[1]** — Match output for Timer 1, channel 1.
P1[26]/PWM1[6]/ CAP0[0]	40[1]	K6[1]	I/O	**P1[26]** — General purpose digital input/output pin.
			O	**PWM1[6]** — Pulse Width Modulator 1, channel 6 output.
			I	**CAP0[0]** — Capture input for Timer 0, channel 0.
P1[27]/CAP0[1]	43[1]	K7[1]	I/O	**P1[27]** — General purpose digital input/output pin.
			I	**CAP0[1]** — Capture input for Timer 0, channel 1.
P1[28]/ PCAP1[0]/ MAT0[0]	44[1]	J7[1]	I/O	**P1[28]** — General purpose digital input/output pin.
			I	**PCAP1[0]** — Capture input for PWM1, channel 0.
			O	**MAT0[0]** — Match output for Timer 0, channel 0.
P1[29]/ PCAP1[1]/ MAT0[1]	45[1]	G6[1]	I/O	**P1[29]** — General purpose digital input/output pin.
			I	**PCAP1[1]** — Capture input for PWM1, channel 1.
			O	**MAT0[1]** — Match output for Timer 0, channel 0.
P1[30]/V_{BUS}/ AD0[4]	21[2]	H1[2]	I/O	**P1[30]** — General purpose digital input/output pin.
			I	**V_{BUS}** — Monitors the presence of USB bus power. (LPC2364/66/68 only) **Note:** This signal must be HIGH for USB reset to occur.
			I	**AD0[4]** — A/D converter 0, input 4.
P1[31]/SCK1/ AD0[5]	20[2]	F4[2]	I/O	**P1[31]** — General purpose digital input/output pin.
			I/O	**SCK1** — Serial Clock for SSP1.
			I	**AD0[5]** — A/D converter 0, input 5.
P2[0] to P2[31]			I/O	**Port 2:** Port 2 is a 32-bit I/O port with individual direction controls for each bit. The operation of Port 2 pins depends upon the pin function selected via the pin connect block. Pins 14 through 31 of this port are not available.
P2[0]/PWM1[1]/ TXD1/ TRACECLK	75[1]	B9[1]	I/O	**P2[0]** — General purpose digital input/output pin.
			O	**PWM1[1]** — Pulse Width Modulator 1, channel 1 output.
			O	**TXD1** — Transmitter output for UART1.
			O	**TRACECLK** — Trace Clock.
P2[1]/PWM1[2]/ RXD1/ PIPESTAT0	74[1]	B10[1]	I/O	**P2[1]** — General purpose digital input/output pin.
			O	**PWM1[2]** — Pulse Width Modulator 1, channel 2 output.
			I	**RXD1** — Receiver input for UART1.
			O	**PIPESTAT0** — Pipeline Status, bit 0.
P2[2]/PWM1[3]/ CTS1/ PIPESTAT1	73[1]	D8[1]	I/O	**P2[2]** — General purpose digital input/output pin.
			O	**PWM1[3]** — Pulse Width Modulator 1, channel 3 output.
			I	**CTS1** — Clear to Send input for UART1.
			O	**PIPESTAT1** — Pipeline Status, bit 1.

Table 4. Pin description *...continued*

Symbol	Pin	Ball	Type	Description
P2[3]/PWM1[4]/ DCD1/ PIPESTAT2	70[1]	E7[1]	I/O	**P2[3]** — General purpose digital input/output pin.
			O	**PWM1[4]** — Pulse Width Modulator 1, channel 4 output.
			I	**DCD1** — Data Carrier Detect input for UART1.
			O	**PIPESTAT2** — Pipeline Status, bit 2.
P2[4]/PWM1[5]/ DSR1/ TRACESYNC	69[1]	D9[1]	I/O	**P2[4]** — General purpose digital input/output pin.
			O	**PWM1[5]** — Pulse Width Modulator 1, channel 5 output.
			I	**DSR1** — Data Set Ready input for UART1.
			O	**TRACESYNC** — Trace Synchronization.
P2[5]/PWM1[6]/ DTR1/ TRACEPKT0	68[1]	D10[1]	I/O	**P2[5]** — General purpose digital input/output pin.
			O	**PWM1[6]** — Pulse Width Modulator 1, channel 6 output.
			O	**DTR1** — Data Terminal Ready output for UART1.
			O	**TRACEPKT0** — Trace Packet, bit 0.
P2[6]/PCAP1[0]/ RI1/ TRACEPKT1	67[1]	E8[1]	I/O	**P2[6]** — General purpose digital input/output pin.
			I	**PCAP1[0]** — Capture input for PWM1, channel 0.
			I	**RI1** — Ring Indicator input for UART1.
			O	**TRACEPKT1** — Trace Packet, bit 1.
P2[7]/RD2/ RTS1/ TRACEPKT2	66[1]	E9[1]	I/O	**P2[7]** — General purpose digital input/output pin.
			I	**RD2** — CAN2 receiver input. (LPC2364/66/68 only)
			O	**RTS1** — Request to Send output for UART1.
			O	**TRACEPKT2** — Trace Packet, bit 2.
P2[8]/TD2/ TXD2/ TRACEPKT3	65[1]	E10[1]	I/O	**P2[8]** — General purpose digital input/output pin.
			O	**TD2** — CAN2 transmitter output. (LPC2364/66/68 only)
			O	**TXD2** — Transmitter output for UART2.
			O	**TRACEPKT3** — Trace Packet, bit 3.
P2[9]/ USB_CONNECT/ RXD2/EXTIN0	64[1]	F7[1]	I/O	**P2[9]** — General purpose digital input/output pin.
			O	**USB_CONNECT** — Signal used to switch an external 1.5 kΩ resistor under software control. Used with the SoftConnect USB feature. (LPC2364/66/68 only)
			I	**RXD2** — Receiver input for UART2.
			I	**EXTIN0** — External Trigger Input.
P2[10]/$\overline{\text{EINT0}}$	53[6]	J10[6]	I/O	**P2[10]** — General purpose digital input/output pin. **Note:** LOW on this pin while $\overline{\text{RESET}}$ is LOW forces on-chip bootloader to take over control of the part after a reset.
			I	**$\overline{\text{EINT0}}$** — External interrupt 0 input.
P2[11]/$\overline{\text{EINT1}}$/ MCIDAT1/ I2STX_CLK	52[6]	H8[6]	I/O	**P2[11]** — General purpose digital input/output pin.
			I	**$\overline{\text{EINT1}}$** — External interrupt 1 input.
			O	**MCIDAT1** — Data line for SD/MMC interface. (LPC2367/68 only)
			I/O	**I2STX_CLK** — Transmit Clock. It is driven by the master and received by the slave. Corresponds to the signal SCK in the *I^2S-bus specification*.

Table 4. Pin description *...continued*

Symbol	Pin	Ball	Type	Description
P2[12]/$\overline{\text{EINT2}}$/ MCIDAT2/ I2STX_WS	51[6]	K10[6]	I/O	**P2[12]** — General purpose digital input/output pin.
			I	**$\overline{\text{EINT2}}$** — External interrupt 2 input.
			O	**MCIDAT2** — Data line for SD/MMC interface. (LPC2367/68 only)
			I/O	**I2STX_WS** — Transmit Word Select. It is driven by the master and received by the slave. Corresponds to the signal WS in the *I^2S-bus specification*.
P2[13]/$\overline{\text{EINT3}}$/ MCIDAT3/ I2STX_SDA	50[6]	J9[6]	I/O	**P2[13]** — General purpose digital input/output pin.
			I	**$\overline{\text{EINT3}}$** — External interrupt 3 input.
			O	**MCIDAT3** — Data line for SD/MMC interface. (LPC2367/68 only)
			I/O	**I2STX_SDA** — Transmit data. It is driven by the transmitter and read by the receiver. Corresponds to the signal SD in the *I^2S-bus specification*.
P3[0] to P3[31]			I/O	**Port 3:** Port 3 is a 32-bit I/O port with individual direction controls for each bit. The operation of Port 3 pins depends upon the pin function selected via the pin connect block. Pins 0 through 24, and 27 through 31 of this port are not available.
P3[25]/MAT0[0]/ PWM1[2]	27[1]	H3[1]	I/O	**P3[25]** — General purpose digital input/output pin.
			O	**MAT0[0]** — Match output for Timer 0, channel 0.
			O	**PWM1[2]** — Pulse Width Modulator 1, output 2.
P3[26]/MAT0[1]/ PWM1[3]	26[1]	K1[1]	I/O	**P3[26]** — General purpose digital input/output pin.
			O	**MAT0[1]** — Match output for Timer 0, channel 1.
			O	**PWM1[3]** — Pulse Width Modulator 1, output 3.
P4[0] to P4[31]			I/O	**Port 4:** Port 4 is a 32-bit I/O port with individual direction controls for each bit. The operation of Port 4 pins depends upon the pin function selected via the pin connect block. Pins 0 through 27, 30, and 31 of this port are not available.
P4[28]/MAT2[0]/ TXD3	82[1]	C7[1]	I/O	**P4[28]** — General purpose digital input/output pin.
			O	**MAT2[0]** — Match output for Timer 2, channel 0.
			O	**TXD3** — Transmitter output for UART3.
P4[29]/MAT2[1]/ RXD3	85[1]	E6[1]	I/O	**P4[29]** — General purpose digital input/output pin.
			O	**MAT2[1]** — Match output for Timer 2, channel 1.
			I	**RXD3** — Receiver input for UART3.
DBGEN	-	D4[1][8]	I	**DBGEN** — JTAG interface control signal. Also used for boundary scanning. **Note:** This pin is available in LPC2364FET100 and LPC2368FET100 devices only (TFBGA package).
TDO	1[1][7]	A1[1][7]	O	**TDO** — Test Data out for JTAG interface.
TDI	2[1][8]	C3[1][8]	I	**TDI** — Test Data in for JTAG interface.
TMS	3[1][8]	B1[1][8]	I	**TMS** — Test Mode Select for JTAG interface.
$\overline{\text{TRST}}$	4[1][8]	C2[1][8]	I	**$\overline{\text{TRST}}$** — Test Reset for JTAG interface.
TCK	5[1][7]	C1[1][7]	I	**TCK** — Test Clock for JTAG interface. This clock must be slower than $\frac{1}{6}$ of the CPU clock (CCLK) for the JTAG interface to operate
RTCK	100[1][8]	B2[1][8]	I/O	**RTCK** — JTAG interface control signal. **Note:** LOW on this pin while $\overline{\text{RESET}}$ is LOW enables ETM pins (P2[9:0]) to operate as trace port after reset.

Table 4. Pin description *...continued*

Symbol	Pin	Ball	Type	Description
$\overline{\text{RSTOUT}}$	14	-	O	**$\overline{\text{RSTOUT}}$ —** This is a 3.3 V pin. LOW on this pin indicates LPC2364/65/66/67/68 being in Reset state. **Note:** This pin is available in LPC2364FBD100, LPC2365FBD100, LPC2366FBD100, LPC2367FBD100, and LPC2368FBD100 devices only (LQFP100 package).
$\overline{\text{RESET}}$	17[9]	F3[9]	I	**External reset input:** A LOW on this pin resets the device, causing I/O ports and peripherals to take on their default states, and processor execution to begin at address 0. TTL with hysteresis, 5 V tolerant.
XTAL1	22[10][11]	H2[10][11]	I	Input to the oscillator circuit and internal clock generator circuits.
XTAL2	23[10][11]	G3[10][11]	O	Output from the oscillator amplifier.
RTCX1	16[10][12]	F2[10][12]	I	Input to the RTC oscillator circuit.
RTCX2	18[10]	G1[10]	O	Output from the RTC oscillator circuit.
V_{SS}	15, 31, 41, 55, 72, 97, 83[13]	B3, B7, C9, F1, G7, J6, K3 [13]	I	**ground:** 0 V reference.
V_{SSA}	11[14]	E1[14]	I	**analog ground:** 0 V reference. This should nominally be the same voltage as V_{SS}, but should be isolated to minimize noise and error.
$V_{DD(3V3)}$	28, 54, 71, 96[15]	A3, C10, H9, K2[15]	I	**3.3 V supply voltage:** This is the power supply voltage for the I/O ports.
$V_{DD(DCDC)(3V3)}$	13, 42, 84[16]	A7, E4, H6[16]	I	**3.3 V DC-to-DC converter supply voltage:** This is the supply voltage for the on-chip DC-to-DC converter only.
V_{DDA}	10[17]	E2[17]	I	**analog 3.3 V pad supply voltage:** This should be nominally the same voltage as $V_{DD(3V3)}$ but should be isolated to minimize noise and error. This voltage is used to power the ADC and DAC.
VREF	12[17]	E3[17]	I	**ADC reference:** This should be nominally the same voltage as $V_{DD(3V3)}$ but should be isolated to minimize noise and error. Level on this pin is used as a reference for ADC and DAC.
VBAT	19[17]	G2[17]	I	**RTC pin power supply:** 3.3 V on this pin supplies the power to the RTC peripheral.

[1] 5 V tolerant pad providing digital I/O functions with TTL levels and hysteresis.

[2] 5 V tolerant pad providing digital I/O functions (with TTL levels and hysteresis) and analog input. When configured as a DAC input, digital section of the pad is disabled.

[3] 5 V tolerant pad providing digital I/O with TTL levels and hysteresis and analog output function. When configured as the DAC output, digital section of the pad is disabled.

[4] Open-drain 5 V tolerant digital I/O pad, compatible with I^2C-bus 400 kHz specification. This pad requires an external pull-up to provide output functionality. When power is switched off, this pin connected to the I^2C-bus is floating and does not disturb the I^2C lines. Open-drain configuration applies to all functions on this pin.

[5] Pad provides digital I/O and USB functions (LPC2364/66/68 only). It is designed in accordance with the *USB specification, revision 2.0* (Full-speed and Low-speed mode only).

[6] 5 V tolerant pad with 10 ns glitch filter providing digital I/O functions with TTL levels and hysteresis.

[7] This pin has no built-in pull-up and no built-in pull-down resistor.

[8] This pin has a built-in pull-up resistor.

[9] 5 V tolerant pad with 20 ns glitch filter providing digital I/O function with TTL levels and hysteresis.

[10] Pad provides special analog functionality.

[11] When the main oscillator is not used, connect XTAL1 and XTAL2 as follows: XTAL1 can be left floating or can be grounded (grounding is preferred to reduce susceptibility to noise). XTAL2 should be left floating.

[12] If the RTC is not used, these pins can be left floating.

[13] Pad provides special analog functionality.

[14] Pad provides special analog functionality.

[15] Pad provides special analog functionality.

[16] Pad provides special analog functionality.

[17] Pad provides special analog functionality.

7. Functional description

7.1 Architectural overview

The LPC2364/65/66/67/68 microcontroller consists of an ARM7TDMI-S CPU with emulation support, the ARM7 local bus for closely coupled, high-speed access to the majority of on-chip memory, the AMBA AHB interfacing to high-speed on-chip peripherals, and the AMBA APB for connection to other on-chip peripheral functions. The microcontroller permanently configures the ARM7TDMI-S processor for little-endian byte order.

The LPC2364/65/66/67/68 implements two AHB in order to allow the Ethernet block to operate without interference caused by other system activity. The primary AHB, referred to as AHB1, includes the VIC and GPDMA controller.

The second AHB, referred to as AHB2, includes only the Ethernet block and an associated 16 kB SRAM. In addition, a bus bridge is provided that allows the secondary AHB to be a bus master on AHB1, allowing expansion of Ethernet buffer space into off-chip memory or unused space in memory residing on AHB1.

In summary, bus masters with access to AHB1 are the ARM7 itself, the GPDMA function, and the Ethernet block (via the bus bridge from AHB2). Bus masters with access to AHB2 are the ARM7 and the Ethernet block.

AHB peripherals are allocated a 2 MB range of addresses at the very top of the 4 GB ARM memory space. Each AHB peripheral is allocated a 16 kB address space within the AHB address space. Lower speed peripheral functions are connected to the APB. The AHB to APB bridge interfaces the APB to the AHB. APB peripherals are also allocated a 2 MB range of addresses, beginning at the 3.5 GB address point. Each APB peripheral is allocated a 16 kB address space within the APB address space.

The ARM7TDMI-S processor is a general purpose 32-bit microprocessor, which offers high performance and very low power consumption. The ARM architecture is based on Reduced Instruction Set Computer (RISC) principles, and the instruction set and related decode mechanism are much simpler than those of microprogrammed complex instruction set computers. This simplicity results in a high instruction throughput and impressive real-time interrupt response from a small and cost-effective processor core.

Pipeline techniques are employed so that all parts of the processing and memory systems can operate continuously. Typically, while one instruction is being executed, its successor is being decoded, and a third instruction is being fetched from memory.

The ARM7TDMI-S processor also employs a unique architectural strategy known as Thumb, which makes it ideally suited to high-volume applications with memory restrictions, or applications where code density is an issue.

The key idea behind Thumb is that of a super-reduced instruction set. Essentially, the ARM7TDMI-S processor has two instruction sets:

- The standard 32-bit ARM set
- A 16-bit Thumb set

The Thumb set's 16-bit instruction length allows it to approach twice the density of standard ARM code while retaining most of the ARM's performance advantage over a traditional 16-bit processor using 16-bit registers. This is possible because Thumb code operates on the same 32-bit register set as ARM code.

Thumb code is able to provide up to 65 % of the code size of ARM, and 160 % of the performance of an equivalent ARM processor connected to a 16-bit memory system.

7.2 On-chip flash programming memory

The LPC2364/65/66/67/68 incorporate a 128 kB, 256 kB, and 512 kB flash memory system respectively. This memory may be used for both code and data storage. Programming of the flash memory may be accomplished in several ways. It may be programmed In System via the serial port (UART0). The application program may also erase and/or program the flash while the application is running, allowing a great degree of flexibility for data storage field and firmware upgrades.

The flash memory is 128 bits wide and includes pre-fetching and buffering techniques to allow it to operate at SRAM speeds of 72 MHz. LPC2364HBD flash operates up to 72 MHz from −40 °C to +85 °C, up to 60 MHz from 85 °C to 125 °C.

7.3 On-chip SRAM

The LPC2364/65/66/67/68 include SRAM memory of 8 kB or 32 kB, reserved for the ARM processor exclusive use. This RAM may be used for code and/or data storage and may be accessed as 8 bits, 16 bits, and 32 bits.

A 16 kB SRAM block serving as a buffer for the Ethernet controller and an 8 kB SRAM used by the GPDMA controller or the USB device can be used both for data and code storage. The 2 kB RTC SRAM can be used for data storage only. The RTC SRAM is battery powered and retains the content in the absence of the main power supply.

7.4 Memory map

The LPC2364/65/66/67/68 memory map incorporates several distinct regions as shown in Figure 4.

In addition, the CPU interrupt vectors may be remapped to allow them to reside in either flash memory (default), boot ROM, or SRAM (see Section 7.25.6).

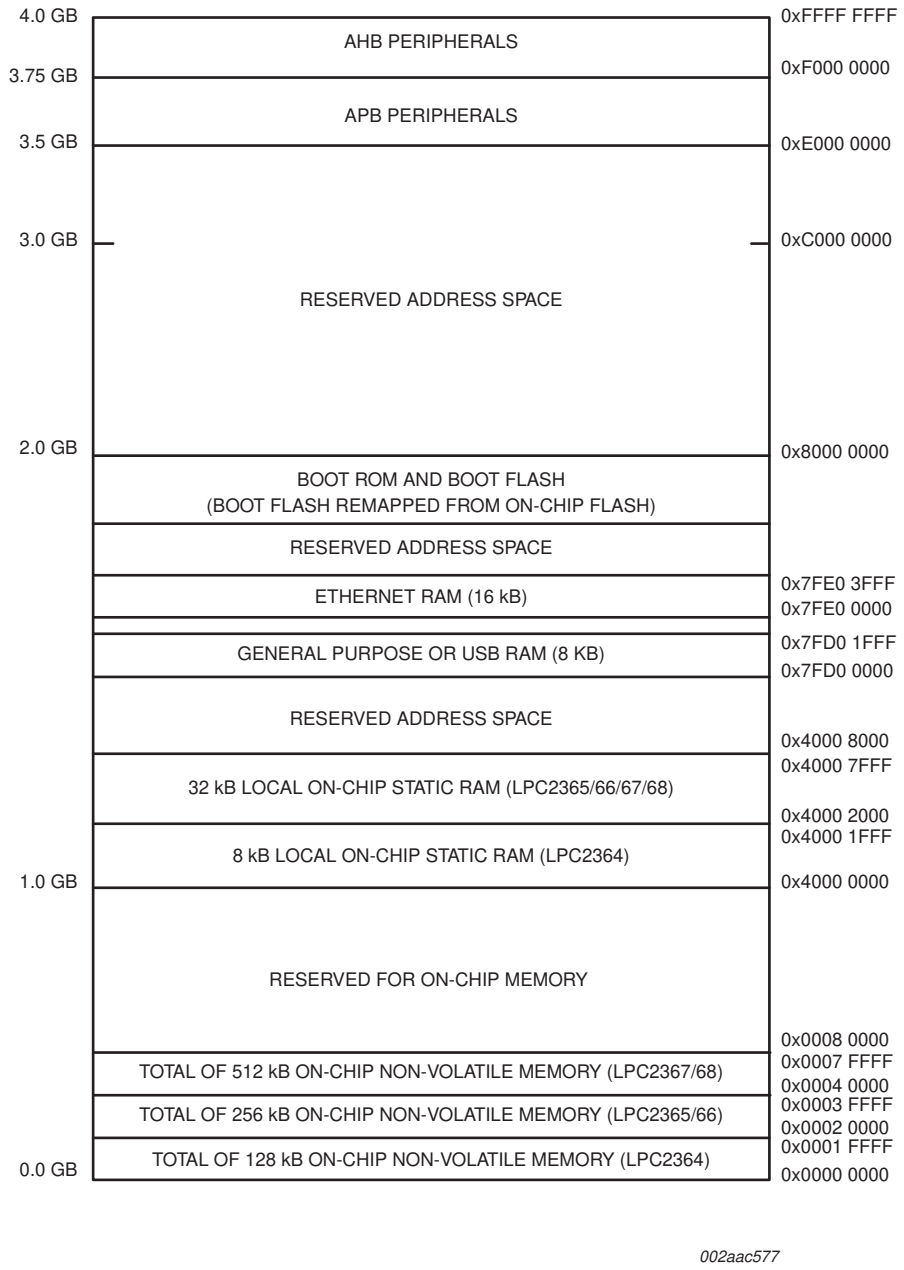


Fig 4. LPC2364/65/66/67/68 memory map

7.5 Interrupt controller

The ARM processor core has two interrupt inputs called Interrupt Request (IRQ) and Fast Interrupt Request (FIQ). The VIC takes 32 interrupt request inputs which can be programmed as FIQ or vectored IRQ types. The programmable assignment scheme means that priorities of interrupts from the various peripherals can be dynamically assigned and adjusted.

FIQs have the highest priority. If more than one request is assigned to FIQ, the VIC ORs the requests to produce the FIQ signal to the ARM processor. The fastest possible FIQ latency is achieved when only one request is classified as FIQ, because then the FIQ service routine can simply start dealing with that device. But if more than one request is assigned to the FIQ class, the FIQ service routine can read a word from the VIC that identifies which FIQ source(s) is (are) requesting an interrupt.

Vectored IRQs, which include all interrupt requests that are not classified as FIQs, have a programmable interrupt priority. When more than one interrupt is assigned the same priority and occur simultaneously, the one connected to the lowest numbered VIC channel will be serviced first.

The VIC ORs the requests from all of the vectored IRQs to produce the IRQ signal to the ARM processor. The IRQ service routine can start by reading a register from the VIC and jumping to the address supplied by that register.

7.5.1 Interrupt sources

Each peripheral device has one interrupt line connected to the VIC but may have several interrupt flags. Individual interrupt flags may also represent more than one interrupt source.

Any pin on Port 0 and Port 2 (total of 42 pins) regardless of the selected function, can be programmed to generate an interrupt on a rising edge, a falling edge, or both. Such interrupt request coming from Port 0 and/or Port 2 will be combined with the $\overline{\text{EINT3}}$ interrupt requests.

7.6 Pin connect block

The pin connect block allows selected pins of the microcontroller to have more than one function. Configuration registers control the multiplexers to allow connection between the pin and the on chip peripherals.

Peripherals should be connected to the appropriate pins prior to being activated and prior to any related interrupt(s) being enabled. Activity of any enabled peripheral function that is not mapped to a related pin should be considered undefined.

7.7 General purpose DMA controller

The GPDMA is an AMBA AHB compliant peripheral allowing selected LPC2364/65/66/67/68 peripherals to have DMA support.

The GPDMA enables peripheral-to-memory, memory-to-peripheral, peripheral-to-peripheral, and memory-to-memory transactions. Each DMA stream provides unidirectional serial DMA transfers for a single source and destination. For example, a bidirectional port requires one stream for transmit and one for receive. The source and destination areas can each be either a memory region or a peripheral, and can be accessed through the AHB master.

7.7.1 Features

- Two DMA channels. Each channel can support a unidirectional transfer.
- The GPDMA can transfer data between the 8 kB SRAM and peripherals such as the SD/MMC, two SSP, and I^2S interfaces.

- Single DMA and burst DMA request signals. Each peripheral connected to the GPDMA can assert either a burst DMA request or a single DMA request. The DMA burst size is set by programming the GPDMA.
- Memory-to-memory, memory-to-peripheral, peripheral-to-memory, and peripheral-to-peripheral transfers.
- Scatter or gather DMA is supported through the use of linked lists. This means that the source and destination areas do not have to occupy contiguous areas of memory.
- Hardware DMA channel priority. Each DMA channel has a specific hardware priority. DMA channel 0 has the highest priority and channel 1 has the lowest priority. If requests from two channels become active at the same time the channel with the highest priority is serviced first.
- AHB slave DMA programming interface. The GPDMA is programmed by writing to the DMA control registers over the AHB slave interface.
- One AHB master for transferring data. This interface transfers data when a DMA request goes active.
- 32-bit AHB master bus width.
- Incrementing or non-incrementing addressing for source and destination.
- Programmable DMA burst size. The DMA burst size can be programmed to more efficiently transfer data. Usually the burst size is set to half the size of the FIFO in the peripheral.
- Internal four-word FIFO per channel.
- Supports 8-bit, 16-bit, and 32-bit wide transactions.
- An interrupt to the processor can be generated on a DMA completion or when a DMA error has occurred.
- Interrupt masking. The DMA error and DMA terminal count interrupt requests can be masked.
- Raw interrupt status. The DMA error and DMA count raw interrupt status can be read prior to masking.

7.8 Fast general purpose parallel I/O

Device pins that are not connected to a specific peripheral function are controlled by the GPIO registers. Pins may be dynamically configured as inputs or outputs. Separate registers allow setting or clearing any number of outputs simultaneously. The value of the output register may be read back as well as the current state of the port pins.

LPC2364/65/66/67/68 use accelerated GPIO functions:

- GPIO registers are relocated to the ARM local bus so that the fastest possible I/O timing can be achieved.
- Mask registers allow treating sets of port bits as a group, leaving other bits unchanged.
- All GPIO registers are byte and half-word addressable.
- Entire port value can be written in one instruction.

Additionally, any pin on Port 0 and Port 2 (total of 42 pins) providing a digital function can be programmed to generate an interrupt on a rising edge, a falling edge, or both. The edge detection is asynchronous, so it may operate when clocks are not present such as during Power-down mode. Each enabled interrupt can be used to wake up the chip from Power-down mode.

7.8.1 Features

- Bit level set and clear registers allow a single instruction to set or clear any number of bits in one port.
- Direction control of individual bits.
- All I/O default to inputs after reset.
- Backward compatibility with other earlier devices is maintained with legacy Port 0 and Port 1 registers appearing at the original addresses on the APB.

7.9 Ethernet

The Ethernet block contains a full featured 10 Mbit/s or 100 Mbit/s Ethernet MAC designed to provide optimized performance through the use of DMA hardware acceleration. Features include a generous suite of control registers, half or full duplex operation, flow control, control frames, hardware acceleration for transmit retry, receive packet filtering and wake-up on LAN activity. Automatic frame transmission and reception with scatter-gather DMA off-loads many operations from the CPU.

The Ethernet block and the CPU share a dedicated AHB subsystem that is used to access the Ethernet SRAM for Ethernet data, control, and status information. All other AHB traffic in the LPC2364/65/66/67/68 takes place on a different AHB subsystem, effectively separating Ethernet activity from the rest of the system. The Ethernet DMA can also access the USB SRAM if it is not being used by the USB block.

The Ethernet block interfaces between an off-chip Ethernet PHY using the Reduced MII (RMII) protocol and the on-chip Media Independent Interface Management (MIIM) serial bus.

7.9.1 Features

- Ethernet standards support:
  - Supports 10 Mbit/s or 100 Mbit/s PHY devices including 10 Base-T, 100 Base-TX, 100 Base-FX, and 100 Base-T4.
  - Fully compliant with *IEEE standard 802.3*.
  - Fully compliant with 802.3x full duplex flow control and half duplex back pressure.
  - Flexible transmit and receive frame options.
  - Virtual Local Area Network (VLAN) frame support.
- Memory management:
  - Independent transmit and receive buffers memory mapped to shared SRAM.
  - DMA managers with scatter/gather DMA and arrays of frame descriptors.
  - Memory traffic optimized by buffering and pre-fetching.
- Enhanced Ethernet features:

- Receive filtering.
- Multicast and broadcast frame support for both transmit and receive.
- Optional automatic Frame Check Sequence (FCS) insertion with Circular Redundancy Check (CRC) for transmit.
- Selectable automatic transmit frame padding.
- Over-length frame support for both transmit and receive allows any length frames.
- Promiscuous receive mode.
- Automatic collision back-off and frame retransmission.
- Includes power management by clock switching.
- Wake-on-LAN power management support allows system wake-up: using the receive filters or a magic frame detection filter.

- Physical interface:
  - Attachment of external PHY chip through standard RMII interface.
  - PHY register access is available via the MIIM interface.

7.10 USB interface (LPC2364/66/68 only)

The Universal Serial Bus (USB) is a 4-wire bus that supports communication between a host and a number (127 maximum) of peripherals. The host controller allocates the USB bandwidth to attached devices through a token based protocol. The bus supports hot plugging, unplugging, and dynamic configuration of the devices. All transactions are initiated by the host controller.

7.10.1 USB device controller

The device controller enables 12 Mbit/s data exchange with a USB host controller. It consists of register interface, serial interface engine, endpoint buffer memory, and the DMA controller. The serial interface engine decodes the USB data stream and writes data to the appropriate end point buffer memory. The status of a completed USB transfer or error condition is indicated via status registers. An interrupt is also generated if enabled. The DMA controller when enabled transfers data between the endpoint buffer and the USB RAM.

7.10.2 Features

- Fully compliant with *USB 2.0 specification* (full speed).
- Supports 32 physical (16 logical) endpoints with a 4 kB USB endpoint buffer RAM.
- Supports Control, Bulk, Interrupt and Isochronous endpoints.
- Scalable realization of endpoints at run time.
- Endpoint Maximum packet size selection (up to USB maximum specification) by software at run time.
- Supports SoftConnect and GoodLink features.
- While USB is in the Suspend mode, LPC2364/65/66/67/68 can enter one of the reduced power modes and wake up on a USB activity.
- Supports DMA transfers with the DMA RAM of 8 kB on all non-control endpoints.
- Allows dynamic switching between CPU-controlled and DMA modes.

- Double buffer implementation for Bulk and Isochronous endpoints.

7.11 CAN controller and acceptance filters (LPC2364/66/68 only)

The Controller Area Network (CAN) is a serial communications protocol which efficiently supports distributed real-time control with a very high level of security. Its domain of application ranges from high-speed networks to low cost multiplex wiring.

The CAN block is intended to support multiple CAN buses simultaneously, allowing the device to be used as a gateway, switch, or router among a number of CAN buses in industrial or automotive applications.

Each CAN controller has a register structure similar to the NXP SJA1000 and the PeliCAN Library block, but the 8-bit registers of those devices have been combined in 32-bit words to allow simultaneous access in the ARM environment. The main operational difference is that the recognition of received Identifiers, known in CAN terminology as Acceptance Filtering, has been removed from the CAN controllers and centralized in a global Acceptance Filter.

7.11.1 Features

- Two CAN controllers and buses.
- Data rates to 1 Mbit/s on each bus.
- 32-bit register and RAM access.
- Compatible with *CAN specification 2.0B, ISO 11898-1*.
- Global Acceptance Filter recognizes 11-bit and 29-bit receive identifiers for all CAN buses.
- Acceptance Filter can provide FullCAN-style automatic reception for selected Standard Identifiers.
- FullCAN messages can generate interrupts.

7.12 10-bit ADC

The LPC2364/65/66/67/68 contain one ADC. It is a single 10-bit successive approximation ADC with six channels.

7.12.1 Features

- 10-bit successive approximation ADC.
- Input multiplexing among 6 pins.
- Power-down mode.
- Measurement range 0 V to $V_{i(VREF)}$.
- 10-bit conversion time $\geq$ 2.44 μs.
- Burst conversion mode for single or multiple inputs.
- Optional conversion on transition of input pin or Timer Match signal.
- Individual result registers for each ADC channel to reduce interrupt overhead.