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LPC3141/3143

Low-cost, low-power ARM926EJ microcontrollers with USB High-speed OTG, SD/MMC, and NAND flash controller

1. General description

The NXP LPC3141/3143 combine a 270 MHz ARM926EJ-S CPU core, High-speed USB 2.0 OTG, 192 KB SRAM, NAND flash controller, flexible external bus interface, four channel 10-bit A/D, and a myriad of serial and parallel interfaces in a single chip targeted at consumer, industrial, medical, and communication markets. To optimize system power consumption, the LPC3141/3143 have multiple power domains and a very flexible Clock Generation Unit (CGU) that provides dynamic clock gating and scaling.

2. Features and benefits

2.1 Key features

- CPU platform
  - 270 MHz, 32-bit ARM926EJ-S
  - 16 kB D-cache and 16 kB I-cache
  - Memory Management Unit (MMU)
- Internal memory
  - 192 kB embedded SRAM
- External memory interface
  - NAND flash controller with 8-bit ECC and AES decryption support (LPC3143 only)
  - 8/16-bit Multi-Port Memory Controller (MPMC): SDRAM and SRAM
- Security
  - AES decryption engine (LPC3143 only)
  - Secure one-time programmable memory for AES key storage and customer use
  - 128 bit unique ID per device for DRM schemes
- Communication and connectivity
  - High-speed USB 2.0 (OTG, Host, Device) with on-chip PHY
  - Two I^2S interfaces
  - Integrated master/slave SPI
  - Two master/slave I^2C-bus interfaces
  - Fast UART
  - Memory Card Interface (MCI): MMC/SD/SDIO/CE-ATA
  - Four-channel 10-bit ADC
  - Integrated 4/8/16-bit 6800/8080 compatible LCD interface
- System functions
  - Dynamic clock gating and scaling
  - Multiple power domains

◆ Selectable boot-up: SPI flash, NAND flash, SD/MMC cards, UART, or USB
◆ On the LPC3143 only: secure booting using an AES decryption engine from SPI flash, NAND flash, SD/MMC cards, UART, or USB.
◆ DMA controller
◆ Four 32-bit timers
◆ Watchdog timer
◆ PWM module
◆ Master/slave PCM interface
◆ Random Number Generator (RNG)
◆ General Purpose I/O pins (GPIO)
◆ Flexible and versatile interrupt structure
◆ JTAG interface with boundary scan and ARM debug access
■ Operating voltage and temperature
◆ Core voltage: 1.2 V
◆ I/O voltages: 1.8 V, 3.3 V
◆ Temperature: −40 °C to +85 °C
■ TFBGA180 package: 12 x 12 mm, 0.8 mm pitch

3. Ordering information

Table 1.   Ordering information

Type number	Package		
	Name	**Description**	**Version**
LPC3141FET180	TFBGA180	Plastic thin fine pitch ball grid array package, 180 balls, body 12 × 12 × 0.8 mm	SOT570-3
LPC3143FET180	TFBGA180	Plastic thin fine pitch ball grid array package, 180 balls, body 12 × 12 × 0.8 mm	SOT570-3

3.1 Ordering options

Table 2.   Ordering options for LPC3141/3143

Type number	Core/bus frequency	Total SRAM	Security engine AES	High-speed USB	10-bit ADC channels	I^{2}S/ I^{2}C	MCI SDHC/ SDIO/ CE-ATA	Temperature range
LPC3141FET180	270/ 90 MHz	192 kB	no	Device/ Host/OTG	4	2 each	yes	−40 °C to +85 °C
LPC3143FET180	270/ 90 MHz	192 kB	yes	Device/ Host/OTG	4	2 each	yes	−40 °C to +85 °C

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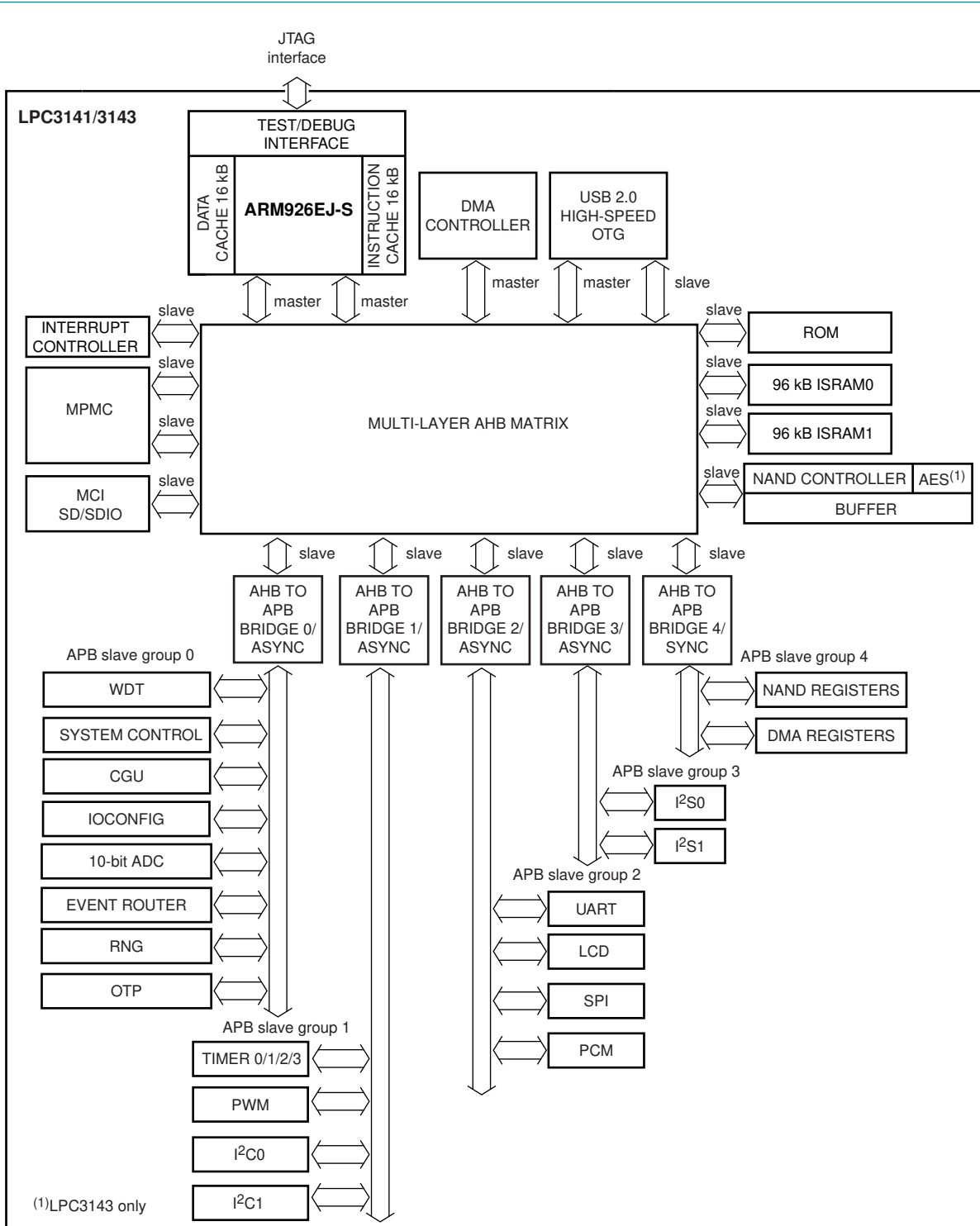
4. Block diagram

Fig 1.   LPC3141/3143 block diagram

5. Pinning information

5.1 Pinning

ball A1 index area

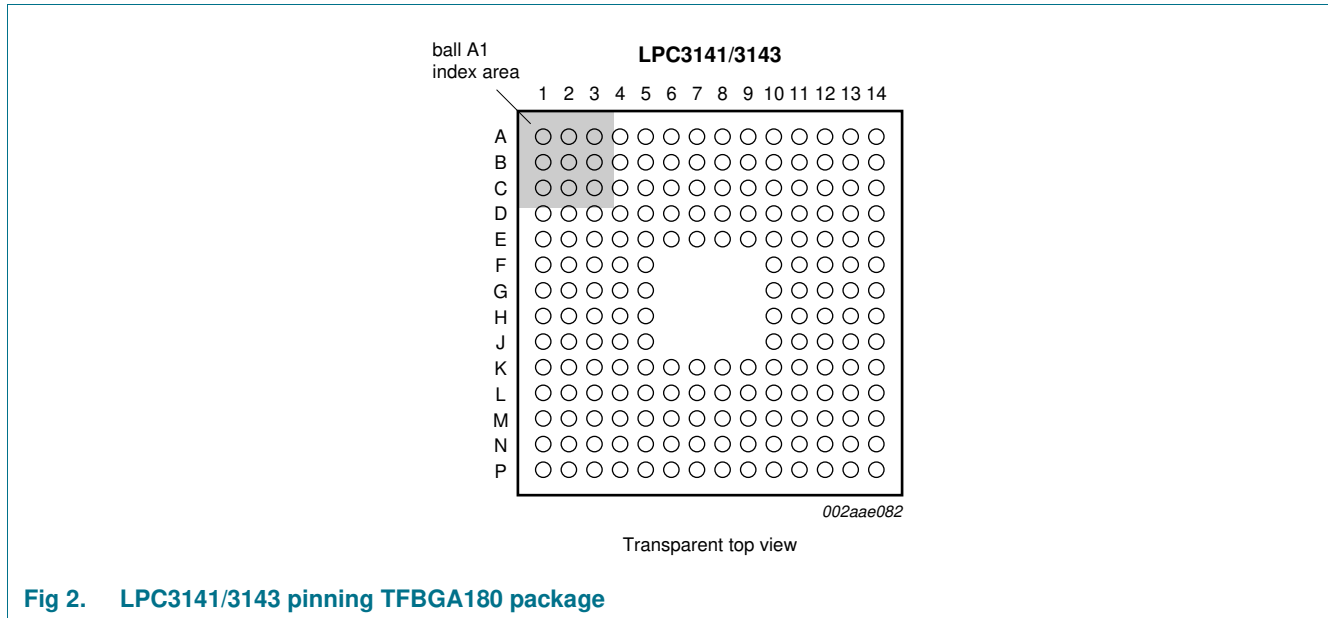**LPC3141/3143**

Transparent top view

002aae082

Fig 2.   LPC3141/3143 pinning TFBGA180 package

Table 3.   Pin allocation table

Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
Row A							
1	EBI_D_10	2	EBI_A_1_CLE	3	EBI_D_9	4	mGPIO10
5	mGPIO7	6	mGPIO6	7	SPI_CS_OUT0	8	SPI_SCK
9	VPP	10	FFAST_IN	11	VSSI	12	ADC10B_GNDA
13	ADC10B_VDDA33	14	ADC10B_GPA1	-	-	-	-
Row B							
1	EBI_D_8	2	VDDE_IOA	3	EBI_A_0_ALE	4	mNAND_RYBN2
5	mGPIO8	6	mGPIO5	7	SPI_MOSI	8	SPI_CS_IN
9	PWM_DATA	10	FFAST_OUT	11	GPIO3	12	VSSE_IOC
13	ADC10B_GPA2	14	ADC10B_GPA0	-	-	-	-
Row C							
1	EBI_D_7	2	EBI_D_11	3	VSSE_IOA	4	VSSE_IOA
5	mGPIO9	6	VDDI	7	VSSI	8	SPI_MISO
9	VPP	10	I2C_SDA0	11	GPIO4	12	VDDI
13	VDDE_IOC	14	ADC10B_GPA3	-	-	-	-
Row D							
1	EBI_D_5	2	EBI_D_6	3	EBI_D_13	4	mNAND_RYBN3
5	VDDE_IOC	6	VSSE_IOC	7	VDDE_IOC	8	VSSE_IOC
9	VSSE_IOC	10	I2C_SCL0	11	VDDA12	12	VSSI
13	BUF_TCK	14	BUF_TMS	-	-	-	-

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Table 3. **Pin allocation table** …*continued*

Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
Row E							
1	EBI_D_3	2	EBI_D_4	3	EBI_D_14	4	VSSE_IOA
5	VDDE_IOA	6	mNAND_RYBN0	7	mNAND_RYBN1	8	VDDE_IOC
9	VSSA12	10	VDDA12	11	ARM_TDO	12	I2C_SDA1
13	I2C_SCL1	14	I2STX_BCK1	-	-	-	-
Row F							
1	EBI_D_2	2	EBI_D_1	3	EBI_D_15	4	VSSE_IOA
5	VDDE_IOA	10	SCAN_TDO	11	BUF_TRST_N	12	I2STX_DATA1
13	I2SRX_WS1	14	I2SRX_BCK1	-	-	-	-
Row G							
1	EBI_NCAS_BLOUT_0	2	EBI_D_0	3	EBI_D_12	4	VSSI
5	VDDE_IOA	10	I2STX_WS1	11	VSSE_IOC	12	VDDE_IOC
13	SYSCLK_O	14	I2SRX_DATA1	-	-	-	-
Row H							
1	EBI_DQM_0_NOE	2	EBI_NRAS_BLOUT_1	3	VDDI	4	VSSE_IOA
5	VDDE_IOA	10	GPIO12	11	GPIO19	12	CLK_256FS_O
13	GPIO11	14	RSTIN_N	-	-	-	-
Row J							
1	NAND_NCS_0	2	EBI_NWE	3	NAND_NCS_1	4	CLOCK_OUT
5	USB_RREF	10	GPIO1	11	GPIO16	12	GPIO13
13	GPIO15	14	GPIO14	-	-	-	-
Row K							
1	NAND_NCS_2	2	NAND_NCS_3	3	VSSE_IOA	4	USB_VSSA_REF
5	mLCD_DB_12	6	mLCD_DB_6	7	mLCD_DB_10	8	mLCD_CSB
9	TDI	10	GPIO0	11	VDDE_IOC	12	GPIO17
13	GPIO20	14	GPIO18	-	-	-	-
Row L							
1	USB_VDDA12_PLL	2	USB_VBUS	3	USB_VSSA_TERM	4	VDDE_IOB
5	mLCD_DB_9	6	VSSI	7	VDDI	8	mLCD_E_RD
9	VSSE_IOC	10	VDDE_IOC	11	VSSI	12	VDDI
13	VSSE_IOC	14	GPIO2	-	-	-	-
Row M							
1	USB_ID	2	USB_VDDA33_DRV	3	VSSE_IOB	4	VSSE_IOB
5	VDDE_IOB	6	VSSE_IOB	7	VDDE_IOB	8	VSSE_IOB
9	VDDE_IOB	10	I2SRX_DATA0	11	mI2STX_WS0	12	mI2STX_BCK0
13	mI2STX_DATA0	14	TCK	-	-	-	-
Row N							
1	USB_GNDA	2	USB_DM	3	mLCD_DB_15	4	mLCD_DB_11
5	mLCD_DB_8	6	mLCD_DB_2	7	mLCD_DB_4	8	mLCD_DB_0
9	mLCD_RW_WR	10	I2SRX_BCK0	11	JTAGSEL	12	UART_TXD
13	mUART_CTS_N	14	mI2STX_CLK0	-	-	-	-

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Table 3.   Pin allocation table ...*continued*

Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
Row P							
1	USB_VDDA33	2	USB_DP	3	mLCD_DB_14	4	mLCD_DB_13
5	mLCD_DB_7	6	mLCD_DB_3	7	mLCD_DB_5	8	mLCD_RS
9	mLCD_DB_1	10	TMS	11	I2SRX_WS0	12	UART_RXD
13	TRST_N	14	mUART_RTS_N	-	-	-	-

Table 4.   Pin description
Pin names with prefix m are multiplexed pins. See Table 10 for pin function selection of multiplexed pins.

Pin name	BGA Ball	Digital I/O level [1]	Application function	Pin state after reset[2]	Cell type [3]	Description
Clock Generation Unit (CGU)						
FFAST_IN	A10	SUP1	AI	-	AIO2	12 MHz oscillator clock input.
FFAST_OUT	B10	SUP1	AO	-	AIO2	12 MHz oscillator clock output.
VDDA12	D11; E10	SUP1	Supply	-	PS3	12 MHz oscillator/PLLs analog supply.
VSSA12	E9	-	Ground	-	CG1	12 MHz oscillator/PLLs analog ground.
RSTIN_N	H14	SUP3	DI	I:PU	DIO2	System Reset Input (active LOW).
CLK_256FS_O	H12	SUP3	DO	O	DIO1	Programmable clock output; fractionally derived from CLK1024FS_BASE clock domain. Generally used for external audio codec master clock.
CLOCK_OUT	J4	SUP4	DO	O	DIO4	Programmable clock output; fractionally derived from SYS_BASE clock domain.
SYSCLK_O[4]	G13	SUP3	DO	O	DIO1	Programmable clock output. Output one of seven base/reference input clocks. No fractional divider.
10-bit ADC						
ADC10B_VDDA33	A13	SUP3	Supply	-	PS3	10-bit ADC analog supply.
ADC10B_GNDA	A12	-	Ground	-	CG1	10-bit ADC analog ground.
ADC10B_GPA0	B14	SUP3	AI	-	AIO1	10-bit ADC analog input.
ADC10B_GPA1	A14	SUP3	AI	-	AIO1	10-bit ADC analog input.
ADC10B_GPA2	B13	SUP3	AI	-	AIO1	10-bit ADC analog input.
ADC10B_GPA3	C14	SUP3	AI	-	AIO1	10-bit ADC analog input.
USB HS 2.0 OTG						
USB_VBUS	L2	SUP5	AI	-	AIO3	USB supply detection line.
USB_ID	M1	SUP3	AI	-	AIO1	Indicates to the USB transceiver whether in device (USB_ID HIGH) or host (USB_ID LOW) mode (contains internal pull-up resistor).
USB_RREF	J5	SUP3	AIO	-	AIO1	USB connection for external reference resistor (12 k$\Omega \pm$ 1%) to analog ground supply.
USB_DP	P2	SUP3	AIO	-	AIO1	USB D+ connection with integrated 45 Ω termination resistor.

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Table 4.   Pin description …continued
Pin names with prefix m are multiplexed pins. See Table 10 for pin function selection of multiplexed pins.

Pin name	BGA Ball	Digital I/O level [1]	Application function	Pin state after reset[2]	Cell type [3]	Description
USB_DM	N2	SUP3	AIO	-	AIO1	USB D− connection with integrated 45 Ω termination resistor.
USB_VDDA12_PLL	L1	SUP1	Supply	-	PS3	USB PLL supply.
USB_VDDA33_DRV	M2	SUP3	Supply	-	PS3	USB analog supply for driver.
USB_VDDA33	P1	SUP3	Supply	-	PS3	USB analog supply for PHY.
USB_VSSA_TERM	L3	-	Ground	-	CG1	USB analog ground for clean reference for on chip termination resistors.
USB_GNDA	N1	-	Ground	-	CG1	USB analog ground.
USB_VSSA_REF	K4	-	Ground	-	CG1	USB analog ground for clean reference.
JTAG						
JTAGSEL	N11	SUP3	DI	I:PD	DIO1	JTAG selection. Controls output function of SCAN_TDO and ARM_TDO signals. Must be LOW during power-on reset.
TDI	K9	SUP3	DI	I:PU	DIO1	JTAG data input.
TRST_N	P13	SUP3	DI	I:PD	DIO1	JTAG TAP Controller Reset Input. Must be LOW during power-on reset.
TCK	M14	SUP3	DI	I:PD	DIO1	JTAG clock input.
TMS	P10	SUP3	DI	I:PU	DIO1	JTAG mode select input.
SCAN_TDO	F10	SUP3	DO	O/Z	DIO1	JTAG TDO signal from scan TAP controller. Pin state is controlled by JTAGSEL.
ARM_TDO	E11	SUP3	DO	O	DIO1	JTAG TPO signal from ARM926 TAP controller.
BUF_TRST_N	F11	SUP3	DO	O	DIO1	Buffered TRST_N out signal. Used for connecting an on board TAP controller (FPGA, DSP, etc.).
BUF_TCK	D13	SUP3	DO	O	DIO1	Buffered TCK out signal. Used for connecting an on board TAP controller (FPGA, DSP, etc.).
BUF_TMS	D14	SUP3	DO	O	DIO1	Buffered TMS out signal. Used for connecting an on board TAP controller (FPGA, DSP, etc.).
UART						
mUART_CTS_N[4][5]	N13	SUP3	DI/GPIO	I	DIO1	UART clear to send (active LOW).
mUART_RTS_N[4][5]	P14	SUP3	DO/GPIO	O	DIO1	UART ready to send (active LOW).
UART_RXD[4]	P12	SUP3	DI/GPIO	I	DIO1	UART serial input.
UART_TXD[4]	N12	SUP3	DO/GPIO	O	DIO1	UART serial output.
I2C-bus master/slave interface						
I2C_SDA0	C10	SUP3	DIO	I	IICD	I2C0-bus serial data line.
I2C_SCL0	D10	SUP3	DIO	I	IICC	I2C0-bus serial clock line.
I2C_SDA1[4]	E12	SUP3	DIO	O	DIO1	I2C1-bus serial data line.
I2C_SCL1[4]	E13	SUP3	DIO	O	DIO1	I2C1-bus serial clock line.

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Table 4.   Pin description *…continued*
Pin names with prefix m are multiplexed pins. See Table 10 for pin function selection of multiplexed pins.

Pin name	BGA Ball	Digital I/O level [1]	Application function	Pin state after reset[2]	Cell type [3]	Description
Serial Peripheral Interface (SPI)						
SPI_CS_OUT0[4]	A7	SUP3	DO	O	DIO4	SPI chip select output (master).
SPI_SCK[4]	A8	SUP3	DIO	I	DIO4	SPI clock input (slave)/clock output (master).
SPI_MISO[4]	C8	SUP3	DIO	I	DIO4	SPI data input (master)/data output (slave).
SPI_MOSI[4]	B7	SUP3	DIO	I	DIO4	SPI data output (master)/data input (slave).
SPI_CS_IN[4]	B8	SUP3	DI	I	DIO4	SPI chip select input (slave).
Digital power supply						
VDDI	H3; L7; L12; C12; C6	SUP1	Supply	-	CS2	Digital core supply.
VSSI	A11; C7; D12; G4; L6; L11		Ground	-	CG2	Digital core ground.
Peripheral power supply						
VDDE_IOA	B2; E5; F5; G5; H5	SUP4	Supply	-	PS1	Peripheral supply for NAND flash interface.
VDDE_IOB	L4; M5; M7; M9	SUP8	Supply	-	PS1	Peripheral supply for SDRAM/LCD.
VDDE_IOC	C13; D5; D7; E8; G12; L10; K11	SUP3	Supply	-	PS1	Peripheral supply.
VSSE_IOA	C3; C4; E4; F4; H4; K3	-	Ground	-	PG1	-
VSSE_IOB	M3; M4; M6; M8	-	Ground	-	PG1	-

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Table 4.   **Pin description**   *…continued*
Pin names with prefix m are multiplexed pins. See Table 10 *for pin function selection of multiplexed pins.*

Pin name	BGA Ball	Digital I/O level [1]	Application function	Pin state after reset[2]	Cell type [3]	Description
VSSE_IOC	B12; D6; D8; D9; G11; L9; L13	-	Ground	-	PG1	-
LCD interface						
mLCD_CSB[4]	K8	SUP8	DO	O	DIO4	LCD chip select (active LOW).
mLCD_E_RD[4]	L8	SUP8	DO	O	DIO4	LCD 6800 enable or 8080 read enable (active HIGH).
mLCD_RS[4]	P8	SUP8	DO	O	DIO4	LCD instruction register (LOW)/data register (HIGH) select.
mLCD_RW_WR[4]	N9	SUP8	DO	O	DIO4	LCD 6800 read/write select or 8080 write enable (active HIGH).
mLCD_DB_0[4]	N8	SUP8	DIO	O	DIO4	LCD data 0.
mLCD_DB_1[4]	P9	SUP8	DIO	O	DIO4	LCD data 1.
mLCD_DB_2[4]	N6	SUP8	DIO	O	DIO4	LCD data 2.
mLCD_DB_3[4]	P6	SUP8	DIO	O	DIO4	LCD data 3.
mLCD_DB_4[4]	N7	SUP8	DIO	O	DIO4	LCD data 4.
mLCD_DB_5[4]	P7	SUP8	DIO	O	DIO4	LCD data 5.
mLCD_DB_6[4]	K6	SUP8	DIO	O	DIO4	LCD data 6.
mLCD_DB_7[4]	P5	SUP8	DIO	O	DIO4	LCD data 7.
mLCD_DB_8[4]	N5	SUP8	DIO	O	DIO4	LCD data 8/8-bit data 0.
mLCD_DB_9[4]	L5	SUP8	DIO	O	DIO4	LCD data 9/8-bit data 1.
mLCD_DB_10[4]	K7	SUP8	DIO	O	DIO4	LCD data 10/8-bit data 2.
mLCD_DB_11[4]	N4	SUP8	DIO	O	DIO4	LCD data 11/8-bit data 3.
mLCD_DB_12[4]	K5	SUP8	DIO	O	DIO4	LCD data 12/8-bit data 4/4-bit data 0.
mLCD_DB_13[4]	P4	SUP8	DIO	O	DIO4	LCD data 13/8-bit data 5/4-bit data 1/serial clock output.
mLCD_DB_14[4]	P3	SUP8	DIO	O	DIO4	LCD data 14/8-bit data 6/4-bit data 2/serial data input.
mLCD_DB_15[4]	N3	SUP8	DIO	O	DIO4	LCD data 15/8-bit data 7/4-bit data 3/serial data output.
I^{2}S/digital audio input						
I2SRX_DATA0[4]	M10	SUP3	DI/GPIO	I	DIO1	I^{2}S serial data receive input.
I2SRX_DATA1[4]	G14	SUP3	DI/GPIO	I	DIO1	I^{2}S serial data receive input.
I2SRX_BCK0[4]	N10	SUP3	DIO/GPIO	I	DIO1	I^{2}S bit clock.
I2SRX_BCK1[4]	F14	SUP3	DIO/GPIO	I	DIO1	I^{2}S bit clock.
I2SRX_WS0[4]	P11	SUP3	DIO/GPIO	I	DIO1	I^{2}S word select.
I2SRX_WS1[4]	F13	SUP3	DIO/GPIO	I	DIO1	I^{2}S word select.

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Table 4. Pin description *…continued*
Pin names with prefix m are multiplexed pins. See Table 10 for pin function selection of multiplexed pins.

Pin name	BGA Ball	Digital I/O level [1]	Application function	Pin state after reset[2]	Cell type [3]	Description
I²S/digital audio output						
mI2STX_DATA0[4]	M13	SUP3	DO/GPIO	O	DIO1	I²S serial data transmit output.
mI2STX_BCK0[4]	M12	SUP3	DO/GPIO	O	DIO1	I²S bit clock.
mI2STX_WS0[4]	M11	SUP3	DO/GPIO	O	DIO1	I²S word select.
mI2STX_CLK0[4]	N14	SUP3	DO/GPIO	O	DIO1	I²S serial clock.
I2STX_DATA1[4]	F12	SUP3	DO/GPIO	O	DIO1	I²S serial data transmit output.
I2STX_BCK1[4]	E14	SUP3	DO/GPIO	O	DIO1	I²S bit clock.
I2STX_WS1[4]	G10	SUP3	DO/GPIO	O	DIO1	I²S word select.
General Purpose IO (GPIO)						
GPIO0[7]	K10	SUP3	GPIO	I:PD	DIO1	General Purpose IO pin 0 (mode pin 0).
GPIO1[7]	J10	SUP3	GPIO	I:PD	DIO1	General Purpose IO pin 1 (mode pin 1).
GPIO2[7]	L14	SUP3	GPIO	I	DIO1	General Purpose IO pin 2 (mode pin 2).
GPIO3	B11	SUP3	GPIO	I	DIO1	General Purpose IO pin 3.
GPIO4	C11	SUP3	GPI	I	DIO1	General Purpose input pin 4.
mGPIO5[4]	B6	SUP3	GPIO	I	DIO4	General Purpose IO pin 5.
mGPIO6[4]	A6	SUP3	GPIO	I	DIO4	General Purpose IO pin 6.
mGPIO7[4]	A5	SUP3	GPIO	I	DIO4	General Purpose IO pin 7.
mGPIO8[4]	B5	SUP3	GPIO	I	DIO4	General Purpose IO pin 8.
mGPIO9[4]	C5	SUP3	GPIO	I	DIO4	General Purpose IO pin 9.
mGPIO10[4]	A4	SUP3	GPIO	I	DIO4	General Purpose IO pin 10.
GPIO11	H13	SUP3	GPIO	I	DIO1	General Purpose IO pin 11.
GPIO12	H10	SUP3	GPIO	I	DIO1	General Purpose IO pin 12.
GPIO13	J12	SUP3	GPIO	I	DIO1	General Purpose IO pin 13.
GPIO14	J14	SUP3	GPIO	I	DIO1	General Purpose IO pin 14.
GPIO15	J13	SUP3	GPIO	I	DIO1	General Purpose IO pin 15.
GPIO16	J11	SUP3	GPIO	I	DIO1	General Purpose IO pin 16.
GPIO17	K12	SUP3	GPIO	I	DIO1	General Purpose IO pin 17.
GPIO18	K14	SUP3	GPIO	I	DIO1	General Purpose IO pin 18.
GPIO19	H11	SUP3	GPIO	I	DIO1	General Purpose IO pin 19.
GPIO20	K13	SUP3	GPIO	I	DIO1	General Purpose IO pin 20.
External Bus Interface (EBI)/NAND flash controller						
EBI_A_0_ALE[4]	B3	SUP4	DO	O	DIO4	EBI address latch enable.
EBI_A_1_CLE[4]	A2	SUP4	DO	O	DIO4	EBI command latch enable.
EBI_D_0[4]	G2	SUP4	DIO	I	DIO4	EBI data I/O 0.
EBI_D_1[4]	F2	SUP4	DIO	I	DIO4	EBI data I/O 1.
EBI_D_2[4]	F1	SUP4	DIO	I	DIO4	EBI data I/O 2.
EBI_D_3[4]	E1	SUP4	DIO	I	DIO4	EBI data I/O 3.
EBI_D_4[4]	E2	SUP4	DIO	I	DIO4	EBI data I/O 4.

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Table 4. **Pin description** *…continued*

Pin names with prefix m are multiplexed pins. See Table 10 for pin function selection of multiplexed pins.

Pin name	BGA Ball	Digital I/O level [1]	Application function	Pin state after reset[2]	Cell type [3]	Description
EBI_D_5[4]	D1	SUP4	DIO	I	DIO4	EBI data I/O 5.
EBI_D_6[4]	D2	SUP4	DIO	I	DIO4	EBI data I/O 6.
EBI_D_7[4]	C1	SUP4	DIO	I	DIO4	EBI data I/O 7.
EBI_D_8[4]	B1	SUP4	DIO	I	DIO4	EBI data I/O 8.
EBI_D_9[4]	A3	SUP4	DIO	I	DIO4	EBI data I/O 9.
EBI_D_10[4]	A1	SUP4	DIO	I	DIO4	EBI data I/O 10.
EBI_D_11[4]	C2	SUP4	DIO	I	DIO4	EBI data I/O 11.
EBI_D_12[4]	G3	SUP4	DIO	I	DIO4	EBI data I/O 12.
EBI_D_13[4]	D3	SUP4	DIO	I	DIO4	EBI data I/O 13.
EBI_D_14[4]	E3	SUP4	DIO	I	DIO4	EBI data I/O 14.
EBI_D_15[4]	F3	SUP4	DIO	I	DIO4	EBI data I/O 15.
EBI_DQM_0_NOE[4]	H1	SUP4	DO	O	DIO4	NAND read enable (active LOW).
EBI_NWE[4]	J2	SUP4	DO	O	DIO4	NAND write enable (active LOW).
NAND_NCS_0[4]	J1	SUP4	DO	O	DIO4	NAND chip enable 0.
NAND_NCS_1[4]	J3	SUP4	DO	O	DIO4	NAND chip enable 1.
NAND_NCS_2[4]	K1	SUP4	DO	O	DIO4	NAND chip enable 2.
NAND_NCS_3[4]	K2	SUP4	DO	O	DIO4	NAND chip enable 3.
mNAND_RYBN0[4]	E6	SUP4	DI	I	DIO4	NAND ready/busy 0.
mNAND_RYBN1[4]	E7	SUP4	DI	I	DIO4	NAND ready/busy 1.
mNAND_RYBN2[4]	B4	SUP4	DI	I	DIO4	NAND ready/busy 2.
mNAND_RYBN3[4]	D4	SUP4	DI	I	DIO4	NAND ready/busy 3.
EBI_NCAS_BLOUT_0[4]	G1	SUP4	DO	O	DIO4	EBI lower lane byte select (7:0).
EBI_NRAS_BLOUT_1[4]	H2	SUP4	DO	O	DIO4	EBI upper lane byte select (15:8).
Secure one-time programmable memory						
VPP[6]	A9; C9	SUP1/ SUP3	Supply	-	PS3	Supply for polyfuse programming.
Pulse Width Modulation (PWM)						
PWM_DATA[4]	B9	SUP3	DO/GPIO	O	DIO1	PWM output.

[1] Digital IO levels are explained in Table 5.

[2] I = input; I:PU = input with internal weak pull-up; I:PD = input with internal weak pull-down; O = output.

[3] Cell types are explained in Table 6.

[4] Pin can be configured as GPIO pin in the IOCONFIG block.

[5] The UART flow control lines (mUART_CTS_N and mUART_RTS_N) are multiplexed. This means that if these balls are not required for UART flow control, they can be selected to be used for alternative functions: SPI chip select signals (SPI_CS_OUT1 and SPI_CS_OUT2).

[6] The polyfuses get unintentionally burned at random if VPP is powered to 2.3 V or greater before the VDDI is powered up to minimum nominal voltage. This will destroy the sample because randomly blowing security fuses will lock the sample and also can corrupt the AES key. For this reason it is recommended that VPP be powered by SUP1 at power on.

[7] To ensure that GPIO0, GPIO1 and GPIO2 pins come up as inputs, pins TRST_N and JTAGSEL must be LOW at power-on reset, see *UM10362 JTAG chapter* for details.

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Table 5.   Supply domains

Supply domain	Voltage range	Related supply pins	Description
SUP1	1.0 V to 1.3 V	VDDI, VDDA12, USB_VDDA12_PLL, VPP (OTP read)	Digital core supply
SUP3	2.7 V to 3.6 V	VDDE_IOC, ADC10B_VDDA33, USB_VDDA33_DRV, USB_VDDA33, VPP (during OTP write)	Peripheral supply
SUP4	1.65 V to 1.95 V (in 1.8 V mode) 2.5 V to 3.6 V (in 3.3 V mode)	VDDE_IOA	Peripheral supply for NAND flash interface
SUP5	4.5 V to 5.5 V	USB_VBUS	USB VBUS voltage
SUP8	1.65 V to 1.95 V (in 1.8 V mode) 2.5 V to 3.6 V (in 3.3 V mode)	VDDE_IOB	Peripheral supply for SDRAM/SRAM/bus-based LCD [1]

[1] When the SDRAM is used, the supply voltage of the NAND flash, SDRAM, and the LCD interface must be the same, i.e. SUP4 and SUP8 should be connected to the same rail. (See also Section 6.28.3.)

Table 6:   I/O pads

Cell type	Pad type	Function	Description
DIO1	bspts3chp	Digital input/output	Bidirectional 3.3 V; 3-state output; 3 ns slew rate control; plain input; CMOS with hysteresis; programmable pull-up, pull-down, repeater
DIO2	bpts5pcph	Digital input/output	Bidirectional 5 V; plain input; 3-state output; CMOS with programmable hysteresis; programmable pull-up, pull-down, repeater
DIO4	mem1 bsptz40pchp	Digital input/output	Bidirectional 1.8 V or 3.3 V; plain input; 3-state output; programmable hysteresis; programmable pull-up, pull-down, repeater
IICC	iic3m4scl	Digital input/output	I^{2}C-bus; clock signal
IICD	iic3mvsda	Digital input/output	I^{2}C-bus; data signal
AIO1	apio3v3	Analog input/output	Analog input/output; protection to external 3.3 V supply rail
AIO2	apio	Analog input/output	Analog input/output
AIO3	apiot5v	Analog input/output	Analog input/output; 5 V tolerant pad-based ESD protection
CS1	vddco	Core supply	-
CS2	vddi	Core supply	-
PS1	vdde3v3	Peripheral supply	-
PS2	vdde	Peripheral supply	-
PS3	vddco3v3	Analog power supply	-
CG1	vssco	Core ground	-
CG2	vssis	Core ground	-
PG1	vsse	Peripheral ground	-

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6. Functional description

6.1 ARM926EJ-S

The processor embedded in the chip is the ARM926EJ-S. It is a member of the ARM9 family of general-purpose microprocessors. The ARM926EJ-S is intended for multi-tasking applications where full memory management, high performance, and low power are important.

This module has the following features:

- ARM926EJ-S processor core which uses a five-stage pipeline consisting of fetch, decode, execute, memory and write stages. The processor supports both the 32-bit ARM and 16-bit Thumb instruction sets, which allows a trade off between high performance and high code density. The ARM926EJ-S also executes an extended ARMv5TE instruction set which includes support for Java byte code execution.

- Contains an AMBA BIU for both data accesses and instruction fetches.

- Memory Management Unit (MMU).

- 16 kB instruction and 16 kB data separate cache memories with an 8 word line length. The caches are organized using Harvard architecture.

- Little endian is supported.

- The ARM926EJ-S processor supports the ARM debug architecture and includes logic to assist in both hardware and software debugging.

- Supports dynamic clock gating for power reduction.

- The processor core clock can be set equal to the AHB bus clock or to an integer number times the AHB bus clock. The processor can be switched dynamically between these settings.

- ARM stall support.

6.2 Memory map

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Left column (address)		Right column domains	
4 GB	0xFFFF FFFF		
reserved		APB4 domain	0x1700 8000
2 GB	0x8000 0000		
reserved	0x7000 0800	reserved	
NAND flash/AES buffer[1]			0x1700 1000
	0x7000 0000	NAND flash controller	0x1700 0800
reserved	0x6000 1000	DMA	0x1700 0000
interrupt controller	0x6000 0000		
reserved	0x4000 0000	reserved	
external SDRAM bank 0	0x3000 0000	APB3 domain	0x1600 0280
		I2SRX_1	0x1600 0200
	0x2004 0000	I2SRX_0	0x1600 0180
external SRAM bank 1	0x2002 0000	I2STX_1	0x1600 0100
external SRAM bank 0	0x2000 0000	I2STX_0	0x1600 0080
reserved	0x1900 1000	I2S system config	0x1600 0000
USB OTG	0x1900 0000	reserved	0x1500 3000
reserved	0x1800 0900	SPI	0x1500 2000
MCI/SD/SDIO	0x1800 0000	UART	0x1500 1000
reserved	0x1700 9000	reserved	0x1500 0800
MPMC configuration registers	0x1700 8000	LCD	0x1500 0400
APB4 domain	0x1700 0000	PCM	0x1500 0000
APB3 domain	0x1600 0000	I2C1	0x1300 B000
APB2 domain	0x1500 0000	I2C0	0x1300 A400
reserved	0x1300 B000	PWM	0x1300 A000
APB1 domain	0x1300 8000	timer 3	0x1300 9000
APB0 domain	0x1300 0000	timer 2	0x1300 8C00
reserved	0x1202 0000	timer 1	0x1300 8800
128 kB ISROM	0x1200 0000	timer 0	0x1300 8400
reserved	0x1105 8000	RNG	0x1300 8000
96 kB ISRAM1	0x1104 0000	OTP	0x1300 6000
96 kB ISRAM0	0x1102 8000	CGU	0x1300 5000
reserved	0x0000 1000	IOCONFIG	0x1300 4000
shadow area		SysCReg	0x1300 3000
0 GB	0x0000 0000	WDT	0x1300 2800
		ADC10B	0x1300 2400
		event router	0x1300 2000
			0x1300 0000

APB2 domain, APB1 domain, APB0 domain labels as shown.

002aae307

(1) LPC3143 only.

Fig 3. **LPC3141/3143 memory map**

6.3 JTAG

The Joint Test Action Group (JTAG) interface allows the incorporation of the LPC3141/3143 in a JTAG scan chain.

This module has the following features:

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- ARM926 debug access

- Boundary scan

- The ARM926 debug access can be permanently disabled through JTAG security bits in the One-Time Programmable memory (OTP) block.

6.4 NAND flash controller

The NAND flash controller is used as a dedicated interface to NAND flash devices. Figure 4 shows a block diagram of the NAND flash controller module. The heart of the module is formed by a controller block that controls the flow of data from/to the AHB bus through the NAND flash controller block to/from the (external) NAND flash. An Error Correction Code (ECC) module allows for hardware error correction for support of Multi-Level Cell (MLC) NAND flash devices. The NAND flash controller is connected to the AES block to support secure (encrypted) code execution (see Section 6.21).

Before data is written from the buffer to the NAND flash, optionally it is first protected by an error correction code generated by the ECC module. After data is read from the NAND flash, the error correction module corrects errors, and/or the AES decryption module can decrypt data.

(1) AES decoder available on LPC3143 only.

Fig 4.   Block diagram of the NAND flash controller
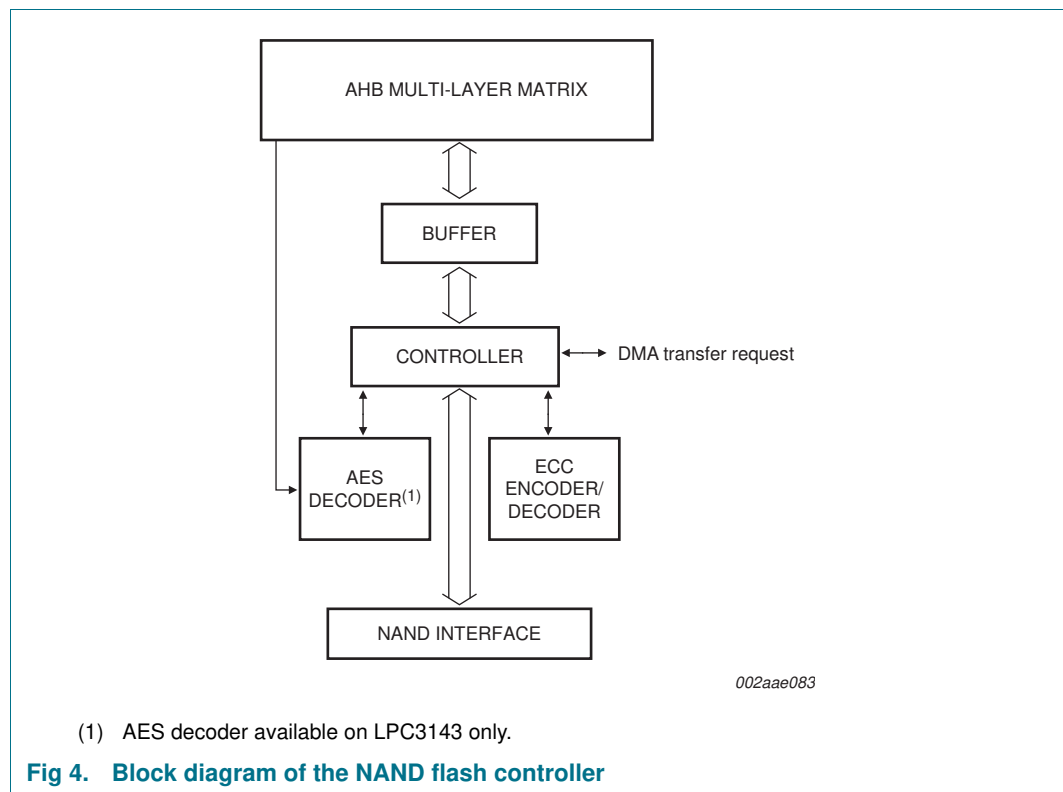
This module has the following features:

- Dedicated NAND flash interface with hardware controlled read and write accesses.

- Wear leveling support with 516-byte mode.

- Software controlled command and address transfers to support wide range of flash devices.

- Software control mode where the ARM is directly master of the flash device.

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- Support for 8-bit and 16-bit flash devices.

- Support for any page size from 0.5 kB upwards.

- Programmable NAND flash timing parameters.

- Support for up to 4 NAND devices.

- Hardware AES decryption (LPC3143 only).

- Error Correction Module (ECC) for MLC NAND flash support:

  - Reed-Solomon error correction encoding and decoding.

  - Uses Reed-Solomon code words with 9-bit symbols over $GF(2^9)$, a total codeword length of 469 symbols, including 10 parity symbols, giving a minimum Hamming distance of 11.

  - Up to 8 symbol errors can be corrected per codeword.

  - Error correction can be turned on and off to match the demands of the application.

  - Parity generator for error correction encoding.

  - Wear leveling information can be integrated into protected data.

  - Interrupts generated after completion of error correction task with three interrupt registers.

  - Error correction statistics distributed to ARM using interrupt scheme.

  - Interface is compatible with the ARM External Bus Interface (EBI).

6.5 Multi-Port Memory Controller (MPMC)

The multi-port memory controller supports the interface to different memory types, for example:

- SDRAM

- Low-power SDRAM

- Static memory interface

This module has the following features:

- Dynamic memory interface support including SDRAM, JEDEC low-power SDRAM.

- Address line supporting up to 128 MB (two 64Mx8 devices connected to a single chip select) of dynamic memory.

- The MPMC has two AHB interfaces:

  a. an interface for accessing external memory.

  b. a separate control interface to program the MPMC. This enables the MPMC registers to be situated in memory with other system peripheral registers.

- Low transaction latency.

- Read and write buffers to reduce latency and to improve performance, particularly for un-cached processors.

- Static memory features include:

  - asynchronous page mode read

  - programmable wait states

  - bus turnaround delay

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- – output enable and write enable delays
- – extended wait
- One chip select for synchronous memory and two chip selects for static memory devices.
- Power-saving modes.
- Dynamic memory self-refresh mode supported.
- Controller support for 2 k, 4 k, and 8 k row address synchronous memory parts.
- Support for all AHB burst types.
- Little and big endian support.
- Support for the External Bus Interface (EBI) that enables the memory controller pads to be shared.

6.6 External Bus Interface (EBI)

The EBI module acts as multiplexer with arbitration between the NAND flash and the SDRAM/SRAM memory modules connected externally through the MPMC.

The main purpose for using the EBI module is to save external pins. However only data and address pins are multiplexed. Control signals towards and from the external memory devices are not multiplexed.

Table 7. Memory map of the external SRAM/SDRAM memory modules

Module	Maximum address space		Data width	Device size
External SRAM0	0x2000 0000	0x2000 FFFF	8 bit	64 kB
	0x2000 0000	0x2001 FFFF	16 bit	128 kB
External SRAM1	0x2002 0000	0x2002 FFFF	8 bit	64 kB
	0x2002 0000	0x2003 FFFF	16 bit	128 kB
External SDRAM0	0x3000 0000	0x37FF FFFF	16 bit	128 MB

6.7 Internal Static ROM (ISROM)

The internal static ROM is used to store the boot code of the LPC3141/3143. After a reset, the ARM processor will start its code execution from this memory.

The LPC3143 ROM memory has the following features:

- Supports secure booting from SPI flash, NAND flash, SD/SDHC/MMC cards, UART, and USB (DFU class) interfaces.
- Supports SHA1 hash checking on the boot image.
- Supports non-secure boot from UART and USB (DFU class) interfaces during development. Once AES key is programmed in OTP, only secure boot is allowed through UART and USB.
- Supports secure booting from managed NAND devices such as moviNAND, iNAND, eMMC-NAND and eSD-NAND using SD/MMC boot mode.
- Contains pre-defined MMU table (16 kB) for simple systems.

The LPC3141 ROM memory has the following features:

- Supports booting from SPI flash, NAND flash, SD/SDHC/MMC cards, UART, and USB (DFU class) interfaces.
- Supports option to perform CRC32 checking on the boot image.
- Contains pre-defined MMU table (16 kB) for simple systems.
- Supports booting from managed NAND devices such as movi-NAND, iNAND, eMMC-NAND and eSD-NAND using SD/MMC boot mode.

The boot ROM determines the boot mode based on reset state of GPIO0, GPIO1, and GPIO2 pins. To ensure that GPIO0, GPIO1 and GPIO2 pins come up as inputs, pins TRST_N and JTAGSEL must be LOW during power-on reset (see *UM10362 JTAG chapter* for details). Table 8 shows the various boot modes supported on the LPC3141/3143:

Table 8.   LPC3141/3143 boot modes

Boot mode	GPIO0	GPIO1	GPIO2	Description
NAND	0	0	0	Boots from NAND flash. If proper image is not found, boot ROM will switch to DFU boot mode.
SPI	0	0	1	Boot from SPI NOR flash connected to SPI_CS_OUT0. If proper image is not found, boot ROM will switch to DFU boot mode.
DFU	0	1	0	Device boots via USB using DFU class specification.
SD/MMC	0	1	1	Boot ROM searches all the partitions on the SD/MMC/SDHC/MMC+/eMMC/eSD card for boot image. If partition table is missing, it will start searching from sector 0. A valid image is said to be found if a valid image header is found, followed by a valid image. If a proper image is not found, boot ROM will switch to DFU boot mode.
Reserved 0	1	0	0	Reserved for testing.
NOR flash	1	0	1	Boot from parallel NOR flash connected to EBI_NSTCS_1.[1]
UART	1	1	0	Boot ROM tries to download boot image from UART ((115200 - 8 - n -1) assuming 12 MHz FFAST clock).
Test	1	1	1	Boot ROM is testing ISRAM using memory pattern test. Switches to UART boot mode on receiving three ASCI dots ("...") on UART.

[1] For security reasons this mode is disabled when JTAG security feature is used.

6.8 Internal RAM memory

The ISRAM (Internal Static RAM Memory) controller module is used as controller between the AHB bus and the internal RAM memory. The internal RAM memory can be used as working memory for the ARM processor and as temporary storage to execute the code that is loaded by boot ROM from external devices such as SPI flash, NAND flash, and SD/MMC cards.

This module has the following features:

- Capacity of 192 kB

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- Implemented as two independent 96 kB memory banks

6.9 Memory Card Interface (MCI)

The MCI controller interface can be used to access memory cards according to the Secure Digital (SD) and Multi-Media Card (MMC) standards. The host controller can be used to interface to small form factor expansion cards compliant to the SDIO card standard as well. Finally, the MCI supports CE-ATA 1.1 compliant hard disk drives.

This module has the following features:

- One 8-bit wide interface.
- Supports high-speed SD, versions 1.01, 1.10 and 2.0.
- Supports SDIO version 1.10.
- Supports MMCplus, MMCmobile and MMCmicro cards based on MMC 4.1.
- Supports SDHC memory cards.
- CRC generation and checking.
- Supports 1/4-bit SD cards.
- Card detection and write protection.
- FIFO buffers of 16 byte deep.
- Host pull-up control.
- SDIO suspend and resume.
- 1 to 65 535 byte blocks.
- Suspend and resume operations.
- SDIO read-wait.
- Individual clock and power ON/OFF features to each card.
- Maximum clock speed of 52 MHz (MMC 4.1).
- Supports CE-ATA 1.1.
- Supports 1-bit, 4-bit, and 8-bit MMC cards and CE-ATA devices.

6.10 High-speed Universal Serial Bus 2.0 On-The-Go (OTG)

The USB OTG module allows the LPC3141/3143 to connect directly to a USB host such as a PC (in device mode) or to a USB device in host mode. In addition, the LPC3141/3143 has a special, built-in mode in which it enumerates as a Device Firmware Upgrade (DFU) class, and which allows for a (factory) download of the device firmware through USB.

This module has the following features:

- Complies with *Universal Serial Bus specification 2.0*.
- Complies with *USB On-The-Go supplement*.
- Complies with *Enhanced Host Controller Interface Specification*.
- Supports auto USB 2.0 mode discovery.
- Supports all high-speed USB-compliant peripherals.
- Supports all full-speed USB-compliant peripherals.

- Supports software Host Negotiation Protocol (HNP) and Session Request Protocol (SRP) for OTG peripherals.
- Contains UTMI+ compliant transceiver (PHY).
- Supports interrupts.
- This module has its own, integrated DMA engine.

6.11 DMA controller

The DMA controller can perform DMA transfers on the AHB without using the CPU.

This module has the following features:

- Supported transfer types:

  Memory to memory copy

  – Memory can be copied from the source address to the destination address with a specified length, while incrementing the address for both the source and destination.

  Memory to peripheral

  – Data is transferred from incrementing memory to a fixed address of a peripheral. The flow is controlled by the peripheral.

  Peripheral to memory

  – Data is transferred from a fixed address of a peripheral to incrementing memory. The flow is controlled by the peripheral.

- Supports single data transfers for all transfer types.
- Supports burst transfers for memory to memory transfers. A burst always consists of multiples of 4 (32 bit) words.
- The DMA controller has 12 channels.
- Scatter-gather is used to gather data located at different areas of memory. Two channels are needed per scatter-gather action.
- Supports byte, half-word, and word transfers and correctly aligns them over the AHB bus.
- Compatible with ARM flow control for single requests, last single requests, terminal count info, and DMA clearing.
- Supports swapping endian property of the transported data.

Table 9: Peripherals that support DMA

Peripheral name	Supported transfer types
NAND flash controller/AES decryption engine[1]	Memory to memory
SPI	Memory to peripheral and peripheral to memory
MCI	Memory to peripheral and peripheral to memory
LCD interface	Memory to peripheral
UART	Memory to peripheral and peripheral to memory
$I^2C0/1$-bus interfaces	Memory to peripheral and peripheral to memory

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Table 9:   Peripherals that support DMA *…continued*

Peripheral name	Supported transfer types
I^{2}S0/1 receive	Peripheral to Memory
I^{2}S0/1 transmit	Memory to peripheral
PCM interface	Memory to peripheral and peripheral to memory

[1]   AES decryption engine is available on LPC3143 only.

6.12 Interrupt controller

The interrupt controller collects interrupt requests from multiple devices, masks interrupt requests, and forwards the combined requests to the processor. The interrupt controller also provides facilities to identify the interrupt requesting devices to be served.

This module has the following features:

• The interrupt controller decodes all the interrupt requests issued by the on-chip peripherals.

• Two interrupt lines (Fast Interrupt Request (FIQ), Interrupt Request (IRQ)) to the ARM core. The ARM core supports two distinct levels of priority on all interrupt sources, FIQ for high priority interrupts and IRQ for normal priority interrupts.

• Software interrupt request capability associated with each request input.

• Visibility of interrupts request state before masking.

• Support for nesting of interrupt service routines.

• Interrupts routed to IRQ and to FIQ are vectored.

• Level interrupt support.
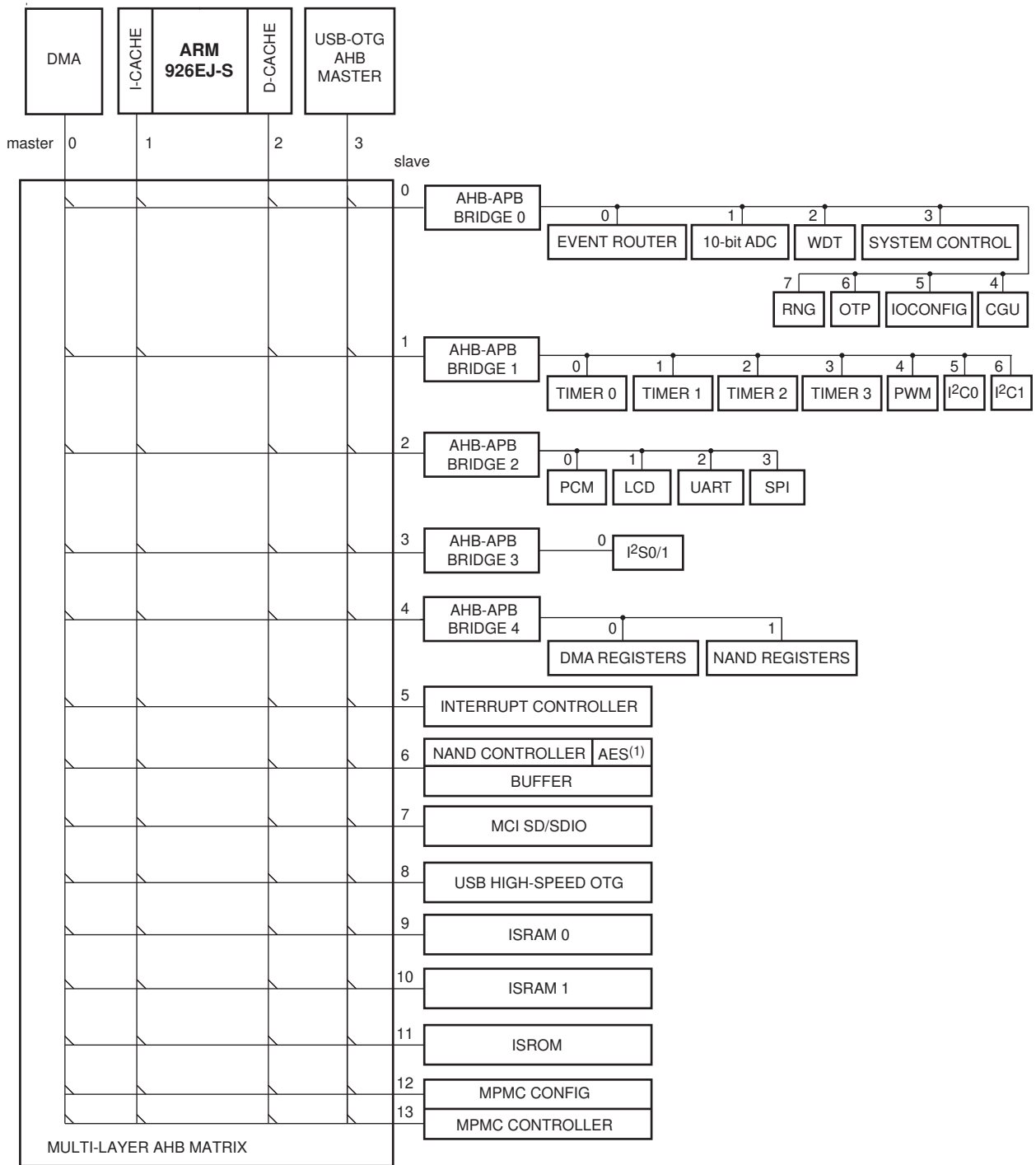
The following blocks can generate interrupts:

• NAND flash controller

• USB 2.0 HS OTG

• Event router

• 10 bit ADC

• UART

• LCD interface

• MCI

• SPI

• I^{2}C0-bus and I^{2}C1-bus controllers

• Timer 0, timer 1, timer 2, and timer 3

• I^{2}S transmit: I2STX_0 and I2STX_1

• I^{2}S receive: I2SRX_0 and I2SRX_1

• DMA

6.13 Multi-layer AHB

The multi-layer AHB is an interconnection scheme based on the AHB protocol that enables parallel access paths between multiple masters and slaves in a system.

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Multiple masters can have access to different slaves at the same time.

Figure 5 gives an overview of the multi-layer AHB configuration in the LPC3141/3143. AHB masters and slaves are numbered according to their AHB port number.

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(1) AES is available for LPC3143 only.

Fig 5.   LPC3141/3143 multi-layer AHB matrix connections

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This module has the following features:

- Supports all combinations of 32-bit masters and slaves (fully connected interconnect matrix).
- Round-Robin priority mechanism for bus arbitration: all masters have the same priority and get bus access in their natural order.
- Four devices on a master port (listed in their natural order for bus arbitration):
  - DMA
  - ARM926 instruction port
  - ARM926 data port
  - USB OTG
- Devices on a slave port (some ports are shared between multiple devices):
  - AHB to APB bridge 0
  - AHB to APB bridge 1
  - AHB to APB bridge 2
  - AHB to APB bridge 3
  - AHB to APB bridge 4
  - Interrupt controller
  - NAND flash controller
  - MCI SD/SDIO
  - USB 2.0 HS OTG
  - 96 kB ISRAM
  - 96 kB ISRAM
  - 128 kB ROM
  - MPMC (Multi-Purpose Memory Controller)

6.14 APB bridge

The APB bridge is a bus bridge between AMBA Advanced High-performance Bus (AHB) and the ARM Peripheral Bus (APB) interface.

The module supports two different architectures:

- Single-clock architecture, synchronous bridge. The same clock is used at the AHB side and at the APB side of the bridge. The AHB-to-APB4 bridge uses this architecture.
- Dual-clock architecture, asynchronous bridge. Different clocks are used at the AHB side and at the APB side of the bridge. The AHB-to-APB0, AHB-to-APB1, AHB-to-APB2, and AHB-to-APB3 bridges use this architecture.

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6.15 Clock Generation Unit (CGU)

The clock generation unit generates all clock signals in the system and controls the reset signals for all modules. The structure of the CGU is shown in Figure 6. Each output clock generated by the CGU belongs to one of the domains. Each clock domain is fed by a single base clock that originates from one of the available clock sources. Within a clock domain, fractional dividers are available to divide the base clock to a lower frequency.

Within most clock domains, the output clocks are again grouped into one or more subdomains. All output clocks within one subdomain are either all generated by the same fractional divider or they are connected directly to the base clock. Therefore all output clocks within one subdomain have the same frequency and all output clocks within one clock domain are synchronous because they originate from the same base clock.

The CGU reference clock is generated by the external crystal. Furthermore the CGU has several Phase Locked Loop (PLL) circuits to generate clock signals that can be used for system clocks and/or audio clocks. All clock sources, except the output of the PLLs, can be used as reference input for the PLLs.

This module has the following features:

- Advanced features to optimize the system for low power:
  - All output clocks can be disabled individually for flexible power optimization.
  - Some modules have automatic clock gating: they are only active when (bus) access to the module is required.
  - Variable clock scaling for automatic power optimization of the AHB bus (high clock frequency when the bus is active, low clock frequency when the bus is idle).
  - Clock wake-up feature: module clocks can be programmed to be activated automatically on the basis of an event detected by the event router (see also Section 6.19). For example, all clocks (including the core/bus clocks) are off and activated automatically when a button is pressed.
- Supports five clock sources:
  - Reference clock generated by the oscillator with an external crystal.
  - Pins I2SRX_BCK0, I2SRX_WS0, I2SRX_BCK1 and I2SRX_WS1 are used to input external clock signals (used for generating audio frequencies in I2SRX slave mode, see also Section 6.4).
- Supports two PLLs:
  - System PLL generates programmable system clock frequency from its reference input.
  - I^{2}S/Audio PLL generates programmable audio clock frequency (typically $256 \times$ fs) from its reference input.

    Remark: Both the System PLL and the I^{2}S/Audio PLL generate their frequencies based on their (individual) reference clocks. The reference clocks can be programmed to the oscillator clock or one of the external clock signals.
- Highly flexible switchbox to distribute the signals from the clock sources to the module clocks.
  - Each clock generated by the CGU is derived from one of the base clocks and optionally divided by a fractional divider.

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