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LPC408x/7x

32-bit ARM Cortex-M4 MCU; up to 512 kB flash, 96 kB SRAM; USB Device/Host/OTG; Ethernet; LCD; EMC; SPIFI

Rev. 3 — 11 January 2017 Product data sheet

1. General description

The LPC408x/7x is an ARM Cortex-M4 based digital signal controller for embedded applications requiring a high level of integration and low power dissipation.

The ARM Cortex-M4 is a next generation core that offers system enhancements such as low power consumption, enhanced debug features, and a high level of support block integration. The ARM Cortex-M4 CPU incorporates a 3-stage pipeline, uses a Harvard architecture with separate local instruction and data buses as well as a third bus for peripherals, and includes an internal prefetch unit that supports speculative branching. The ARM Cortex-M4 supports single-cycle digital signal processing and SIMD instructions. A hardware floating-point processor is integrated in the core for several versions of the part.

The LPC408x/7x adds a specialized flash memory accelerator to accomplish optimal performance when executing code from flash. The LPC408x/7x is targeted to operate at up to 120 MHz CPU frequency.

The peripheral complement of the LPC408x/7x includes up to 512 kB of flash program memory, up to 96 kB of SRAM data memory, up to 4032 byte of EEPROM data memory, External Memory controller (EMC), LCD, Ethernet, USB Device/Host/OTG, an SPI Flash Interface (SPIFI), a General Purpose DMA controller, five UARTs, three SSP controllers, three I^2C-bus interfaces, a Quadrature Encoder Interface, four general purpose timers, two general purpose PWMs with six outputs each and one motor control PWM, an ultra-low power RTC with separate battery supply and event recorder, a windowed watchdog timer, a CRC calculation engine and up to 165 general purpose I/O pins.

The analog peripherals include one eight-channel 12-bit ADC, two analog comparators, and a DAC.

The pinout of LPC408x/7x is intended to allow pin function compatibility with the LPC24xx/23xx as well as the LPC178x/7x families.

For additional documentation, see Section 17 “References”.

2. Features and benefits

- Functional replacement for LPC23xx/24xx and LPC178x/7x family devices.
- ARM Cortex-M4 core:
  - ARM Cortex-M4 processor, running at frequencies of up to 120 MHz.
  - ARM Cortex-M4 built-in Memory Protection Unit (MPU) supporting eight regions.
  - ARM Cortex-M4 built-in Nested Vectored Interrupt Controller (NVIC).

- Hardware floating-point unit (not all versions).
- Non-maskable Interrupt (NMI) input.
- JTAG and Serial Wire Debug (SWD), serial trace, eight breakpoints, and four watch points.
- System tick timer.

- System:
  - Multilayer AHB matrix interconnect provides a separate bus for each AHB master. AHB masters include the CPU, and General Purpose DMA controller. This interconnect provides communication with no arbitration delays unless two masters attempt to access the same slave at the same time.
  - Split APB bus allows for higher throughput with fewer stalls between the CPU and DMA. A single level of write buffering allows the CPU to continue without waiting for completion of APB writes if the APB was not already busy.
  - Embedded Trace Macrocell (ETM) module supports real-time trace.
  - Boundary scan for simplified board testing.
- Memory:
  - 512 kB on-chip flash program memory with In-System Programming (ISP) and In-Application Programming (IAP) capabilities. The combination of an enhanced flash memory accelerator and location of the flash memory on the CPU local code/data bus provides high code performance from flash.
  - Up to 96 kB on-chip SRAM includes:

    64 kB of main SRAM on the CPU with local code/data bus for high-performance CPU access.

    Two 16 kB peripheral SRAM blocks with separate access paths for higher throughput. These SRAM blocks may be used for DMA memory as well as for general purpose instruction and data storage.
  - Up to 4032 byte on-chip EEPROM.
- LCD controller, supporting both Super-Twisted Nematic (STN) and Thin-Film Transistors (TFT) displays.
  - Dedicated DMA controller.
  - Selectable display resolution (up to 1024 $\times$ 768 pixels).
  - Supports up to 24-bit true-color mode.
- External Memory Controller (EMC) provides support for asynchronous static memory devices such as RAM, ROM and flash, as well as dynamic memories such as single data rate SDRAM.
- Eight channel General Purpose DMA controller (GPDMA) on the AHB multilayer matrix that can be used with the SSP, I2S, UART, CRC engine, Analog-to-Digital and Digital-to-Analog converter peripherals, timer match signals, GPIO, and for memory-to-memory transfers.
- Serial interfaces:
  - Quad SPI Flash Interface (SPIFI) with four lanes and up to 40 MB per second.
  - Ethernet MAC with MII/RMII interface and associated DMA controller. These functions reside on an independent AHB.
  - USB 2.0 full-speed dual port device/host/OTG controller with on-chip PHY and associated DMA controller.

- Five UARTs with fractional baud rate generation, internal FIFO, DMA support, and RS-485/EIA-485 support. One UART (UART1) has full modem control I/O, and one UART (USART4) supports IrDA, synchronous mode, and a smart card mode conforming to ISO7816-3.
- Three SSP controllers with FIFO and multi-protocol capabilities. The SSP interfaces can be used with the GPDMA controller.
- Three enhanced I^2C-bus interfaces, one with a true open-drain output supporting the full I^2C-bus specification and Fast-mode Plus with data rates of 1 Mbit/s, two with standard port pins. Enhancements include multiple address recognition and monitor mode.
- I^2S (Inter-IC Sound) interface for digital audio input or output. It can be used with the GPDMA.
- CAN controller with two channels.

- Digital peripherals:
  - SD/MMC memory card interface.
  - Up to 165 General Purpose I/O (GPIO) pins depending on the packaging, with configurable pull-up/down resistors, open-drain mode, and repeater mode. All GPIOs are located on an AHB bus for fast access and support Cortex-M4 bit-banding. GPIOs can be accessed by the General Purpose DMA Controller. Any pin of ports 0 and 2 can be used to generate an interrupt.
  - Two external interrupt inputs configurable as edge/level sensitive. All pins on port 0 and port 2 can be used as edge sensitive interrupt sources.
  - Four general purpose timers/counters, with a total of eight capture inputs and ten compare outputs. Each timer block has an external count input. Specific timer events can be selected to generate DMA requests.
  - Quadrature encoder interface that can monitor one external quadrature encoder.
  - Two standard PWM/timer blocks with external count input option.
  - One motor control PWM with support for three-phase motor control.
  - Real-Time Clock (RTC) with a separate power domain. The RTC is clocked by a dedicated RTC oscillator. The RTC block includes 20 bytes of battery-powered backup registers, allowing system status to be stored when the rest of the chip is powered off. Battery power can be supplied from a standard 3 V lithium button cell. The RTC will continue working when the battery voltage drops to as low as 2.1 V. An RTC interrupt can wake up the CPU from any reduced power mode.
  - Event Recorder that can capture the clock value when an event occurs on any of three inputs. The event identification and the time it occurred are stored in registers. The Event Recorder is located in the RTC power domain and can therefore operate as long as there is RTC power.
  - Windowed Watchdog Timer (WWDT). Windowed operation, dedicated internal oscillator, watchdog warning interrupt, and safety features.
  - CRC Engine block can calculate a CRC on supplied data using one of three standard polynomials. The CRC engine can be used in conjunction with the DMA controller to generate a CRC without CPU involvement in the data transfer.
- Analog peripherals:
  - 12-bit Analog-to-Digital Converter (ADC) with input multiplexing among eight pins, conversion rates up to 400 kHz, and multiple result registers. The 12-bit ADC can be used with the GPDMA controller.

- 10-bit Digital-to-Analog Converter (DAC) with dedicated conversion timer and DMA support.
- Two analog comparators.

- Power control:
  - Four reduced power modes: Sleep, Deep-sleep, Power-down, and Deep power-down.
  - The Wake-up Interrupt Controller (WIC) allows the CPU to automatically wake up from any priority interrupt that can occur while the clocks are stopped in Deep-sleep, Power-down, and Deep power-down modes.
  - Processor wake-up from Power-down mode via any interrupt able to operate during Power-down mode (includes external interrupts, RTC interrupt, PORT0/2 pin interrupt, and NMI).
  - Brownout detect with separate threshold for interrupt and forced reset.
  - On-chip Power-On Reset (POR).
- Clock generation:
  - Clock output function that can reflect the main oscillator clock, IRC clock, RTC clock, CPU clock, USB clock, or the watchdog timer clock.
  - On-chip crystal oscillator with an operating range of 1 MHz to 25 MHz.
  - 12 MHz Internal RC oscillator (IRC) trimmed to 1 % accuracy that can optionally be used as a system clock.
  - An on-chip PLL allows CPU operation up to the maximum CPU rate without the need for a high-frequency crystal. May be run from the main oscillator or the internal RC oscillator.
  - A second, dedicated PLL may be used for USB interface in order to allow added flexibility for the Main PLL settings.
- Versatile pin function selection feature allows many possibilities for using on-chip peripheral functions.
- Unique device serial number for identification purposes.
- Single 3.3 V power supply (2.4 V to 3.6 V). Temperature range of −40 °C to 85 °C.
- Available as LQFP208, TFBGA208, TFBGA180, LQFP144, TFBGA80, and LQFP80 package.

3. Applications

- Communications:
  - Point-of-sale terminals, web servers, multi-protocol bridges
- Industrial/Medical:
  - Automation controllers, application control, robotics control, HVAC, PLC, inverters, circuit breakers, medical scanning, security monitoring, motor drive, video intercom
- Consumer/Appliance:
  - Audio, MP3 decoders, alarm systems, displays, printers, scanners, small appliances, fitness equipment
- Automotive:
  - After-market, car alarms, GPS/fleet monitors

4. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
LPC4088			
LPC4088FBD208	LQFP208	plastic low profile quad flat package; 208 leads; body 28 × 28 × 1.4 mm	SOT459-1
LPC4088FET208	TFBGA208	plastic thin fine-pitch ball grid array package; 208 balls; body 15 × 15 × 0.7 mm	SOT950-1
LPC4088FET180	TFBGA180	thin fine-pitch ball grid array package; 180 balls	SOT570-3
LPC4088FBD144	LQFP144	plastic low profile quad flat package; 144 leads; body 20 × 20 × 1.4 mm	SOT486-1
LPC4078			
LPC4078FBD208	LQFP208	plastic low profile quad flat package; 208 leads; body 28 × 28 × 1.4 mm	SOT459-1
LPC4078FET208	TFBGA208	plastic thin fine-pitch ball grid array package; 208 balls; body 15 × 15 × 0.7 mm	SOT950-1
LPC4078FET180	TFBGA180	thin fine-pitch ball grid array package; 180 balls	SOT570-3
LPC4078FBD144	LQFP144	plastic low profile quad flat package; 144 leads; body 20 × 20 × 1.4 mm	SOT486-1
LPC4078FBD80	LQFP80	plastic low-profile quad package; 80 leads; body 12 × 12 × 1.4 mm	SOT315-1
LPC4078FBD100	LQFP100	plastic low profile quad flat package; 100 leads; body 14 × 14 × 1.4 mm	SOT407-1
LPC4076			
LPC4076FET180	TFBGA180	thin fine-pitch ball grid array package; 180 balls	SOT570-3
LPC4076FBD144	LQFP144	plastic low profile quad flat package; 144 leads; body 20 × 20 × 1.4 mm	SOT486-1
LPC4074			
LPC4074FBD144	LQFP144	plastic low profile quad flat package; 144 leads; body 20 × 20 × 1.4 mm	SOT486-1
LPC4074FBD80	LQFP80	plastic low-profile quad package; 80 leads; body 12 × 12 × 1.4 mm	SOT315-1
LPC4072			
LPC4072FET80	TFBGA80	plastic thin fine-pitch ball grid array package; 80 balls	SOT1328-1
LPC4072FBD80	LQFP80	plastic low-profile quad package; 80 leads; body 12 × 12 × 1.4 mm	SOT315-1

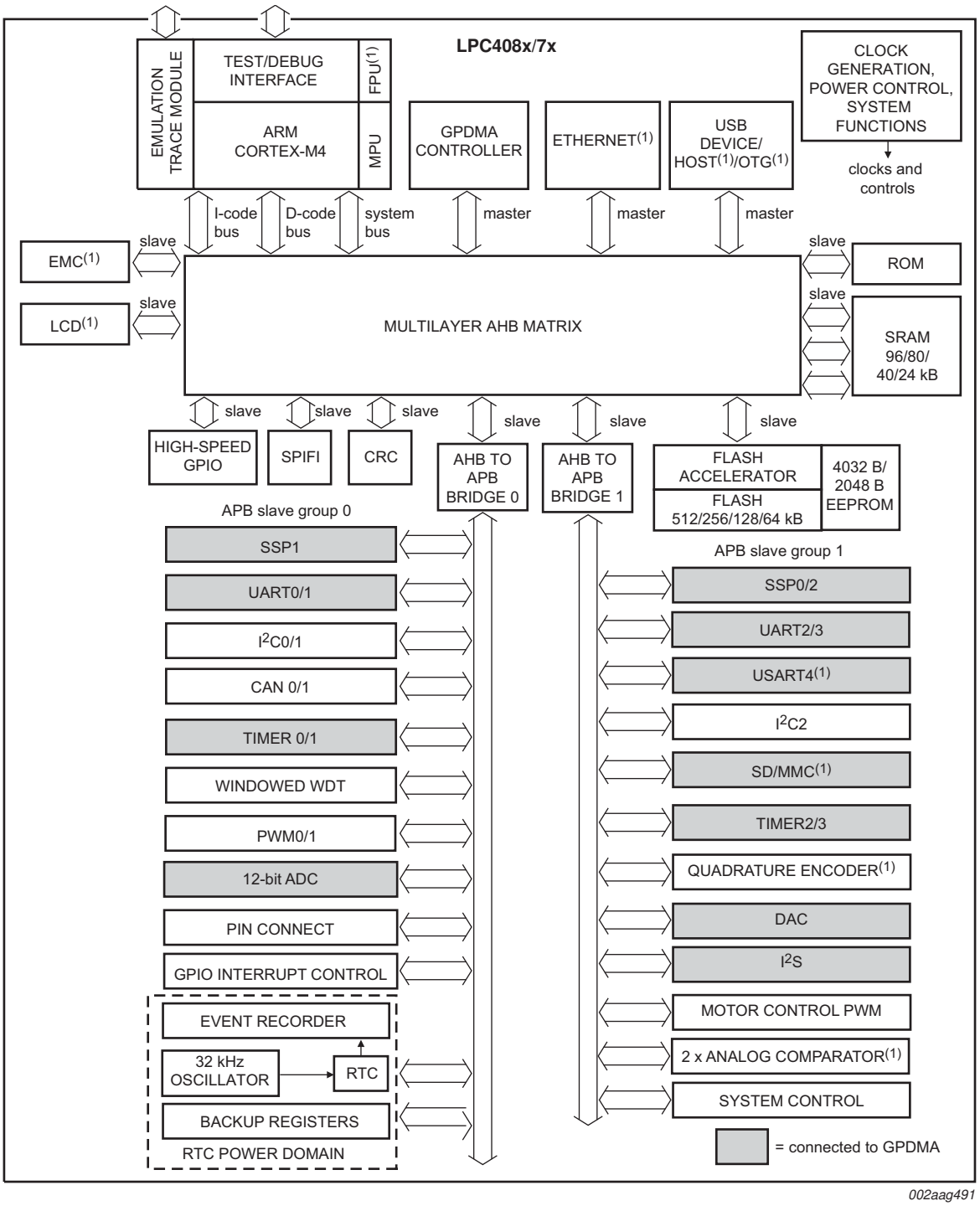
Table 2. Ordering options

Type number	Flash (kB)	SRAM (kB)	EEPROM (B)	EMC bus width (bit)	LCD	Ethernet	USB	CAN	UART	QEI	SD/MMC	Comparator	FPU	Package
LPC4088														
LPC4088FBD208	512	96	4032	32	yes	yes	H/O/D	2	5	yes	yes	yes	yes	LQFP208
LPC4088FET208	512	96	4032	32	yes	yes	H/O/D	2	5	yes	yes	yes	yes	TFBGA208
LPC4088FET180	512	96	4032	16	yes	yes	H/O/D	2	5	yes	yes	yes	yes	TFBGA180
LPC4088FBD144	512	96	4032	8	yes	yes	H/O/D	2	5	yes	yes	yes	yes	LQFP144
LPC4078														
LPC4078FBD208	512	96	4032	32	no	yes	H/O/D	2	5	yes	yes	yes	yes	LQFP208
LPC4078FET208	512	96	4032	32	no	yes	H/O/D	2	5	yes	yes	yes	yes	TFBGA208
LPC4078FET180	512	96	4032	16	no	yes	H/O/D	2	5	yes	yes	yes	yes	TFBGA180

Table 2. Ordering options *…continued*

Type number	Flash (kB)	SRAM (kB)	EEPROM (B)	EMC bus width (bit)	LCD	Ethernet	USB	CAN	UART	QEI	SD/MMC	Comparator	FPU	Package
LPC4078FBD144	512	96	4032	8	no	yes	H/O/D	2	5	yes	yes	yes	yes	LQFP144
LPC4078FBD100	512	96	4032	-	no	yes	H/O/D	2	5	yes	yes	yes	yes	LQFP100
LPC4078FBD80	512	96	4032	-	no	yes	H/O/D	2	5	yes	no	yes	yes	LQFP80
LPC4076														
LPC4076FET180	256	80	2048	16	no	yes	H/O/D	2	5	yes	yes	yes	yes	TFBGA180
LPC4076FBD144	256	80	2048	8	no	yes	H/O/D	2	5	yes	yes	yes	yes	LQFP144
LPC4074														
LPC4074FBD144	128	40	2048	-	no	no	D	2	4	no	no	no	no	LQFP144
LPC4074FBD80	128	40	2048	-	no	no	D	2	4	no	no	no	no	LQFP80
LPC4072														
LPC4072FET80	64	24	2048	-	no	no	D	2	4	no	no	no	no	TFBGA80
LPC4072FBD80	64	24	2048	-	no	no	D	2	4	no	no	no	no	LQFP80

5. Block diagram



(1) Not available on all parts.

Fig 1. Block diagram

6. Pinning information

6.1 Pinning

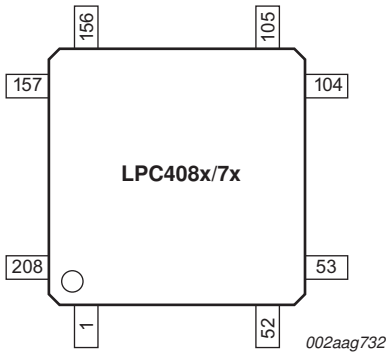


Fig 2. Pin configuration (LQFP208)

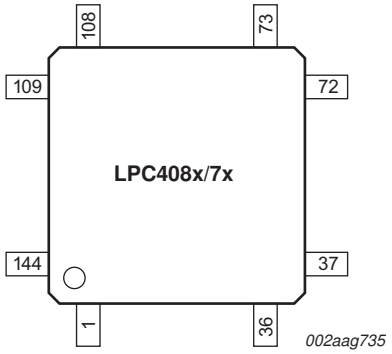


Fig 3. Pin configuration (LQFP144)

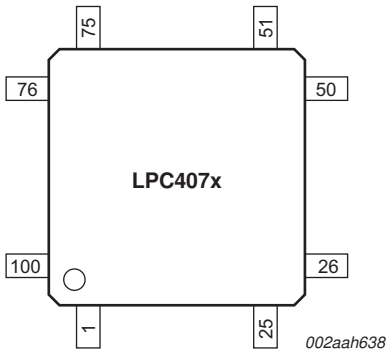


Fig 4. Pin configuration (LQFP100)

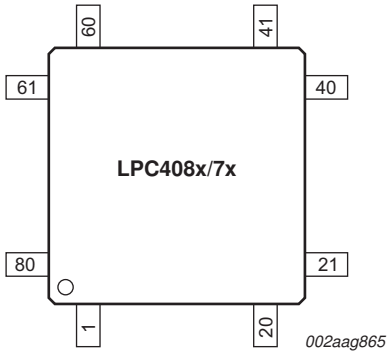
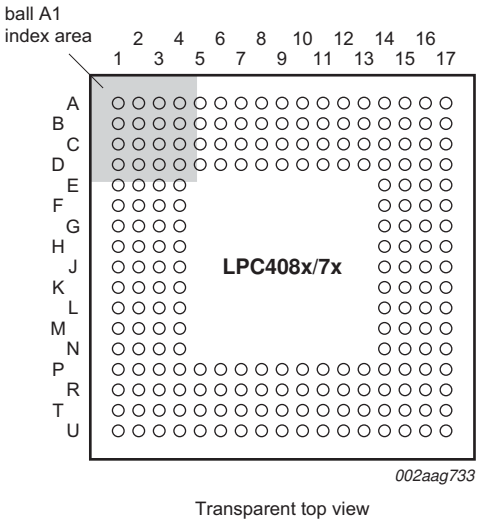


Fig 5. Pin configuration (LQFP80)



Transparent top view

Fig 6. Pin configuration (TFBGA208)

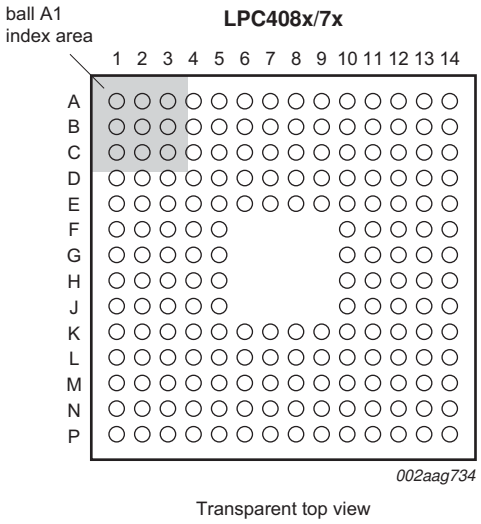


Fig 7. Pin configuration (TFBGA180)

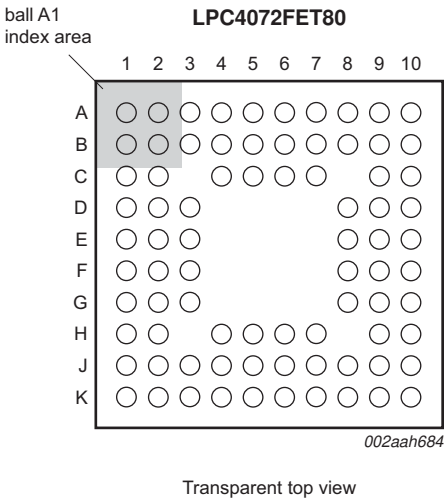


Fig 8. Pin configuration (TFBGA80)

6.2 Pin description

I/O pins on the LPC408x/7x are 5 V tolerant and have input hysteresis unless otherwise indicated in the table below. Crystal pins, power pins, and reference voltage pins are not 5 V tolerant. In addition, when pins are selected to be ADC inputs, they are no longer 5 V tolerant and the input voltage must be limited to the voltage at the ADC positive reference pin (VREFP).

All port pins Pn[m] are multiplexed, and the multiplexed functions appear in Table 3 in the order defined by the FUNC bits of the corresponding IOCON register up to the highest used function number. Each port pin can support up to eight multiplexed functions. IOCON register FUNC values which are reserved are noted as “R” in the pin configuration table.

Table 3. Pin description

Not all functions are available on all parts. See Table 2 (Ethernet, USB, LCD, QEI, SD/MMC, comparator pins) and Table 5 (EMC pins).

Symbol	Pin LQFP208	Ball TFBGA208	Ball TFBGA180	Pin LQFP144	Pin LQFP100	Pin LQFP80	Pin TFBGA80		Reset state[1]	Type[2]	Description
P0[0] to P0[31]										I/O	**Port 0:** Port 0 is a 32-bit I/O port with individual direction controls for each bit. The operation of port 0 pins depends upon the pin function selected via the pin connect block.
P0[0]	94	U15	M10	66	46	37	J9	[3]	I; PU	I/O	**P0[0] —** General purpose digital input/output pin.
										I	**CAN_RD1 —** CAN1 receiver input.
										O	**U3_TXD —** Transmitter output for UART3.
										I/O	**I2C1_SDA —** I^2C1 data input/output (this pin does not use a specialized I2C pad).
										O	**U0_TXD —** Transmitter output for UART0.
P0[1]	96	T14	N11	67	47	38	J10	[3]	I; PU	I/O	**P0[1] —** General purpose digital input/output pin.
										O	**CAN_TD1 —** CAN1 transmitter output.
										I	**U3_RXD —** Receiver input for UART3.
										I/O	**I2C1_SCL —** I^2C1 clock input/output (this pin does not use a specialized I2C pad).
										I	**U0_RXD —** Receiver input for UART0.
P0[2]	202	C4	D5	141	98	79	A2	[3]	I; PU	I/O	**P0[2] —** General purpose digital input/output pin.
										O	**U0_TXD —** Transmitter output for UART0.
										O	**U3_TXD —** Transmitter output for UART3.
P0[3]	204	D6	A3	142	99	80	A1	[3]	I; PU	I/O	**P0[3] —** General purpose digital input/output pin.
										I	**U0_RXD —** Receiver input for UART0.
										I	**U3_RXD —** Receiver input for UART3.

Table 3. Pin description *...continued*

Not all functions are available on all parts. See Table 2 (Ethernet, USB, LCD, QEI, SD/MMC, comparator pins) and Table 5 (EMC pins).

Symbol	Pin LQFP208	Ball TFBGA208	Ball TFBGA180	Pin LQFP144	Pin LQFP100	Pin LQFP80	Pin TFBGA80		Reset state[1]	Type[2]	Description
P0[4]	168	B12	A11	116	81	-	-	[3]	I; PU	I/O	**P0[4] —** General purpose digital input/output pin.
										I/O	**I2S_RX_SCK —** I^2S Receive clock. It is driven by the master and received by the slave. Corresponds to the signal SCK in the *I^2S-bus specification*.
										I	**CAN_RD2 —** CAN2 receiver input.
										I	**T2_CAP0 —** Capture input for Timer 2, channel 0.
										-	**R —** Function reserved.
										I/O	**CMP_ROSC —** Comparator relaxation oscillator for 555 timer applications.
										-	**R —** Function reserved.
										O	**LCD_VD[0] —** LCD data.
P0[5]	166	C12	B11	115	80	-	-	[3]	I; PU	I/O	**P0[5] —** General purpose digital input/output pin.
										I/O	**I2S_RX_WS —** I^2S Receive word select. It is driven by the master and received by the slave. Corresponds to the signal WS in the *I^2S-bus specification*.
										O	**CAN_TD2 —** CAN2 transmitter output.
										I	**T2_CAP1 —** Capture input for Timer 2, channel 1.
										-	**R —** Function reserved.
										I	**CMP_RESET —** Comparator reset.
										-	**R —** Function reserved.
										O	**LCD_VD[1] —** LCD data.

Table 3. Pin description *...continued*

Not all functions are available on all parts. See Table 2 (Ethernet, USB, LCD, QEI, SD/MMC, comparator pins) and Table 5 (EMC pins).

Symbol	Pin LQFP208	Ball TFBGA208	Ball TFBGA180	Pin LQFP144	Pin LQFP100	Pin LQFP80	Pin TFBGA80		Reset state[1]	Type[2]	Description
P0[6]	164	D13	D11	113	79	64	A7	[3]	I; PU	I/O	**P0[6] —** General purpose digital input/output pin.
										I/O	**I2S_RX_SDA —** I^2S Receive data. It is driven by the transmitter and read by the receiver. Corresponds to the signal SD in the *I^2S-bus specification*.
										I/O	**SSP1_SSEL —** Slave Select for SSP1.
										O	**T2_MAT0 —** Match output for Timer 2, channel 0.
										O	**U1_RTS —** Request to Send output for UART1. Can also be configured to be an RS-485/EIA-485 output enable signal for UART1.
										I/O	**CMP_ROSC —** Comparator relaxation oscillator for 555 timer applications.
										-	**R —** Function reserved.
										O	**LCD_VD[8] —** LCD data.
P0[7]	162	C13	B12	112	78	63	A8	[4]	I; IA	I/O	**P0[7] —** General purpose digital input/output pin.
										I/O	**I2S_TX_SCK —** I^2S transmit clock. It is driven by the master and received by the slave. Corresponds to the signal SCK in the *I^2S-bus specification*.
										I/O	**SSP1_SCK —** Serial Clock for SSP1.
										O	**T2_MAT1 —** Match output for Timer 2, channel 1.
										I	**RTC_EV0 —** Event input 0 to Event Monitor/Recorder.
										I	**CMP_VREF —** Comparator reference voltage.
										-	**R —** Function reserved.
										O	**LCD_VD[9] —** LCD data.

Table 3. Pin description *...continued*

Not all functions are available on all parts. See Table 2 (Ethernet, USB, LCD, QEI, SD/MMC, comparator pins) and Table 5 (EMC pins).

Symbol	Pin LQFP208	Ball TFBGA208	Ball TFBGA180	Pin LQFP144	Pin LQFP100	Pin LQFP80	Pin TFBGA80		Reset state[1]	Type[2]	Description
P0[8]	160	A15	C12	111	77	62	A10	[4]	I; IA	I/O	**P0[8] —** General purpose digital input/output pin.
										I/O	**I2S_TX_WS —** I^2S Transmit word select. It is driven by the master and received by the slave. Corresponds to the signal WS in the *I^2S-bus specification*.
										I/O	**SSP1_MISO —** Master In Slave Out for SSP1.
										O	**T2_MAT2 —** Match output for Timer 2, channel 2.
										I	**RTC_EV1 —** Event input 1 to Event Monitor/Recorder.
										I	**CMP1_IN[3] —** Comparator 1, input 3.
										-	**R —** Function reserved.
										O	**LCD_VD[16] —** LCD data.
P0[9]	158	C14	A13	109	76	61	A9	[4]	I; IA	I/O	**P0[9] —** General purpose digital input/output pin.
										I/O	**I2S_TX_SDA —** I^2S transmit data. It is driven by the transmitter and read by the receiver. Corresponds to the signal SD in the *I^2S-bus specification*.
										I/O	**SSP1_MOSI —** Master Out Slave In for SSP1.
										O	**T2_MAT3 —** Match output for Timer 2, channel 3.
										I	**RTC_EV2 —** Event input 2 to Event Monitor/Recorder.
										I	**CMP1_IN[2] —** Comparator 1, input 2.
										-	**R —** Function reserved.
										O	**LCD_VD[17] —** LCD data.

Table 3. Pin description *...continued*

Not all functions are available on all parts. See Table 2 (Ethernet, USB, LCD, QEI, SD/MMC, comparator pins) and Table 5 (EMC pins).

Symbol	Pin LQFP208	Ball TFBGA208	Ball TFBGA180	Pin LQFP144	Pin LQFP100	Pin LQFP80	Pin TFBGA80		Reset state[1]	Type[2]	Description
P0[10]	98	T15	L10	69	48	39	K9	[3]	I; PU	I/O	**P0[10] —** General purpose digital input/output pin.
										O	**U2_TXD —** Transmitter output for UART2.
										I/O	**I2C2_SDA —** I^2C2 data input/output (this pin does not use a specialized I2C pad).
										O	**T3_MAT0 —** Match output for Timer 3, channel 0.
										-	**R —** Function reserved.
										-	**R —** Function reserved.
										-	**R —** Function reserved.
										O	**LCD_VD[5] —** LCD data.
P0[11]	100	R14	P12	70	49	40	K10	[3]	I; PU	I/O	**P0[11] —** General purpose digital input/output pin.
										I	**U2_RXD —** Receiver input for UART2.
										I/O	**I2C2_SCL —** I^2C2 clock input/output (this pin does not use a specialized I2C pad).
										O	**T3_MAT1 —** Match output for Timer 3, channel 1.
										-	**R —** Function reserved.
										-	**R —** Function reserved.
										-	**R —** Function reserved.
										O	**LCD_VD[10] —** LCD data.
P0[12]	41	R1	J4	29	-	-	-	[5]	I; PU	I/O	**P0[12] —** General purpose digital input/output pin.
										O	**$\overline{\text{USB\_PPWR2}}$ —** Port Power enable signal for USB port 2.
										I/O	**SSP1_MISO —** Master In Slave Out for SSP1.
										I	**ADC0_IN[6] —** A/D converter 0, input 6. When configured as an ADC input, the digital function of the pin must be disabled.

Table 3. Pin description *...continued*

Not all functions are available on all parts. See Table 2 (Ethernet, USB, LCD, QEI, SD/MMC, comparator pins) and Table 5 (EMC pins).

Symbol	Pin LQFP208	Ball TFBGA208	Ball TFBGA180	Pin LQFP144	Pin LQFP100	Pin LQFP80	Pin TFBGA80		Reset state[1]	Type[2]	Description
P0[13]	45	R2	J5	32	-	-	-	[5]	I; PU	I/O	**P0[13] —** General purpose digital input/output pin.
										O	**USB_UP_LED2 —** USB port 2 GoodLink LED indicator. It is LOW when the device is configured (non-control endpoints enabled), or when the host is enabled and has detected a device on the bus. It is HIGH when the device is not configured, or when host is enabled and has not detected a device on the bus, or during global suspend. It transitions between LOW and HIGH (flashes) when the host is enabled and detects activity on the bus.
										I/O	**SSP1_MOSI —** Master Out Slave In for SSP1.
										I	**ADC0_IN[7] —** A/D converter 0, input 7. When configured as an ADC input, the digital function of the pin must be disabled.
P0[14]	69	T7	M5	48	-	-	-	[3]	I; PU	I/O	**P0[14] —** General purpose digital input/output pin.
										O	**USB_HSTEN2 —** Host Enabled status for USB port 2.
										I/O	**SSP1_SSEL —** Slave Select for SSP1.
										O	**USB_CONNECT2 —** SoftConnect control for USB port 2. Signal used to switch an external 1.5 kΩ resistor under software control. Used with the SoftConnect USB feature.
P0[15]	128	J16	H13	89	62	47	F9	[3]	I; PU	I/O	**P0[15] —** General purpose digital input/output pin.
										O	**U1_TXD —** Transmitter output for UART1.
										I/O	**SSP0_SCK —** Serial clock for SSP0.
										-	**R —** Function reserved.
										-	**R —** Function reserved.
										I/O	**SPIFI_IO[2] —** Data bit 0 for SPIFI.

Table 3. Pin description *...continued*

Not all functions are available on all parts. See Table 2 (Ethernet, USB, LCD, QEI, SD/MMC, comparator pins) and Table 5 (EMC pins).

Symbol	Pin LQFP208	Ball TFBGA208	Ball TFBGA180	Pin LQFP144	Pin LQFP100	Pin LQFP80	Pin TFBGA80		Reset state[1]	Type[2]	Description
P0[16]	130	J14	H14	90	63	48	F8	[3]	I; PU	I/O	**P0[16] —** General purpose digital input/output pin.
										I	**U1_RXD —** Receiver input for UART1.
										I/O	**SSP0_SSEL —** Slave Select for SSP0.
										-	**R —** Function reserved.
										-	**R —** Function reserved.
										I/O	**SPIFI_IO[3] —** Data bit 0 for SPIFI.
P0[17]	126	K17	J12	87	61	46	F10	[3]	I; PU	I/O	**P0[17] —** General purpose digital input/output pin.
										I	**U1_CTS —** Clear to Send input for UART1.
										I/O	**SSP0_MISO —** Master In Slave Out for SSP0.
										-	**R —** Function reserved.
										-	**R —** Function reserved.
										I/O	**SPIFI_IO[1] —** Data bit 0 for SPIFI.
P0[18]	124	K15	J13	86	60	45	G10	[3]	I; PU	I/O	**P0[18] —** General purpose digital input/output pin.
										I	**U1_DCD —** Data Carrier Detect input for UART1.
										I/O	**SSP0_MOSI —** Master Out Slave In for SSP0.
										-	**R —** Function reserved.
										-	**R —** Function reserved.
										I/O	**SPIFI_IO[0] —** Data bit 0 for SPIFI.
P0[19]	122	L17	J10	85	59	-	-	[3]	I; PU	I/O	**P0[19] —** General purpose digital input/output pin.
										I	**U1_DSR —** Data Set Ready input for UART1.
										O	**SD_CLK —** Clock output line for SD card interface.
										I/O	**I2C1_SDA —** I^2C1 data input/output (this pin does not use a specialized I2C pad).
										-	**R —** Function reserved.
										-	**R —** Function reserved.
										-	**R —** Function reserved.
										O	**LCD_VD[13] —** LCD data.

Table 3. Pin description *...continued*

Not all functions are available on all parts. See Table 2 (Ethernet, USB, LCD, QEI, SD/MMC, comparator pins) and Table 5 (EMC pins).

Symbol	Pin LQFP208	Ball TFBGA208	Ball TFBGA180	Pin LQFP144	Pin LQFP100	Pin LQFP80	Pin TFBGA80		Reset state[1]	Type[2]	Description
P0[20]	120	M17	K14	83	58	-	-	[3]	I; PU	I/O	**P0[20] —** General purpose digital input/output pin.
										O	**U1_DTR —** Data Terminal Ready output for UART1. Can also be configured to be an RS-485/EIA-485 output enable signal for UART1.
										I/O	**SD_CMD —** Command line for SD card interface.
										I/O	**I2C1_SCL —** I^2C1 clock input/output (this pin does not use a specialized I2C pad).
										-	**R —** Function reserved.
										-	**R —** Function reserved.
										-	**R —** Function reserved.
										O	**LCD_VD[14] —** LCD data.
P0[21]	118	M16	K11	82	57	-	-	[3]	I; PU	I/O	**P0[21] —** General purpose digital input/output pin.
										I	**U1_RI —** Ring Indicator input for UART1.
										O	**SD_PWR —** Power Supply Enable for external SD card power supply.
										O	**U4_OE —** RS-485/EIA-485 output enable signal for UART4.
										I	**CAN_RD1 —** CAN1 receiver input.
										I/O	**U4_SCLK —** USART 4 clock input or output in synchronous mode.
P0[22]	116	N17	L14	80	56	44	H10	[6]	I; PU	I/O	**P0[22] —** General purpose digital input/output pin.
										O	**U1_RTS —** Request to Send output for UART1. Can also be configured to be an RS-485/EIA-485 output enable signal for UART1.
										I/O	**SD_DAT[0] —** Data line 0 for SD card interface.
										O	**U4_TXD —** Transmitter output for USART4 (input/output in smart card mode).
										O	**CAN_TD1 —** CAN1 transmitter output.
										O	**SPIFI_CLK —** Clock output for SPIFI.

Table 3. Pin description *...continued*

Not all functions are available on all parts. See Table 2 (Ethernet, USB, LCD, QEI, SD/MMC, comparator pins) and Table 5 (EMC pins).

Symbol	Pin LQFP208	Ball TFBGA208	Ball TFBGA180	Pin LQFP144	Pin LQFP100	Pin LQFP80	Pin TFBGA80		Reset state[1]	Type[2]	Description
P0[23]	18	H1	F5	13	9	-	-	[5]	I; PU	I/O	**P0[23] —** General purpose digital input/output pin.
										I	**ADC0_IN[0] —** A/D converter 0, input 0. When configured as an ADC input, the digital function of the pin must be disabled.
										I/O	**I2S_RX_SCK —** Receive Clock. It is driven by the master and received by the slave. Corresponds to the signal SCK in the *I²S-bus specification*.
										I	**T3_CAP0 —** Capture input for Timer 3, channel 0.
P0[24]	16	G2	E1	11	8	-	-	[5]	I; PU	I/O	**P0[24] —** General purpose digital input/output pin.
										I	**ADC0_IN[1] —** A/D converter 0, input 1. When configured as an ADC input, the digital function of the pin must be disabled.
										I/O	**I2S_RX_WS —** Receive Word Select. It is driven by the master and received by the slave. Corresponds to the signal WS in the *I²S-bus specification*.
										I	**T3_CAP1 —** Capture input for Timer 3, channel 1.
P0[25]	14	F1	E4	10	7	7	D1	[5]	I; PU	I/O	**P0[25] —** General purpose digital input/output pin.
										I	**ADC0_IN[2] —** A/D converter 0, input 2. When configured as an ADC input, the digital function of the pin must be disabled.
										I/O	**I2S_RX_SDA —** Receive data. It is driven by the transmitter and read by the receiver. Corresponds to the signal SD in the *I²S-bus specification*.
										O	**U3_TXD —** Transmitter output for UART3.

Table 3. Pin description *...continued*

Not all functions are available on all parts. See Table 2 (Ethernet, USB, LCD, QEI, SD/MMC, comparator pins) and Table 5 (EMC pins).

Symbol	Pin LQFP208	Ball TFBGA208	Ball TFBGA180	Pin LQFP144	Pin LQFP100	Pin LQFP80	Pin TFBGA80		Reset state[1]	Type[2]	Description
P0[26]	12	E1	D1	8	6	6	D2	[7]	I; PU	I/O	**P0[26] —** General purpose digital input/output pin.
										I	**ADC0_IN[3] —** A/D converter 0, input 3. When configured as an ADC input, the digital function of the pin must be disabled.
										O	**DAC_OUT —** D/A converter output. When configured as the DAC output, the digital function of the pin must be disabled.
										I	**U3_RXD —** Receiver input for UART3.
P0[27]	50	T1	L3	35	25	-	-	[8]	I	I/O	**P0[27] —** General purpose digital input/output pin.
										I/O	**I2C0_SDA —** I^2C0 data input/output. (This pin uses a specialized I2C pad).
										I/O	**USB_SDA1 —** I2C serial data for communication with an external USB transceiver.
P0[28]	48	R3	M1	34	24	-	-	[8]	I	I/O	**P0[28] —** General purpose digital input/output pin.
										I/O	**I2C0_SCL —** I^2C0 clock input/output (this pin uses a specialized I2C pad.
										I/O	**USB_SCL1 —** I2C serial clock for communication with an external USB transceiver.
P0[29]	61	U4	K5	42	29	22	J3	[9]	I	I/O	**P0[29] —** General purpose digital input/output pin.
										I/O	**USB_D+1 —** USB port 1 bidirectional D+ line.
										I	**$\overline{\text{EINT0}}$ —** External interrupt 0 input.
P0[30]	62	R6	N4	43	30	23	K3	[9]	I	I/O	**P0[30] —** General purpose digital input/output pin.
										I/O	**USB_D–1 —** USB port 1 bidirectional D– line.
										I	**$\overline{\text{EINT1}}$ —** External interrupt 1 input.
P0[31]	51	T2	N1	36	-	-	-	[9]	I	I/O	**P0[31] —** General purpose digital input/output pin.
										I/O	**USB_D+2 —** USB port 2 bidirectional D+ line.
P1[0] to P1[31]										I/O	**Port 1:** Port 1 is a 32 bit I/O port with individual direction controls for each bit. The operation of port 1 pins depends upon the pin function selected via the pin connect block

Table 3. Pin description *...continued*

Not all functions are available on all parts. See Table 2 (Ethernet, USB, LCD, QEI, SD/MMC, comparator pins) and Table 5 (EMC pins).

Symbol	Pin LQFP208	Ball TFBGA208	Ball TFBGA180	Pin LQFP144	Pin LQFP100	Pin LQFP80	Pin TFBGA80		Reset state[1]	Type[2]	Description
P1[0]	196	A3	B5	136	95	76	A3	[3]	I; PU	I/O	**P1[0] —** General purpose digital input/output pin.
										O	**ENET_TXD0 —** Ethernet transmit data 0 (RMII/MII interface).
										-	**R —** Function reserved.
										I	**T3_CAP1 —** Capture input for Timer 3, channel 1.
										I/O	**SSP2_SCK —** Serial clock for SSP2.
P1[1]	194	B5	A5	135	94	75	B4	[3]	I; PU	I/O	**P1[1] —** General purpose digital input/output pin.
										O	**ENET_TXD1 —** Ethernet transmit data 1 (RMII/MII interface).
										-	**R —** Function reserved.
										O	**T3_MAT3 —** Match output for Timer 3, channel 3.
										I/O	**SSP2_MOSI —** Master Out Slave In for SSP2.
P1[2]	185	D9	B7	-	-	-	-	[3]	I; PU	I/O	**P1[2] —** General purpose digital input/output pin.
										O	**ENET_TXD2 —** Ethernet transmit data 2 (MII interface).
										O	**SD_CLK —** Clock output line for SD card interface.
										O	**PWM0[1] —** Pulse Width Modulator 0, output 1.
P1[3]	177	A10	A9	-	-	-	-	[3]	I; PU	I/O	**P1[3] —** General purpose digital input/output pin.
										O	**ENET_TXD3 —** Ethernet transmit data 3 (MII interface).
										I/O	**SD_CMD —** Command line for SD card interface.
										O	**PWM0[2] —** Pulse Width Modulator 0, output 2.
P1[4]	192	A5	C6	133	93	74	B5	[3]	I; PU	I/O	**P1[4] —** General purpose digital input/output pin.
										O	**ENET_TX_EN —** Ethernet transmit data enable (RMII/MII interface).
										-	**R —** Function reserved.
										O	**T3_MAT2 —** Match output for Timer 3, channel 2.
										I/O	**SSP2_MISO —** Master In Slave Out for SSP2.

Table 3. Pin description *...continued*

Not all functions are available on all parts. See Table 2 (Ethernet, USB, LCD, QEI, SD/MMC, comparator pins) and Table 5 (EMC pins).

Symbol	Pin LQFP208	Ball TFBGA208	Ball TFBGA180	Pin LQFP144	Pin LQFP100	Pin LQFP80	Pin TFBGA80		Reset state[1]	Type[2]	Description
P1[5]	156	A17	B13	-	-	-	-	[3]	I; PU	I/O	**P1[5] —** General purpose digital input/output pin.
										O	**ENET_TX_ER —** Ethernet Transmit Error (MII interface).
										O	**SD_PWR —** Power Supply Enable for external SD card power supply.
										O	**PWM0[3] —** Pulse Width Modulator 0, output 3.
										-	**R —** Function reserved.
										I	**CMP1_IN[1] —** Comparator 1, input 1.
P1[6]	171	B11	B10	-	-	-	-	[3]	I; PU	I/O	**P1[6] —** General purpose digital input/output pin.
										I	**ENET_TX_CLK —** Ethernet Transmit Clock (MII interface).
										I/O	**SD_DAT[0] —** Data line 0 for SD card interface.
										O	**PWM0[4] —** Pulse Width Modulator 0, output 4.
										-	**R —** Function reserved.
										I	**CMP0_IN[3] —** Comparator 0, input 3.
P1[7]	153	D14	C13	-	-	-	-	[3]	I; PU	I/O	**P1[7] —** General purpose digital input/output pin.
										I	**ENET_COL —** Ethernet Collision detect (MII interface).
										I/O	**SD_DAT[1] —** Data line 1 for SD card interface.
										O	**PWM0[5] —** Pulse Width Modulator 0, output 5.
										-	**R —** Function reserved.
										I	**CMP1_IN[0] —** Comparator 1, input 0.
P1[8]	190	C7	B6	132	92	73	C5	[3]	I; PU	I/O	**P1[8] —** General purpose digital input/output pin.
										I	**ENET_CRS (ENET_CRS_DV) —** Ethernet Carrier Sense (MII interface) or Ethernet Carrier Sense/Data Valid (RMII interface).
										-	**R —** Function reserved.
										O	**T3_MAT1 —** Match output for Timer 3, channel 1.
										I/O	**SSP2_SSEL —** Slave Select for SSP2.

Table 3. Pin description *...continued*

Not all functions are available on all parts. See Table 2 (Ethernet, USB, LCD, QEI, SD/MMC, comparator pins) and Table 5 (EMC pins).

Symbol	Pin LQFP208	Ball TFBGA208	Ball TFBGA180	Pin LQFP144	Pin LQFP100	Pin LQFP80	Pin TFBGA80		Reset state[1]	Type[2]	Description
P1[9]	188	A6	D7	131	91	72	A4	[3]	I; PU	I/O	**P1[9] —** General purpose digital input/output pin.
										I	**ENET_RXD0 —** Ethernet receive data 0 (RMII/MII interface).
										-	**R —** Function reserved.
										O	**T3_MAT0 —** Match output for Timer 3, channel 0.
P1[10]	186	C8	A7	129	90	71	A5	[3]	I; PU	I/O	**P1[10] —** General purpose digital input/output pin.
										I	**ENET_RXD1 —** Ethernet receive data 1 (RMII/MII interface).
										-	**R —** Function reserved.
										I	**T3_CAP0 —** Capture input for Timer 3, channel 0.
P1[11]	163	A14	A12	-	-	-	-	[3]	I; PU	I/O	**P1[11] —** General purpose digital input/output pin.
										I	**ENET_RXD2 —** Ethernet Receive Data 2 (MII interface).
										I/O	**SD_DAT[2] —** Data line 2 for SD card interface.
										O	**PWM0[6] —** Pulse Width Modulator 0, output 6.
P1[12]	157	A16	A14	-	-	-	-	[3]	I; PU	I/O	**P1[12] —** General purpose digital input/output pin.
										I	**ENET_RXD3 —** Ethernet Receive Data (MII interface).
										I/O	**SD_DAT[3] —** Data line 3 for SD card interface.
										I	**PWM0_CAP0 —** Capture input for PWM0, channel 0.
										-	**R —** Function reserved.
										O	**CMP1_OUT —** Comparator 1, output.
P1[13]	147	D16	D14	-	-	-	-	[3]	I; PU	I/O	**P1[13] —** General purpose digital input/output pin.
										I	**ENET_RX_DV —** Ethernet Receive Data Valid (MII interface).

Table 3. Pin description *...continued*

Not all functions are available on all parts. See Table 2 (Ethernet, USB, LCD, QEI, SD/MMC, comparator pins) and Table 5 (EMC pins).

Symbol	Pin LQFP208	Ball TFBGA208	Ball TFBGA180	Pin LQFP144	Pin LQFP100	Pin LQFP80	Pin TFBGA80		Reset state[1]	Type[2]	Description
P1[14]	184	A7	D8	128	89	70	C6	[3]	I; PU	I/O	**P1[14] —** General purpose digital input/output pin.
										I	**ENET_RX_ER —** Ethernet receive error (RMII/MII interface).
										-	**R —** Function reserved.
										I	**T2_CAP0 —** Capture input for Timer 2, channel 0.
										-	**R —** Function reserved.
										I	**CMP0_IN[0] —** Comparator 0, input 0.
P1[15]	182	A8	A8	126	88	69	B6	[3]	I; PU	I/O	**P1[15] —** General purpose digital input/output pin.
										I	**ENET_RX_CLK (ENET_REF_CLK) —** Ethernet Receive Clock (MII interface) or Ethernet Reference Clock (RMII interface).
										-	**R —** Function reserved.
										I/O	**I2C2_SDA —** I^2C2 data input/output (this pin does not use a specialized I2C pad).
P1[16]	180	D10	B8	125	87	-	-	[3]	I; PU	I/O	**P1[16] —** General purpose digital input/output pin.
										O	**ENET_MDC —** Ethernet MIIM clock.
										O	**I2S_TX_MCLK —** I2S transmit master clock.
										-	**R —** Function reserved.
										-	**R —** Function reserved.
										I	**CMP0_IN[1] —** Comparator 0, input 1.
P1[17]	178	A9	C9	123	86	-	-	[3]	I; PU	I/O	**P1[17] —** General purpose digital input/output pin.
										I/O	**ENET_MDIO —** Ethernet MIIM data input and output.
										O	**I2S_RX_MCLK —** I2S receive master clock.
										-	**R —** Function reserved.
										-	**R —** Function reserved.
										I	**CMP0_IN[2] —** Comparator 0, input 2.

Table 3. Pin description *...continued*

Not all functions are available on all parts. See Table 2 (Ethernet, USB, LCD, QEI, SD/MMC, comparator pins) and Table 5 (EMC pins).

Symbol	Pin LQFP208	Ball TFBGA208	Ball TFBGA180	Pin LQFP144	Pin LQFP100	Pin LQFP80	Pin TFBGA80		Reset state[1]	Type[2]	Description
P1[18]	66	P7	L5	46	32	25	K4	[3]	I; PU	I/O	**P1[18] —** General purpose digital input/output pin.
										O	**USB_UP_LED1 —** It is LOW when the device is configured (non-control endpoints enabled), or when the host is enabled and has detected a device on the bus. It is HIGH when the device is not configured, or when host is enabled and has not detected a device on the bus, or during global suspend. It transitions between LOW and HIGH (flashes) when the host is enabled and detects activity on the bus.
										O	**PWM1[1] —** Pulse Width Modulator 1, channel 1 output.
										I	**T1_CAP0 —** Capture input for Timer 1, channel 0.
										-	**R —** Function reserved.
										I/O	**SSP1_MISO —** Master In Slave Out for SSP1.
P1[19]	68	U6	P5	47	33	26	J4	[3]	I; PU	I/O	**P1[19] —** General purpose digital input/output pin.
										O	**USB_TX_E1 —** Transmit Enable signal for USB port 1 (OTG transceiver).
										O	**$\overline{\text{USB\_PPWR1}}$ —** Port Power enable signal for USB port 1.
										I	**T1_CAP1 —** Capture input for Timer 1, channel 1.
										O	**MC_0A —** Motor control PWM channel 0, output A.
										I/O	**SSP1_SCK —** Serial clock for SSP1.
										O	**U2_OE —** RS-485/EIA-485 output enable signal for UART2.