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LPC4350/30/20/10

32-bit ARM Cortex-M4/M0 flashless MCU; up to 264 kB SRAM; Ethernet; two HS USBs; advanced configurable peripherals

Rev. 4.6 — 14 March 2016 Product data sheet

1. General description

The LPC4350/30/20/10 are ARM Cortex-M4 based microcontrollers for embedded applications which include an ARM Cortex-M0 coprocessor, up to 264 kB of SRAM, advanced configurable peripherals such as the State Configurable Timer/PWM (SCTimer/PWM) and the Serial General-Purpose I/O (SGPIO) interface, two high-speed USB controllers, Ethernet, LCD, an external memory controller, and multiple digital and analog peripherals. The LPC4350/30/20/10 operate at CPU frequencies of up to 204 MHz.

The ARM Cortex-M4 is a 32-bit core that offers system enhancements such as low power consumption, enhanced debug features, and a high level of support block integration. The ARM Cortex-M4 CPU incorporates a 3-stage pipeline, uses a Harvard architecture with separate local instruction and data buses as well as a third bus for peripherals, and includes an internal prefetch unit that supports speculative branching. The ARM Cortex-M4 supports single-cycle digital signal processing and SIMD instructions. A hardware floating-point processor is integrated in the core.

The ARM Cortex-M0 coprocessor is an energy-efficient and easy-to-use 32-bit core which is code- and tool-compatible with the Cortex-M4 core. The Cortex-M0 coprocessor offers up to 204 MHz performance with a simple instruction set and reduced code size. In LPC43x0, the Cortex-M0 coprocessor hardware multiply is implemented as a 32-cycle iterative multiplier.

See Section 17 “References” for additional documentation.

2. Features and benefits

- Cortex-M4 Processor core
  - ARM Cortex-M4 processor, running at frequencies of up to 204 MHz.
  - Built-in Memory Protection Unit (MPU) supporting eight regions.
  - Built-in Nested Vectored Interrupt Controller (NVIC).
  - Hardware floating-point unit.
  - Non-maskable Interrupt (NMI) input.
  - JTAG and Serial Wire Debug (SWD), serial trace, eight breakpoints, and four watch points.
  - Enhanced Trace Module (ETM) and Enhanced Trace Buffer (ETB) support.
  - System tick timer.

- Cortex-M0 Processor core
  - ARM Cortex-M0 co-processor capable of off-loading the main ARM Cortex-M4 application processor.
  - Running at frequencies of up to 204 MHz.
  - JTAG and built-in NVIC.
- On-chip memory
  - Up to 264 kB SRAM for code and data use.
  - Multiple SRAM blocks with separate bus access. Two SRAM blocks can be powered down individually.
  - 64 kB ROM containing boot code and on-chip software drivers.
  - 64 bit + 256 bit general-purpose One-Time Programmable (OTP) memory.
- Clock generation unit
  - Crystal oscillator with an operating range of 1 MHz to 25 MHz.
  - 12 MHz Internal RC (IRC) oscillator trimmed to 1.5 % accuracy over temperature and voltage.
  - Ultra-low power Real-Time Clock (RTC) crystal oscillator.
  - Three PLLs allow CPU operation up to the maximum CPU rate without the need for a high-frequency crystal. The second PLL is dedicated to the High-speed USB, the third PLL can be used as audio PLL.
  - Clock output.
- Configurable digital peripherals
  - Serial GPIO (SGPIO) interface.
  - State Configurable Timer (SCTimer/PWM) subsystem on AHB.
  - Global Input Multiplexer Array (GIMA) allows to cross-connect multiple inputs and outputs to event driven peripherals like the timers, SCTimer/PWM, and ADC0/1.
- Serial interfaces
  - Quad SPI Flash Interface (SPIFI) with 1-, 2-, or 4-bit data at rates of up to 52 MB per second.
  - 10/100T Ethernet MAC with RMII and MII interfaces and DMA support for high throughput at low CPU load. Support for IEEE 1588 time stamping/advanced time stamping (IEEE 1588-2008 v2).
  - One High-speed USB 2.0 Host/Device/OTG interface with DMA support and on-chip high-speed PHY (USB0).
  - One High-speed USB 2.0 Host/Device interface with DMA support, on-chip full-speed PHY and ULPI interface to external high-speed PHY (USB1).
  - USB interface electrical test software included in ROM USB stack.
  - Four 550 UARTs with DMA support: one UART with full modem interface; one UART with IrDA interface; three USARTs support UART synchronous mode and a smart card interface conforming to ISO7816 specification.
  - Up to two C_CAN 2.0B controllers with one channel each. Use of C_CAN controller excludes operation of all other peripherals connected to the same bus bridge. See Figure 1 and Ref. 2.
  - Two SSP controllers with FIFO and multi-protocol support. Both SSPs with DMA support.
  - One SPI controller.

- One Fast-mode Plus I^2C-bus interface with monitor mode and with open-drain I/O pins conforming to the full I^2C-bus specification. Supports data rates of up to 1 Mbit/s.
- One standard I^2C-bus interface with monitor mode and with standard I/O pins.
- Two I^2S interfaces, each with DMA support and with one input and one output.

- Digital peripherals
  - External Memory Controller (EMC) supporting external SRAM, ROM, NOR flash, and SDRAM devices.
  - LCD controller with DMA support and a programmable display resolution of up to 1024 H $\times$ 768 V. Supports monochrome and color STN panels and TFT color panels; supports 1/2/4/8 bpp Color Look-Up Table (CLUT) and 16/24-bit direct pixel mapping.
  - Secure Digital Input Output (SD/MMC) card interface.
  - Eight-channel General-Purpose DMA controller can access all memories on the AHB and all DMA-capable AHB slaves.
  - Up to 164 General-Purpose Input/Output (GPIO) pins with configurable pull-up/pull-down resistors.
  - GPIO registers are located on the AHB for fast access. GPIO ports have DMA support.
  - Up to eight GPIO pins can be selected from all GPIO pins as edge and level sensitive interrupt sources.
  - Two GPIO group interrupt modules enable an interrupt based on a programmable pattern of input states of a group of GPIO pins.
  - Four general-purpose timer/counters with capture and match capabilities.
  - One motor control Pulse Width Modulator (PWM) for three-phase motor control.
  - One Quadrature Encoder Interface (QEI).
  - Repetitive Interrupt timer (RI timer).
  - Windowed watchdog timer (WWDT).
  - Ultra-low power Real-Time Clock (RTC) on separate power domain with 256 bytes of battery powered backup registers.
  - Alarm timer; can be battery powered.
- Analog peripherals
  - One 10-bit DAC with DMA support and a data conversion rate of 400 kSamples/s.
  - Two 10-bit ADCs with DMA support and a data conversion rate of 400 kSamples/s. Up to eight input channels per ADC.
- Unique ID for each device.
- Power
  - Single 3.3 V (2.2 V to 3.6 V) power supply with on-chip internal voltage regulator for the core supply and the RTC power domain.
  - RTC power domain can be powered separately by a 3 V battery supply.
  - Four reduced power modes: Sleep, Deep-sleep, Power-down, and Deep power-down.
  - Processor wake-up from Sleep mode via wake-up interrupts from various peripherals.
  - Wake-up from Deep-sleep, Power-down, and Deep power-down modes via external interrupts and interrupts generated by battery powered blocks in the RTC power domain.

- Brownout detect with four separate thresholds for interrupt and forced reset.
- Power-On Reset (POR).
- Available as LBGA256, TFBGA180, and TFBGA100 packages and as LQFP144 package.

3. Applications

- Motor control
- Power management
- White goods
- RFID readers
- Embedded audio applications
- Industrial automation
- e-metering

4. Ordering information

Table 1. Ordering information

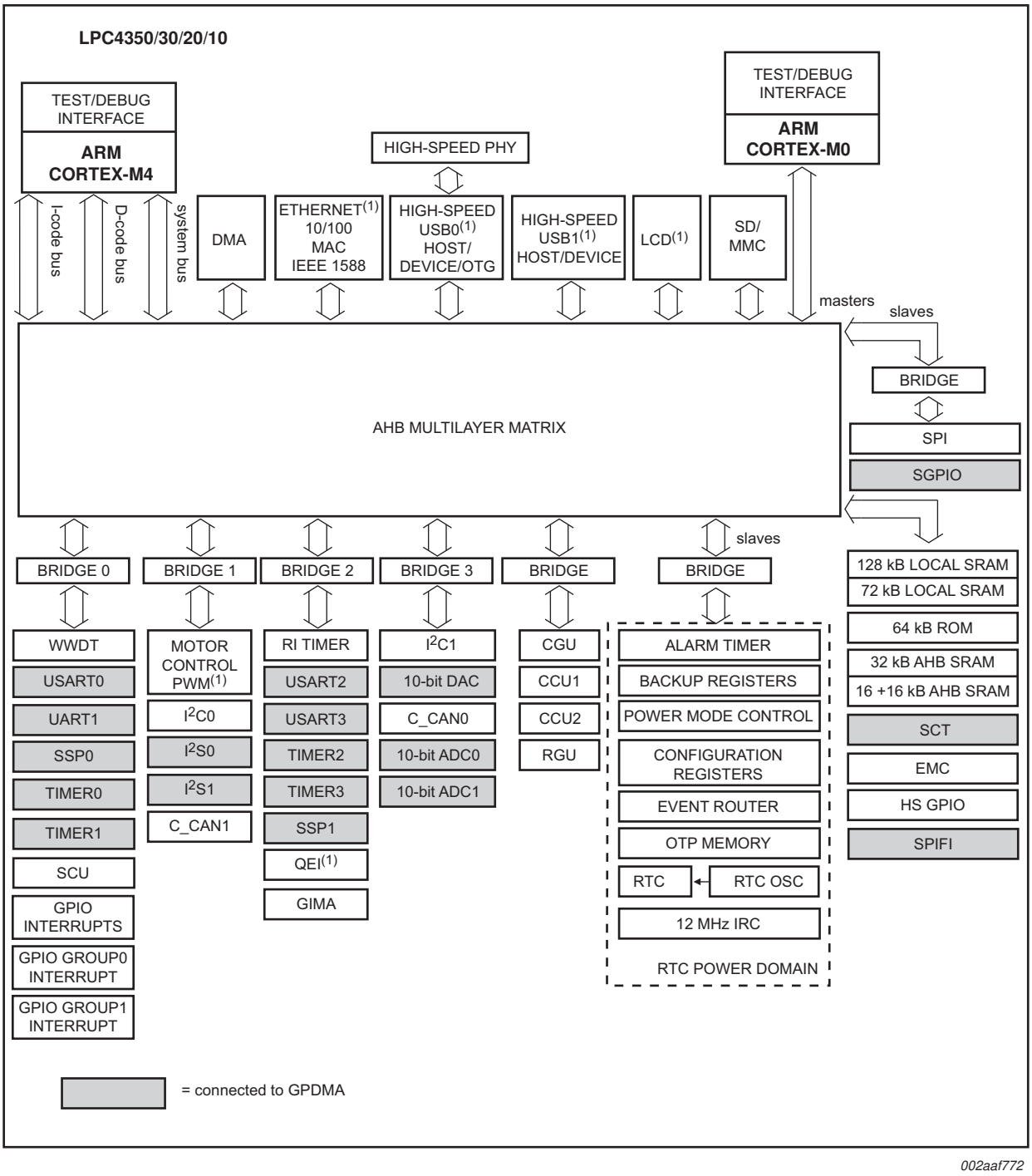
Type number	Package		
	Name	Description	Version
LPC4350FET256	LBGA256	Plastic low profile ball grid array package; 256 balls; body 17 × 17 × 1 mm	SOT740-2
LPC4350FET180	TFBGA180	Thin fine-pitch ball grid array package; 180 balls	SOT570-3
LPC4330FET256	LBGA256	Plastic low profile ball grid array package; 256 balls; body 17 × 17 × 1 mm	SOT740-2
LPC4330FET180	TFBGA180	Thin fine-pitch ball grid array package; 180 balls	SOT570-3
LPC4330FET100	TFBGA100	Plastic thin fine-pitch ball grid array package; 100 balls; body 9 × 9 × 0.7 mm	SOT926-1
LPC4330FBD144	LQFP144	Plastic low profile quad flat package; 144 leads; body 20 × 20 × 1.4 mm	SOT486-1
LPC4320FET100	TFBGA100	Plastic thin fine-pitch ball grid array package; 100 balls; body 9 × 9 × 0.7 mm	SOT926-1
LPC4320FBD144	LQFP144	Plastic low profile quad flat package; 144 leads; body 20 × 20 × 1.4 mm	SOT486-1
LPC4310FET100	TFBGA100	Plastic thin fine-pitch ball grid array package; 100 balls; body 9 × 9 × 0.7 mm	SOT926-1
LPC4310FBD144	LQFP144	Plastic low profile quad flat package; 144 leads; body 20 × 20 × 1.4 mm	SOT486-1

4.1 Ordering options

Table 2. Ordering options

Type number	Total SRAM	LCD	Ethernet	USB0 (Host, Device, OTG)	USB1 (Host, Device)/ ULPI interface	ADC channels	Motor control PWM	QEI	GPIO	Package
LPC4350FET256	264 kB	yes	yes	yes	yes/yes	8	yes	yes	164	LBGA256
LPC4350FET180	264 kB	yes	yes	yes	yes/yes	8	yes	yes	118	TFBGA180
LPC4330FET256	264 kB	no	yes	yes	yes/yes	8	yes	yes	164	LBGA256
LPC4330FET180	264 kB	no	yes	yes	yes/yes	8	yes	yes	118	TFBGA180
LPC4330FET100	264 kB	no	yes	yes	yes/no	4	no	no	49	TFBGA100
LPC4330FBD144	264 kB	no	yes	yes	yes/no	8	yes	no	83	LQFP144
LPC4320FET100	200 kB	no	no	yes	no	4	no	no	49	TFBGA100
LPC4320FBD144	200 kB	no	no	yes	no	8	yes	no	83	LQFP144
LPC4310FET100	168 kB	no	no	no	no	4	no	no	49	TFBGA100
LPC4310FBD144	168 kB	no	no	no	no	8	yes	no	83	LQFP144

5. Block diagram



(1) Not available on all parts (see Table 2).

Fig 1. LPC4350/30/20/10 Block diagram

6. Pinning information

6.1 Pinning

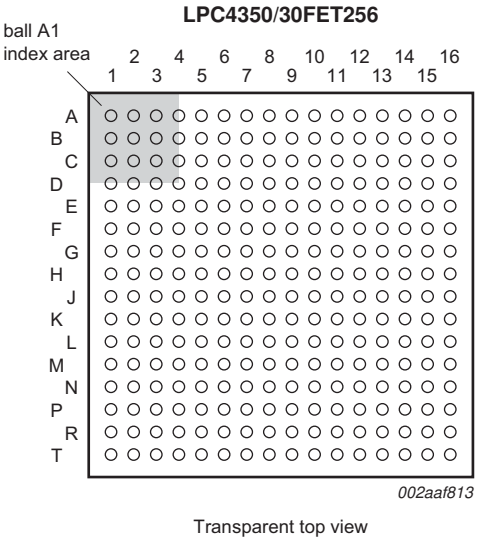


Fig 2. Pin configuration LBGA256 package

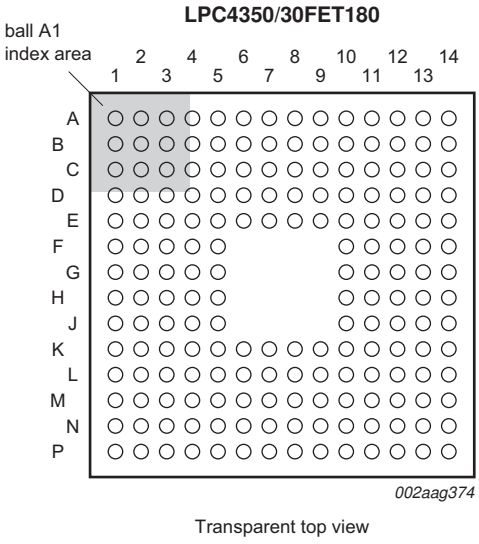


Fig 3. Pin configuration TFBGA180 package

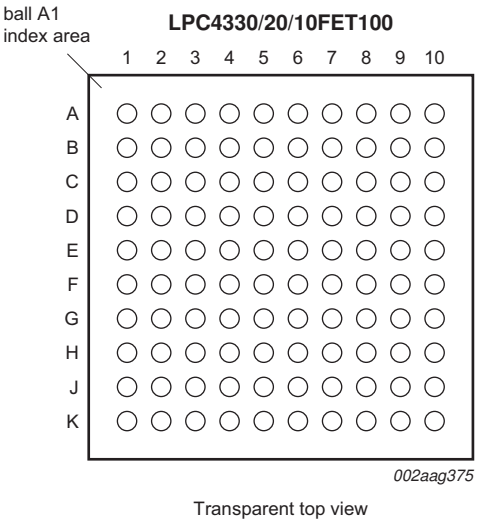


Fig 4. Pin configuration TFBGA100 package

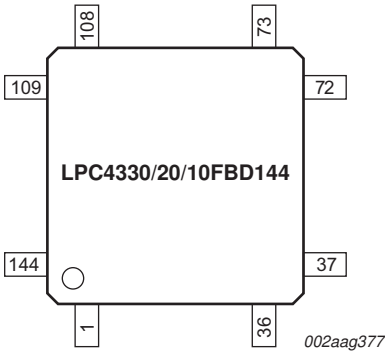


Fig 5. Pin configuration LQFP144 package

6.2 Pin description

On the LPC4350/30/20/10, digital pins are grouped into 16 ports, named P0 to P9 and PA to PF, with up to 20 pins used per port. Each digital pin can support up to eight different digital functions, including General-Purpose I/O (GPIO), selectable through the System Configuration Unit (SCU) registers. The pin name is not indicative of the GPIO port assigned to it.

Not all functions listed in Table 3 are available on all packages. See Table 2 for availability of USB0, USB1, Ethernet, and LCD functions.

The parts contain two 10-bit ADCs (ADC0 and ADC1). The input channels of ADC0 and ADC1 on dedicated pins and multiplexed pins are combined in such a way that all channel 0 inputs (named ADC0_0 and ADC1_0) are tied together and connected to both, channel 0 on ADC0 and channel 0 on ADC1, channel 1 inputs (named ADC0_1 and ADC1_1) are tied together and connected to channel 1 on ADC0 and ADC1, and so forth. There are eight ADC channels total for the two ADCs.

Table 3. Pin description

LCD, Ethernet, USB0, and USB1 functions are not available on all parts. See Table 2.

Symbol	LBGA256	TFBGA180	TFBGA100	LQFP144		Reset state [1]	Type	Description
Multiplexed digital pins								
P0_0	L3	K3	G2	32	[2]	N; PU	I/O	**GPIO0[0] —** General purpose digital input/output pin.
							I/O	**SSP1_MISO —** Master In Slave Out for SSP1.
							I	**ENET_RXD1 —** Ethernet receive data 1 (RMII/MII interface).
							I/O	**SGPIO0 —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							I/O	**I2S0_TX_WS —** Transmit Word Select. It is driven by the master and received by the slave. Corresponds to the signal WS in the *I²S-bus specification*.
							I/O	**I2S1_TX_WS —** Transmit Word Select. It is driven by the master and received by the slave. Corresponds to the signal WS in the *I²S-bus specification*.
P0_1	M2	K2	G1	34	[2]	N; PU	I/O	**GPIO0[1] —** General purpose digital input/output pin.
							I/O	**SSP1_MOSI —** Master Out Slave in for SSP1.
							I	**ENET_COL —** Ethernet Collision detect (MII interface).
							I/O	**SGPIO1 —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
								ENET_TX_EN — Ethernet transmit enable (RMII/MII interface).
							I/O	**I2S1_TX_SDA —** I2S1 transmit data. It is driven by the transmitter and read by the receiver. Corresponds to the signal SD in the *I²S-bus specification*.
P1_0	P2	L1	H1	38	[2]	N; PU	I/O	**GPIO0[4] —** General purpose digital input/output pin.
							I	**CTIN_3 —** SCTimer/PWM input 3. Capture input 1 of timer 1.
							I/O	**EMC_A5 —** External memory address line 5.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							I/O	**SSP0_SSEL —** Slave Select for SSP0.
							I/O	**SGPIO7 —** General purpose digital input/output pin.
							-	**R —** Function reserved.

Table 3. Pin description *...continued*

LCD, Ethernet, USB0, and USB1 functions are not available on all parts. See Table 2.

Symbol	LBGA256	TFBGA180	TFBGA100	LQFP144		Reset state [1]	Type	Description
P1_1	R2	N1	K2	42	[2]	N; PU	I/O	**GPIO0[8] —** General purpose digital input/output pin. Boot pin (see Table 5).
							O	**CTOUT_7 —** SCTimer/PWM output 7. Match output 3 of timer 1.
							I/O	**EMC_A6 —** External memory address line 6.
							I/O	**SGPIO8 —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							I/O	**SSP0_MISO —** Master In Slave Out for SSP0.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
P1_2	R3	N2	K1	43	[2]	N; PU	I/O	**GPIO0[9] —** General purpose digital input/output pin. Boot pin (see Table 5).
							O	**CTOUT_6 —** SCTimer/PWM output 6. Match output 2 of timer 1.
							I/O	**EMC_A7 —** External memory address line 7.
							I/O	**SGPIO9 —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							I/O	**SSP0_MOSI —** Master Out Slave in for SSP0.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
P1_3	P5	M2	J1	44	[2]	N; PU	I/O	**GPIO0[10] —** General purpose digital input/output pin.
							O	**CTOUT_8 —** SCTimer/PWM output 8. Match output 0 of timer 2.
							I/O	**SGPIO10 —** General purpose digital input/output pin.
							O	**$\overline{\text{EMC\_OE}}$ —** LOW active Output Enable signal.
							O	**USB0_IND1 —** USB0 port indicator LED control output 1.
							I/O	**SSP1_MISO —** Master In Slave Out for SSP1.
							-	**R —** Function reserved.
							O	**SD_RST —** SD/MMC reset signal for MMC4.4 card.
P1_4	T3	P2	J2	47	[2]	N; PU	I/O	**GPIO0[11] —** General purpose digital input/output pin.
							O	**CTOUT_9 —** SCTimer/PWM output 9. Match output 3 of timer 3.
							I/O	**SGPIO11 —** General purpose digital input/output pin.
							O	**$\overline{\text{EMC\_BLS0}}$ —** LOW active Byte Lane select signal 0.
							O	**USB0_IND0 —** USB0 port indicator LED control output 0.
							I/O	**SSP1_MOSI —** Master Out Slave in for SSP1.
							-	**R —** Function reserved.
							O	**SD_VOLT1 —** SD/MMC bus voltage select output 1.

Table 3. Pin description *...continued*

LCD, Ethernet, USB0, and USB1 functions are not available on all parts. See Table 2.

Symbol	LBGA256	TFBGA180	TFBGA100	LQFP144		Reset state [1]	Type	Description
P1_5	R5	N3	J4	48	[2]	N; PU	I/O	**GPIO1[8] —** General purpose digital input/output pin.
							O	**CTOUT_10 —** SCTimer/PWM output 10. Match output 3 of timer 3.
							-	**R —** Function reserved.
							O	**$\overline{\text{EMC\_CS0}}$ —** LOW active Chip Select 0 signal.
							I	**USB0_PWR_FAULT —** Port power fault signal indicating overcurrent condition; this signal monitors over-current on the USB bus (external circuitry required to detect over-current condition).
							I/O	**SSP1_SSEL —** Slave Select for SSP1.
							I/O	**SGPIO15 —** General purpose digital input/output pin.
							O	**SD_POW —** SD/MMC power monitor output.
P1_6	T4	P3	K4	49	[2]	N; PU	I/O	**GPIO1[9] —** General purpose digital input/output pin.
							I	**CTIN_5 —** SCTimer/PWM input 5. Capture input 2 of timer 2.
							-	**R —** Function reserved.
							O	**$\overline{\text{EMC\_WE}}$ —** LOW active Write Enable signal.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							I/O	**SGPIO14 —** General purpose digital input/output pin.
							I/O	**SD_CMD —** SD/MMC command signal.
P1_7	T5	N4	G4	50	[2]	N; PU	I/O	**GPIO1[0] —** General purpose digital input/output pin.
							I	**U1_DSR —** Data Set Ready input for UART1.
							O	**CTOUT_13 —** SCTimer/PWM output 13. Match output 3 of timer 3.
							I/O	**EMC_D0 —** External memory data line 0.
							O	**USB0_PPWR —** VBUS drive signal (towards external charge pump or power management unit); indicates that VBUS must be driven (active HIGH). Add a pull-down resistor to disable the power switch at reset. This signal has opposite polarity compared to the $\overline{\text{USB\_PPWR}}$ used on other NXP LPC parts.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.

Table 3. Pin description *...continued*

LCD, Ethernet, USB0, and USB1 functions are not available on all parts. See Table 2.

Symbol	LBGA256	TFBGA180	TFBGA100	LQFP144		Reset state [1]	Type	Description
P1_8	R7	M5	H5	51	[2]	N; PU	I/O	**GPIO1[1]** — General purpose digital input/output pin.
							O	**U1_DTR** — Data Terminal Ready output for UART1.
							O	**CTOUT_12** — SCTimer/PWM output 12. Match output 3 of timer 3.
							I/O	**EMC_D1** — External memory data line 1.
							-	**R** — Function reserved.
							-	**R** — Function reserved.
							-	**R** — Function reserved.
							O	**SD_VOLT0** — SD/MMC bus voltage select output 0.
P1_9	T7	N5	J5	52	[2]	N; PU	I/O	**GPIO1[2]** — General purpose digital input/output pin.
							O	**U1_RTS** — Request to Send output for UART1.
							O	**CTOUT_11** — SCTimer/PWM output 11. Match output 3 of timer 2.
							I/O	**EMC_D2** — External memory data line 2.
							-	**R** — Function reserved.
							-	**R** — Function reserved.
							-	**R** — Function reserved.
							I/O	**SD_DAT0** — SD/MMC data bus line 0.
P1_10	R8	N6	H6	53	[2]	N; PU	I/O	**GPIO1[3]** — General purpose digital input/output pin.
							I	**U1_RI** — Ring Indicator input for UART1.
							O	**CTOUT_14** — SCTimer/PWM output 14. Match output 2 of timer 3.
							I/O	**EMC_D3** — External memory data line 3.
							-	**R** — Function reserved.
							-	**R** — Function reserved.
							-	**R** — Function reserved.
							I/O	**SD_DAT1** — SD/MMC data bus line 1.
P1_11	T9	P8	J7	55	[2]	N; PU	I/O	**GPIO1[4]** — General purpose digital input/output pin.
							I	**U1_CTS** — Clear to Send input for UART1.
							O	**CTOUT_15** — SCTimer/PWM output 15. Match output 3 of timer 3.
							I/O	**EMC_D4** — External memory data line 4.
							-	**R** — Function reserved.
							-	**R** — Function reserved.
							-	**R** — Function reserved.
							I/O	**SD_DAT2** — SD/MMC data bus line 2.

Table 3. Pin description *...continued*

LCD, Ethernet, USB0, and USB1 functions are not available on all parts. See Table 2.

Symbol	LBGA256	TFBGA180	TFBGA100	LQFP144		Reset state [1]	Type	Description
P1_12	R9	P7	K7	56	[2]	N; PU	I/O	**GPIO1[5] —** General purpose digital input/output pin.
							I	**U1_DCD —** Data Carrier Detect input for UART1.
							-	**R —** Function reserved.
							I/O	**EMC_D5 —** External memory data line 5.
							I	**T0_CAP1 —** Capture input 1 of timer 0.
							-	**R —** Function reserved.
							I/O	**SGPIO8 —** General purpose digital input/output pin.
							I/O	**SD_DAT3 —** SD/MMC data bus line 3.
P1_13	R10	L8	H8	60	[2]	N; PU	I/O	**GPIO1[6] —** General purpose digital input/output pin.
							O	**U1_TXD —** Transmitter output for UART1.
							-	**R —** Function reserved.
							I/O	**EMC_D6 —** External memory data line 6.
							I	**T0_CAP0 —** Capture input 0 of timer 0.
							-	**R —** Function reserved.
							I/O	**SGPIO9 —** General purpose digital input/output pin.
							I	**SD_CD —** SD/MMC card detect input.
P1_14	R11	K7	J8	61	[2]	N; PU	I/O	**GPIO1[7] —** General purpose digital input/output pin.
							I	**U1_RXD —** Receiver input for UART1.
							-	**R —** Function reserved.
							I/O	**EMC_D7 —** External memory data line 7.
							O	**T0_MAT2 —** Match output 2 of timer 0.
							-	**R —** Function reserved.
							I/O	**SGPIO10 —** General purpose digital input/output pin.
							-	**R —** Function reserved.
P1_15	T12	P11	K8	62	[2]	N; PU	I/O	**GPIO0[2] —** General purpose digital input/output pin.
							O	**U2_TXD —** Transmitter output for USART2.
							I/O	**SGPIO2 —** General purpose digital input/output pin.
							I	**ENET_RXD0 —** Ethernet receive data 0 (RMII/MII interface).
							O	**T0_MAT1 —** Match output 1 of timer 0.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.

Table 3. Pin description *...continued*

LCD, Ethernet, USB0, and USB1 functions are not available on all parts. See Table 2.

Symbol	LBGA256	TFBGA180	TFBGA100	LQFP144		Reset state [1]	Type	Description
P1_16	M7	L5	H9	64	[2]	N; PU	I/O	**GPIO0[3] —** General purpose digital input/output pin.
							I	**U2_RXD —** Receiver input for USART2.
							I/O	**SGPIO3 —** General purpose digital input/output pin.
							I	**ENET_CRS —** Ethernet Carrier Sense (MII interface).
							O	**T0_MAT0 —** Match output 0 of timer 0.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							I	**ENET_RX_DV —** Ethernet Receive Data Valid (RMII/MII interface).
P1_17	M8	L6	H10	66	[3]	N; PU	I/O	**GPIO0[12] —** General purpose digital input/output pin.
							I/O	**U2_UCLK —** Serial clock input/output for USART2 in synchronous mode.
							-	**R —** Function reserved.
							I/O	**ENET_MDIO —** Ethernet MIIM data input and output.
							I	**T0_CAP3 —** Capture input 3 of timer 0.
							O	**CAN1_TD —** CAN1 transmitter output.
							I/O	**SGPIO11 —** General purpose digital input/output pin.
							-	**R —** Function reserved.
P1_18	N12	N10	J10	67	[2]	N; PU	I/O	**GPIO0[13] —** General purpose digital input/output pin.
							I/O	**U2_DIR —** RS-485/EIA-485 output enable/direction control for USART2.
							-	**R —** Function reserved.
							O	**ENET_TXD0 —** Ethernet transmit data 0 (RMII/MII interface).
							O	**T0_MAT3 —** Match output 3 of timer 0.
							I	**CAN1_RD —** CAN1 receiver input.
							I/O	**SGPIO12 —** General purpose digital input/output pin.
							-	**R —** Function reserved.
P1_19	M11	N9	K9	68	[2]	N; PU	I	**ENET_TX_CLK (ENET_REF_CLK) —** Ethernet Transmit Clock (MII interface) or Ethernet Reference Clock (RMII interface).
							I/O	**SSP1_SCK —** Serial clock for SSP1.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							O	**CLKOUT —** Clock output pin.
							-	**R —** Function reserved.
							O	**I2S0_RX_MCLK —** I2S receive master clock.
							I/O	**I2S1_TX_SCK —** Transmit Clock. It is driven by the master and received by the slave. Corresponds to the signal SCK in the I^2S-bus specification.

Table 3. Pin description *...continued*

LCD, Ethernet, USB0, and USB1 functions are not available on all parts. See Table 2.

Symbol	LBGA256	TFBGA180	TFBGA100	LQFP144		Reset state [1]	Type	Description
P1_20	M10	J10	K10	70	[2]	N; PU	I/O	**GPIO0[15] —** General purpose digital input/output pin.
							I/O	**SSP1_SSEL —** Slave Select for SSP1.
							-	**R —** Function reserved.
							O	**ENET_TXD1 —** Ethernet transmit data 1 (RMII/MII interface).
							I	**T0_CAP2 —** Capture input 2 of timer 0.
							-	**R —** Function reserved.
							I/O	**SGPIO13 —** General purpose digital input/output pin.
							-	**R —** Function reserved.
P2_0	T16	N14	G10	75	[2]	N; PU	I/O	**SGPIO4 —** General purpose digital input/output pin.
							O	**U0_TXD —** Transmitter output for USART0.
							I/O	**EMC_A13 —** External memory address line 13.
							O	**USB0_PPWR —** VBUS drive signal (towards external charge pump or power management unit); indicates that VBUS must be driven (active HIGH). Add a pull-down resistor to disable the power switch at reset. This signal has opposite polarity compared to the USB_PPWR used on other NXP LPC parts.
							I/O	**GPIO5[0] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							I	**T3_CAP0 —** Capture input 0 of timer 3.
							O	**ENET_MDC —** Ethernet MIIM clock.
P2_1	N15	M13	G7	81	[2]	N; PU	I/O	**SGPIO5 —** General purpose digital input/output pin.
							I	**U0_RXD —** Receiver input for USART0.
							I/O	**EMC_A12 —** External memory address line 12.
							I	**USB0_PWR_FAULT —** Port power fault signal indicating overcurrent condition; this signal monitors over-current on the USB bus (external circuitry required to detect over-current condition).
							I/O	**GPIO5[1] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							I	**T3_CAP1 —** Capture input 1 of timer 3.
							-	**R —** Function reserved.

Table 3. Pin description *...continued*

LCD, Ethernet, USB0, and USB1 functions are not available on all parts. See Table 2.

Symbol	LBGA256	TFBGA180	TFBGA100	LQFP144		Reset state [1]	Type	Description
P2_2	M15	L13	F5	84	[2]	N; PU	I/O	**SGPIO6 —** General purpose digital input/output pin.
							I/O	**U0_UCLK —** Serial clock input/output for USART0 in synchronous mode.
							I/O	**EMC_A11 —** External memory address line 11.
							O	**USB0_IND1 —** USB0 port indicator LED control output 1.
							I/O	**GPIO5[2] —** General purpose digital input/output pin.
							I	**CTIN_6 —** SCTimer/PWM input 6. Capture input 1 of timer 3.
							I	**T3_CAP2 —** Capture input 2 of timer 3.
							-	**R —** Function reserved.
P2_3	J12	G11	D8	87	[3]	N; PU	I/O	**SGPIO12 —** General purpose digital input/output pin.
							I/O	**I2C1_SDA —** I^2C1 data input/output (this pin does not use a specialized I2C pad).
							O	**U3_TXD —** Transmitter output for USART3.
							I	**CTIN_1 —** SCTimer/PWM input 1. Capture input 1 of timer 0. Capture input 1 of timer 2.
							I/O	**GPIO5[3] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							O	**T3_MAT0 —** Match output 0 of timer 3.
							O	**USB0_PPWR —** VBUS drive signal (towards external charge pump or power management unit); indicates that VBUS must be driven (active HIGH). Add a pull-down resistor to disable the power switch at reset. This signal has opposite polarity compared to the USB_PPWR used on other NXP LPC parts.
P2_4	K11	L9	D9	88	[3]	N; PU	I/O	**SGPIO13 —** General purpose digital input/output pin.
							I/O	**I2C1_SCL —** I^2C1 clock input/output (this pin does not use a specialized I2C pad).
							I	**U3_RXD —** Receiver input for USART3.
							I	**CTIN_0 —** SCTimer/PWM input 0. Capture input 0 of timer 0, 1, 2, 3.
							I/O	**GPIO5[4] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							O	**T3_MAT1 —** Match output 1 of timer 3.
							I	**USB0_PWR_FAULT —** Port power fault signal indicating overcurrent condition; this signal monitors over-current on the USB bus (external circuitry required to detect over-current condition).

Table 3. Pin description *...continued*

LCD, Ethernet, USB0, and USB1 functions are not available on all parts. See Table 2.

Symbol	LBGA256	TFBGA180	TFBGA100	LQFP144		Reset state [1]	Type	Description
P2_5	K14	J12	D10	91	[3]	N; PU	I/O	**SGPIO14 —** General purpose digital input/output pin.
							I	**CTIN_2 —** SCTimer/PWM input 2. Capture input 2 of timer 0.
							I	**USB1_VBUS —** Monitors the presence of USB1 bus power. **Note:** This signal must be HIGH for USB reset to occur.
							I	**ADCTRIG1 —** ADC trigger input 1.
							I/O	**GPIO5[5] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							O	**T3_MAT2 —** Match output 2 of timer 3.
							O	**USB0_IND0 —** USB0 port indicator LED control output 0.
P2_6	K16	J14	G9	95	[2]	N; PU	I/O	**SGPIO7 —** General purpose digital input/output pin.
							I/O	**U0_DIR —** RS-485/EIA-485 output enable/direction control for USART0.
							I/O	**EMC_A10 —** External memory address line 10.
							O	**USB0_IND0 —** USB0 port indicator LED control output 0.
							I/O	**GPIO5[6] —** General purpose digital input/output pin.
							I	**CTIN_7 —** SCTimer/PWM input 7.
							I	**T3_CAP3 —** Capture input 3 of timer 3.
							-	**R —** Function reserved.
P2_7	H14	G12	C10	96	[2]	N; PU	I/O	**GPIO0[7] —** General purpose digital input/output pin. If this pin is pulled LOW at reset, the part enters ISP mode using USART0.
							O	**CTOUT_1 —** SCTimer/PWM output 1. Match output 3 of timer 3.
							I/O	**U3_UCLK —** Serial clock input/output for USART3 in synchronous mode.
							I/O	**EMC_A9 —** External memory address line 9.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							O	**T3_MAT3 —** Match output 3 of timer 3.
							-	**R —** Function reserved.

Table 3. Pin description *...continued*

LCD, Ethernet, USB0, and USB1 functions are not available on all parts. See Table 2.

Symbol	LBGA256	TFBGA180	TFBGA100	LQFP144		Reset state [1]	Type	Description
P2_8	J16	H14	C6	98	[2]	N; PU	I/O	**SGPIO15 —** General purpose digital input/output pin. Boot pin (see Table 5).
							O	**CTOUT_0 —** SCTimer/PWM output 0. Match output 0 of timer 0.
							I/O	**U3_DIR —** RS-485/EIA-485 output enable/direction control for USART3.
							I/O	**EMC_A8 —** External memory address line 8.
							I/O	**GPIO5[7] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
P2_9	H16	G14	B10	102	[2]	N; PU	I/O	**GPIO1[10] —** General purpose digital input/output pin. Boot pin (see Table 5.
							O	**CTOUT_3 —** SCTimer/PWM output 3. Match output 3 of timer 0.
							I/O	**U3_BAUD —** Baud pin for USART3.
							I/O	**EMC_A0 —** External memory address line 0.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
P2_10	G16	F14	E8	104	[2]	N; PU	I/O	**GPIO0[14] —** General purpose digital input/output pin.
							O	**CTOUT_2 —** SCTimer/PWM output 2. Match output 2 of timer 0.
							O	**U2_TXD —** Transmitter output for USART2.
							I/O	**EMC_A1 —** External memory address line 1.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
P2_11	F16	E13	A9	105	[2]	N; PU	I/O	**GPIO1[11] —** General purpose digital input/output pin.
							O	**CTOUT_5 —** SCTimer/PWM output 5. Match output 3 of timer 3.
							I	**U2_RXD —** Receiver input for USART2.
							I/O	**EMC_A2 —** External memory address line 2.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.

Table 3. Pin description *...continued*

LCD, Ethernet, USB0, and USB1 functions are not available on all parts. See Table 2.

Symbol	LBGA256	TFBGA180	TFBGA100	LQFP144		Reset state [1]	Type	Description
P2_12	E15	D13	B9	106	[2]	N; PU	I/O	**GPIO1[12] —** General purpose digital input/output pin.
							O	**CTOUT_4 —** SCTimer/PWM output 4. Match output 3 of timer 3.
							-	**R —** Function reserved.
							I/O	**EMC_A3 —** External memory address line 3.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							I/O	**U2_UCLK —** Serial clock input/output for USART2 in synchronous mode.
P2_13	C16	E14	A10	108	[2]	N; PU	I/O	**GPIO1[13] —** General purpose digital input/output pin.
							I	**CTIN_4 —** SCTimer/PWM input 4. Capture input 2 of timer 1.
							-	**R —** Function reserved.
							I/O	**EMC_A4 —** External memory address line 4.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							I/O	**U2_DIR —** RS-485/EIA-485 output enable/direction control for USART2.
P3_0	F13	D12	A8	112	[2]	N; PU	I/O	**I2S0_RX_SCK —** I2S receive clock. It is driven by the master and received by the slave. Corresponds to the signal SCK in the *I^2S-bus specification*.
							O	**I2S0_RX_MCLK —** I2S receive master clock.
							I/O	**I2S0_TX_SCK —** Transmit Clock. It is driven by the master and received by the slave. Corresponds to the signal SCK in the I^2S-bus specification.
							O	**I2S0_TX_MCLK —** I2S transmit master clock.
							I/O	**SSP0_SCK —** Serial clock for SSP0.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.

Table 3. Pin description *...continued*

LCD, Ethernet, USB0, and USB1 functions are not available on all parts. See Table 2.

Symbol	LBGA256	TFBGA180	TFBGA100	LQFP144		Reset state [1]	Type	Description
P3_1	G11	D10	F7	114	[2]	N; PU	I/O	**I2S0_TX_WS —** Transmit Word Select. It is driven by the master and received by the slave. Corresponds to the signal WS in the *I²S-bus specification*.
							I/O	**I2S0_RX_WS —** Receive Word Select. It is driven by the master and received by the slave. Corresponds to the signal WS in the *I²S-bus specification*.
							I	**CAN0_RD —** CAN receiver input.
							O	**USB1_IND1 —** USB1 Port indicator LED control output 1.
							I/O	**GPIO5[8] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							O	**LCD_VD15 —** LCD data.
							-	**R —** Function reserved.
P3_2	F11	D9	G6	116	[2]	OL; PU	I/O	**I2S0_TX_SDA —** I2S transmit data. It is driven by the transmitter and read by the receiver. Corresponds to the signal SD in the *I²S-bus specification*.
							I/O	**I2S0_RX_SDA —** I2S Receive data. It is driven by the transmitter and read by the receiver. Corresponds to the signal SD in the *I²S-bus specification*.
							O	**CAN0_TD —** CAN transmitter output.
							O	**USB1_IND0 —** USB1 Port indicator LED control output 0.
							I/O	**GPIO5[9] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							O	**LCD_VD14 —** LCD data.
							-	**R —** Function reserved.
P3_3	B14	B13	A7	118	[4]	N; PU	-	**R —** Function reserved.
							I/O	**SPI_SCK —** Serial clock for SPI.
							I/O	**SSP0_SCK —** Serial clock for SSP0.
							O	**SPIFI_SCK —** Serial clock for SPIFI.
							O	**CGU_OUT1 —** CGU spare clock output 1.
							-	**R —** Function reserved.
							O	**I2S0_TX_MCLK —** I2S transmit master clock.
							I/O	**I2S1_TX_SCK —** Transmit Clock. It is driven by the master and received by the slave. Corresponds to the signal SCK in the I²S-bus specification.

Table 3. Pin description *...continued*

LCD, Ethernet, USB0, and USB1 functions are not available on all parts. See Table 2.

Symbol	LBGA256	TFBGA180	TFBGA100	LQFP144		Reset state [1]	Type	Description
P3_4	A15	C14	B8	119	[2]	N; PU	I/O	**GPIO1[14] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							I/O	**SPIFI_SIO3 —** I/O lane 3 for SPIFI.
							O	**U1_TXD —** Transmitter output for UART 1.
							I/O	**I2S0_TX_WS —** Transmit Word Select. It is driven by the master and received by the slave. Corresponds to the signal WS in the *I²S-bus specification*.
							I/O	**I2S1_RX_SDA —** I2S1 Receive data. It is driven by the transmitter and read by the receiver. Corresponds to the signal SD in the *I²S-bus specification*.
							O	**LCD_VD13 —** LCD data.
P3_5	C12	C11	B7	121	[2]	N; PU	I/O	**GPIO1[15] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							I/O	**SPIFI_SIO2 —** I/O lane 2 for SPIFI.
							I	**U1_RXD —** Receiver input for UART 1.
							I/O	**I2S0_TX_SDA —** I2S transmit data. It is driven by the transmitter and read by the receiver. Corresponds to the signal SD in the *I²S-bus specification*.
							I/O	**I2S1_RX_WS —** Receive Word Select. It is driven by the master and received by the slave. Corresponds to the signal WS in the *I²S-bus specification*.
							O	**LCD_VD12 —** LCD data.
P3_6	B13	B12	C7	122	[2]	N; PU	I/O	**GPIO0[6] —** General purpose digital input/output pin.
							I/O	**SPI_MISO —** Master In Slave Out for SPI.
							I/O	**SSP0_SSEL —** Slave Select for SSP0.
							I/O	**SPIFI_MISO —** Input 1 in SPIFI quad mode; SPIFI output IO1.
							-	**R —** Function reserved.
							I/O	**SSP0_MISO —** Master In Slave Out for SSP0.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
P3_7	C11	C10	D7	123	[2]	N; PU	-	**R —** Function reserved.
							I/O	**SPI_MOSI —** Master Out Slave In for SPI.
							I/O	**SSP0_MISO —** Master In Slave Out for SSP0.
							I/O	**SPIFI_MOSI —** Input I0 in SPIFI quad mode; SPIFI output IO0.
							I/O	**GPIO5[10] —** General purpose digital input/output pin.
							I/O	**SSP0_MOSI —** Master Out Slave in for SSP0.
							-	**R —** Function reserved.
							-	**R —** Function reserved.

Table 3. Pin description *...continued*

LCD, Ethernet, USB0, and USB1 functions are not available on all parts. See Table 2.

Symbol	LBGA256	TFBGA180	TFBGA100	LQFP144		Reset state [1]	Type	Description
P3_8	C10	C9	E7	124	[2]	N; PU	-	**R —** Function reserved.
							I	**SPI_SSEL —** Slave Select for SPI. Note that this pin in an input pin only. The SPI in master mode cannot drive the CS input on the slave. Any GPIO pin can be used for SPI chip select in master mode.
							I/O	**SSP0_MOSI —** Master Out Slave in for SSP0.
							I/O	**SPIFI_CS —** SPIFI serial flash chip select.
							I/O	**GPIO5[11] —** General purpose digital input/output pin.
							I/O	**SSP0_SSEL —** Slave Select for SSP0.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
P4_0	D5	D4	-	1	[2]	N; PU	I/O	**GPIO2[0] —** General purpose digital input/output pin.
							O	**MCOA0 —** Motor control PWM channel 0, output A.
							I	**NMI —** External interrupt input to NMI.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							O	**LCD_VD13 —** LCD data.
							I/O	**U3_UCLK —** Serial clock input/output for USART3 in synchronous mode.
							-	**R —** Function reserved.
P4_1	A1	D3	-	3	[5]	N; PU	I/O	**GPIO2[1] —** General purpose digital input/output pin.
							O	**CTOUT_1 —** SCTimer/PWM output 1. Match output 3 of timer 3.
							O	**LCD_VD0 —** LCD data.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							O	**LCD_VD19 —** LCD data.
							O	**U3_TXD —** Transmitter output for USART3.
							I	**ENET_COL —** Ethernet Collision detect (MII interface).
							AI	**ADC0_1 —** ADC0 and ADC1, input channel 1. Configure the pin as GPIO input and use the ADC function select register in the SCU to select the ADC.

Table 3. Pin description *...continued*

LCD, Ethernet, USB0, and USB1 functions are not available on all parts. See Table 2.

Symbol	LBGA256	TFBGA180	TFBGA100	LQFP144		Reset state [1]	Type	Description
P4_2	D3	A2	-	8	[2]	N; PU	I/O	**GPIO2[2] —** General purpose digital input/output pin.
							O	**CTOUT_0 —** SCTimer/PWM output 0. Match output 0 of timer 0.
							O	**LCD_VD3 —** LCD data.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							O	**LCD_VD12 —** LCD data.
							I	**U3_RXD —** Receiver input for USART3.
							I/O	**SGPIO8 —** General purpose digital input/output pin.
P4_3	C2	B2	-	7	[5]	N; PU	I/O	**GPIO2[3] —** General purpose digital input/output pin.
							O	**CTOUT_3 —** SCTimer/PWM output 3. Match output 3 of timer 0.
							O	**LCD_VD2 —** LCD data.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							O	**LCD_VD21 —** LCD data.
							I/O	**U3_BAUD —** Baud pin for USART3.
							I/O	**SGPIO9 —** General purpose digital input/output pin.
							AI	**ADC0_0 —** DAC output; ADC0 and ADC1, input channel 0. Configure the pin as GPIO input and use the ADC function select register in the SCU to select the ADC.
P4_4	B1	A1	-	9	[5]	N; PU	I/O	**GPIO2[4] —** General purpose digital input/output pin.
							O	**CTOUT_2 —** SCTimer/PWM output 2. Match output 2 of timer 0.
							O	**LCD_VD1 —** LCD data.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							O	**LCD_VD20 —** LCD data.
							I/O	**U3_DIR —** RS-485/EIA-485 output enable/direction control for USART3.
							I/O	**SGPIO10 —** General purpose digital input/output pin.
							O	**DAC —** DAC output. Shared between 10-bit ADC0/1 and DAC.. Configure the pin as GPIO input and use the analog function select register in the SCU to select the DAC.

Table 3. Pin description *...continued*

LCD, Ethernet, USB0, and USB1 functions are not available on all parts. See Table 2.

Symbol	LBGA256	TFBGA180	TFBGA100	LQFP144		Reset state [1]	Type	Description
P4_5	D2	C2	-	10	[2]	N; PU	I/O	**GPIO2[5] —** General purpose digital input/output pin.
							O	**CTOUT_5 —** SCTimer/PWM output 5. Match output 3 of timer 3.
							O	**LCD_FP —** Frame pulse (STN). Vertical synchronization pulse (TFT).
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							I/O	**SGPIO11 —** General purpose digital input/output pin.
P4_6	C1	B1	-	11	[2]	N; PU	I/O	**GPIO2[6] —** General purpose digital input/output pin.
							O	**CTOUT_4 —** SCTimer/PWM output 4. Match output 3 of timer 3.
							O	**LCD_ENAB/LCDM —** STN AC bias drive or TFT data enable input.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							I/O	**SGPIO12 —** General purpose digital input/output pin.
P4_7	H4	F4	-	14	[2]	O; PU	O	**LCD_DCLK —** LCD panel clock.
							I	**GP_CLKIN —** General-purpose clock input to the CGU.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							I/O	**I2S1_TX_SCK —** Transmit Clock. It is driven by the master and received by the slave. Corresponds to the signal SCK in the I^2S-bus specification.
							I/O	**I2S0_TX_SCK —** Transmit Clock. It is driven by the master and received by the slave. Corresponds to the signal SCK in the I^2S-bus specification.
P4_8	E2	D2	-	15	[2]	N; PU	-	**R —** Function reserved.
							I	**CTIN_5 —** SCTimer/PWM input 5. Capture input 2 of timer 2.
							O	**LCD_VD9 —** LCD data.
							-	**R —** Function reserved.
							I/O	**GPIO5[12] —** General purpose digital input/output pin.
							O	**LCD_VD22 —** LCD data.
							O	**CAN1_TD —** CAN1 transmitter output.
							I/O	**SGPIO13 —** General purpose digital input/output pin.

Table 3. Pin description *...continued*

LCD, Ethernet, USB0, and USB1 functions are not available on all parts. See Table 2.

Symbol	LBGA256	TFBGA180	TFBGA100	LQFP144		Reset state [1]	Type	Description
P4_9	L2	J2	-	33	[2]	N; PU	-	**R** — Function reserved.
							I	**CTIN_6** — SCTimer/PWM input 6. Capture input 1 of timer 3.
							O	**LCD_VD11** — LCD data.
							-	**R** — Function reserved.
							I/O	**GPIO5[13]** — General purpose digital input/output pin.
							O	**LCD_VD15** — LCD data.
							I	**CAN1_RD** — CAN1 receiver input.
							I/O	**SGPIO14** — General purpose digital input/output pin.
P4_10	M3	L3	-	35	[2]	N; PU	-	**R** — Function reserved.
							I	**CTIN_2** — SCTimer/PWM input 2. Capture input 2 of timer 0.
							O	**LCD_VD10** — LCD data.
							-	**R** — Function reserved.
							I/O	**GPIO5[14]** — General purpose digital input/output pin.
							O	**LCD_VD14** — LCD data.
							-	**R** — Function reserved.
							I/O	**SGPIO15** — General purpose digital input/output pin.
P5_0	N3	L2	-	37	[2]	N; PU	I/O	**GPIO2[9]** — General purpose digital input/output pin.
							O	**MCOB2** — Motor control PWM channel 2, output B.
							I/O	**EMC_D12** — External memory data line 12.
							-	**R** — Function reserved.
							I	**U1_DSR** — Data Set Ready input for UART 1.
							I	**T1_CAP0** — Capture input 0 of timer 1.
							-	**R** — Function reserved.
							-	**R** — Function reserved.
P5_1	P3	M1	-	39	[2]	N; PU	I/O	**GPIO2[10]** — General purpose digital input/output pin.
							I	**MCI2** — Motor control PWM channel 2, input.
							I/O	**EMC_D13** — External memory data line 13.
							-	**R** — Function reserved.
							O	**U1_DTR** — Data Terminal Ready output for UART 1. Can also be configured to be an RS-485/EIA-485 output enable signal for UART 1.
							I	**T1_CAP1** — Capture input 1 of timer 1.
							-	**R** — Function reserved.
							-	**R** — Function reserved.