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# LPC4370

**32-bit ARM Cortex-M4 + 2 x M0 MCU; 282 kB SRAM; Ethernet; two HS USBs; 80 Msps 12-bit ADC; configurable peripherals**

Rev. 2.3 — 15 March 2016

Product data sheet

## 1. General description

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The LPC4370 are ARM Cortex-M4 based microcontrollers for embedded applications which include an ARM Cortex-M0 coprocessor and an ARM Cortex-M0 subsystem for managing peripherals, 282 kB of SRAM, advanced configurable peripherals such as the State Configurable Timer (SCTimer/PWM) and the Serial General Purpose I/O (SGPIO) interface, two high-speed USB controllers, Ethernet, LCD, an external memory controller, and multiple digital and analog peripherals, including a high-speed 12-bit ADC. The LPC4370 operate at CPU frequencies of up to 204 MHz.

The ARM Cortex-M4 is a 32-bit core that offers system enhancements such as low power consumption, enhanced debug features, and a high level of support block integration. The ARM Cortex-M4 CPU incorporates a 3-stage pipeline, uses a Harvard architecture with separate local instruction and data buses as well as a third bus for peripherals, and includes an internal prefetch unit that supports speculative branching. The ARM Cortex-M4 supports single-cycle digital signal processing and SIMD instructions. A hardware floating-point processor is integrated in the core.

The LPC4370 include an application ARM Cortex-M0 coprocessor and a second ARM Cortex-M0 subsystem for managing the SGPIO and SPI peripherals. The ARM Cortex-M0 core is an energy-efficient and easy-to-use 32-bit core which is code- and tool-compatible with the Cortex-M4 core. Both Cortex-M0 cores offer up to 204 MHz performance with a simple instruction set and reduced code size. In LPC43x0, the Cortex-M0 coprocessor hardware multiply is implemented as a 32-cycle iterative multiplier.

## 2. Features and benefits

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- Main Cortex-M4 processor
  - ◆ ARM Cortex-M4 processor, running at frequencies of up to 204 MHz.
  - ◆ ARM Cortex-M4 built-in Memory Protection Unit (MPU) supporting eight regions.
  - ◆ ARM Cortex-M4 built-in Nested Vectored Interrupt Controller (NVIC).
  - ◆ Hardware floating-point unit.
  - ◆ Non-maskable Interrupt (NMI) input.
  - ◆ JTAG and Serial Wire Debug (SWD), serial trace, eight breakpoints, and four watch points.
  - ◆ Enhanced Trace Module (ETM) and Enhanced Trace Buffer (ETB) support.
  - ◆ System tick timer.
- Cortex-M0 coprocessor
  - ◆ ARM Cortex-M0 coprocessor capable of off-loading the main ARM Cortex-M4 processor.



- ◆ Running at frequencies of up to 204 MHz.
- ◆ JTAG and built-in NVIC.
- Cortex-M0 subsystem
  - ◆ ARM Cortex-M0 processor controlling the SPI and SGPIO peripherals residing on a separate AHB multilayer matrix with direct access to 2 kB + 16 kB of SRAM.
  - ◆ Running at frequencies of up to 204 MHz.
  - ◆ Connected via a core-to-core bridge to the main AHB multilayer matrix and the main ARM Cortex-M4 processor.
  - ◆ JTAG and built-in NVIC.
- On-chip memory
  - ◆ 264 kB SRAM for code and data use on the main AHB multilayer matrix plus 18 kB of SRAM on the Cortex-M0 subsystem.
  - ◆ Multiple SRAM blocks with separate bus access. Two SRAM blocks can be powered down individually.
  - ◆ 64 kB ROM containing boot code and on-chip software drivers.
  - ◆ 64-bit + 256 bit general-purpose One-Time Programmable (OTP) memory.
- Configurable digital peripherals
  - ◆ Serial GPIO (SGPIO) interface.
  - ◆ State Configurable Timer (SCTimer/PWM) subsystem on AHB.
  - ◆ Global Input Multiplexer Array (GIMA) allows to cross-connect multiple inputs and outputs to event driven peripherals like the timers, SCTimer/PWM, and ADC0/1.
- Serial interfaces
  - ◆ Quad SPI Flash Interface (SPIFI) with four lanes and up to 52 MB per second.
  - ◆ 10/100T Ethernet MAC with RMII and MII interfaces and DMA support for high throughput at low CPU load. Support for IEEE 1588 time stamping/advanced time stamping (IEEE 1588-2008 v2).
  - ◆ One High-speed USB 2.0 Host/Device/OTG interface with DMA support and on-chip high-speed PHY.
  - ◆ One High-speed USB 2.0 Host/Device interface with DMA support, on-chip full-speed PHY and ULPI interface to external high-speed PHY.
  - ◆ USB interface electrical test software included in ROM USB stack.
  - ◆ One 550 UART with DMA support and full modem interface.
  - ◆ Three 550 USARTs with DMA and synchronous mode support and a smart card interface conforming to ISO7816 specification. One USART with IrDA interface.
  - ◆ Two C\_CAN 2.0B controllers with one channel each. Use of C\_CAN controller excludes operation of all other peripherals connected to the same bus bridge. See [Figure 1](#) and [Ref. 1](#).
  - ◆ Two SSP controllers with FIFO and multi-protocol support. Both SSPs with DMA support.
  - ◆ One SPI controller.
  - ◆ One Fast-mode Plus I<sup>2</sup>C-bus interface with monitor mode and with open-drain I/O pins conforming to the full I<sup>2</sup>C-bus specification. Supports data rates of up to 1 Mbit/s.
  - ◆ One standard I<sup>2</sup>C-bus interface with monitor mode and with standard I/O pins.
  - ◆ Two I<sup>2</sup>S interfaces, each with DMA support and with one input and one output.
- Digital peripherals

- ◆ External Memory Controller (EMC) supporting external SRAM, ROM, NOR flash, and SDRAM devices.
- ◆ LCD controller with DMA support and a programmable display resolution of up to 1024 H × 768 V. Supports monochrome and color STN panels and TFT color panels; supports 1/2/4/8 bpp Color Look-Up Table (CLUT) and 16/24-bit direct pixel mapping.
- ◆ Secure Digital Input Output (SD/MMC) card interface.
- ◆ Eight-channel General-Purpose DMA (GPDMA) controller can access all memories on the AHB and all DMA-capable AHB slaves.
- ◆ 164 General-Purpose Input/Output (GPIO) pins with configurable pull-up/pull-down resistors and open-drain mode.
- ◆ GPIO registers are located on the AHB for fast access. GPIO ports have DMA support.
- ◆ Up to eight GPIO pins can be selected from all GPIO pins as edge and level sensitive interrupt sources.
- ◆ Two GPIO group interrupt modules enable an interrupt based on a programmable pattern of input states of a group of GPIO pins.
- ◆ Four general-purpose timer/counters with capture and match capabilities.
- ◆ One motor control Pulse Width Modulator (PWM) for three-phase motor control.
- ◆ One Quadrature Encoder Interface (QEI).
- ◆ Repetitive Interrupt timer (RI timer).
- ◆ Windowed watchdog timer (WWDT).
- ◆ Ultra-low power Real-Time Clock (RTC) on separate power domain with 256 bytes of battery powered backup registers.
- ◆ Alarm timer; can be battery powered.
- Analog peripherals
  - ◆ One 10-bit DAC with DMA support and a data conversion rate of 400 kSamples/s. LBG256 package only.
  - ◆ Two 8-channel, 10-bit ADCs (ADC0/1) with DMA support and a data conversion rate of 400 kSamples/s for a total of 16 independent channels. The 10-bit ADCs are only available on the LBG256 package.
  - ◆ One 6-channel, 12-bit high-speed ADC (ADCHS) with DMA support and a data conversion rate of 80 MSamples/s.
- Unique ID for each device.
- Clock generation unit
  - ◆ Crystal oscillator with an operating range of 1 MHz to 25 MHz.
  - ◆ 12 MHz Internal RC (IRC) oscillator trimmed to 1 % accuracy over temperature and voltage.
  - ◆ Ultra-low power Real-Time Clock (RTC) crystal oscillator.
  - ◆ Three PLLs allow CPU operation up to the maximum CPU rate without the need for a high-frequency crystal. The second PLL is dedicated to the High-speed USB, the third PLL can be used as audio PLL.
  - ◆ Clock output.
- Power
  - ◆ Single 3.3 V (2.2 V to 3.6 V) power supply with on-chip DC-to-DC converter for the core supply and the RTC power domain.
  - ◆ RTC power domain can be powered separately by a 3 V battery supply.

- ◆ Four reduced power modes: Sleep, Deep-sleep, Power-down, and Deep power-down.
- ◆ Processor wake-up from Sleep mode via wake-up interrupts from various peripherals.
- ◆ Wake-up from Deep-sleep, Power-down, and Deep power-down modes via external interrupts and interrupts generated by battery powered blocks in the RTC power domain.
- ◆ Brownout detect with four separate thresholds for interrupt and forced reset.
- ◆ Power-On Reset (POR).
- ◆ Available as LBG256 and TFBGA100 packages.

### 3. Applications

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- Motor control
- Power management
- White goods
- RFID readers
- Embedded audio applications
- Industrial automation
- e-metering

## 4. Ordering information

Table 1. Ordering information

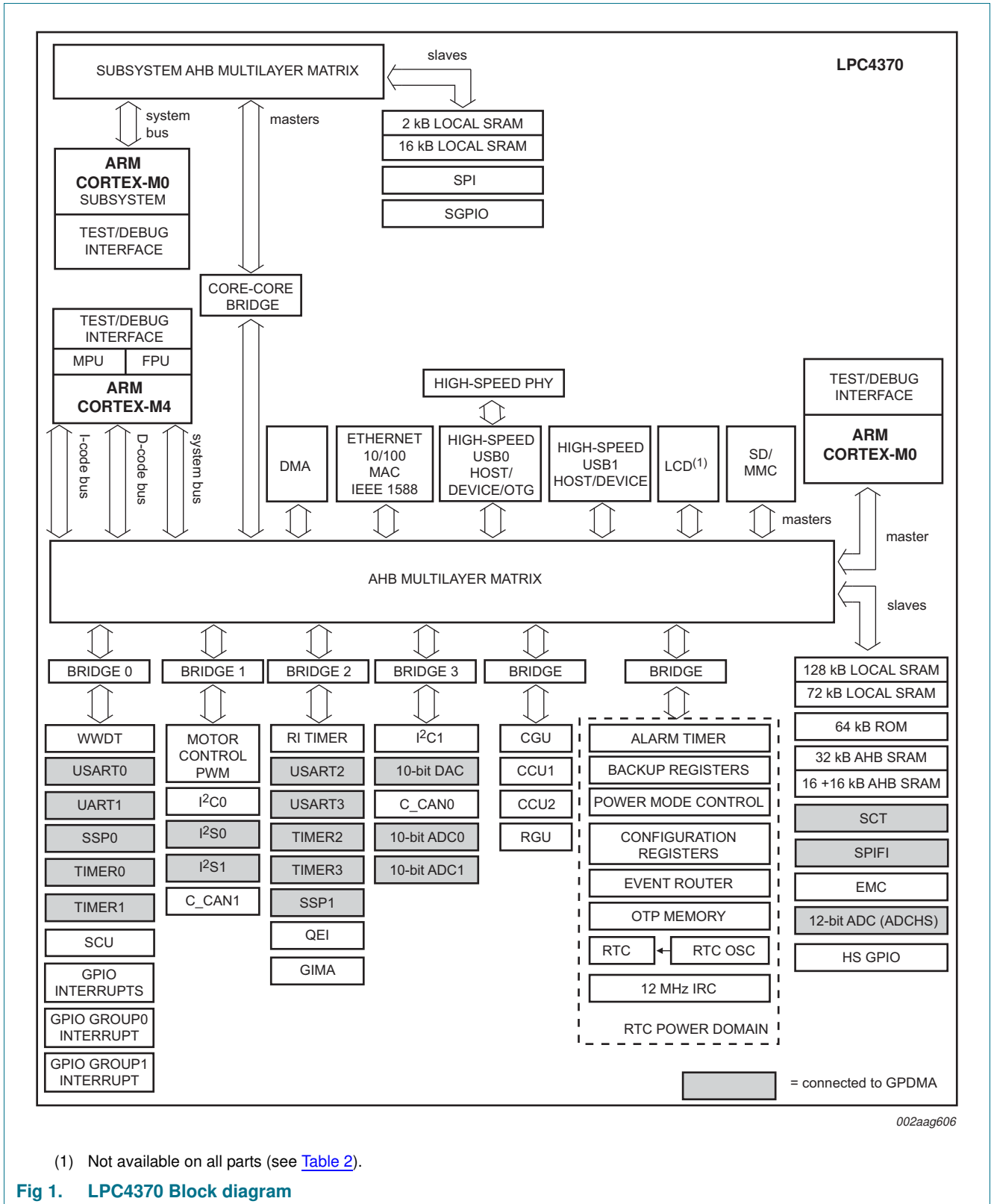
Type number	Package		
	Name	Description	Version
LPC4370FET256	LBGA256	Plastic low profile ball grid array package; 256 balls; body 17 × 17 × 1 mm	SOT740-2
LPC4370FET100	TFBGA100	Plastic thin fine-pitch ball grid array package; 100 balls; body 9 × 9 × 0.7 mm	SOT926-1

### 4.1 Ordering options

Table 2. Ordering options

Type number	Total SRAM	LCD	Ethernet	USB0 (Host, Device, OTG)	USB1 (Host, Device)/ULPI interface	10-bit ADC channels ADC0/ADC1	12-bit ADC channels	Motor control PWM	QEI	GPIO	Package
LPC4370FET256	282 kB	yes	yes	yes	yes/yes	8/8	6	yes	yes	164	LBGA256
LPC4370FET100	282 kB	no	yes	yes	yes/no	n/a	3	no	no	49	TFBGA100

5. Block diagram



## 6. Pinning information

### 6.1 Pinning

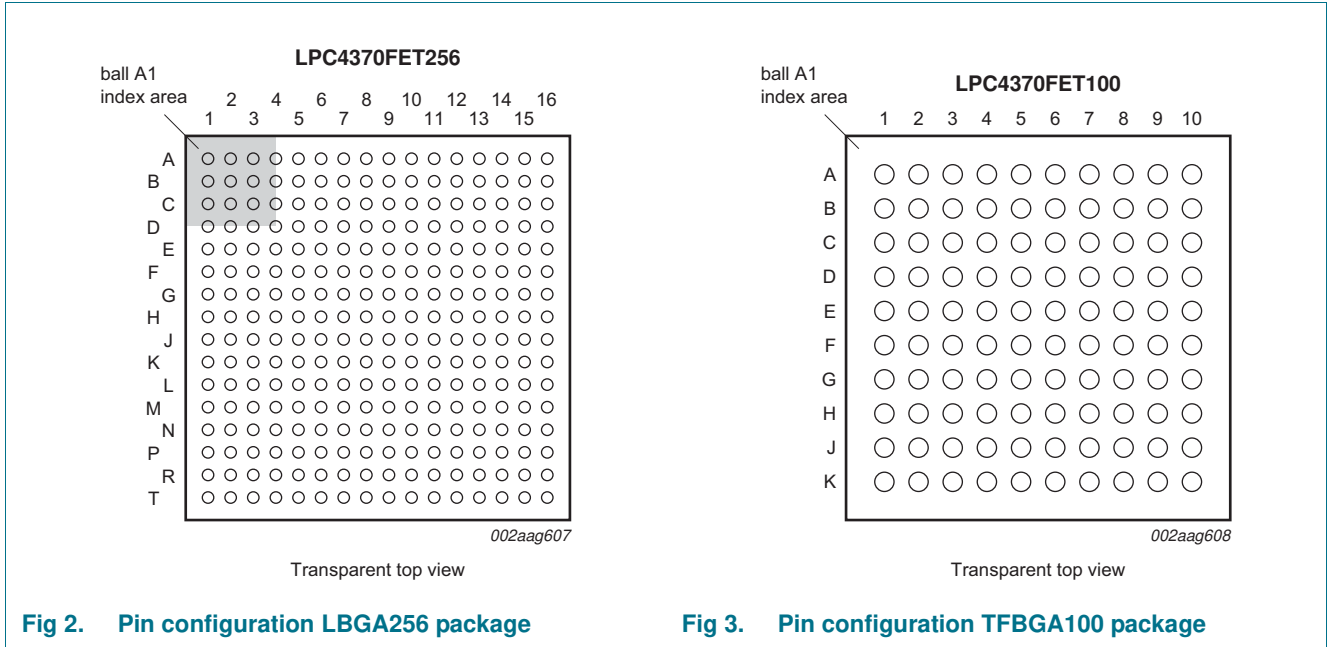


Fig 2. Pin configuration LPGA256 package

Fig 3. Pin configuration TFBGA100 package

### 6.2 Pin description

On the LPC4370, digital pins are grouped into 16 ports, named P0 to P9 and PA to PF, with up to 20 pins used per port. Each digital pin can support up to eight different digital functions, including General Purpose I/O (GPIO), selectable through the System Configuration Unit (SCU) registers. The pin name is not indicative of the GPIO port assigned to it.

Not all functions listed in [Table 3](#) are available on all packages. See [Table 2](#) for availability of USB0, USB1, Ethernet, and LCD functions.



**Table 3. Pin description**

LCD, Ethernet, USB0, and USB1 functions are not available on all parts. See [Table 2](#).

Symbol	LBGA256	TFBGA100		Reset state <a href="#">[2]</a>	Type	Description
<b>Multiplexed digital pins</b>						
P0_0	L3	G2	<a href="#">[3]</a>	I; PU	I/O	<b>GPIO0[0]</b> — General purpose digital input/output pin.
					I/O	<b>SSP1_MISO</b> — Master In Slave Out for SSP1.
					I	<b>ENET_RXD1</b> — Ethernet receive data 1 (RMII/MII interface).
					I/O	<b>SGPIO0</b> — General purpose digital input/output pin.
					-	<b>R</b> — Function reserved.
					-	<b>R</b> — Function reserved.
					I/O	<b>I2S0_TX_WS</b> — Transmit Word Select. It is driven by the master and received by the slave. Corresponds to the signal WS in the <i>I<sup>2</sup>S-bus specification</i> .
P0_1	M2	G1	<a href="#">[3]</a>	I; PU	I/O	<b>GPIO0[1]</b> — General purpose digital input/output pin.
					I/O	<b>SSP1_MOSI</b> — Master Out Slave in for SSP1.
					I	<b>ENET_COL</b> — Ethernet Collision detect (MII interface).
					I/O	<b>SGPIO1</b> — General purpose digital input/output pin.
					-	<b>R</b> — Function reserved.
					-	<b>R</b> — Function reserved.
					I/O	<b>ENET_TX_EN</b> — Ethernet transmit enable (RMII/MII interface).
P1_0	P2	H1	<a href="#">[3]</a>	I; PU	I/O	<b>GPIO0[4]</b> — General purpose digital input/output pin.
					I	<b>CTIN_3</b> — SCT input 3. Capture input 1 of timer 1.
					I/O	<b>EMC_A5</b> — External memory address line 5.
					-	<b>R</b> — Function reserved.
					-	<b>R</b> — Function reserved.
					I/O	<b>SSP0_SSEL</b> — Slave Select for SSP0.
					I/O	<b>SGPIO7</b> — General purpose digital input/output pin.
P1_1	R2	K2	<a href="#">[3]</a>	I; PU	I/O	<b>GPIO0[8]</b> — General purpose digital input/output pin. Boot pin (see <a href="#">Table 5</a> ).
					O	<b>CTOUT_7</b> — SCT output 7. Match output 3 of timer 1.
					I/O	<b>EMC_A6</b> — External memory address line 6.
					I/O	<b>SGPIO8</b> — General purpose digital input/output pin.
					-	<b>R</b> — Function reserved.
					I/O	<b>SSP0_MISO</b> — Master In Slave Out for SSP0.
					-	<b>R</b> — Function reserved.
-	<b>R</b> — Function reserved.					

**Table 3. Pin description ...continued**

LCD, Ethernet, USB0, and USB1 functions are not available on all parts. See [Table 2](#).

Symbol	LBGA256	TFBGA100		Reset state <a href="#">2</a>	Type	Description
P1_2	R3	K1	<a href="#">3</a>	I; PU	I/O	<b>GPIO0[9]</b> — General purpose digital input/output pin. Boot pin (see <a href="#">Table 5</a> ).
					O	<b>CTOUT_6</b> — SCT output 6. Match output 2 of timer 1.
					I/O	<b>EMC_A7</b> — External memory address line 7.
					I/O	<b>SGPIO9</b> — General purpose digital input/output pin.
					-	<b>R</b> — Function reserved.
					I/O	<b>SSP0_MOSI</b> — Master Out Slave in for SSP0.
					-	<b>R</b> — Function reserved.
P1_3	P5	J1	<a href="#">3</a>	I; PU	I/O	<b>GPIO0[10]</b> — General purpose digital input/output pin.
					O	<b>CTOUT_8</b> — SCT output 8. Match output 0 of timer 2.
					I/O	<b>SGPIO10</b> — General purpose digital input/output pin.
					O	<b>EMC_OE</b> — LOW active Output Enable signal.
					O	<b>USB0_IND1</b> — USB0 port indicator LED control output 1.
					I/O	<b>SSP1_MISO</b> — Master In Slave Out for SSP1.
					-	<b>R</b> — Function reserved.
P1_4	T3	J2	<a href="#">3</a>	I; PU	I/O	<b>GPIO0[11]</b> — General purpose digital input/output pin.
					O	<b>CTOUT_9</b> — SCT output 9. Match output 1 of timer 2.
					I/O	<b>SGPIO11</b> — General purpose digital input/output pin.
					O	<b>EMC_BLS0</b> — LOW active Byte Lane select signal 0.
					O	<b>USB0_IND0</b> — USB0 port indicator LED control output 0.
					I/O	<b>SSP1_MOSI</b> — Master Out Slave in for SSP1.
					-	<b>R</b> — Function reserved.
P1_5	R5	J4	<a href="#">3</a>	I; PU	I/O	<b>GPIO1[8]</b> — General purpose digital input/output pin.
					O	<b>CTOUT_10</b> — SCT output 10. Match output 2 of timer 2.
					-	<b>R</b> — Function reserved.
					O	<b>EMC_CS0</b> — LOW active Chip Select 0 signal.
					I	<b>USB0_PWR_FAULT</b> — Port power fault signal indicating overcurrent condition; this signal monitors over-current on the USB bus (external circuitry required to detect over-current condition).
					I/O	<b>SSP1_SSEL</b> — Slave Select for SSP1.
					I/O	<b>SGPIO15</b> — General purpose digital input/output pin.
O	<b>SD_POW</b> — SD/MMC power monitor output.					

**Table 3. Pin description ...continued**

LCD, Ethernet, USB0, and USB1 functions are not available on all parts. See [Table 2](#).

Symbol	LPGA256	TFBGA100		Reset state [2]	Type	Description
P1_6	T4	K4	[3]	I; PU	I/O	<b>GPIO1[9]</b> — General purpose digital input/output pin.
					I	<b>CTIN_5</b> — SCT input 5. Capture input 2 of timer 2.
					-	<b>R</b> — Function reserved.
					O	<b>EMC_WE</b> — LOW active Write Enable signal.
					-	<b>R</b> — Function reserved.
					-	<b>R</b> — Function reserved.
					I/O	<b>SGPIO14</b> — General purpose digital input/output pin.
					I/O	<b>SD_CMD</b> — SD/MMC command signal.
P1_7	T5	G4	[3]	I; PU	I/O	<b>GPIO1[0]</b> — General purpose digital input/output pin.
					I	<b>U1_DSR</b> — Data Set Ready input for UART1.
					O	<b>CTOUT_13</b> — SCT output 13. Match output 1 of timer 3.
					I/O	<b>EMC_D0</b> — External memory data line 0.
					O	<b>USB0_PPWR</b> — VBUS drive signal (towards external charge pump or power management unit); indicates that VBUS must be driven (active HIGH). Add a pull-down resistor to disable the power switch at reset. This signal has opposite polarity compared to the USB_PPWR used on other NXP LPC parts.
					-	<b>R</b> — Function reserved.
					-	<b>R</b> — Function reserved.
					-	<b>R</b> — Function reserved.
P1_8	R7	H5	[3]	I; PU	I/O	<b>GPIO1[1]</b> — General purpose digital input/output pin.
					O	<b>U1_DTR</b> — Data Terminal Ready output for UART1.
					O	<b>CTOUT_12</b> — SCT output 12. Match output 0 of timer 3.
					I/O	<b>EMC_D1</b> — External memory data line 1.
					-	<b>R</b> — Function reserved.
					-	<b>R</b> — Function reserved.
					-	<b>R</b> — Function reserved.
					O	<b>SD_VOLT0</b> — SD/MMC bus voltage select output 0.
P1_9	T7	J5	[3]	I; PU	I/O	<b>GPIO1[2]</b> — General purpose digital input/output pin.
					O	<b>U1_RTS</b> — Request to Send output for UART1.
					O	<b>CTOUT_11</b> — SCT output 11. Match output 3 of timer 2.
					I/O	<b>EMC_D2</b> — External memory data line 2.
					-	<b>R</b> — Function reserved.
					-	<b>R</b> — Function reserved.
					-	<b>R</b> — Function reserved.
					I/O	<b>SD_DAT0</b> — SD/MMC data bus line 0.

**Table 3. Pin description ...continued**

LCD, Ethernet, USB0, and USB1 functions are not available on all parts. See [Table 2](#).

Symbol	LBGA256	TFBGA100		Reset state ②	Type	Description
P1_10	R8	H6	③	I; PU	I/O	<b>GPIO1[3]</b> — General purpose digital input/output pin.
					I	<b>U1_RI</b> — Ring Indicator input for UART1.
					O	<b>CTOUT_14</b> — SCT output 14. Match output 2 of timer 3.
					I/O	<b>EMC_D3</b> — External memory data line 3.
					-	<b>R</b> — Function reserved.
					-	<b>R</b> — Function reserved.
					-	<b>R</b> — Function reserved.
					I/O	<b>SD_DAT1</b> — SD/MMC data bus line 1.
P1_11	T9	J7	③	I; PU	I/O	<b>GPIO1[4]</b> — General purpose digital input/output pin.
					I	<b>U1_CTS</b> — Clear to Send input for UART1.
					O	<b>CTOUT_15</b> — SCT output 15. Match output 3 of timer 3.
					I/O	<b>EMC_D4</b> — External memory data line 4.
					-	<b>R</b> — Function reserved.
					-	<b>R</b> — Function reserved.
					-	<b>R</b> — Function reserved.
					I/O	<b>SD_DAT2</b> — SD/MMC data bus line 2.
P1_12	R9	K7	③	I; PU	I/O	<b>GPIO1[5]</b> — General purpose digital input/output pin.
					I	<b>U1_DCD</b> — Data Carrier Detect input for UART1.
					-	<b>R</b> — Function reserved.
					I/O	<b>EMC_D5</b> — External memory data line 5.
					I	<b>T0_CAP1</b> — Capture input 1 of timer 0.
					-	<b>R</b> — Function reserved.
					I/O	<b>SGPIO8</b> — General purpose digital input/output pin.
					I/O	<b>SD_DAT3</b> — SD/MMC data bus line 3.
P1_13	R10	H8	③	I; PU	I/O	<b>GPIO1[6]</b> — General purpose digital input/output pin.
					O	<b>U1_TXD</b> — Transmitter output for UART1.
					-	<b>R</b> — Function reserved.
					I/O	<b>EMC_D6</b> — External memory data line 6.
					I	<b>T0_CAP0</b> — Capture input 0 of timer 0.
					-	<b>R</b> — Function reserved.
					I/O	<b>SGPIO9</b> — General purpose digital input/output pin.
					I	<b>SD_CD</b> — SD/MMC card detect input.

**Table 3. Pin description ...continued**

LCD, Ethernet, USB0, and USB1 functions are not available on all parts. See [Table 2](#).

Symbol	LBGA256	TFBGA100		Reset state [2]	Type	Description
P1_14	R11	J8	[3]	I; PU	I/O	<b>GPIO1[7]</b> — General purpose digital input/output pin.
					I	<b>U1_RXD</b> — Receiver input for UART1.
					-	<b>R</b> — Function reserved.
					I/O	<b>EMC_D7</b> — External memory data line 7.
					O	<b>T0_MAT2</b> — Match output 2 of timer 0.
					-	<b>R</b> — Function reserved.
					I/O	<b>SGPIO10</b> — General purpose digital input/output pin.
-	<b>R</b> — Function reserved.					
P1_15	T12	K8	[3]	I; PU	I/O	<b>GPIO0[2]</b> — General purpose digital input/output pin.
					O	<b>U2_TXD</b> — Transmitter output for USART2.
					I/O	<b>SGPIO2</b> — General purpose digital input/output pin.
					I	<b>ENET_RXD0</b> — Ethernet receive data 0 (RMII/MII interface).
					O	<b>T0_MAT1</b> — Match output 1 of timer 0.
					-	<b>R</b> — Function reserved.
					-	<b>R</b> — Function reserved.
-	<b>R</b> — Function reserved.					
P1_16	M7	H9	[3]	I; PU	I/O	<b>GPIO0[3]</b> — General purpose digital input/output pin.
					I	<b>U2_RXD</b> — Receiver input for USART2.
					I/O	<b>SGPIO3</b> — General purpose digital input/output pin.
					I	<b>ENET_CRS</b> — Ethernet Carrier Sense (MII interface).
					O	<b>T0_MAT0</b> — Match output 0 of timer 0.
					-	<b>R</b> — Function reserved.
					-	<b>R</b> — Function reserved.
I	<b>ENET_RX_DV</b> — Ethernet Receive Data Valid (RMII/MII interface).					
P1_17	M8	H10	[4]	I; PU	I/O	<b>GPIO0[12]</b> — General purpose digital input/output pin.
					I/O	<b>U2_UCLK</b> — Serial clock input/output for USART2 in synchronous mode.
					-	<b>R</b> — Function reserved.
					I/O	<b>ENET_MDIO</b> — Ethernet MIIM data input and output.
					I	<b>T0_CAP3</b> — Capture input 3 of timer 0.
					O	<b>CAN1_TD</b> — CAN1 transmitter output.
					I/O	<b>SGPIO11</b> — General purpose digital input/output pin.
-	<b>R</b> — Function reserved.					

**Table 3. Pin description ...continued**

LCD, Ethernet, USB0, and USB1 functions are not available on all parts. See [Table 2](#).

Symbol	LPGA256	TFBGA100		Reset state ②	Type	Description
P1_18	N12	J10	③	I; PU	I/O	<b>GPIO0[13]</b> — General purpose digital input/output pin.
					I/O	<b>U2_DIR</b> — RS-485/EIA-485 output enable/direction control for USART2.
					-	<b>R</b> — Function reserved.
					O	<b>ENET_TXD0</b> — Ethernet transmit data 0 (RMII/MII interface).
					O	<b>T0_MAT3</b> — Match output 3 of timer 0.
					I	<b>CAN1_RD</b> — CAN1 receiver input.
					I/O	<b>SGPIO12</b> — General purpose digital input/output pin.
-	<b>R</b> — Function reserved.					
P1_19	M11	K9	③	I; PU	I	<b>ENET_TX_CLK (ENET_REF_CLK)</b> — Ethernet Transmit Clock (MII interface) or Ethernet Reference Clock (RMII interface).
					I/O	<b>SSP1_SCK</b> — Serial clock for SSP1.
					-	<b>R</b> — Function reserved.
					-	<b>R</b> — Function reserved.
					O	<b>CLKOUT</b> — Clock output pin.
					-	<b>R</b> — Function reserved.
					O	<b>I2S0_RX_MCLK</b> — I2S receive master clock.
I/O	<b>I2S1_TX_SCK</b> — Transmit Clock. It is driven by the master and received by the slave. Corresponds to the signal SCK in the I <sup>2</sup> S-bus specification.					
P1_20	M10	K10	③	I; PU	I/O	<b>GPIO0[15]</b> — General purpose digital input/output pin.
					I/O	<b>SSP1_SSEL</b> — Slave Select for SSP1.
					-	<b>R</b> — Function reserved.
					O	<b>ENET_TXD1</b> — Ethernet transmit data 1 (RMII/MII interface).
					I	<b>T0_CAP2</b> — Capture input 2 of timer 0.
					-	<b>R</b> — Function reserved.
					I/O	<b>SGPIO13</b> — General purpose digital input/output pin.
-	<b>R</b> — Function reserved.					
P2_0	T16	G10	③	I; PU	I/O	<b>SGPIO4</b> — General purpose digital input/output pin.
					O	<b>U0_TXD</b> — Transmitter output for USART0.
					I/O	<b>EMC_A13</b> — External memory address line 13.
					O	<b>USB0_PPWR</b> — VBUS drive signal (towards external charge pump or power management unit); indicates that VBUS must be driven (active HIGH). Add a pull-down resistor to disable the power switch at reset. This signal has opposite polarity compared to the USB_PPWR used on other NXP LPC parts.
					I/O	<b>GPIO5[0]</b> — General purpose digital input/output pin.
					-	<b>R</b> — Function reserved.
					I	<b>T3_CAP0</b> — Capture input 0 of timer 3.
O	<b>ENET_MDC</b> — Ethernet MIIM clock.					

**Table 3. Pin description ...continued**  
 LCD, Ethernet, USB0, and USB1 functions are not available on all parts. See [Table 2](#).

Symbol	LPGA256	TFBGA100		Reset state [2]	Type	Description
P2_1	N15	G7	[3]	I; PU	I/O	<b>SGPIO5</b> — General purpose digital input/output pin.
					I	<b>U0_RXD</b> — Receiver input for USART0.
					I/O	<b>EMC_A12</b> — External memory address line 12.
					I	<b>USB0_PWR_FAULT</b> — Port power fault signal indicating overcurrent condition; this signal monitors over-current on the USB bus (external circuitry required to detect over-current condition).
					I/O	<b>GPIO5[1]</b> — General purpose digital input/output pin.
					-	<b>R</b> — Function reserved.
					I	<b>T3_CAP1</b> — Capture input 1 of timer 3.
					-	<b>R</b> — Function reserved.
P2_2	M15	F5	[3]	I; PU	I/O	<b>SGPIO6</b> — General purpose digital input/output pin.
					I/O	<b>U0_UCLK</b> — Serial clock input/output for USART0 in synchronous mode.
					I/O	<b>EMC_A11</b> — External memory address line 11.
					O	<b>USB0_IND1</b> — USB0 port indicator LED control output 1.
					I/O	<b>GPIO5[2]</b> — General purpose digital input/output pin.
					I	<b>CTIN_6</b> — SCT input 6. Capture input 1 of timer 3.
					I	<b>T3_CAP2</b> — Capture input 2 of timer 3.
					-	<b>R</b> — Function reserved.
P2_3	J12	D8	[4]	I; PU	I/O	<b>SGPIO12</b> — General purpose digital input/output pin.
					I/O	<b>I2C1_SDA</b> — I <sup>2</sup> C1 data input/output (this pin does not use a specialized I2C pad).
					O	<b>U3_TXD</b> — Transmitter output for USART3.
					I	<b>CTIN_1</b> — SCT input 1. Capture input 1 of timer 0. Capture input 1 of timer 2.
					I/O	<b>GPIO5[3]</b> — General purpose digital input/output pin.
					-	<b>R</b> — Function reserved.
					O	<b>T3_MAT0</b> — Match output 0 of timer 3.
					I	<b>USB0_PWR_EN</b> — VBUS drive signal (towards external charge pump or power management unit); indicates that Vbus must be driven (active HIGH).
P2_4	K11	D9	[4]	I; PU	I/O	<b>SGPIO13</b> — General purpose digital input/output pin.
					I/O	<b>I2C1_SCL</b> — I <sup>2</sup> C1 clock input/output (this pin does not use a specialized I2C pad).
					I	<b>U3_RXD</b> — Receiver input for USART3.
					I	<b>CTIN_0</b> — SCT input 0. Capture input 0 of timer 0, 1, 2, 3.
					I/O	<b>GPIO5[4]</b> — General purpose digital input/output pin.
					-	<b>R</b> — Function reserved.
					O	<b>T3_MAT1</b> — Match output 1 of timer 3.
					I	<b>USB0_PWR_FAULT</b> — Port power fault signal indicating overcurrent condition; this signal monitors over-current on the USB bus (external circuitry required to detect over-current condition).

**Table 3. Pin description ...continued**

LCD, Ethernet, USB0, and USB1 functions are not available on all parts. See [Table 2](#).

Symbol	LBGA256	TFBGA100		Reset state <a href="#">[2]</a>	Type	Description
P2_5	K14	D10	<a href="#">[4]</a>	I; PU	I/O	<b>SGPIO14</b> — General purpose digital input/output pin.
					I	<b>CTIN_2</b> — SCT input 2. Capture input 2 of timer 0.
					I	<b>USB1_VBUS</b> — Monitors the presence of USB1 bus power. <b>Note:</b> This signal must be HIGH for USB reset to occur.
					I	<b>ADCTRIG1</b> — ADC trigger input 1.
					I/O	<b>GPIO5[5]</b> — General purpose digital input/output pin.
					-	<b>R</b> — Function reserved.
					O	<b>T3_MAT2</b> — Match output 2 of timer 3.
					O	<b>USB0_IND0</b> — USB0 port indicator LED control output 0.
P2_6	K16	G9	<a href="#">[3]</a>	I; PU	I/O	<b>SGPIO7</b> — General purpose digital input/output pin.
					I/O	<b>U0_DIR</b> — RS-485/EIA-485 output enable/direction control for USART0.
					I/O	<b>EMC_A10</b> — External memory address line 10.
					O	<b>USB0_IND0</b> — USB0 port indicator LED control output 0.
					I/O	<b>GPIO5[6]</b> — General purpose digital input/output pin.
					I	<b>CTIN_7</b> — SCT input 7.
					I	<b>T3_CAP3</b> — Capture input 3 of timer 3.
					-	<b>R</b> — Function reserved.
P2_7	H14	C10	<a href="#">[3]</a>	I; PU	I/O	<b>GPIO0[7]</b> — General purpose digital input/output pin. If this pin is pulled LOW at reset, the part enters ISP mode using USART0.
					O	<b>CTOUT_1</b> — SCT output 1. Match output 1 of timer 0.
					I/O	<b>U3_UCLK</b> — Serial clock input/output for USART3 in synchronous mode.
					I/O	<b>EMC_A9</b> — External memory address line 9.
					-	<b>R</b> — Function reserved.
					-	<b>R</b> — Function reserved.
					O	<b>T3_MAT3</b> — Match output 3 of timer 3.
					-	<b>R</b> — Function reserved.
P2_8	J16	C6	<a href="#">[3]</a>	I; PU	I/O	<b>SGPIO15</b> — General purpose digital input/output pin. Boot pin (see <a href="#">Table 5</a> ).
					O	<b>CTOUT_0</b> — SCT output 0. Match output 0 of timer 0.
					I/O	<b>U3_DIR</b> — RS-485/EIA-485 output enable/direction control for USART3.
					I/O	<b>EMC_A8</b> — External memory address line 8.
					I/O	<b>GPIO5[7]</b> — General purpose digital input/output pin.
					-	<b>R</b> — Function reserved.
					-	<b>R</b> — Function reserved.
					-	<b>R</b> — Function reserved.



**Table 3. Pin description ...continued**

LCD, Ethernet, USB0, and USB1 functions are not available on all parts. See [Table 2](#).

Symbol	LPGA256	TFBGA100		Reset state 2	Type	Description
P2_9	H16	B10	3	I; PU	I/O	<b>GPIO1[10]</b> — General purpose digital input/output pin. Boot pin (see <a href="#">Table 5</a> ).
					O	<b>CTOUT_3</b> — SCT output 3. Match output 3 of timer 0.
					I/O	<b>U3_BAUD</b> — Baud pin for USART3.
					I/O	<b>EMC_A0</b> — External memory address line 0.
					-	<b>R</b> — Function reserved.
					-	<b>R</b> — Function reserved.
					-	<b>R</b> — Function reserved.
P2_10	G16	E8	3	I; PU	I/O	<b>GPIO0[14]</b> — General purpose digital input/output pin.
					O	<b>CTOUT_2</b> — SCT output 2. Match output 2 of timer 0.
					O	<b>U2_TXD</b> — Transmitter output for USART2.
					I/O	<b>EMC_A1</b> — External memory address line 1.
					-	<b>R</b> — Function reserved.
					-	<b>R</b> — Function reserved.
P2_11	F16	A9	3	I; PU	I/O	<b>GPIO1[11]</b> — General purpose digital input/output pin.
					O	<b>CTOUT_5</b> — SCT output 5. Match output 1 of timer 1.
					I	<b>U2_RXD</b> — Receiver input for USART2.
					I/O	<b>EMC_A2</b> — External memory address line 2.
					-	<b>R</b> — Function reserved.
					-	<b>R</b> — Function reserved.
P2_12	E15	B9	3	I; PU	I/O	<b>GPIO1[12]</b> — General purpose digital input/output pin.
					O	<b>CTOUT_4</b> — SCT output 4. Match output 0 of timer 1.
					-	<b>R</b> — Function reserved.
					I/O	<b>EMC_A3</b> — External memory address line 3.
					-	<b>R</b> — Function reserved.
					-	<b>R</b> — Function reserved.
					I/O	<b>U2_UCLK</b> — Serial clock input/output for USART2 in synchronous mode.

**Table 3. Pin description ...continued**

LCD, Ethernet, USB0, and USB1 functions are not available on all parts. See [Table 2](#).

Symbol	LBGA256	TFBGA100		Reset state 2	Type	Description
P2_13	C16	A10	3	I; PU	I/O	<b>GPIO1[13]</b> — General purpose digital input/output pin.
					I	<b>CTIN_4</b> — SCT input 4. Capture input 2 of timer 1.
					-	<b>R</b> — Function reserved.
					I/O	<b>EMC_A4</b> — External memory address line 4.
					-	<b>R</b> — Function reserved.
					-	<b>R</b> — Function reserved.
					I/O	<b>U2_DIR</b> — RS-485/EIA-485 output enable/direction control for USART2.
P3_0	F13	A8	3	I; PU	I/O	<b>I2S0_RX_SCK</b> — I2S receive clock. It is driven by the master and received by the slave. Corresponds to the signal SCK in the <i>I<sup>2</sup>S-bus specification</i> .
					O	<b>I2S0_RX_MCLK</b> — I2S receive master clock.
					I/O	<b>I2S0_TX_SCK</b> — Transmit Clock. It is driven by the master and received by the slave. Corresponds to the signal SCK in the <i>I<sup>2</sup>S-bus specification</i> .
					O	<b>I2S0_TX_MCLK</b> — I2S transmit master clock.
					I/O	<b>SSP0_SCK</b> — Serial clock for SSP0.
					-	<b>R</b> — Function reserved.
					-	<b>R</b> — Function reserved.
P3_1	G11	F7	3	I; PU	I/O	<b>I2S0_TX_WS</b> — Transmit Word Select. It is driven by the master and received by the slave. Corresponds to the signal WS in the <i>I<sup>2</sup>S-bus specification</i> .
					I/O	<b>I2S0_RX_WS</b> — Receive Word Select. It is driven by the master and received by the slave. Corresponds to the signal WS in the <i>I<sup>2</sup>S-bus specification</i> .
					I	<b>CAN0_RD</b> — CAN receiver input.
					O	<b>USB1_IND1</b> — USB1 Port indicator LED control output 1.
					I/O	<b>GPIO5[8]</b> — General purpose digital input/output pin.
					-	<b>R</b> — Function reserved.
					O	<b>LCD_VD15</b> — LCD data.
P3_2	F11	G6	3	I; PU	I/O	<b>I2S0_TX_SDA</b> — I2S transmit data. It is driven by the transmitter and read by the receiver. Corresponds to the signal SD in the <i>I<sup>2</sup>S-bus specification</i> .
					I/O	<b>I2S0_RX_SDA</b> — I2S Receive data. It is driven by the transmitter and read by the receiver. Corresponds to the signal SD in the <i>I<sup>2</sup>S-bus specification</i> .
					O	<b>CAN0_TD</b> — CAN transmitter output.
					O	<b>USB1_IND0</b> — USB1 Port indicator LED control output 0.
					I/O	<b>GPIO5[9]</b> — General purpose digital input/output pin.
					-	<b>R</b> — Function reserved.
					O	<b>LCD_VD14</b> — LCD data.
-	<b>R</b> — Function reserved.					

**Table 3. Pin description ...continued**

LCD, Ethernet, USB0, and USB1 functions are not available on all parts. See [Table 2](#).

Symbol	LBGA256	TFBGA100		Reset state <a href="#">[2]</a>	Type	Description
P3_3	B14	A7	<a href="#">[5]</a>	I; PU	-	R — Function reserved.
					I/O	SPI_SCK — Serial clock for SPI.
					I/O	SSP0_SCK — Serial clock for SSP0.
					O	SPIFI_SCK — Serial clock for SPIFI.
					O	CGU_OUT1 — CGU spare clock output 1.
					-	R — Function reserved.
					O	I2S0_TX_MCLK — I2S transmit master clock.
P3_4	A15	B8	<a href="#">[3]</a>	I; PU	I/O	GPIO1[14] — General purpose digital input/output pin.
					-	R — Function reserved.
					-	R — Function reserved.
					I/O	SPIFI_SIO3 — I/O lane 3 for SPIFI.
					O	U1_TXD — Transmitter output for UART 1.
					I/O	I2S0_TX_WS — Transmit Word Select. It is driven by the master and received by the slave. Corresponds to the signal WS in the I <sup>2</sup> S-bus specification.
					I/O	I2S1_RX_SDA — I2S1 Receive data. It is driven by the transmitter and read by the receiver. Corresponds to the signal SD in the I <sup>2</sup> S-bus specification.
P3_5	C12	B7	<a href="#">[3]</a>	I; PU	I/O	GPIO1[15] — General purpose digital input/output pin.
					-	R — Function reserved.
					-	R — Function reserved.
					I/O	SPIFI_SIO2 — I/O lane 2 for SPIFI.
					I	U1_RXD — Receiver input for UART 1.
					I/O	I2S0_TX_SDA — I2S transmit data. It is driven by the transmitter and read by the receiver. Corresponds to the signal SD in the I <sup>2</sup> S-bus specification.
					I/O	I2S1_RX_WS — Receive Word Select. It is driven by the master and received by the slave. Corresponds to the signal WS in the I <sup>2</sup> S-bus specification.
P3_6	B13	C7	<a href="#">[3]</a>	I; PU	I/O	GPIO0[6] — General purpose digital input/output pin.
					I/O	SPI_MISO — Master In Slave Out for SPI.
					I/O	SSP0_SSEL — Slave Select for SSP0.
					I/O	SPIFI_MISO — Input 1 in SPIFI quad mode; SPIFI output IO1.
					-	R — Function reserved.
					I/O	SSP0_MISO — Master In Slave Out for SSP0.
					-	R — Function reserved.
-	R — Function reserved.					

**Table 3. Pin description ...continued**LCD, Ethernet, USB0, and USB1 functions are not available on all parts. See [Table 2](#).

Symbol	LBGA256	TFBGA100		Reset state [2]	Type	Description
P3_7	C11	D7	[3]	I; PU	-	R — Function reserved.
					I/O	SPI_MOSI — Master Out Slave In for SPI.
					I/O	SSP0_MISO — Master In Slave Out for SSP0.
					I/O	SPIFI_MOSI — Input I0 in SPIFI quad mode; SPIFI output IO0.
					I/O	GPIO5[10] — General purpose digital input/output pin.
					I/O	SSP0_MOSI — Master Out Slave in for SSP0.
					-	R — Function reserved.
P3_8	C10	E7	[3]	I; PU	-	R — Function reserved.
					I	SPI_SSEL — Slave Select for SPI. Note that this pin is an input pin only. The SPI in master mode cannot drive the CS input on the slave. Any GPIO pin can be used for SPI chip select in master mode.
					I/O	SSP0_MOSI — Master Out Slave in for SSP0.
					I/O	SPIFI_CS — SPIFI serial flash chip select.
					I/O	GPIO5[11] — General purpose digital input/output pin.
					I/O	SSP0_SSEL — Slave Select for SSP0.
					-	R — Function reserved.
P4_0	D5	-	[3]	I; PU	I/O	GPIO2[0] — General purpose digital input/output pin.
					O	MCOA0 — Motor control PWM channel 0, output A.
					I	NMI — External interrupt input to NMI.
					-	R — Function reserved.
					-	R — Function reserved.
					O	LCD_VD13 — LCD data.
					I/O	U3_UCLK — Serial clock input/output for USART3 in synchronous mode.
-	R — Function reserved.					
P4_1	A1	-	[6] [13]	I; PU	I/O	GPIO2[1] — General purpose digital input/output pin.
					O	CTOUT_1 — SCT output 1. Match output 1 of timer 0.
					O	LCD_VD0 — LCD data.
					-	R — Function reserved.
					-	R — Function reserved.
					O	LCD_VD19 — LCD data.
					O	U3_TXD — Transmitter output for USART3.
I	ENET_COL — Ethernet Collision detect (MII interface).					
AI	ADC0_1 — ADC0, input channel 1. Configure the pin as GPIO input and use the ADC function select register in the SCU to select the ADC.					

**Table 3. Pin description ...continued**LCD, Ethernet, USB0, and USB1 functions are not available on all parts. See [Table 2](#).

Symbol	LPGA256	TFBGA100		Reset state <a href="#">[2]</a>	Type	Description
P4_2	D3	-	<a href="#">[3]</a>	I; PU	I/O	<b>GPIO2[2]</b> — General purpose digital input/output pin.
						O <b>CTOUT_0</b> — SCT output 0. Match output 0 of timer 0.
						O <b>LCD_VD3</b> — LCD data.
						- <b>R</b> — Function reserved.
						- <b>R</b> — Function reserved.
						O <b>LCD_VD12</b> — LCD data.
						I <b>U3_RXD</b> — Receiver input for USART3.
						I/O <b>SGPIO8</b> — General purpose digital input/output pin.
P4_3	C2	-	<a href="#">[6]</a> <a href="#">[13]</a>	I; PU	I/O	<b>GPIO2[3]</b> — General purpose digital input/output pin.
						O <b>CTOUT_3</b> — SCT output 3. Match output 3 of timer 0.
						O <b>LCD_VD2</b> — LCD data.
						- <b>R</b> — Function reserved.
						- <b>R</b> — Function reserved.
						O <b>LCD_VD21</b> — LCD data.
						I/O <b>U3_BAUD</b> — Baud pin for USART3.
						I/O <b>SGPIO9</b> — General purpose digital input/output pin.
P4_4	B1	-	<a href="#">[6]</a>	I; PU	I/O	<b>GPIO2[4]</b> — General purpose digital input/output pin.
						O <b>CTOUT_2</b> — SCT output 2. Match output 2 of timer 0.
						O <b>LCD_VD1</b> — LCD data.
						- <b>R</b> — Function reserved.
						- <b>R</b> — Function reserved.
						O <b>LCD_VD20</b> — LCD data.
						I/O <b>U3_DIR</b> — RS-485/EIA-485 output enable/direction control for USART3.
						I/O <b>SGPIO10</b> — General purpose digital input/output pin.
P4_5	D2	-	<a href="#">[3]</a>	I; PU	I/O	<b>GPIO2[5]</b> — General purpose digital input/output pin.
						O <b>CTOUT_5</b> — SCT output 5. Match output 1 of timer 1.
						O <b>LCD_FP</b> — Frame pulse (STN). Vertical synchronization pulse (TFT).
						- <b>R</b> — Function reserved.
						- <b>R</b> — Function reserved.
						- <b>R</b> — Function reserved.
						- <b>R</b> — Function reserved.
						I/O <b>SGPIO11</b> — General purpose digital input/output pin.

**Table 3. Pin description ...continued**  
 LCD, Ethernet, USB0, and USB1 functions are not available on all parts. See [Table 2](#).

Symbol	LBGA256	TFBGA100		Reset state [2]	Type	Description
P4_6	C1	-	[3]	I; PU	I/O	<b>GPIO2[6]</b> — General purpose digital input/output pin.
					O	<b>CTOUT_4</b> — SCT output 4. Match output 0 of timer 1.
					O	<b>LCD_ENAB/LCDM</b> — STN AC bias drive or TFT data enable input.
					-	<b>R</b> — Function reserved.
					-	<b>R</b> — Function reserved.
					-	<b>R</b> — Function reserved.
					-	<b>R</b> — Function reserved.
					I/O	<b>SGPIO12</b> — General purpose digital input/output pin.
P4_7	H4	-	[3]	O; PU	O	<b>LCD_DCLK</b> — LCD panel clock.
					I	<b>GP_CLKIN</b> — General purpose clock input to the CGU.
					-	<b>R</b> — Function reserved.
					-	<b>R</b> — Function reserved.
					-	<b>R</b> — Function reserved.
					-	<b>R</b> — Function reserved.
					I/O	<b>I2S1_TX_SCK</b> — Transmit Clock. It is driven by the master and received by the slave. Corresponds to the signal SCK in the I <sup>2</sup> S-bus specification.
					I/O	<b>I2S0_TX_SCK</b> — Transmit Clock. It is driven by the master and received by the slave. Corresponds to the signal SCK in the I <sup>2</sup> S-bus specification.
P4_8	E2	-	[3]	I; PU	-	<b>R</b> — Function reserved.
					I	<b>CTIN_5</b> — SCT input 5. Capture input 2 of timer 2.
					O	<b>LCD_VD9</b> — LCD data.
					-	<b>R</b> — Function reserved.
					I/O	<b>GPIO5[12]</b> — General purpose digital input/output pin.
					O	<b>LCD_VD22</b> — LCD data.
					O	<b>CAN1_TD</b> — CAN1 transmitter output.
					I/O	<b>SGPIO13</b> — General purpose digital input/output pin.
P4_9	L2	-	[3]	I; PU	-	<b>R</b> — Function reserved.
					I	<b>CTIN_6</b> — SCT input 6. Capture input 1 of timer 3.
					O	<b>LCD_VD11</b> — LCD data.
					-	<b>R</b> — Function reserved.
					I/O	<b>GPIO5[13]</b> — General purpose digital input/output pin.
					O	<b>LCD_VD15</b> — LCD data.
					I	<b>CAN1_RD</b> — CAN1 receiver input.
					I/O	<b>SGPIO14</b> — General purpose digital input/output pin.

**Table 3. Pin description ...continued**

LCD, Ethernet, USB0, and USB1 functions are not available on all parts. See [Table 2](#).

Symbol	LBGA256	TFBGA100		Reset state ②	Type	Description
P4_10	M3	-	③	I; PU	-	R — Function reserved.
					I	CTIN_2 — SCT input 2. Capture input 2 of timer 0.
					O	LCD_VD10 — LCD data.
					-	R — Function reserved.
					I/O	GPIO5[14] — General purpose digital input/output pin.
					O	LCD_VD14 — LCD data.
					-	R — Function reserved.
					I/O	SGPIO15 — General purpose digital input/output pin.
P5_0	N3	-	③	I; PU	I/O	GPIO2[9] — General purpose digital input/output pin.
					O	MCOB2 — Motor control PWM channel 2, output B.
					I/O	EMC_D12 — External memory data line 12.
					-	R — Function reserved.
					I	U1_DSR — Data Set Ready input for UART 1.
					I	T1_CAP0 — Capture input 0 of timer 1.
					-	R — Function reserved.
					-	R — Function reserved.
P5_1	P3	-	③	I; PU	I/O	GPIO2[10] — General purpose digital input/output pin.
					I	MCI2 — Motor control PWM channel 2, input.
					I/O	EMC_D13 — External memory data line 13.
					-	R — Function reserved.
					O	U1_DTR — Data Terminal Ready output for UART 1. Can also be configured to be an RS-485/EIA-485 output enable signal for UART 1.
					I	T1_CAP1 — Capture input 1 of timer 1.
					-	R — Function reserved.
					-	R — Function reserved.
P5_2	R4	-	③	I; PU	I/O	GPIO2[11] — General purpose digital input/output pin.
					I	MCI1 — Motor control PWM channel 1, input.
					I/O	EMC_D14 — External memory data line 14.
					-	R — Function reserved.
					O	U1_RTS — Request to Send output for UART 1. Can also be configured to be an RS-485/EIA-485 output enable signal for UART 1.
					I	T1_CAP2 — Capture input 2 of timer 1.
					-	R — Function reserved.
					-	R — Function reserved.

**Table 3. Pin description ...continued**

LCD, Ethernet, USB0, and USB1 functions are not available on all parts. See [Table 2](#).

Symbol	LBGA256	TFBGA100		Reset state ②	Type	Description
P5_3	T8	-	③	I; PU	I/O	<b>GPIO2[12]</b> — General purpose digital input/output pin.
					I	<b>MCIO</b> — Motor control PWM channel 0, input.
					I/O	<b>EMC_D15</b> — External memory data line 15.
					-	<b>R</b> — Function reserved.
					I	<b>U1_RI</b> — Ring Indicator input for UART 1.
					I	<b>T1_CAP3</b> — Capture input 3 of timer 1.
					-	<b>R</b> — Function reserved.
					-	<b>R</b> — Function reserved.
P5_4	P9	-	③	I; PU	I/O	<b>GPIO2[13]</b> — General purpose digital input/output pin.
					O	<b>MCOB0</b> — Motor control PWM channel 0, output B.
					I/O	<b>EMC_D8</b> — External memory data line 8.
					-	<b>R</b> — Function reserved.
					I	<b>U1_CTS</b> — Clear to Send input for UART 1.
					O	<b>T1_MAT0</b> — Match output 0 of timer 1.
					-	<b>R</b> — Function reserved.
					-	<b>R</b> — Function reserved.
P5_5	P10	-	③	I; PU	I/O	<b>GPIO2[14]</b> — General purpose digital input/output pin.
					O	<b>MCOA1</b> — Motor control PWM channel 1, output A.
					I/O	<b>EMC_D9</b> — External memory data line 9.
					-	<b>R</b> — Function reserved.
					I	<b>U1_DCD</b> — Data Carrier Detect input for UART 1.
					O	<b>T1_MAT1</b> — Match output 1 of timer 1.
					-	<b>R</b> — Function reserved.
					-	<b>R</b> — Function reserved.
P5_6	T13	-	③	I; PU	I/O	<b>GPIO2[15]</b> — General purpose digital input/output pin.
					O	<b>MCOB1</b> — Motor control PWM channel 1, output B.
					I/O	<b>EMC_D10</b> — External memory data line 10.
					-	<b>R</b> — Function reserved.
					O	<b>U1_TXD</b> — Transmitter output for UART 1.
					O	<b>T1_MAT2</b> — Match output 2 of timer 1.
					-	<b>R</b> — Function reserved.
					-	<b>R</b> — Function reserved.



**Table 3. Pin description ...continued**

LCD, Ethernet, USB0, and USB1 functions are not available on all parts. See [Table 2](#).

Symbol	LBGA256	TFBGA100		Reset state <a href="#">[2]</a>	Type	Description
P5_7	R12	-	<a href="#">[3]</a>	I; PU	I/O	<b>GPIO2[7]</b> — General purpose digital input/output pin.
					O	<b>MCOA2</b> — Motor control PWM channel 2, output A.
					I/O	<b>EMC_D11</b> — External memory data line 11.
					-	<b>R</b> — Function reserved.
					I	<b>U1_RXD</b> — Receiver input for UART 1.
					O	<b>T1_MAT3</b> — Match output 3 of timer 1.
					-	<b>R</b> — Function reserved.
					-	<b>R</b> — Function reserved.
P6_0	M12	H7	<a href="#">[3]</a>	I; PU	-	<b>R</b> — Function reserved.
					O	<b>I2S0_RX_MCLK</b> — I2S receive master clock.
					-	<b>R</b> — Function reserved.
					-	<b>R</b> — Function reserved.
					I/O	<b>I2S0_RX_SCK</b> — Receive Clock. It is driven by the master and received by the slave. Corresponds to the signal SCK in the <i>I<sup>2</sup>S-bus specification</i> .
					-	<b>R</b> — Function reserved.
					-	<b>R</b> — Function reserved.
					-	<b>R</b> — Function reserved.
P6_1	R15	G5	<a href="#">[3]</a>	I; PU	I/O	<b>GPIO3[0]</b> — General purpose digital input/output pin.
					O	<b>EMC_DYCS1</b> — SDRAM chip select 1.
					I/O	<b>U0_UCLK</b> — Serial clock input/output for USART0 in synchronous mode.
					I/O	<b>I2S0_RX_WS</b> — Receive Word Select. It is driven by the master and received by the slave. Corresponds to the signal WS in the <i>I<sup>2</sup>S-bus specification</i> .
					-	<b>R</b> — Function reserved.
					I	<b>T2_CAP0</b> — Capture input 2 of timer 2.
					-	<b>R</b> — Function reserved.
					-	<b>R</b> — Function reserved.
P6_2	L13	J9	<a href="#">[3]</a>	I; PU	I/O	<b>GPIO3[1]</b> — General purpose digital input/output pin.
					O	<b>EMC_CKEOUT1</b> — SDRAM clock enable 1.
					I/O	<b>U0_DIR</b> — RS-485/EIA-485 output enable/direction control for USART0.
					I/O	<b>I2S0_RX_SDA</b> — I2S Receive data. It is driven by the transmitter and read by the receiver. Corresponds to the signal SD in the <i>I<sup>2</sup>S-bus specification</i> .
					-	<b>R</b> — Function reserved.
					I	<b>T2_CAP1</b> — Capture input 1 of timer 2.
					-	<b>R</b> — Function reserved.
					-	<b>R</b> — Function reserved.

**Table 3. Pin description ...continued**

LCD, Ethernet, USB0, and USB1 functions are not available on all parts. See [Table 2](#).

Symbol	LPGA256	TFBGA100		Reset state 2	Type	Description
P6_3	P15	-	3	I; PU	I/O	<b>GPIO3[2]</b> — General purpose digital input/output pin.
					I	<b>USB0_PWR_EN</b> — VBUS drive signal (towards external charge pump or power management unit); indicates that the VBUS signal must be driven (active HIGH).
					I/O	<b>SGPIO4</b> — General purpose digital input/output pin.
					O	<b>EMC_CS1</b> — LOW active Chip Select 1 signal.
					-	<b>R</b> — Function reserved.
					I	<b>T2_CAP2</b> — Capture input 2 of timer 2.
					-	<b>R</b> — Function reserved.
P6_4	R16	F6	3	I; PU	I/O	<b>GPIO3[3]</b> — General purpose digital input/output pin.
					I	<b>CTIN_6</b> — SCT input 6. Capture input 1 of timer 3.
					O	<b>U0_TXD</b> — Transmitter output for USART0.
					O	<b>EMC_CAS</b> — LOW active SDRAM Column Address Strobe.
					-	<b>R</b> — Function reserved.
					-	<b>R</b> — Function reserved.
					-	<b>R</b> — Function reserved.
P6_5	P16	F9	3	I; PU	I/O	<b>GPIO3[4]</b> — General purpose digital input/output pin.
					O	<b>CTOUT_6</b> — SCT output 6. Match output 2 of timer 1.
					I	<b>U0_RXD</b> — Receiver input for USART0.
					O	<b>EMC_RAS</b> — LOW active SDRAM Row Address Strobe.
					-	<b>R</b> — Function reserved.
					-	<b>R</b> — Function reserved.
					-	<b>R</b> — Function reserved.
P6_6	L14	-	3	I; PU	I/O	<b>GPIO0[5]</b> — General purpose digital input/output pin.
					O	<b>EMC_BLS1</b> — LOW active Byte Lane select signal 1.
					I/O	<b>SGPIO5</b> — General purpose digital input/output pin.
					I	<b>USB0_PWR_FAULT</b> — Port power fault signal indicating overcurrent condition; this signal monitors over-current on the USB bus (external circuitry required to detect over-current condition).
					-	<b>R</b> — Function reserved.
					I	<b>T2_CAP3</b> — Capture input 3 of timer 2.
					-	<b>R</b> — Function reserved.