Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

LPC47M112

Enhanced Super I/O Controller with LPC Interface

Highlights

- 3.3 Volt Operation (5 Volt Tolerant)
- LPC Interface
- ACPI 1.0 Compliant
- Fan Control
  - Fan Speed Control Outputs
  - Fan Tachometer Inputs
- Programmable Wake-up Event Interface
- PC98, PC99 Compliant
- Dual Game Port Interface
- MPU-401 MIDI Support
- General Purpose Input/Output Pins
- ISA Plug-and-Play Compatible Register Set
- Intelligent Auto Power Management
- System Management Interrupt
- 2.88MB Super I/O Floppy Disk Controller
  - Licensed CMOS 765B Floppy Disk Controller
  - Software and Register Compatible with Microchip's Proprietary 82077AA Compatible Core
  - Supports Two Floppy Drives Directly
  - Configurable Open Drain/Push-Pull Output Drivers
  - Supports Vertical Recording Format
  - 16-Byte Data FIFO
  - 100% IBM Compatibility
  - Detects All Overrun and Under-run Conditions
  - Sophisticated Power Control Circuitry (PCC) Including Multiple Powerdown Modes for Reduced Power Consumption
  - DMA Enable Logic
  - Data Rate and Drive Control Registers
  - 480 Address, Up to Eight IRQ and Three DMA Options
- Enhanced Digital Data Separator
  - 2 Mbps, 1 Mbps, 500 Kbps, 300 Kbps, 250 Kbps Data Rates
  - Programmable Precompensation Modes
- Keyboard Controller
  - 8042 Software Compatible
  - 8 Bit Microcomputer
  - 2k Bytes of Program ROM
  - 256 Bytes of Data RAM
  - Four Open Drain Outputs Dedicated for Keyboard/Mouse Interface
  - Asynchronous Access to Two Data Registers and One Status Register
  - Supports Interrupt and Polling Access
  - 8 Bit Counter Timer
  - Port 92 Support
  - Fast Gate A20 and KRESET Outputs
- Serial Ports
  - Two Full Function Serial Ports
  - High Speed NS16C550 Compatible UARTs with Send/Receive 16-Byte FIFOs
  - Supports 230k and 460k Baud
  - Programmable Baud Rate Generator
  - Modem Control Circuitry
  - 480 Address and 15 IRQ Options
- Infrared Port
  - Multi-protocol Infrared Interface
  - IrDA 1.0 Compliant
  - SHARP ASK IR
  - 480 Addresses, Up to 15 IRQ
- Multi-Mode Parallel Port with ChiProtect
  - Standard Mode IBM PC/XT, PC/AT, and PS/2 Compatible Bidirectional Parallel Port
  - Enhanced Parallel Port (EPP) Compatible - EPP 1.7 and EPP 1.9 (IEEE 1284 Compliant)
  - IEEE 1284 Compliant Enhanced Capabilities Port (ECP)
  - ChiProtect Circuitry for Protection
  - 480 Address, Up to 15 IRQ and Three DMA Options
- LPC Interface
  - Multiplexed Command, Address and Data Bus
  - Serial IRQ Interface Compatible with Serialized IRQ Support for PCI Systems
  - PME Interface
- 100-Pin QFP RoHS compliant package in a 3.2mm format

TO OUR VALUED CUSTOMERS

It is our intention to provide our valued customers with the best documentation possible to ensure successful use of your Microchip products. To this end, we will continue to improve our publications to better suit your needs. Our publications will be refined and enhanced as new volumes and updates are introduced.

If you have any questions or comments regarding this publication, please contact the Marketing Communications Department via E-mail at **docerrors@microchip.com**. We welcome your feedback.

Most Current Data Sheet

To obtain the most up-to-date version of this data sheet, please register at our Worldwide Web site at:

http://www.microchip.com

You can determine the version of a data sheet by examining its literature number found on the bottom outside corner of any page. The last character of the literature number is the version number, (e.g., DS30000000A is version A of document DS30000000).

Errata

An errata sheet, describing minor operational differences from the data sheet and recommended workarounds, may exist for current devices. As device/documentation issues become known to us, we will publish an errata sheet. The errata will specify the revision of silicon and revision of document to which it applies.

To determine if an errata sheet exists for a particular device, please check with one of the following:

- Microchip's Worldwide Web site; http://www.microchip.com
- Your local Microchip sales office (see last page)

When contacting a sales office, please specify which device, revision of silicon and data sheet (include -literature number) you are using.

Customer Notification System

Register on our web site at **www.microchip.com** to receive the most current information on all of our products.

Table of Contents

1.0 GENERAL DESCRIPTION

The LPC47M112 is a 3.3V (5V tolerant) PC98/PC99 compliant Super I/O controller. The LPC47M112 implements the LPC interface, a pin reduced ISA bus interface which provides the same or better performance as the ISA/X-bus with a substantial savings in pins used. The LPC47M112 provides fan control through two fan speed control output pins and two fan tachometer input pins. It also provides 37 general purpose input/output (GPIO) pins, a dual game port interface and MPU-401 MIDI support.

The LPC47M112 incorporates a keyboard interface, Microchip's true CMOS 765B floppy disk controller, advanced digital data separator, two 16C550A compatible UARTs, one Multi-Mode parallel port which includes ChiProtect circuitry plus EPP and ECP, on-chip 12 mA AT bus drivers, one floppy direct drive support, and Intelligent Power Management including PME support. The true CMOS 765B core provides 100% compatibility with IBM PC/XT and PC/AT architectures in addition to providing data overflow and underflow protection. The Microchip advanced digital data separator incorporates Microchip's patented data separator technology, allowing for ease of testing and use. Both on-chip UARTs are compatible with the NS16C550A. The parallel port is compatible with IBM PC/AT architecture, as well as IEEE 1284 EPP and ECP. The LPC47M112 incorporates sophisticated power control circuitry (PCC) which includes support for keyboard and mouse wake-up events. The PCC supports multiple low power-down modes.

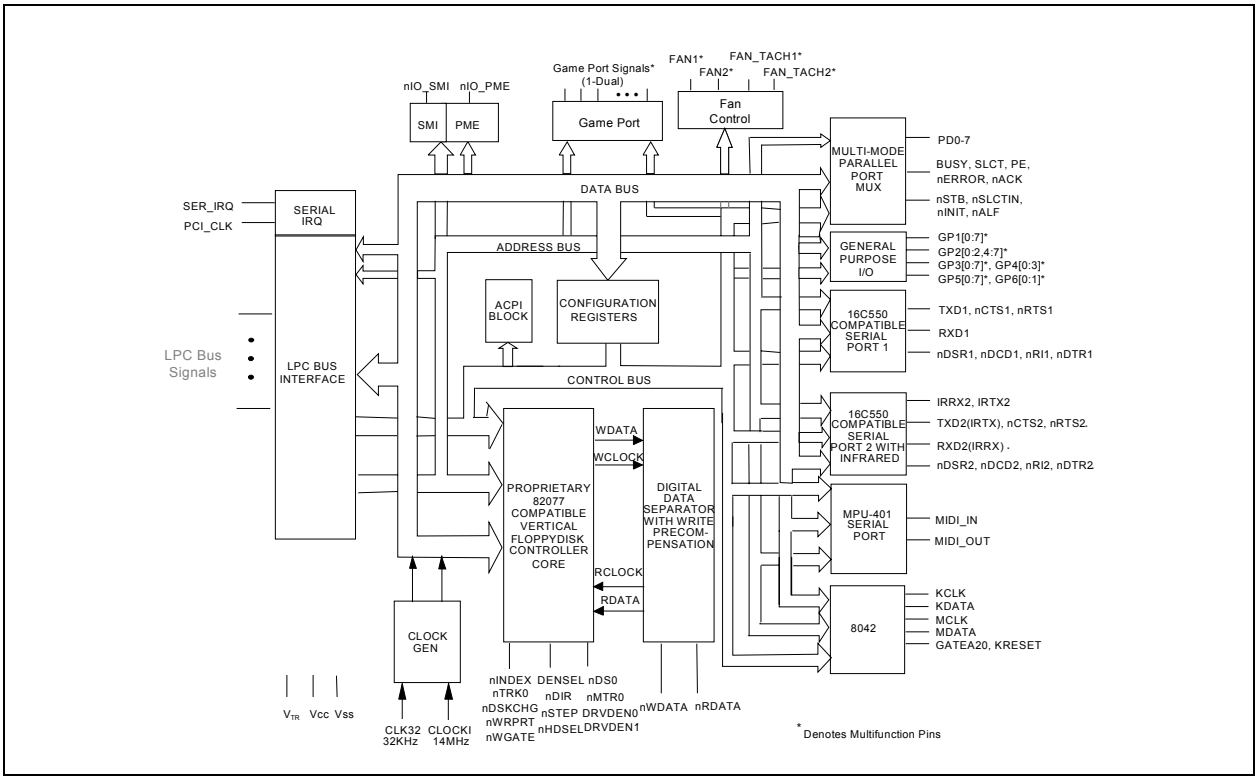
The LPC47M112 supports the ISA Plug-and-Play Standard (Version 1.0a) and provides the recommended functionality to support Windows '95, Windows 98, Windows 2000 and Windows ME.

The I/O Address, DMA Channel and hardware IRQ of each logical device in the LPC47M112 may be reprogrammed through the internal configuration registers. There are 480 I/O address location options, a Serialized IRQ interface, and three DMA channels.

The LPC47M112 does not require any external filter components and is therefore easy to use and offers lower system costs and reduced board area. The LPC47M112 is software and register compatible with Microchip's proprietary 82077AA core.

1.1 Block Diagram

FIGURE 1-1: LPC47M112 BLOCK DIAGRAM



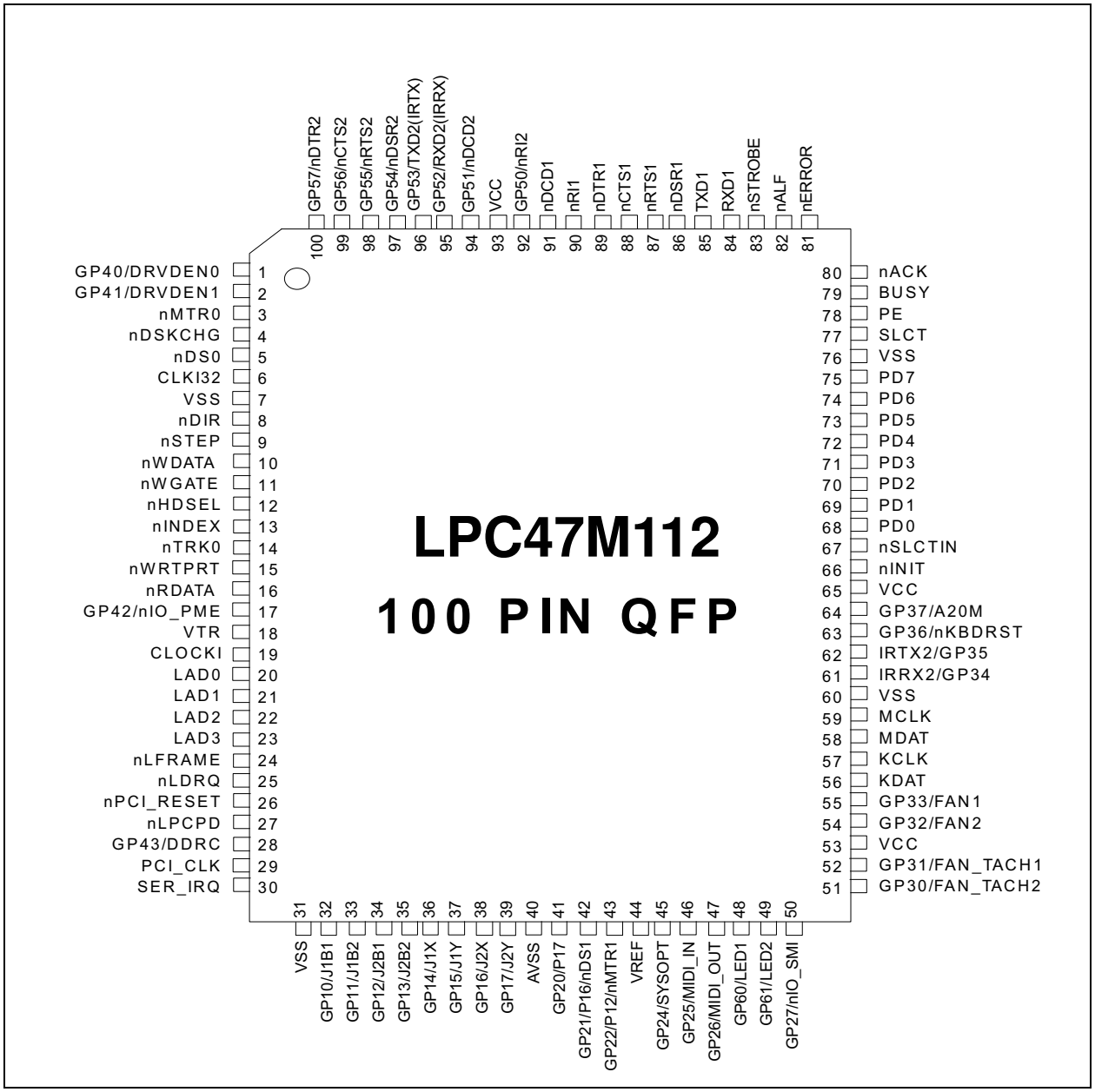
1.2 Reference Documents

1. Microchip Consumer Infrared Communications Controller (CIrCC) V1.X
2. IEEE 1284 Extended Capabilities Port Protocol and ISA Standard, Rev. 1.14, July 14, 1993
3. Hardware Description of the 8042, Intel 8 bit Embedded Controller Handbook
4. PCI Bus Power Management Interface Specification, Rev. 1.0, Draft, March 18, 1997
5. Low Pin Count (LPC) Interface Specification, Revision 1.0, September 29, 1997, Intel Document

2.0 PIN CONFIGURATION

2.1 Pin Diagram

FIGURE 2-1: LPC47M112 PIN DIAGRAM



2.2 Description of Pin Functions

Pin No./ QFP	Name	Total	Symbol	Buffer Type	Buffer Type per Function (Note 1)	Notes
PROCESSOR/HOST LPC INTERFACE (10)						
23:20	Multiplexed Command, Address, Data [3:0]	4	LAD[3:0]	PCI_IO	PCI_IO	
24	Frame	1	nLFRAME	PCI_I	PCI_I	
25	Encoded DMA Request	1	nLDRQ	PCI_O	PCI_O	
26	PCI Reset	1	nPCI_RESET	PCI_I	PCI_I	
27	Power Down	1	nLPCPD	PCI_I	PCI_I	2
29	PCI Clock	1	PCI_CLK	PCI_ICLK	PCI_ICLK	
30	Serial IRQ	1	SER_IRQ	PCI_IO	PCI_IO	
CLOCKS (2)						
6	32.768 Trickle Clock Input	1	CLOCKI32	IS	IS	3
19	14.318MHz Clock Input	1	CLOCKI	IS	IS	
FAN CONTROL (4)						
51	General Purpose I/O /Fan Tachometer 2	1	GP30/ FAN_TACH2	IO8	(I/O8/OD8)/I	
52	General Purpose I/O /Fan Tachometer 1	1	GP31/ FAN_TACH1	IO8	(I/O8/OD8)/I	
54	General Purpose I/O /Fan Speed Control 2	1	GP32/FAN2	IO12	(I/O12/OD12)/ (O12/OD12)	4
55	General Purpose I/O /Fan Speed Control 1	1	GP33/FAN1	IO12	(I/O12/OD12)/ (O12/OD12)	4
INFRARED INTERFACE (2)						
61	Infrared Rx /General Purpose I/O	1	IRRX2/GP34	IS/O8	IS/(IS/O8/OD8)	
62	Infrared Tx /General Purpose I/O	1	IRTX2/GP35	IO12	O12/(I/O12/ OD12)	5, 6
POWER PINS (10)						
53, 65,93	Power	3	VCC			
7, 31, 60,76	Ground	4	VSS			
40	Analog Ground	1	AVSS			
44	Reference Voltage	1	VREF			
18	Trickle Voltage	1	VTR			7
FDD INTERFACE (14)						
16	Read Disk Data	1	nRDATA	IS	IS	
11	Write Gate	1	nWGATE	O12	(O12/OD12)	
10	Write Disk Data	1	nWDATA	O12	(O12/OD12)	
12	Head Select	1	nHDSEL	O12	(O12/OD12)	
8	Step Direction	1	nDIR	O12	(O12/OD12)	
9	Step Pulse	1	nSTEP	O12	(O12/OD12)	
4	Disk Change	1	nDSKCHG	IS	IS	
5	Drive Select 0	1	nDS0	O12	(O12/OD12)	
3	Motor On 0	1	nMTR0	O12	(O12/OD12)	
15	Write Protected	1	nWRTPRT	IS	IS	

Pin No./ QFP	Name	Total	Symbol	Buffer Type	Buffer Type per Function (Note 1)	Notes
14	Track 0	1	nTRKO	IS	IS	
13	Index Pulse Input	1	nINDEX	IS	IS	
1	General Purpose I/O/ Drive Density Select 0	1	GP40/DRVDEN0	IO12	(I/O12/OD12)/ (O12/OD12)	
2	General Purpose I/O/ Drive Density Select 1	1	GP41/DRVDEN1	IO12	(I/O12/OD12)/ (O12/OD12)	
SERIAL PORT 1 INTERFACE (8)						
84	Receive Serial Data 1	1	RXD1	IS	IS	
85	Transmit Serial Data 1	1	TXD1	O12	O12	
87	Request to Send 1	1	nRTS1/SYSOP	O8	O8	
88	Clear to Send 1	1	nCTS1	I	I	
89	Data Terminal Ready 1	1	nDTR1	O6	O6	
86	Data Set Ready 1	1	nDSR1	I	I	
91	Data Carrier Detect 1	1	nDCD1	I	I	
90	Ring Indicator 1	1	nRI1	I	I	
SERIAL PORT 2 INTERFACE (8)						
95	General Purpose I/O /Receive Serial Data 2 (Infrared Rx)	1	GP52/RXD2(IRRX)	IS/O8	(IS/O8/OD8) /IS	
96	General Purpose I/O /Transmit Serial Data 2 (Infrared Tx)	1	GP53/TXD2(IRTX)	IO12	(I/O12/ OD12)/O12	5
98	General Purpose I/O /Request to Send 2	1	GP55/nRTS2	IO8	(I/O8/OD8)/O8	
99	General Purpose I/O /Clear to Send 2	1	GP56/ nCTS2	IO8	(I/O8/OD8)/I	
100	General Purpose I/O /Data Terminal Ready	1	GP57/ nDTR2	IO8	(I/O8/OD8)/O8	
97	General Purpose I/O /Data Set Ready 2	1	GP54/ nDSR2	IO8	(I/O8/OD8)/I	
94	General Purpose I/O/ Data Carrier Detect 2	1	GP51/nDCD2	IO8	(I/O8/OD8)/I	
92	General Purpose I/O/ Ring Indicator 2	1	GP50/nRI2	IO8	(I/O8/OD8)/I	
PARALLEL PORT INTERFACE (17)						
66	Initiate Output	1	nINIT	OP14	(OD14/OP14)	
67	Printer Select Input	1	nSLCTIN	OP14	(OD14/OP14)	
68	Port Data 0	1	PD0	IOP14	IOP14	
69	Port Data 1	1	PD1	IOP14	IOP14	
70	Port Data 2	1	PD2	IOP14	IOP14	
71	Port Data 3	1	PD3	IOP14	IOP14	
72	Port Data 4	1	PD4	IOP14	IOP14	
73	Port Data 5	1	PD5	IOP14	IOP14	
74	Port Data 6	1	PD6	IOP14	IOP14	
75	Port Data 7	1	PD7	IOP14	IOP14	
77	Printer Selected Status	1	SLCT	IO12	I/OD12	

Pin No./ QFP	Name	Total	Symbol	Buffer Type	Buffer Type per Function (Note 1)	Notes
78	Paper End	1	PE	I	I	
79	Busy	1	BUSY	I	I	
80	Acknowledge	1	nACK	I	I	
81	Error	1	nERROR	I	I	
82	Auto-feed Output	1	nALF	OP14	(OD14/OP14)	
83	Strobe Output	1	nSTROBE	OP14	(OD14/OP14)	
KEYBOARD/MOUSE INTERFACE (6)						
56	Keyboard Data	1	KDAT	IOD16	IOD16	
57	Keyboard Clock	1	KCLK	IOD16	IOD16	
58	Mouse Data	1	MDAT	IOD16	IOD16	
59	Mouse Clock	1	MCLK	IOD16	IOD16	
63	General Purpose I/O /Keyboard Reset	1	GP36/nKBDRST	IO8	(I/O8/OD8)/O8	9
64	General Purpose I/O /Gate A20	1	GP37/A20M	IO8	(I/O8/OD8)/O8	9
GENERAL PURPOSE I/O (19)						
32	General Purpose I/O/ Joystick 1 Button 1	1	GP10/J1B1	IS/O8	(IS/O8/OD8)/IS	
33	General Purpose I/O/ Joystick 1 Button 2	1	GP11/J1B2	IS/O8	(IS/O8/OD8)/IS	
34	General Purpose I/O/ Joystick 2 Button 1	1	GP12/J2B1	IS/O8	(IS/O8/OD8)/IS	
35	General Purpose I/O/ Joystick 2 Button 2	1	GP13/J2B2	IS/O8	(IS/O8/OD8)/IS	
36	General Purpose I/O/ Joystick 1 X-Axis	1	GP14/J1X	IO12	(I/O12/ OD12)/ IO12	
37	General Purpose I/O/ Joystick 1 Y-Axis	1	GP15/J1Y	IO12	(I/O12/ OD12)/ IO12	
38	General Purpose I/O/ Joystick 2 X-Axis	1	GP16/J2X	IO12	(I/O12/OD12)/IO12	
39	General Purpose I/O/ Joystick 2 Y-Axis	1	GP17/J2Y	IO12	(I/O12/OD12)/IO12	
41	General Purpose I/O/ P17	1	GP20/P17	IO8	(I/O8/OD8)/IO8	
42	General Purpose I/O/ P16 /nDS1	1	GP21/P16/nDS1	IO12	(I/O12/OD12)/ IO12/(O12/ OD12)	
43	General Purpose I/O/ P12/nMTR1	1	GP22/P12 nMTR1	IO12	(I/O12/ OD12)/ IO12/ (O12/OD12)	
45	General Purpose I/O/ System Option	1	GP24/SYSOPT	IO8	(I/O8/OD8)	8
46	General Purpose I/O/ MIDI_IN	1	GP25/MIDI_IN	IO8	(I/O8/OD8)/I	
47	General Purpose I/O/ MIDI_OUT	1	GP26/MIDI_OUT	IO12	(I/O12/OD12)/O12	
50	General Purpose I/O /SMI Output	1	GP27/nIO_SMI	IO12	(I/O12/OD12)/ OD12	

Pin No./ QFP	Name	Total	Symbol	Buffer Type	Buffer Type per Function (Note 1)	Notes
48	General Purpose I/O/ LED	1	GP60/LED1	IO12	(I/O12/OD12)/O12	10
49	General Purpose I/O/ LED	1	GP61/LED2	IO12	(I/O12/OD12)/O12	10
17	General Purpose I/O/ Power Management Event	1	GP42/nIO_PME	IO12	(I/O12/OD12)/ OD12	
28	General Purpose I/O /Device Disable Reg. Control	1	GP43/DDRC	IO8	(I/O8/OD8)/I	

Note: The "n" as the first letter of a signal name indicates an "Active Low" signal.

Note 1: Buffer types per function on multiplexed pins are separated by a slash “/”. Buffer types in parenthesis represent multiple buffer types for a single pin function.

2: The nLPCPD pin may be tied high. The LPC interface will function properly if the nPCI_RESET signal follows the protocol defined for the nLRESET signal in the “Low Pin Count Interface Specification”.

3: If the 32kHz input clock is not used the CLKI32 pin must be grounded. There is a bit in the configuration register at 0xF0 in Logical Device A that indicates whether or not the 32kHz clock is connected. This bit determines the clock source for the fan tachometer, LED and “wake on specific key” logic. Set this bit to ‘1’ if the clock is not connected.

4: The fan control pins (FAN1 and FAN2) come up as outputs and low following a VCC POR and Hard Reset. These pins revert to their non-inverting GPIO output function when VCC is removed from the part.

5: The IRTX pins (IRTX2/GP35 and GP53/TXD2 (IRTX)) are driven low when the part is powered by VTR (VCC=0V with VTR=3.3V). These pins will remain low following a power-up (VCC POR) until serial port 2 is enabled by setting the activate bit, at which time the pin will reflect the state of the transmit output of the Serial Port 2 block.

6: The VCC power-up default for this pin is Logic “0” if the IRTX function is programmed on the GPIO.

7: VTR can be connected to VCC if no wakeup functionality is required.

8: The GP24 /SYSOPT pin requires an external pulldown resistor to put the base IO address for configuration at 0x02E. An external pullup resistor is required to move the base IO address for configuration to 0x04E.

9: External pullups must be placed on the nKBDRST and A20M pins. These pins are GPIOs that are inputs after an initial power-up (VTR POR). If the nKBDRST and A20M functions are to be used, the system must ensure that these pins are high. See Section 2.4, "Pins That Require External Pullup Resistors".

10: The LED pins are powered by VTR so that the LEDs can be controlled when the part is under VTR power.

2.3 Buffer Type Descriptions

Note: The buffer type values are specified at VCC=3.3V.

IO12	Input/Output, 12mA sink, 6mA source.
IS/O12	Input with Schmitt Trigger/Output, 12mA sink, 6mA source.
O12	Output, 12mA sink, 6mA source.
OD12	Open Drain Output, 12mA sink.
O6	Output, 6mA sink, 3mA source.
O8	Output, 8mA sink, 4mA source.
OD14	Open Drain Output, 14mA sink.
OP14	Output, 14mA sink, 14mA source.

IOP14	Input/Output, 14mA sink, 14mA source. Backdrive protected.
IS/OP14	Input with Schmitt Trigger/Output, 14mA sink, 14mA source, Backdrive Protected.
IOD16	Input/Output (Open Drain), 16mA sink.
O4	Output, 4mA sink, 2mA source.
IO8	Input/Output, 8mA sink, 4mA source.
I	Input TTL Compatible.
IS	Input with Schmitt Trigger.
PCI_IO	Input/Output. These pins must meet the PCI 3.3V AC and DC Characteristics. (Note 1)
PCI_O	Output. These pins must meet the PCI 3.3V AC and DC Characteristics. (Note 1)
PCI_OD	Open Drain Output. These pins must meet the PCI 3.3V AC and DC Characteristics. (Note 1)
PCI_I	Input. These pins must meet the PCI 3.3V AC and DC Characteristics. (Note 1)
PCI_ICLK	Clock Input. These pins must meet the PCI 3.3V AC and DC Characteristics and timing. (Note 2)

Note 1: See the PCI Local Bus Specification, Revision 2.1, Section 4.2.2.

2: See the PCI Local Bus Specification, Revision 2.1, Section 4.2.2. and 4.2.3.

2.4 Pins That Require External Pullup Resistors

The following pins require external pullup resistors:

- KDAT
- KCLK
- MDAT
- MCLK
- GP36/KBDRST if KBDRST function is used
- GP37/A20M if A20M function is used
- GP20/P17 If P17 function is used
- GP21/P16 if P16 function is used
- GP22/P12 if P12 function is used
- GP27/nIO_SMI if nIO_SMI function is used as Open Collector Output
- GP42/nIO_PME if nIO_PME function is used as Open Collector Output
- SER_IRQ
- GP40/DRVDEN0 if DRVDEN0 function is used as Open Collector
- GP41/DRVDEN1 if DRVDEN1 function is used as Open Collector
- nMTR0 if used as Open Collector Output
- nDS0 if used as Open Collector Output
- nDIR if used as Open Collector Output
- nSTEP if used as Open Collector Output
- nWDATA if used as Open Collector Output
- nWGATE if used as Open Collector Output
- nHDSEL if used as Open Collector Output
- nINDEX
- nTRK0
- nWRTPRT
- nRDATA
- nDSKCHG

3.0 3 VOLT OPERATION / 5 VOLT TOLERANCE

The LPC47M112 is a 3.3 Volt part. It is intended solely for 3.3V applications. Non-LPC bus pins are 5V tolerant; that is, the input voltage is 5.5V max, and the I/O buffer output pads are backdrive protected.

The LPC interface pins are 3.3 Volt only. These signals meet PCI DC specifications for 3.3V signaling. These pins are:

- LAD[3:0]
- nLFRAME
- nLDRQ
- nLPCPD

The input voltage for all other pins is 5.5V max. These pins include all non-LPC Bus pins and the following pins:

- nPCI_RESET
- PCI_CLK
- SER_IRQ
- nIO_PME

4.0 POWER FUNCTIONALITY

The LPC47M112 has three power planes: VCC, VTR and VREF.

4.1 VCC Power

The LPC47M112 is a 3.3 Volt part. The VCC supply is 3.3 Volts (nominal). See the Operational Description Section and the Maximum Current Values sub-section.

4.2 VTR Support

The LPC47M112 requires a trickle supply (V_{TR}) to provide sleep current for the programmable wake-up events in the PME interface when V_{CC} is removed. The VTR supply is 3.3 Volts (nominal). See the Operational Description Section. The maximum VTR current that is required depends on the functions that are used in the part. See Trickle Power Functionality and Maximum Current Values sub-sections. If the LPC47M112 is not intended to provide wake-up capabilities on standby current, V_{TR} can be connected to V_{CC}. V_{TR} powers the IR interface, the PME configuration registers and the PME interface. The V_{TR} pin generates a V_{TR} Power-on-Reset signal to initialize these components.

Note:	If V_{TR} is to be used for programmable wake-up events when V_{CC} is removed, V_{TR} must be at its full minimum potential at least 10 μs before V_{cc} begins a power-on cycle. When V_{TR} and V_{cc} are fully powered, the potential difference between the two supplies must not exceed 500mV.

4.3 Internal PWRGOOD

An internal PWRGOOD logical control is included to minimize the effects of pin-state uncertainty in the host interface as V_{cc} cycles on and off. When the internal PWRGOOD signal is “1” (active), V_{cc} > 2.3V (nominal), and the LPC47M112 host interface is active. When the internal PWRGOOD signal is “0” (inactive), $V_{cc} \leq$ 2.3V (nominal), and the LPC47M112 host interface is inactive; that is, LPC bus reads and writes will not be decoded.

The LPC47M112 device pins nIO_PME, CLOCKI32, KDAT, MDAT, IRRX, nRI1, nRI2, RXD2 and most GPIOs (as input) are part of the PME interface and remain active when the internal PWRGOOD signal has gone inactive, provided V_{TR} is powered. The IRTX2/GP35, GP53/TXD2(IRTX), GP60/LED1 and GP61/LED2 pins also remain active when the internal PWRGOOD signal has gone inactive, provided V_{TR} is powered. See Trickle Power Functionality section. The internal PWRGOOD signal is also used to disable the IR Half Duplex Timeout.

4.4 32.768 kHz Trickle Clock Input

The LPC47M112 utilizes a 32.768 kHz trickle input to supply a clock signal for the fan tachometer logic, LED blink and wake on specific key function. See the following section for more information.

4.5 Indication of 32kHz Clock

There is a bit to indicate whether or not the 32kHz clock input is connected to the LPC47M112. This bit is located at bit 0 of the CLOCKI32 register at 0xF0 in Logical Device A. This register is powered by VTR and reset on a VTR POR.

Bit[0] (CLK32_PRSN) is defined as follows:

0=32kHz clock is connected to the CLKI32 pin (default)

1=32kHz clock is not connected to the CLKI32 pin (pin is grounded).

Bit 0 controls the source of the 32kHz (nominal) clock for the fan tachometer logic, the LED blink logic and the “wake on specific key” logic. When the external 32kHz clock is connected, that will be the source for the fan tachometer, LED and “wake on specific key” logic. When the external 32kHz clock is not connected, an internal 32kHz clock source will be derived from the 14MHz clock for the fan tachometer, LED and “wake on specific key” logic.

The following functions will not work under VTR power (VCC removed) if the external 32kHz clock is not connected. These functions will work under VCC power even if the external 32kHz clock is not connected.

- Wake on specific key
- LED blink
- Fan Tachometer

4.6 Trickle Power Functionality

When the LPC47M112 is running under VTR only (VCC removed), PME wakeup events are active and (if enabled) able to assert the nIO_PME pin active low. The following lists the wakeup events:

- UART 1 Ring Indicator
- UART 2 Ring Indicator
- Keyboard data
- Mouse data
- Wake on Specific Key Logic
- Fan Tachometers (Note)
- GPIOs for wakeup. See below.

Note: The Fan Tachometers can generate a PME when VCC=0. Clear the enable bits for the fan tachometers before removing fan power.

The following requirements apply to all I/O pins that are specified to be 5 volt tolerant.

- I/O buffers that are wake-up event compatible are powered by VCC. Under VTR power (VCC=0), these pins may only be configured as inputs. These pins have input buffers into the wakeup logic that are powered by VTR.
- I/O buffers that may be configured as either push-pull or open drain under VTR power (VCC=0), are powered by VTR. This means, at a minimum, they will source their specified current from VTR even when VCC is present.

The GPIOs that are used for PME wakeup as input are GP10-GP17, GP20-GP22, GP24-GP27, GP30-GP33, GP41, GP43, GP50-GP57, GP60, GP61. These GPIOs function as follows (with the exception of GP53, GP60 and GP61 - see below):

- Buffers are powered by VCC, but in the absence of VCC they are backdrive protected (they do not impose a load on any external VTR powered circuitry). They are wakeup compatible as inputs under VTR power. These pins have input buffers into the wakeup logic that are powered by VTR.

All GPIOs listed above are for PME wakeup as a GPIO (or alternate function). Note that GP32 and GP33 cannot be used for wakeup under VTR power (VCC=0) since these are the fan control pins which come up as outputs and low following a VCC POR and Hard Reset. GP53 cannot be used for wakeup under VTR power since this is the IRTX pin which comes up as output and low following a VTR POR, a VCC POR and Hard Reset. Also, GP32 and GP33 revert to their non-inverting GPIO output function when VCC is removed from the part. GP43 reverts to the basic GPIO function when VCC is removed from the part, but its programmed input/output, invert/non-invert and output buffer type is retained.

The other GPIOs function as follows:

GP36, GP37 and GP40:

- Buffers are powered by VCC, but in the absence of VCC they are backdrive protected. These pins do not have input buffers into the wakeup logic that are powered by VTR.

These pins are not used for wakeup.

GP35, GP42, GP53, GP60 and GP61:

- Buffers powered by VTR.

GP35 and GP53 have IRTX as the alternate function and their output buffers are powered by VTR so that the pins are always forced low when not used.

GP42 is the nIO_PME pin which is active under VTR.

GP60 and GP61 have LED as the alternate function and the logic is able to control the pin under VTR.

The IRTX pins (IRTX2/GP35 and GP53/TXD2 (IRTX)) are powered by VTR so that they are driven low when VCC = 0V with VTR = 3.3V. These pins will remain low following a VCC POR until serial port 2 is enabled by setting the activate bit, at which time the pin will reflect the state of the transmit output of the Serial Port 2 block.

The following list summarizes the blocks, registers and pins that are powered by VTR.

- PME interface block
- PME runtime register block (includes all PME, SMI, GPIO, Fan and other miscellaneous registers)
- "Wake on Specific Key" logic
- LED control logic
- Fan Tachometers
- Pins for PME Wakeup:
  - GP42/nIO_PME (output, buffer powered by VTR)
  - nRI1 (input)
  - GP50/nRI2 (input)
  - GP52/RXD2 (input)
  - KDAT (input)
  - MDAT
  - GPIOs (GP10-GP17, GP20-GP22, GP24-GP27, GP30-GP33, GP41, GP43, GP50-GP57, GP60, GP61) – all input-only except GP53, GP60, GP61. See below.
- Other Pins
  - IRTX2/GP35 (output, buffer powered by VTR)
  - GP53/TXD2(IRTX) (output, buffer powered by VTR)
  - GP60/LED1 (output, buffer powered by VTR)
  - GP61/LED2 (output, buffer powered by VTR)

4.7 VREF Pin

The LPC47M112 has a reference voltage pin input on pin 44 of the part. This reference voltage can be connected to either a 5V supply or a 3.3V supply. It is used for the game port. See the "GAME PORT LOGIC" section.

4.8 Maximum Current Values

See the "Operational Description" section for the maximum current values.

The maximum VTR current, I_{TR}, is given with all outputs open (not loaded) and all inputs in a fixed state (i.e., 0V or 3.3V). The total maximum current for the part is the unloaded value PLUS the maximum current sourced by all pins that are driven by VTR. The pins that are powered by VTR are as follows: GP42 / nIO_PME, IRTX2 / GP35, GP53/TXD2 (IRTX), GP60 / LED1, GP61 / LED2. These pins, if configured as push-pull outputs, will source a minimum of 6mA at 2.4V when driving.

The maximum VCC current, I_{CC}, is given with all outputs open (not loaded) and all inputs in a fixed state (i.e., 0V or 3.3V).

The maximum VREF current, I_{REF}, is given with all outputs open (not loaded) and all inputs in a fixed state (i.e., 0V or 3.3V).

4.9 Power Management Events (PME/SCI)

The LPC47M112 offers support for Power Management Events (PMEs), also referred to as System Control Interrupt (SCI) events. The terms PME and SCI are used synonymously throughout this document to refer to the indication of an event to the chipset via the assertion of the nIO_PME output signal on pin 17. See the "PME Support" section.

5.0 FUNCTIONAL DESCRIPTION

5.1 Super I/O Registers

The address map, shown below in Table 5-1, shows the addresses of the different blocks of the Super I/O immediately after power up. The base addresses of the FDC, serial and parallel ports, PME register block, Game port and configuration register block can be moved via the configuration registers. Some addresses are used to access more than one register.

5.2 Host Processor Interface (LPC)

The host processor communicates with the LPC47M112 through a series of read/write registers via the LPC interface. The port addresses for these registers are shown in Table 5-1. Register access is accomplished through I/O cycles or DMA transfers. All registers are 8 bits wide.

TABLE 5-1: SUPER I/O BLOCK ADDRESSES

Address	Block Name	Logical Device
Base+(0-5) and +(7)	Floppy Disk	0
Base+(0-7)	Serial Port Com 1	4
Base1+(0-7) Base2+(0-7)	Serial Port Com 2	5
Base+(0-3) Base+(0-7) Base+(0-3), +(400-402) Base+(0-7), +(400-402)	Parallel Port SPP EPP ECP ECP+EPP+SPP	3
60, 64	KYBD	7
Base + 0	Game Port	9
Base + (0-5F)	Runtime Registers	A
Base + (0-7)	MPU-401	B
Base + (0-1)	Configuration	

Note: Refer to the configuration register descriptions for setting the base address.

5.2.1 LPC INTERFACE

The following sub-sections specify the implementation of the LPC bus.

5.2.2 LPC INTERFACE SIGNAL DEFINITION

The signals required for the LPC bus interface are described in the table below. LPC bus signals use PCI 33MHz electrical signal characteristics.

Signal Name	Type	Description
LAD[3:0]	I/O	LPC address/data bus. Multiplexed command, address and data bus.
nLFRAME	Input	Frame signal. Indicates start of new cycle and termination of broken cycle
nPCI_RESET	Input	PCI Reset. Used as LPC Interface Reset. Same functionality as RST_DRV but active low 3.3V.
nLDRQ	Output	Encoded DMA/Bus Master request for the LPC interface.
nIO_PME	OD	Power Mgt Event signal. Allows the LPC47M112 to request wakeup.
nLPCPD	Input	Powerdown Signal. Indicates that the LPC47M112 should prepare for power to be shut on the LPC interface.
SER_IRQ	I/O	Serial IRQ.
PCI_CLK	Input	PCI Clock.

Note: The nCLKRUN signal is not implemented in this part.

5.2.3 LPC CYCLES

The following cycle types are supported by the LPC protocol.

Cycle Type	Transfer Size
I/O Write	1 Byte
I/O Read	1 Byte
DMA Write	1 Byte
DMA Read	1 Byte

Peripherals must ignore cycles that they do not support.

5.2.4 FIELD DEFINITIONS

The data transfers are based on specific fields that are used in various combinations, depending on the cycle type. These fields are driven onto the LAD[3:0] signal lines to communicate address, control and data information over the LPC bus between the host and the LPC47M112. See the *Low Pin Count (LPC) Interface Specification* Reference, Section 4.2 for definition of these fields.

5.2.4.1 nLFRAME Usage

nLFRAME is used by the host to indicate the start of cycles and the termination of cycles due to an abort or time-out condition. This signal is to be used by the LPC47M112 to know when to monitor the bus for a cycle.

This signal is used as a general notification that the LAD[3:0] lines contain information relative to the start or stop of a cycle, and that the LPC47M112 monitors the bus to determine whether the cycle is intended for it. The use of nLFRAME allows the LPC47M112 to enter a lower power state internally. There is no need for the LPC47M112 to monitor the bus when it is inactive, so it can decouple its state machines from the bus, and internally gate its clocks.

When the LPC47M112 samples nLFRAME active, it immediately stops driving the LAD[3:0] signal lines on the next clock and monitor the bus for new cycle information.

The nLFRAME signal functions as described in the Low Pin Count (LPC) Interface Specification, Revision 1.0.

5.2.4.2 I/O Read and Write Cycles

The LPC47M112 is the target for I/O cycles. I/O cycles are initiated by the host for register or FIFO accesses, and will generally have minimal Sync times. The minimum number of wait-states between bytes is 1. EPP cycles will depend on the speed of the external device, and may have much longer Sync times.

Data transfers are assumed to be exactly 1-byte. If the CPU requested a 16 or 32-bit transfer, the host will break it up into 8-bit transfers.

See the *Low Pin Count (LPC) Interface Specification* Reference, Section 5.2, for the sequence of cycles for the I/O Read and Write cycles.

5.2.4.3 DMA Read and Write Cycles

DMA read cycles involve the transfer of data from the host (main memory) to the LPC47M112. DMA write cycles involve the transfer of data from the LPC47M112 to the host (main memory). Data will be coming from or going to a FIFO and will have minimal Sync times. Data transfers to/from the LPC47M112 are 1, 2 or 4 bytes.

See the *Low Pin Count (LPC) Interface Specification* Reference, Section 6.4, for the field definitions and the sequence of the DMA Read and Write cycles.

5.2.4.4 DMA Protocol

DMA on the LPC bus is handled through the use of the nLDRQ lines from the LPC47M112 and special encodings on LAD[3:0] from the host.

The DMA mechanism for the LPC bus is described in the Low Pin Count (LPC) Interface Specification, Revision 1.0.

5.3 Power Management

5.3.1 CLOCKRUN PROTOCOL

The nCLKRUN pin is not implemented in the LPC47M112. See the *Low Pin Count (LPC) Interface Specification* Section.

5.3.1.1 LPCPD Protocol

See the *Low Pin Count (LPC) Interface Specification* Section.

5.3.1.2 SYNC Protocol

See the *Low Pin Count (LPC) Interface Specification* Section for a table of valid SYNC values.

5.3.2 TYPICAL USAGE

The SYNC pattern is used to add wait states. For read cycles, the LPC47M112 immediately drives the SYNC pattern upon recognizing the cycle. The host immediately drives the sync pattern for write cycles. If the LPC47M112 needs to assert wait states, it does so by driving 0101 or 0110 on LAD[3:0] until it is ready, at which point it will drive 0000 or 1001. The LPC47M112 will choose to assert 0101 or 0110, but not switch between the two patterns.

The data (or wait state SYNC) will immediately follow the 0000 or 1001 value.

The SYNC value of 0101 is intended to be used for normal wait states, wherein the cycle will complete within a few clocks. The LPC47M112 uses a SYNC of 0101 for all wait states in a DMA transfer.

The SYNC value of 0110 is intended to be used where the number of wait states is large. This is provided for EPP cycles, where the number of wait states could be quite large (>1 microsecond). However, the LPC47M112 uses a SYNC of 0110 for all wait states in an I/O transfer.

The SYNC value is driven within 3 clocks.

5.3.3 SYNC TIMEOUT

The SYNC value is driven within 3 clocks. If the host observes 3 consecutive clocks without a valid SYNC pattern, it will abort the cycle.

The LPC47M112 does not assume any particular timeout. When the host is driving SYNC, it may have to insert a very large number of wait states, depending on PCI latencies and retries.

5.3.4 SYNC PATTERNS AND MAXIMUM NUMBER OF SYNCS

If the SYNC pattern is 0101, then the host assumes that the maximum number of SYNCs is 8.

If the SYNC pattern is 0110, then no maximum number of SYNCs is assumed. The LPC47M112 has protection mechanisms to complete the cycle. This is used for EPP data transfers and should utilize the same timeout protection that is in EPP.

5.3.5 SYNC ERROR INDICATION

The LPC47M112 reports errors via the LAD[3:0] = 1010 SYNC encoding.

If the host was reading data from the LPC47M112, data will still be transferred in the next two nibbles. This data may be invalid, but it will be transferred by the LPC47M112. If the host was writing data to the LPC47M112, the data had already been transferred.

In the case of multiple byte cycles, such as memory and DMA cycles, an error SYNC terminates the cycle. Therefore, if the host is transferring 4 bytes from a device, if the device returns the error SYNC in the first byte, the other three bytes will not be transferred.

5.3.5.1 I/O and DMA START Fields

I/O and DMA cycles use a START field of 0000.

5.3.5.2 Reset Policy

The following rules govern the reset policy:

1. When nPCI_RESET goes inactive (high), the clock is assumed to have been running for 100usec prior to the removal of the reset signal, so that everything is stable. This is the same reset active time after clock is stable that is used for the PCI bus.

2. When nPCI_RESET goes active (low):
   a) the host drives the nLFRAME signal high, tristates the LAD[3:0] signals, and ignores the nLDRQ signal.
   b) the LPC47M112 must ignore nLFRAME, tristate the LAD[3:0] pins and drive the nLDRQ signal inactive (high).

5.3.5.3 Electrical Specifications

The LPC interface uses 3.3V signaling. No output from the LPC47M112 drives higher than 3.3V nominal.

The electrical characteristics of each signal is described below.

5.3.5.3.1 LAD[3:0]

The AC and DC specifications for these signals are the same as defined for AD[31:0] in section 4.2.2 of the “PCI Local Bus Specification, Rev 2.1”. That section contains the specifications for the 3.3V signaling environment.

The LAD[3:0] signals go high during the TAR phase. The last device driving the LAD[3:0] is responsible to drive the signals high during the first clock of the TAR phase. During the second clock, neither the host nor the LPC47M112 will drive LAD[3:0] (LAD[3:0] is floated).

Weak pull-up resistors of 10k-100k ohms will be included on LAD[3:0] to keep the signals high. These pull-ups are external to the LPC47M112.

5.3.5.3.2 nLDRQ

The AC and DC specifications for these signals are the same as for non-shared signals as defined in section 4.2.2 of the “PCI Local Bus Specification, Rev 2.1”. That section contains the specifications for the 3.3V signaling environment.

nLDRQ is a standard output from the LPC47M112 and a standard input to the host.

5.3.5.3.3 nLPCPD

The host drives this signal as a standard 3.3V output.

5.3.5.3.4 nLFRAME

The host drives this signal as a standard 3.3V output.

5.3.5.3.5 nPCI_RESET

The host drives this signal as a standard 3.3V output.

5.4 LPC Transfer Sequence Examples

5.4.1 WAIT STATE REQUIREMENTS

5.4.1.1 I/O Transfers

The LPC47M112 inserts three wait states for an I/O read and two wait states for an I/O write cycle. A SYNC of 0110 is used for all I/O transfers. The exception to this is for transfers where IOCHRDY has been deasserted (i.e., EPP or IrCC transfers) in which case the sync pattern of 0110 is used and a large number of syncs may be inserted (up to 330 which corresponds to a timeout of 10us).

5.4.1.2 DMA Transfers

The LPC47M112 inserts three wait states for a DMA read and four wait states for a DMA write cycle. A SYNC of 0101 is used for all DMA transfers.

See the example timing for the LPC cycles in the “Timing Diagrams” section.

6.0 FLOPPY DISK CONTROLLER

The Floppy Disk Controller (FDC) provides the interface between a host microprocessor and the floppy disk drives. The FDC integrates the functions of the Formatter/Controller, Digital Data Separator, Write Precompensation and Data Rate Selection logic for an IBM XT/AT compatible FDC. The true CMOS 765B core ensures 100% IBM PC XT/AT compatibility in addition to providing data overflow and underflow protection.

The FDC is compatible to the 82077AA using Microchip's proprietary floppy disk controller core.

6.1 FDC Internal Registers

The Floppy Disk Controller contains eight internal registers which facilitate the interfacing between the host microprocessor and the disk drive. Table 6-1 shows the addresses required to access these registers. Registers other than the ones shown are not supported. The rest of the description assumes that the primary addresses have been selected.

TABLE 6-1: STATUS, DATA AND CONTROL REGISTERS

Primary Address	Secondary Address	R/W	Register
3F0	370	R	Status Register A (SRA)
3F1	371	R	Status Register B (SRB)
3F2	372	R/W	Digital Output Register (DOR)
3F3	373	R/W	Tape Drive Register (TSR)
3F4	374	R	Main Status Register (MSR)
3F4	374	W	Data Rate Select Register (DSR)
3F5	375	R/W	Data (FIFO)
3F6	376		Reserved
3F7	377	R	Digital Input Register (DIR)
3F7	377	W	Configuration Control Register (CCR)

(Shown with base addresses of 3F0 and 370.)

6.1.1 STATUS REGISTER A (SRA)

Address 3F0 READ ONLY

This register is read-only and monitors the state of the internal interrupt signal and several disk interface pins in PS/2 and Model 30 modes. The SRA can be accessed at any time when in PS/2 mode. In the PC/AT mode the data bus pins D0 - D7 are held in a high impedance state for a read of address 3F0.

PS/2 Mode

	7	6	5	4	3	2	1	0
	INT PENDING	nDRV2	STEP	nTRK0	HDSEL	nINDX	nWP	DIR
RESET COND.	0	1	0	N/A	0	N/A	N/A	0

BIT 0 DIRECTION

Active high status indicating the direction of head movement. A logic "1" indicates inward direction; a logic "0" indicates outward direction.

BIT 1 nWRITE PROTECT

Active low status of the WRITE PROTECT disk interface input. A logic "0" indicates that the disk is write protected.

BIT 2 nINDEX

Active low status of the INDEX disk interface input.

BIT 3 HEAD SELECT

Active high status of the HDSEL disk interface input. A logic "1" selects side 1 and a logic "0" selects side 0.

BIT 4 nTRACK 0

Active low status of the TRK0 disk interface input.

BIT 5 STEP

Active high status of the STEP output disk interface output pin.

BIT 6 nDRV2

This function is not supported. This bit is always read as “1”.

BIT 7 INTERRUPT PENDING

Active high bit indicating the state of the Floppy Disk Interrupt output.

PS/2 Model 30 Mode

	7	6	5	4	3	2	1	0
	INT PENDING	DRQ	STEP F/F	TRK0	nHDSEL	INDX	WP	nDIR
RESET COND.	0	0	0	N/A	1	N/A	N/A	1

BIT 0 nDIRECTION

Active low status indicating the direction of head movement. A logic "0" indicates inward direction; a logic "1" indicates outward direction.

BIT 1 WRITE PROTECT

Active high status of the WRITE PROTECT disk interface input. A logic "1" indicates that the disk is write protected.

BIT 2 INDEX

Active high status of the INDEX disk interface input.

BIT 3 nHEAD SELECT

Active low status of the HDSEL disk interface input. A logic "0" selects side 1 and a logic "1" selects side 0.

BIT 4 TRACK 0

Active high status of the TRK0 disk interface input.

BIT 5 STEP

Active high status of the latched STEP disk interface output pin. This bit is latched with the STEP output going active, and is cleared with a read from the DIR register, or with a hardware or software reset.

BIT 6 DMA REQUEST

Active high status of the DMA request pending.

BIT 7 INTERRUPT PENDING

Active high bit indicating the state of the Floppy Disk Interrupt.

6.1.2 STATUS REGISTER B (SRB)

Address 3F1 READ ONLY

This register is read-only and monitors the state of several disk interface pins in PS/2 and Model 30 modes. The SRB can be accessed at any time when in PS/2 mode. In the PC/AT mode the data bus pins D0 - D7 are held in a high impedance state for a read of address 3F1.

PS/2 Mode

	7	6	5	4	3	2	1	0
	1	1	DRIVE SEL0	WDATA TOGGLE	RDATA TOGGLE	WGATE	MOT EN1	MOT EN0
RESET COND.	1	1	0	0	0	0	0	0

BIT 0 MOTOR ENABLE 0

Active high status of the MTR0 disk interface output pin. This bit is low after a hardware reset and unaffected by a software reset.

BIT 1 MOTOR ENABLE 1

Active high status of the MTR1 disk interface output pin. This bit is low after a hardware reset and unaffected by a software reset.

BIT 2 WRITE GATE

Active high status of the WGATE disk interface output.

BIT 3 READ DATA TOGGLE

Every inactive edge of the RDATA input causes this bit to change state.

BIT 4 WRITE DATA TOGGLE

Every inactive edge of the WDATA input causes this bit to change state.

BIT 5 DRIVE SELECT 0

Reflects the status of the Drive Select 0 bit of the DOR (address 3F2 bit 0). This bit is cleared after a hardware reset and it is unaffected by a software reset.

BIT 6 RESERVED

Always read as a logic "1".

BIT 7 RESERVED

Always read as a logic "1".

PS/2 Model 30 Mode

	7	6	5	4	3	2	1	0
	nDRV2	nDS1	nDS0	WDATA F/F	RDATA F/F	WGATE F/F	nDS3	nDS2
RESET COND.	N/A	1	1	0	0	0	1	1

BIT 0 nDRIVE SELECT 2

The DS2 disk interface is not supported.

BIT 1 nDRIVE SELECT 3

The DS3 disk interface is not supported.

BIT 2 WRITE GATE

Active high status of the latched WGATE output signal. This bit is latched by the active going edge of WGATE and is cleared by the read of the DIR register.

BIT 3 READ DATA

Active high status of the latched RDATA output signal. This bit is latched by the inactive going edge of RDATA and is cleared by the read of the DIR register.

BIT 4 WRITE DATA

Active high status of the latched WDATA output signal. This bit is latched by the inactive going edge of WDATA and is cleared by the read of the DIR register. This bit is not gated with WGATE.

BIT 5 nDRIVE SELECT 0

Active low status of the DS0 disk interface output.

BIT 6 nDRIVE SELECT 1

Active low status of the DS1 disk interface output.

BIT 7 nDRV2

Active low status of the DRV2 disk interface input.

Note: This function is not supported.

6.1.3 DIGITAL OUTPUT REGISTER (DOR)

Address 3F2 READ/WRITE

The DOR controls the drive select and motor enables of the disk interface outputs. It also contains the enable for the DMA logic and a software reset bit. The contents of the DOR are unaffected by a software reset. The DOR can be written to at any time.

	7	6	5	4	3	2	1	0
	MOT EN3	MOT EN2	MOT EN1	MOT EN0	DMAEN	nRESET	DRIVE SEL1	DRIVE SEL0
RESET COND.	0	0	0	0	0	0	0	0

BIT 0 and 1 DRIVE SELECT

These two bits are binary encoded for the drive selects, thereby allowing only one drive to be selected at one time.

BIT 2 nRESET

A logic "0" written to this bit resets the Floppy disk controller. This reset will remain active until a logic "1" is written to this bit. This software reset does not affect the DSR and CCR registers, nor does it affect the other bits of the DOR register. The minimum reset duration required is 100ns, therefore toggling this bit by consecutive writes to this register is a valid method of issuing a software reset.

BIT 3 DMAEN

PC/AT and Model 30 Mode:

Writing this bit to logic "1" will enable the DMA and interrupt functions. This bit being a logic "0" will disable the DMA and interrupt functions. This bit is a logic "0" after a reset and in these modes.

PS/2 Mode:

In this mode the DMA and interrupt functions are always enabled. During a reset, this bit will be cleared to a logic "0".

BIT 4 MOTOR ENABLE 0

This bit controls the MTR0 disk interface output. A logic "1" in this bit will cause the output pin to go active.

Drive	DOR Value
0	1CH
1	2DH

BIT 5 MOTOR ENABLE 1

This bit controls the MTR1 disk interface output. A logic "1" in this bit will cause the output pin to go active.

BIT 6 MOTOR ENABLE 2

The MTR2 disk interface output is not supported in the LPC47M112.

BIT 7 MOTOR ENABLE 3

The MTR3 disk interface output is not supported in the LPC47M112.

6.1.4 TAPE DRIVE REGISTER (TDR)

Address 3F3 READ/WRITE

The Tape Drive Register (TDR) is included for 82077 software compatibility and allows the user to assign tape support to a particular drive during initialization. Any future references to that drive automatically invokes tape support. The TDR Tape Select bits TDR.[1:0] determine the tape drive number. Table 6-2 illustrates the Tape Select Bit encoding. Note that drive 0 is the boot device and cannot be assigned tape support. The remaining Tape Drive Register bits TDR.[7:2] are tristated when read. The TDR is unaffected by a software reset.

TABLE 6-2: TAPE SELECT BITS

Tape SEL1 (TDR.1)	Tape SEL0 (TDR.0)	Drive Selected
0	0	None
0	1	1
1	0	2
1	1	3

TABLE 6-3: INTERNAL 2 DRIVE DECODE - NORMAL

Digital Output Register						Drive Select Outputs (Active Low)		Motor on Outputs (Active Low)	
Bit 7	Bit 6	Bit 5	Bit 4	Bit1	Bit 0	nDS1	nDS0	nMTR1	nMTR0
X	X	X	1	0	0	1	0	nBIT 5	nBIT 4
X	X	1	X	0	1	0	1	nBIT 5	nBIT 4
X	1	X	X	1	0	1	1	nBIT 5	nBIT 4
1	X	X	X	1	1	1	1	nBIT 5	nBIT 4
0	0	0	0	X	X	1	1	nBIT 5	nBIT 4

TABLE 6-4: INTERNAL 2 DRIVE DECODE - DRIVES 0 AND 1 SWAPPED

Digital Output Register						Drive Select Outputs (Active Low)		Motor on Outputs (Active Low)	
Bit 7	Bit 6	Bit 5	Bit 4	Bit1	Bit 0	nDS1	nDS0	nMTR1	nMTR0
X	X	X	1	0	0	0	1	nBIT 4	nBIT 5
X	X	1	X	0	1	1	0	nBIT 4	nBIT 5
X	1	X	X	1	0	1	1	nBIT 4	nBIT 5
1	X	X	X	1	1	1	1	nBIT 4	nBIT 5
0	0	0	0	X	X	1	1	nBIT 4	nBIT 5

	7	6	5	4	3	2	1	0
	S/W RESET	POWER DOWN	0	PRE-COMP2	PRE-COMP1	PRE-COMP0	DRATE SEL1	DRATE SEL0
RESET COND.	0	0	0	0	0	0	1	0