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LPC5410x

32-bit ARM Cortex-M4/M0+ MCU; 104 kB SRAM; 512 kB flash, 3 x I2C, 2 x SPI, 4 x USART, 32-bit counter/ timers, SCTimer/PWM, 12-bit 5.0 Msamples/sec ADC

Rev. 2.9 — 26 January 2018 Product data sheet

1. General description

The LPC5410x are ARM Cortex-M4 based microcontrollers for embedded applications. These devices include an optional ARM Cortex-M0+ coprocessor, 104 kB of on-chip SRAM, up to 512 kB on-chip flash, five general-purpose timers, one State-Configurable Timer with PWM capabilities (SCTimer/PWM), one RTC/alarm timer, one 24-bit Multi-Rate Timer (MRT), a Repetitive Interrupt Timer (RIT), a Windowed Watchdog Timer (WWDT), four USARTs, two SPIs, three Fast-mode plus I^2C-bus interfaces with high-speed slave mode, and one 12-bit 5.0 Msamples/sec ADC.

The ARM Cortex-M4 is a 32-bit core that offers system enhancements such as low power consumption, enhanced debug features, and a high level of support block integration. The ARM Cortex-M4 CPU incorporates a 3-stage pipeline, uses a Harvard architecture with separate local instruction and data buses as well as a third bus for peripherals, and includes an internal prefetch unit that supports speculative branching. The ARM Cortex-M4 supports single-cycle digital signal processing and SIMD instructions. A hardware floating-point unit is integrated in the core.

The ARM Cortex-M0+ coprocessor is an energy-efficient and easy-to-use 32-bit core which is code and tool-compatible with the Cortex-M4 core. The Cortex-M0+ coprocessor offers up to 100 MHz performance with a simple instruction set and reduced code size. In LPC5410x, the Cortex-M0 coprocessor hardware multiply is implemented as a 32-cycle iterative multiplier.

2. Features and benefits

- Dual processor cores: ARM Cortex-M4 and ARM Cortex-M0+. The M0+ core runs at the same frequency as the M4 core. Both cores operate up to a maximum frequency of 100 MHz.
- ARM Cortex-M4 core (version r0p1):
  - ARM Cortex-M4 processor, running at a frequency of up to 100 MHz, using the same clock as the Cortex-M4.
  - Floating Point Unit (FPU) and Memory Protection Unit (MPU).
  - ARM Cortex-M4 built-in Nested Vectored Interrupt Controller (NVIC).
  - Non-maskable Interrupt (NMI) input with a selection of sources.
  - Serial Wire Debug with eight breakpoints and four watch points. Includes Serial Wire Output for enhanced debug capabilities.
  - System tick timer.

- ARM Cortex-M0+ core (version r0p1):
  - ARM Cortex-M0+ processor, running at a frequency of up to 100 MHz.
  - ARM Cortex-M0+ built-in Nested Vectored Interrupt Controller (NVIC).
  - Non-maskable Interrupt (NMI) input with a selection of sources.
  - Serial Wire Debug with four breakpoints and two watch points.
  - System tick timer.
- On-chip memory:
  - Up to 512 kB on-chip flash program memory with flash accelerator and 256 byte page erase and write.
  - 104 kB total SRAM composed of:
  - Up to 96 kB contiguous main SRAM.
  - An additional 8 kB SRAM.
- ROM API support:
  - Flash In-Application Programming (IAP) and In-System Programming (ISP).
  - Power control API.
- Serial interfaces:
  - Four USART interfaces with synchronous mode and 32 kHz mode for wake-up from deep sleep and power down modes. The USARTs have FIFO support from the System FIFO and share a fractional baud-rate generator.
  - Two SPI interfaces, each with four slave selects and flexible data configuration. The SPIs have FIFO support from the System FIFO. The slave function is able to wake up the device from deep sleep and power down modes.
  - Three I^2C-bus interfaces supporting fast mode and Fast-mode Plus with data rates of up to 1Mbit/s and with multiple address recognition and monitor mode. Each I^2C-bus interface also supports High Speed Mode (3.4 Mbit/s) as a slave. The slave function is able to wake up the device from deep sleep and power down modes.
- Digital peripherals:
  - DMA controller with 22 channels and 20 programmable triggers, able to access all memories and DMA-capable peripherals.
  - Up to 50 General-Purpose Input/Output (GPIO) pins. Most GPIOs have configurable pull-up/pull-down resistors, programmable open-drain mode, and input inverter.
  - GPIO registers are located on the AHB for fast access. The DMA supports GPIO ports.
  - Up to eight GPIOs (pin interrupts) can be selected as edge-sensitive (rising or falling edges or both) interrupt requests or level-sensitive (active low or active high) interrupt requests. In addition, up to eight GPIOs can be selected to contribute a boolean expression and interrupt generation using the pattern match engine block.
  - Two GPIO grouped interrupts (GINT) enable an interrupt based on a logical (AND/OR) combination of input states.
  - CRC engine.
- Timers:
  - Five 32-bit standard general purpose timers/counters, four of which support up to 4 capture inputs and 4 compare outputs, PWM mode, and external count input. Specific timer events can be selected to generate DMA requests. The fifth timer does not have external pin connections and may be used for internal timing operations.

- One State Configurable Timer/PWM (SCT/PWM) with 8 inputs (6 external inputs and 2 internal inputs) and 8 output functions (including capture and match). Inputs and outputs can be routed to/from external pins and internally to/from selected peripherals. Internally, the SCT supports 13 captures/matches, 13 events and 13 states.
- 32-bit Real-time clock (RTC) with 1 s resolution running in the always-on power domain. A timer in the RTC can be used for wake-up from all low power modes including deep power-down, with 1 ms resolution.
- Multiple-channel multi-rate 24-bit timer (MRT) for repetitive interrupt generation at up to four programmable, fixed rates.
- Windowed Watchdog Timer (WWDT).
- Ultra-low power Micro-tick Timer, running from the Watchdog oscillator, that can be used to wake up the device from low power modes.
- Repetitive Interrupt Timer (RIT) for debug time-stamping and general-purpose use.

- Analog peripheral: 12-bit, 12-channel, Analog-to-Digital Converter (ADC) supporting 5.0 Msamples/s. The ADC supports two independent conversion sequences.
- Clock generation:
  - 12 MHz internal RC oscillator.
  - External clock input for clock frequencies of up to 25 MHz.
  - Internal low-power, watchdog oscillator (WDOSC) with a nominal frequency of 500 kHz.
  - 32 kHz low-power RTC oscillator.
  - System PLL allows CPU operation up to the maximum CPU rate. May be run from the internal RC oscillator, the external clock input CLKIN, or the RTC oscillator.
  - Clock output function for monitoring internal clocks.
  - Frequency measurement unit for measuring the frequency of any on-chip or off-chip clock signal.
- Power-saving modes and wake-up:
  - Integrated PMU (Power Management Unit) to minimize power consumption.
  - Reduced power modes: sleep, deep sleep, power down, and deep power-down.
  - Wake-up from deep sleep and power down modes via activity on the USART, SPI, and I^2C peripherals.
  - Wake-up from sleep, deep sleep, power down, and deep power-down modes using the RTC alarm.
- Single power supply 1.62 V to 3.6 V.
- Power-On Reset (POR).
- Brown-Out Detect (BOD) with separate thresholds for interrupt and forced reset.
- JTAG boundary scan supported.
- Unique device serial number (128 bit) for identification.
- Operating temperature range −40 °C to 105 °C.
- Available in a 3.288 x 3.288 mm WLCSP49 package and LQFP64 package.

3. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
LPC54102J512UK49	WLCSP49	wafer level chip-size package; 49 (7 x 7) bumps; 3.288 x 3.288 x 0.54 mm	-
LPC54102J256UK49	WLCSP49	wafer level chip-size package; 49 (7 x 7) bumps; 3.288 x 3.288 x 0.54 mm	-
LPC54101J512UK49	WLCSP49	wafer level chip-size package; 49 (7 x 7) bumps; 3.288 x 3.288 x 0.54 mm	-
LPC54101J256UK49	WLCSP49	wafer level chip-size package; 49 (7 x 7) bumps; 3.288 x 3.288 x 0.54 mm	-
LPC54102J512BD64	LQFP64	plastic low profile quad flat package; 64 leads; body 10 × 10 × 1.4 mm	SOT314-2
LPC54102J256BD64	LQFP64	plastic low profile quad flat package; 64 leads; body 10 × 10 × 1.4 mm	SOT314-2
LPC54101J512BD64	LQFP64	plastic low profile quad flat package; 64 leads; body 10 × 10 × 1.4 mm	SOT314-2
LPC54101J256BD64	LQFP64	plastic low profile quad flat package; 64 leads; body 10 × 10 × 1.4 mm	SOT314-2

3.1 Ordering options

Table 2. Ordering options

Type number	Device order part number	Flash/kB	Total SRAM/kB	Core M4 w/ FPU	Core M0+	GPIO
LPC54102J512UK49	LPC54102J512UK49Z	512	104	1	1	39
LPC54102J256UK49	LPC54102J256UK49Z	256	104	1	1	39
LPC54101J512UK49	LPC54101J512UK49Z	512	104	1	0	39
LPC54101J256UK49	LPC54101J256UK49Z	256	104	1	0	39
LPC54102J512BD64	LPC54102J512BD64QL	512	104	1	1	50
LPC54102J256BD64	LPC54102J256BD64QL	256	104	1	1	50
LPC54101J512BD64	LPC54101J512BD64QL	512	104	1	0	50
LPC54101J256BD64	LPC54101J256BD64QL	256	104	1	0	50

[1] All of the parts include five 32-bit general-purpose timers, one State-Configurable Timer with PWM capabilities (SCTimer/PWM), one RTC/alarm timer, one 24-bit Multi-Rate Timer (MRT), a Windowed Watchdog Timer (WWDT), four USARTs, two SPIs, three Fast-mode plus I2C-bus interfaces with high-speed slave mode, and one 12-bit 5.0 Msamples/sec ADC.

4. Marking

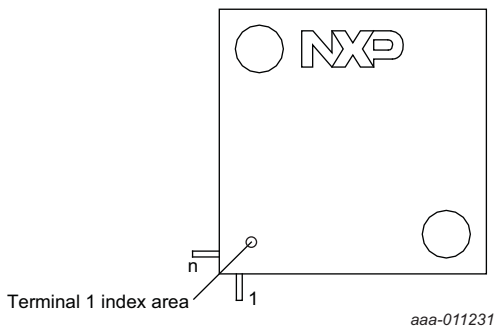


Fig 1. LQFP64 package marking

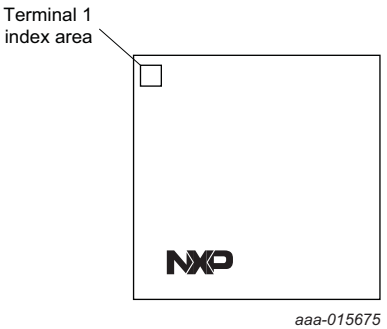


Fig 2. WLCSP49 package marking

The LPC5410x LQFP64 package has the following top-side marking:

- First line: LPC5410xJyyy
  - x: 2 = dual core (M4, M0+), 1 = single core (M4)
  - yyy: flash size
- Second line: BD64
- Third line: xxxxxxxxxxxx
- Fourth line: xxxyywwx[R]z
  - yyww: Date code with yy = year and ww = week.
  - xR = boot code version and device revision.

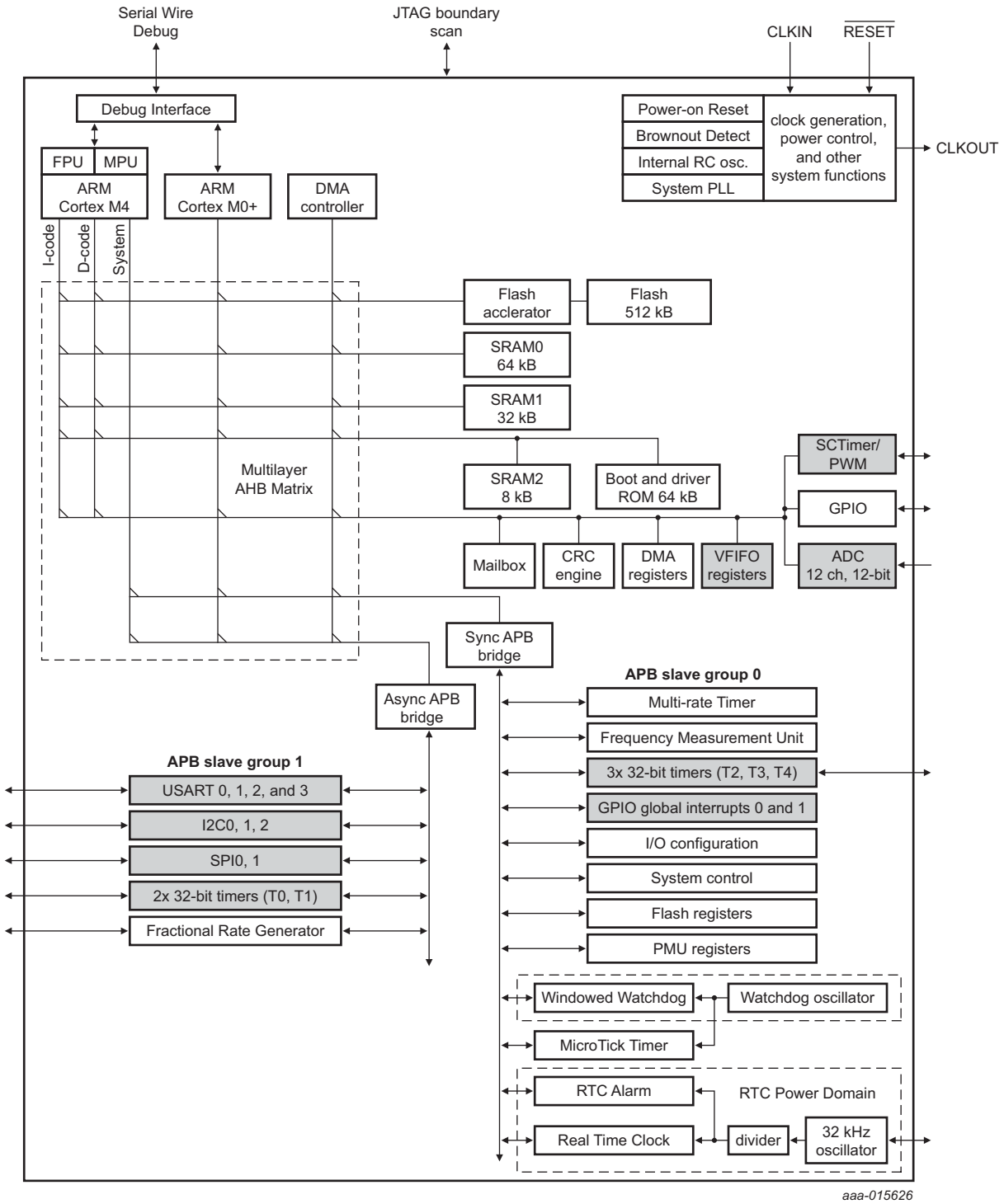
The LPC5410x WLCSP49 package has the following top-side marking:

- First line: LPC5410x
  - x: 2 = dual core (M4, M0+), 1 = single core (M4)
- Second line: JxxxUK49
  - xxx: flash size
- Third line: xxxxxxxx
- Fourth line: xxxyyww
  - yyww: Date code with yy = year and ww = week.
- Fifth line: xxxxx
- Sixth line: NXP x[R]z
  - xR = boot code version and device revision.

Table 3. Device revision table

Revision identifier (R)	Revision description
'1B'	Initial device revision with boot code version 17.1.
'1C'	Second device revision with boot code version 17.1.

5. Block diagram



Gray-shaded peripheral blocks provide dedicated request lines or triggers for DMA transfers.

Fig 3. LPC5410x Block diagram

6. Pinning information

6.1 Pinning

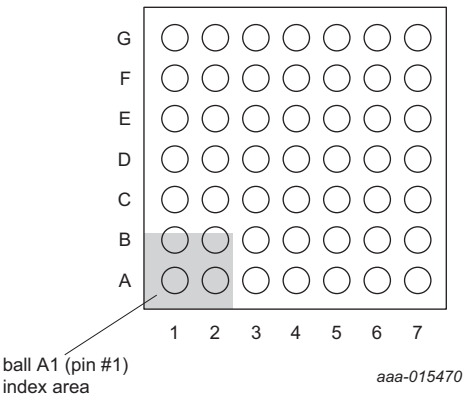


Fig 4. WLCSP49 Pin configuration (bottom view)

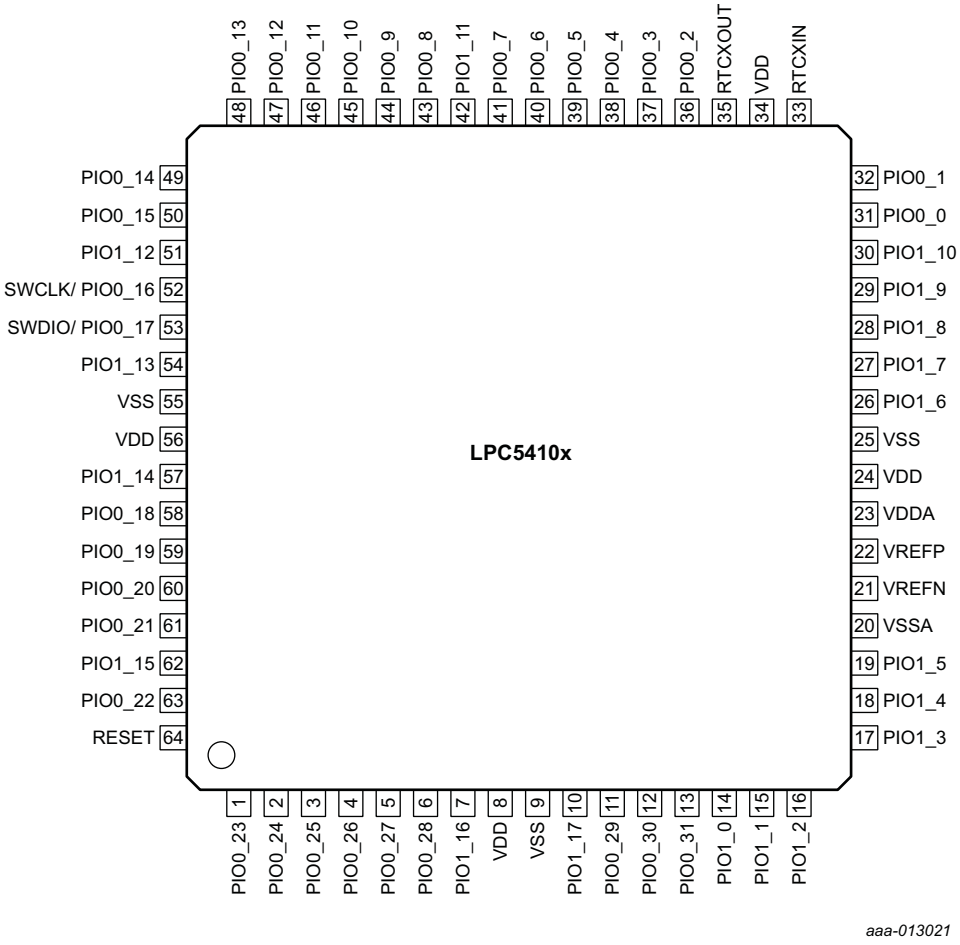


Fig 5. LQFP64 Pin configuration

6.2 Pin description

On the LPC5410x, digital pins are grouped into two ports. Each digital pin may support up to four different digital functions and one analog function, including General Purpose I/O (GPIO).

Table 4. Pin description

Symbol	WLCSP49	LQFP64		Reset state [1]	Type [6]	Description
PIO0_0	A6	31	[2]	PU	I/O	**PIO0_0 —** General-purpose digital input/output pin. **Remark:** In ISP mode, this pin is the UART0 RXD function.
					I	**U0_RXD —** Receiver input for USART0.
					I/O	**SPI0_SSEL0 —** Slave Select 0 for SPI0.
					I	**CT32B0_CAP0 —** 32-bit CT32B0 capture input 0.
					I	**R —** Reserved.
					O	**SCT0_OUT3 —** SCT0 output 3. PWM output 3.
PIO0_1	B6	32	[2]	PU	I/O	**PIO0_1 —** General-purpose digital input/output pin. **Remark:** In ISP mode, this pin is the UART0 TXD function.
					O	**U0_TXD —** Transmitter output for USART0.
					I/O	**SPI0_SSEL1 —** Slave Select 1 for SPI0.
					I	**CT32B0_CAP1 —** 32-bit CT32B0 capture input 1.
					I	**R —** Reserved.
					O	**SCT0_OUT1 —** SCT0 output 1. PWM output 1.
PIO0_2	-	36	[2]	PU	I/O	**PIO0_2 —** General-purpose digital input/output pin.
					I	**$\overline{\text{U0\_CTS}}$ —** Clear To Send input for USART0.
					I	**R —** Reserved.
					I	**CT32B2_CAP1 —** 32-bit CT32B2 capture input 1.
					I	**R —** Reserved.
PIO0_3	-	37	[2]	PU	I/O	**PIO0_3 —** General-purpose digital input/output pin.
					O	**$\overline{\text{U0\_RTS}}$ —** Request To Send output for USART0.
					I	**R —** Reserved.
					O	**CT32B1_MAT3 —** 32-bit CT32B1 match output 3.
					I	**R —** Reserved.
PIO0_4	C7	38	[2]	PU	I/O	**PIO0_4 —** General-purpose digital input/output pin.
					I/O	**U0_SCLK —** USART0 clock in synchronous USART mode.
					I/O	**SPI0_SSEL2 —** Slave Select 2 for SPI0.
					I	**CT32B0_CAP2 —** 32-bit CT32B0 capture input 2.
					I	**R —** Reserved.

Table 4. Pin description *...continued*

Symbol	WLCSP49	LQFP64		Reset state [1]	Type [6]	Description
PIO0_5	C6	39	[2]	PU	I/O	**PIO0_5 —** General-purpose digital input/output pin.
					I	**U1_RXD —** Receiver input for USART1.
					O	**SCT0_OUT6 —** SCT0 output 6. PWM output 6.
					O	**CT32B0_MAT0 —** 32-bit CT32B0 match output 0.
					I	**R —** Reserved.
PIO0_6	D7	40	[2]	PU	I/O	**PIO0_6 —** General-purpose digital input/output pin.
					O	**U1_TXD —** Transmitter output for USART1.
					I	**R —** Reserved.
					O	**CT32B0_MAT1 —** 32-bit CT32B0 match output 1.
					I	**R —** Reserved.
PIO0_7	D6	41	[2]	PU	I/O	**PIO0_7 —** General-purpose digital input/output pin.
					I/O	**U1_SCLK —** USART1 clock in synchronous USART mode.
					O	**SCT0_OUT0 —** SCT0 output 0. PWM output 0.
					O	**CT32B0_MAT2 —** 32-bit CT32B0 match output 2.
					I	**R —** Reserved.
					I	**CT32B0_CAP2 —** 32-bit CT32B0 capture input 2.
PIO0_8	D5	43	[2]	PU	I/O	**PIO0_8 —** General-purpose digital input/output pin.
					I	**U2_RXD —** Receiver input for USART2.
					O	**SCT0_OUT1 —** SCT0 output 1. PWM output 1.
					O	**CT32B0_MAT3 —** 32-bit CT32B0 match output 3.
					I	**R —** Reserved.
PIO0_9	E7	44	[2]	PU	I/O	**PIO0_9 —** General-purpose digital input/output pin.
					O	**U2_TXD —** Transmitter output for USART2.
					O	**SCT0_OUT2 —** SCT0 output 2. PWM output 2.
					I	**CT32B3_CAP0 —** 32-bit CT32B3 capture input 0.
					I	**R —** Reserved.
					I/O	**SPI0_SSEL0 —** Slave Select 0 for SPI0.
PIO0_10	E6	45	[2]	PU	I/O	**PIO0_10 —** General-purpose digital input/output pin.
					I/O	**U2_SCLK —** USART2 clock in synchronous USART mode.
					O	**SCT0_OUT3 —** SCT0 output 3. PWM output 3.
					O	**CT32B3_MAT0 —** 32-bit CT32B3 match output 0.
					I	**R —** Reserved.
PIO0_11	E5	46	[2]	PU	I/O	**PIO0_11 —** General-purpose digital input/output pin.
					I/O	**SPI0_SCK —** Serial clock for SPI0.
					I	**U1_RXD —** Receiver input for USART1.
					O	**CT32B2_MAT1 —** 32-bit CT32B2 match output 1.
					I	**R —** Reserved.

Table 4. Pin description *...continued*

Symbol	WLCSP49	LQFP64		Reset state [1]	Type [6]	Description
PIO0_12	F7	47	[2]	PU	I/O	**PIO0_12 —** General-purpose digital input/output pin.
					I/O	**SPI0_MOSI —** Master Out Slave in for SPI0.
					O	**U1_TXD —** Transmitter output for USART1.
					O	**CT32B2_MAT3 —** 32-bit CT32B2 match output 3.
					I	**R —** Reserved.
PIO0_13	G7	48	[2]	PU	I/O	**PIO0_13 —** General-purpose digital input/output pin.
					I/O	**SPI0_MISO —** Master In Slave Out for SPI0.
					O	**SCT0_OUT4 —** SCT0 output 4. PWM output 4.
					O	**CT32B2_MAT0 —** 32-bit CT32B2 match output 0.
					I	**R —** Reserved.
PIO0_14/TCK	F6	49	[2]	PU	I/O	**PIO0_14 —** General-purpose digital input/output pin. In boundary scan mode: TCK (Test Clock).
					I/O	**SPI0_SSEL0 —** Slave Select 0 for SPI0.
					O	**SCT0_OUT5 —** SCT0 output 5. PWM output 5.
					O	**CT32B2_MAT1 —** 32-bit CT32B2 match output 1.
					I	**R —** Reserved.
PIO0_15/TDO	G6	50	[2]	PU	I/O	**PIO0_15 —** General-purpose digital input/output pin. In boundary scan mode: TDO (Test Data Out).
					I/O	**SPI0_SSEL1 —** Slave Select 1 for SPI0.
					I/O	**SWO —** Serial wire trace output.
					O	**CT32B2_MAT2 —** 32-bit CT32B2 match output 2.
					I	**R —** Reserved.
SWCLK/ PIO0_16	F5	52	[2]	PU	I/O	**PIO0_16 —** General-purpose digital input/output pin. After booting, this pin is connected to the SWCLK.
					I/O	**SPI0_SSEL2 —** Slave Select 2 for SPI0.
					I	**$\overline{\text{U1\_CTS}}$ —** Clear To Send input for USART1.
					O	**CT32B3_MAT1 —** 32-bit CT32B3 match output 1.
					I	**R —** Reserved.
					I/O	**SWCLK —** Serial Wire Clock. This is the default function after booting.
SWDIO/ PIO0_17	G5	53	[2]	PU	I/O	**PIO0_17 —** General-purpose digital input/output pin. After booting, this pin is connected to SWDIO.
					I/O	**SPI0_SSEL3 —** Slave Select 3 for SPI0.
					O	**$\overline{\text{U1\_RTS}}$ —** Request To Send output for USART1.
					O	**CT32B3_MAT2 —** 32-bit CT32B3 match output 2.
					I	**R —** Reserved.
					I/O	**SWDIO —** Serial Wire Debug I/O. This is the default function after booting.

Table 4. Pin description *…continued*

Symbol	WLCSP49	LQFP64		Reset state [1]	Type [6]	Description
PIO0_18/TRST	G4	58	[2]	PU	I/O	**PIO0_18 —** General-purpose digital input/output pin. In boundary scan mode: TRST (Test Reset).
					O	**U3_TXD —** Transmitter output for USART3.
					O	**SCT0_OUT0 —** SCT0 output 0. PWM output 0.
					O	**CT32B0_MAT0 —** 32-bit CT32B0 match output 0.
					I	**R —** Reserved.
PIO0_19/TDI	G3	59	[2]	PU	I/O	**PIO0_19 —** General-purpose digital input/output pin. In boundary scan mode: TDI (Test Data In).
					I/O	**U3_SCLK —** USART3 clock in synchronous USART mode.
					O	**SCT0_OUT1 —** SCT0 output 1. PWM output 1.
					O	**CT32B0_MAT1 —** 32-bit CT32B0 match output 1.
					I	**R —** Reserved.
PIO0_20/TMS	F3	60	[2]	PU	I/O	**PIO0_20 —** General-purpose digital input/output pin. In boundary scan mode: TMS (Test Mode Select).
					I	**U3_RXD —** Receiver input for USART3.
					I/O	**U0_SCLK —** USART0 clock in synchronous USART mode.
					I	**CT32B3_CAP0 —** 32-bit CT32B3 capture input 0.
					I	**R —** Reserved.
PIO0_21	E3	61	[2]	PU	I/O	**PIO0_21 —** General-purpose digital input/output pin.
					O	**CLKOUT —** Clock output pin.
					O	**U0_TXD —** Transmitter output for USART0.
					O	**CT32B3_MAT0 —** 32-bit CT32B3 match output 0.
					I	**R —** Reserved.
PIO0_22	G2	63	[2]	PU	I/O	**PIO0_22 —** General-purpose digital input/output pin.
					I	**CLKIN —** Clock input.
					I	**U0_RXD —** Receiver input for USART0.
					O	**CT32B3_MAT3 —** 32-bit CT32B3 match output 3.
					I	**R —** Reserved.
PIO0_23	F2	1	[3]	Z	I/O	**PIO0_23 —** General-purpose digital input/output pin.
					I/O	**I2C0_SCL —** I^2C0 clock input/output.
					I	**R —** Reserved.
					I	**CT32B0_CAP0 —** 32-bit CT32B0 capture input 0.
					I	**R —** Reserved.

Table 4. Pin description *...continued*

Symbol	WLCSP49	LQFP64		Reset state [1]	Type [6]	Description
PIO0_24	F1	2	[3]	Z	I/O	**PIO0_24 —** General-purpose digital input/output pin.
					I/O	**I2C0_SDA —** I²C0 data input/output.
					I	**R —** Reserved.
					I	**CT32B0_CAP1 —** 32-bit CT32B0 capture input 1.
					I	**R —** Reserved.
					O	**CT32B0_MAT0 —** 32-bit CT32B0 match output 0.
PIO0_25	E2	3	[3]	Z	I/O	**PIO0_25 —** General-purpose digital input/output pin.
					I/O	**I2C1_SCL —** I²C1 clock input/output.
					I	**$\overline{\text{U1\_CTS}}$ —** Clear To Send input for USART1.
					I	**CT32B0_CAP2 —** 32-bit CT32B0 capture input 2.
					I	**R —** Reserved.
					I	**CT32B1_CAP1 —** 32-bit CT32B1 capture input 1.
PIO0_26	E1	4	[3]	Z	I/O	**PIO0_26 —** General-purpose digital input/output pin.
					I/O	**I2C1_SDA —** I²C1 data input/output.
					I	**R —** Reserved.
					I	**CT32B0_CAP3 —** 32-bit CT32B0 capture input 3.
					I	**R —** Reserved.
PIO0_27	D2	5	[3]	Z	I/O	**PIO0_27 —** General-purpose digital input/output pin.
					I/O	**I2C2_SCL —** I²C2 clock input/output.
					I	**R —** Reserved.
					I	**CT32B2_CAP0 —** 32-bit CT32B2 capture input 0.
					I	**R —** Reserved.
PIO0_28	D1	6	[3]	Z	I/O	**PIO0_28 —** General-purpose digital input/output pin.
					I/O	**I2C2_SDA —** I²C2 data input/output.
					I	**R —** Reserved.
					O	**CT32B2_MAT0 —** 32-bit CT32B2 match output 0.
					I	**R —** Reserved.
PIO0_29/ ADC0_0	D3	11	[4]	PU	I/O; AI	**PIO0_29/ADC0_0 —** General-purpose digital input/output pin (default). ADC input channel 0 if the DIGIMODE bit is set to 0 in the IOCON register for this pin.
					-	**R —** Reserved.
					O	**SCT0_OUT2 —** SCT0 output 2.
					O	**CT32B0_MAT3 —** 32-bit CT32B0 match output 3.
					I	**R —** Reserved.
					I	**CT32B0_CAP1 —** 32-bit CT32B0 capture input 1.
					O	**CT32B0_MAT1 —** 32-bit CT32B0 match output 1.

Table 4. Pin description *...continued*

Symbol	WLCSP49	LQFP64		Reset state [1]	Type [6]	Description
PIO0_30/ ADC0_1	C1	12	[4]	PU	I/O; AI	**PIO0_30/ADC0_1 —** General-purpose digital input/output pin (default). ADC input channel 1 if the DIGIMODE bit is set to 0 in the IOCON register for this pin.
					-	**R —** Reserved.
					O	**SCT0_OUT3 —** SCT0 output 3.
					O	**CT32B0_MAT2 —** 32-bit CT32B0 match output 2.
					I	**R —** Reserved.
					I	**CT32B0_CAP2 —** 32-bit CT32B0 capture input 2.
PIO0_31/ ADC0_2	C2	13	[4]	PU	I/O; AI	**PIO0_31/ADC0_2 —** General-purpose digital input/output pin (default). ADC input channel 2 if the DIGIMODE bit is set to 0 in the IOCON register for this pin. **Remark:** This pin is also used to force In-System Programming mode (ISP) after device reset. See the LPC5410x User Manual (Boot Process chapter) for details.
					-	**R —** Reserved.
					I	**$\overline{\text{U2\_CTS}}$ —** Clear To Send input for USART2.
					I	**CT32B2_CAP2 —** 32-bit CT32B2 capture input 2.
					I	**R —** Reserved.
					I	**CT32B0_CAP3 —** 32-bit CT32B0 capture input 3.
					O	**CT32B0_MAT3 —** 32-bit CT32B0 match output 3.
PIO1_0/ ADC0_3	C3	14	[4]	PU	I/O; AI	**PIO1_0/ADC0_3 —** General-purpose digital input/output pin (default). ADC input channel 3 if the DIGIMODE bit is set to 0 in the IOCON register for this pin.
					-	**R —** Reserved.
					O	**$\overline{\text{U2\_RTS}}$ —** Request To Send output for USART2.
					O	**CT32B3_MAT1 —** 32-bit CT32B3 match output 1.
					I	**R —** Reserved.
					I	**CT32B0_CAP0 —** 32-bit CT32B0 capture input 0.
PIO1_1/ ADC0_4	B1	15	[4]	PU	I/O; AI	**PIO1_1/ADC0_4 —** General-purpose digital input/output pin (default). ADC input channel 4 if the DIGIMODE bit is set to 0 in the IOCON register for this pin.
					-	**R —** Reserved.
					I/O	**SWO —** Serial wire trace output.
					O	**SCT0_OUT4 —** SCT0 output 4.
PIO1_2/ ADC0_5	A1	16	[4]	PU	I/O; AI	**PIO1_2/ADC0_5 —** General-purpose digital input/output pin (default). ADC input channel 5 if the DIGIMODE bit is set to 0 in the IOCON register for this pin.
					-	**R —** Reserved.
					I/O	**SPI1_SSEL3 —** Slave Select 3 for SPI1.
					O	**SCT0_OUT5 —** SCT0 output 5.

Table 4. Pin description *...continued*

Symbol	WLCSP49	LQFP64		Reset state [1]	Type [6]	Description
PIO1_3/ ADC0_6	B2	17	[4]	PU	I/O; AI	**PIO1_3/ADC0_6 —** General-purpose digital input/output pin (default). ADC input channel 6 if the DIGIMODE bit is set to 0 in the IOCON register for this pin.
					-	**R —** Reserved.
					I/O	**SPI1_SSEL2 —** Slave Select 2 for SPI1.
					O	**SCT0_OUT6 —** SCT0 output 6.
					I	**R —** Reserved.
					I/O	**SPI0_SCK —** Serial clock for SPI0.
					I	**CT32B0_CAP1 —** 32-bit CT32B0 capture input 1.
PIO1_4/ ADC0_7	A2	18	[4]	PU	I/O; AI	**PIO1_4/ADC0_7 —** General-purpose digital input/output pin (default). ADC input channel 7 if the DIGIMODE bit is set to 0 in the IOCON register for this pin.
					-	**R —** Reserved.
					I/O	**SPI1_SSEL1 —** Slave Select 1 for SPI1.
					O	**SCT0_OUT7 —** SCT0 output 7.
					I	**R —** Reserved.
					I/O	**SPI0_MISO —** Master In Slave Out for SPI0.
					O	**CT32B0_MAT1 —** 32-bit CT32B0 match output 1.
PIO1_5/ ADC0_8	B3	19	[4]	PU	I/O; AI	**PIO1_5/ADC0_8 —** General-purpose digital input/output pin (default). ADC input channel 8 if the DIGIMODE bit is set to 0 in the IOCON register for this pin.
					-	**R —** Reserved.
					I/O	**SPI1_SSEL0 —** Slave Select 0 for SPI1.
					I	**CT32B1_CAP0 —** 32-bit CT32B1 capture input 0.
					I	**R —** Reserved.
					O	**CT32B1_MAT3 —** 32-bit CT32B1 match output 3.
					I	**R —** Reserved.
PIO1_6/ ADC0_9	A5	26	[4]	PU	I/O; AI	**PIO1_6/ADC0_9 —** General-purpose digital input/output pin (default). ADC input channel 9 if the DIGIMODE bit is set to 0 in the IOCON register for this pin.
					-	**R —** Reserved.
					I/O	**SPI1_SCK —** Serial clock for SPI1.
					I	**CT32B1_CAP2 —** 32-bit CT32B1 capture input 2.
					-	**R —** Reserved.
					O	**CT32B1_MAT2 —** 32-bit CT32B1 match output 2.
					I	**R —** Reserved.

Table 4. Pin description *...continued*

Symbol	WLCSP49	LQFP64		Reset state [1]	Type [6]	Description
PIO1_7/ ADC0_10	B5	27	[4]	PU	I/O; AI	**PIO1_7/ADC0_10 —** General-purpose digital input/output pin (default). ADC input channel 10 if the DIGIMODE bit is set to 0 in the IOCON register for this pin.
					-	**R —** Reserved.
					I/O	**SPI1_MOSI —** Master Out Slave in for SPI1.
					O	**CT32B1_MAT2 —** 32-bit CT32B1 match output 2.
					-	**R —** Reserved.
					I	**CT32B1_CAP2 —** 32-bit CT32B1 capture input 2.
					I	**R —** Reserved.
PIO1_8/ ADC0_11	C5	28	[4]	PU	I/O; AI	**PIO1_8/ADC0_11 —** General-purpose digital input/output pin (default). ADC input channel 11 if the DIGIMODE bit is set to 0 in the IOCON register for this pin.
					-	**R —** Reserved.
					I/O	**SPI1_MISO —** Master In Slave Out for SPI1.
					O	**CT32B1_MAT3 —** 32-bit CT32B1 match output 3.
					I	**R —** Reserved.
					I	**CT32B1_CAP3 —** 32-bit CT32B1 capture input 3.
					I	**R —** Reserved.
PIO1_9	-	29	[2]	PU	I/O	**PIO1_9 —** General-purpose digital input/output pin.
					I	**R —** Reserved.
					I/O	**SPI0_MOSI —** Master Out Slave In for SPI0.
					I	**CT32B0_CAP2 —** 32-bit CT32B0 capture input 2.
PIO1_10	-	30	[2]	PU	I/O	**PIO1_10 —** General-purpose digital input/output pin.
					I	**R —** Reserved.
					O	**U1_TXD —** Transmitter output for USART1.
					O	**SCT0_OUT4 —** SCT0 output 4.
PIO1_11	-	42	[2]	PU	I/O	**PIO1_11 —** General-purpose digital input/output pin.
					I	**R —** Reserved.
					O	**$\overline{\text{U1\_RTS}}$ —** Request To Send output for USART1.
					I	**CT32B1_CAP0 —** 32-bit CT32B1 capture input 0.
PIO1_12	-	51	[2]	PU	I/O	**PIO1_12 —** General-purpose digital input/output pin.
					I	**R —** Reserved.
					I	**U3_RXD —** Receiver input for USART3.
					O	**CT32B1_MAT0 —** 32-bit CT32B1 match output 0.
					I/O	**SPI1_SCK —** Serial clock for SPI1.
PIO1_13	-	54	[2]	PU	I/O	**PIO1_13 —** General-purpose digital input/output pin.
					I	**R —** Reserved.
					O	**U3_TXD —** Transmitter output for USART3.
					O	**CT32B1_MAT1 —** 32-bit CT32B1 match output 1.
					I/O	**SPI1_MOSI —** Master Out Slave In for SPI1.

Table 4. Pin description *...continued*

Symbol	WLCSP49	LQFP64		Reset state [1]	Type [6]	Description
PIO1_14	-	57	[2]	PU	I/O	**PIO1_14 —** General-purpose digital input/output pin.
					I	**R —** Reserved.
					I	**U2_RXD —** Receiver input for USART2.
					O	**SCT0_OUT7 —** SCT0 output 7.
					I/O	**SPI1_MISO —** Master In Slave Out for SPI1.
PIO1_15	-	62	[2]	PU	I/O	**PIO1_15 —** General-purpose digital input/output pin.
					I	**R —** Reserved.
					O	**SCT0_OUT5 —** SCT0 output 5.
					I	**CT32B1_CAP3 —** 32-bit CT32B1 capture input 3.
					I/O	**SPI1_SSEL0 —** Slave Select 0 for SPI1.
PIO1_16	-	7	[2]	PU	I/O	**PIO1_16 —** General-purpose digital input/output pin.
					I	**R —** Reserved.
					O	**CT32B0_MAT0 —** 32-bit CT32B0 match output 0.
					I	**CT32B0_CAP0 —** 32-bit CT32B0 capture input 0.
					I/O	**SPI1_SSEL1 —** Slave Select 1 for SPI1.
PIO1_17	-	10	[2]	PU	I/O	**PIO1_17 —** General-purpose digital input/output pin.
$\overline{\text{RESET}}$	G1	64	[5]	PU	I	External reset input: A LOW on this pin resets the device, causing I/O ports and peripherals to take on their default states, and processor execution to begin at address 0. Wakes up the part from deep power-down mode.
RTCXIN	A7	33		-	-	RTC oscillator input.
RTCXOUT	B7	35		-	-	RTC oscillator output.
VREFP	B4	22		-	-	ADC positive reference voltage.
VREFN	-	21		-	-	ADC negative reference voltage.
VDDA	A4	23		-	-	Analog supply voltage.
VDD	C4, F4	8, 24, 56, 34		-	-	Single 1.62 V to 3.6 V power supply powers internal digital functions and I/Os.
VSS	D4, E4	9, 25, 55		-	-	Ground.
VSSA	A3	20		-	-	Analog ground.

[1] PU = input mode, pull-up enabled (pull-up resistor pulls up pin to V_{DD}). Z = high impedance; pull-up or pull-down disabled. Reset state reflects the pin state at reset without boot code operation. For pin states in the different power modes, see Section 6.2.2 “Pin states in different power modes”. For termination on unused pins, see Section 6.2.1 “Termination of unused pins”.

[2] 5 V tolerant pad with programmable glitch filter (5 V tolerant if V_{DD} present; if V_{DD} not present, do not exceed 3.6 V); provides digital I/O functions with TTL levels and hysteresis; normal drive strength. See Figure 27. Pulse width of spikes or glitches suppressed by input filter is from 3 ns to 16 ns (simulated value).

[3] True open-drain pin. I2C-bus pins compliant with the I2C-bus specification for I2C standard mode, I2C Fast-mode, and I2C Fast-mode Plus. The pin requires an external pull-up to provide output functionality. When power is switched off, this pin is floating and does not disturb the I2C lines. Open-drain configuration applies to all functions on this pin.

[4] 5 V tolerant pin providing standard digital I/O functions with configurable modes, configurable hysteresis, and analog input. When configured as an analog input, the digital section of the pin is disabled, and the pin is not 5 V tolerant.

[5] Reset pad.5 V tolerant pad with glitch filter with hysteresis. Pulse width of spikes or glitches suppressed by input filter is from 3 ns to 20 ns (simulated value)

[6] I = Input; AI = Analog input; O = Output

6.2.1 Termination of unused pins

Table 5 shows how to terminate pins that are **not** used in the application. In many cases, unused pins should be connected externally or configured correctly by software to minimize the overall power consumption of the part.

Unused pins with GPIO function should be configured as outputs set to LOW with their internal pull-up disabled. To configure a GPIO pin as output and drive it LOW, select the GPIO function in the IOCON register, select output in the GPIO DIR register, and write a 0 to the GPIO PORT register for that pin. Disable the pull-up in the pin's IOCON register.

In addition, it is recommended to configure all GPIO pins that are not bonded out on smaller packages as outputs driven LOW with their internal pull-up disabled.

Table 5. Termination of unused pins

Pin	Default state[1]	Recommended termination of unused pins
$\overline{\text{RESET}}$	I; PU	The $\overline{\text{RESET}}$ pin can be left unconnected if the application does not use it.
all PIOn_m (not open-drain)	I; PU	Can be left unconnected if driven LOW and configured as GPIO output with pull-up disabled by software.
PIOn_m (I2C open-drain)	IA	Can be left unconnected if driven LOW and configured as GPIO output by software.
RTCXIN	-	Connect to ground. When grounded, the RTC oscillator is disabled.
RTCXOUT	-	Can be left unconnected.
VREFP	-	Tie to VDD.
VREFN	-	Tie to VSS.
VDDA	-	Tie to VDD.
VSSA	-	Tie to VSS.

[1] I = Input, IA = Inactive (no pull-up/pull-down enabled), PU = Pull-Up.

6.2.2 Pin states in different power modes

Table 6. Pin states in different power modes

Pin	Active	Sleep	Deep sleep/Power down	Deep power-down
PIOn_m pins (not I2C)	As configured in the IOCON[1]. Default: internal pull-up enabled.			Floating.
PIO0_23 to PIO0_28 (open-drain I2C-bus pins)	As configured in the IOCON[1].			Floating.
$\overline{\text{RESET}}$	Reset function enabled. Default: input, internal pull-up enabled. Reset function disabled.			

[1] Default and programmed pin states are retained in sleep, deep sleep, and power down modes.

7. Functional description

7.1 Architectural overview

The ARM Cortex-M4 includes three AHB-Lite buses, one system bus and the I-code and D-code buses. One bus is dedicated for instruction fetch (I-code), and one bus is dedicated for data access (D-code). The use of two core buses allows for simultaneous operations if concurrent operations target different devices.

A multi-layer AHB matrix connects the CPU buses and other bus masters to peripherals in a flexible manner that optimizes performance by allowing peripherals on different slaves ports of the matrix to be accessed simultaneously by different bus masters. Connections in the multilayer matrix are shown in Figure 3.

APB peripherals are connected to the AHB matrix via two APB buses using separate slave ports from the multilayer AHB matrix. This allows for better performance by reducing collisions between the CPU and the DMA controller, and also for peripherals on the asynchronous bridge to have a fixed clock that does not track the system clock.

7.2 ARM Cortex-M4 processor

The ARM Cortex-M4 is a general purpose, 32-bit microprocessor, which offers high performance and very low power consumption. The ARM Cortex-M4 offers many new features, including a Thumb-2 instruction set, low interrupt latency, hardware multiply and divide, interruptable/continuable multiple load and store instructions, automatic state save and restore for interrupts, tightly integrated interrupt controller with wake-up interrupt controller, and multiple core buses capable of simultaneous accesses.

A 3-stage pipeline is employed so that all parts of the processing and memory systems can operate continuously. Typically, while one instruction is being executed, its successor is being decoded, and a third instruction is being fetched from memory.

7.3 ARM Cortex-M4 integrated Floating Point Unit (FPU)

The FPU fully supports single-precision add, subtract, multiply, divide, multiply and accumulate, and square root operations. It also provides conversions between fixed-point and floating-point data formats, and floating-point constant instructions.

The FPU provides floating-point computation functionality that is compliant with the ANSI/IEEE Std 754-2008, IEEE Standard for Binary Floating-Point Arithmetic, referred to as the IEEE 754 standard.

7.4 Memory Protection Unit (MPU)

The Cortex-M4 includes a Memory Protection Unit (MPU) which can be used to improve the reliability of an embedded system by protecting critical data within the user application.

The MPU allows separating processing tasks by disallowing access to each other's data, disabling access to memory regions, allowing memory regions to be defined as read-only and detecting unexpected memory accesses that could potentially break the system.

The MPU separates the memory into distinct regions and implements protection by preventing disallowed accesses. The MPU supports up to eight regions each of which can be divided into eight subregions. Accesses to memory locations that are not defined in the MPU regions, or not permitted by the region setting, will cause the Memory Management Fault exception to take place.

7.5 Nested Vectored Interrupt Controller (NVIC) for Cortex-M4

The NVIC is an integral part of the Cortex-M4. The tight coupling to the CPU allows for low interrupt latency and efficient processing of late arriving interrupts.

7.5.1 Features

- Controls system exceptions and peripheral interrupts.
- 37 vectored interrupts.
- Eight programmable interrupt priority levels, with hardware priority level masking.
- Relocatable vector table.
- Non-Maskable Interrupt (NMI).
- Software interrupt generation.

7.5.2 Interrupt sources

Each peripheral device has one interrupt line connected to the NVIC but may have several interrupt flags.

7.6 ARM Cortex-M0+ co-processor

The ARM Cortex-M0+ co-processor offers high performance and very low power consumption. This processor uses a 2-stage pipeline von Neumann architecture and a small but powerful instruction set providing high-end processing hardware. The processor includes an NVIC with 32 interrupts and a separate system tick timer. In LPC5410x, the Cortex-M0 coprocessor hardware multiply is implemented as a 32-cycle iterative multiplier.

7.7 Nested Vectored Interrupt Controller (NVIC) for Cortex-M0+

The NVIC is an integral part of the Cortex-M0+. The tight coupling to the CPU allows for low interrupt latency and efficient processing of late arriving interrupts.

7.7.1 Features

- Controls system exceptions and peripheral interrupts.
- 32 vectored interrupts.
- Four programmable interrupt priority levels, with hardware priority level masking.
- Relocatable vector table.
- Non-Maskable Interrupt (NMI).
- Software interrupt generation.

7.7.2 Interrupt sources

Each peripheral device has one interrupt line connected to the NVIC but may have several interrupt flags.

7.8 System Tick timer (SysTick)

The ARM Cortex-M4 and ARM Cortex-M0+ cores include a system tick timer (SysTick) that is intended to generate a dedicated SYSTICK exception. The clock source for the SysTick can be the system clock or the SYSTICK clock.

7.9 On-chip static RAM

The LPC5410x support 104 kB SRAM with separate bus master access for higher throughput and individual power control for low-power operation.

7.10 On-chip flash

The LPC5410x supports 512 kB of on-chip flash memory.

7.11 On-chip ROM

The 64 kB on-chip ROM contains the boot loader and the following Application Programming Interfaces (API):

- In-System Programming (ISP) and In-Application Programming (IAP) support for flash programming.
- Power control API for configuring power consumption and PLL settings.

7.12 Memory mapping

The LPC5410x incorporates several distinct memory regions. The APB peripheral area is 512 kB in size and is divided to allow for up to 32 peripherals.Each peripheral is allocated 16 kB of space simplifying the address decoding. The registers incorporated into the CPU, such as NVIC, SysTick, and sleep mode control, are located on the private peripheral bus.

Figure 6 shows the overall map of the entire address space from the user program viewpoint following reset.

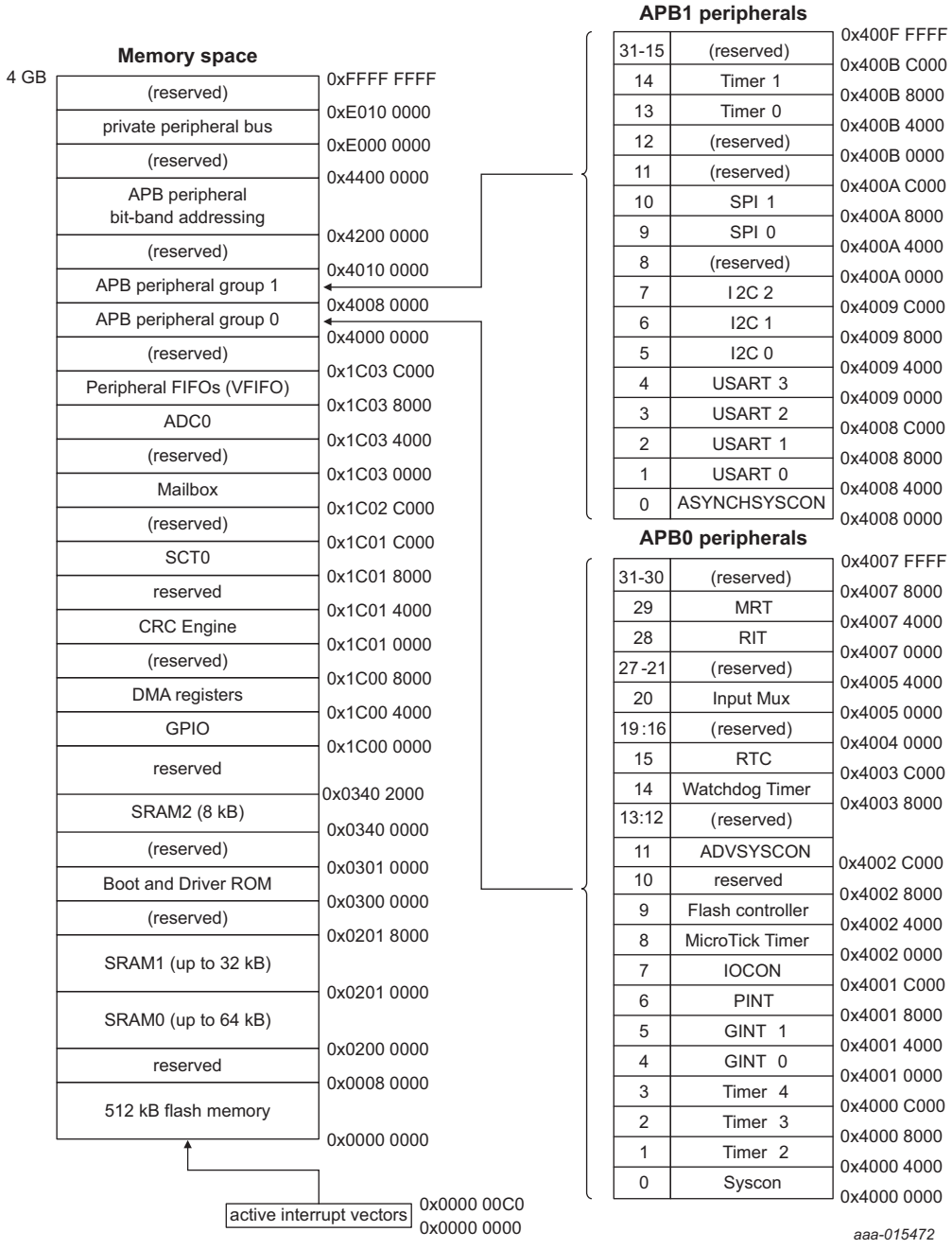


Fig 6. LPC5410x Memory mapping

7.13 General Purpose I/O (GPIO)

The LPC5410x provides two GPIO ports with a total of 50 GPIO pins.

Device pins that are not connected to a specific peripheral function are controlled by the GPIO registers. Pins may be dynamically configured as inputs or outputs. Separate registers allow setting or clearing any number of outputs simultaneously. The current level of a port pin can be read back no matter what peripheral is selected for that pin.

See Table 4 for the default state on reset.

7.13.1 Features

- Accelerated GPIO functions:
  - GPIO registers are located on the AHB so that the fastest possible I/O timing can be achieved.
  - Mask registers allow treating sets of port bits as a group, leaving other bits unchanged.
  - All GPIO registers are byte and half-word addressable.
  - Entire port value can be written in one instruction.
- Bit-level set, clear and toggle registers allow a single instruction set, clear or toggle of any number of bits in one port.
- Direction control of individual bits.
- All I/O default to inputs after reset.
- All GPIO pins can be selected to create an edge or level-sensitive GPIO interrupt request.
- One GPIO group interrupt can be triggered by a combination of any pin or pins.

7.14 Pin interrupt/pattern engine

The pin interrupt block configures up to eight pins from all digital pins for providing eight external interrupts connected to the NVIC. The pattern match engine can be used in conjunction with software to create complex state machines based on pin inputs. Any digital pin, independent of the function selected through the switch matrix can be configured through the SYSCON block as an input to the pin interrupt or pattern match engine. The registers that control the pin interrupt or pattern match engine are located on the I/O+ bus for fast single-cycle access.

7.14.1 Features

- Pin interrupts:
  - Up to eight pins can be selected from all GPIO pins on ports 0 and 1 as edge-sensitive or level-sensitive interrupt requests. Each request creates a separate interrupt in the NVIC.
  - Edge-sensitive interrupt pins can interrupt on rising or falling edges or both.
  - Level-sensitive interrupt pins can be HIGH-active or LOW-active.
  - Level-sensitive interrupt pins can be HIGH-active or LOW-active.
  - Pin interrupts can wake up the device from sleep mode, deep sleep mode, and power down mode.

- Pattern match engine:
  - Up to eight pins can be selected from all digital pins on ports 0 and 1 to contribute to a boolean expression. The boolean expression consists of specified levels and/or transitions on various combinations of these pins.
  - Each bit slice minterm (product term) comprising of the specified boolean expression can generate its own, dedicated interrupt request.
  - Any occurrence of a pattern match can also be programmed to generate an RXEV notification to the CPU. The RXEV signal can be connected to a pin.
  - Pattern match can be used in conjunction with software to create complex state machines based on pin inputs.
  - Pattern match engine facilities wake-up only from active and sleep modes.

7.15 AHB peripherals

7.15.1 DMA controller

The DMA controller allows peripheral-to memory, memory-to-peripheral, and memory-to-memory transactions. Each DMA stream provides unidirectional DMA transfers for a single source and destination.

7.15.1.1 Features

- 22 channels, 21 of which are connected to peripheral DMA requests. These come from the USART, SPI, and I^2C peripherals. One spare channels has no DMA request connected, and can be used for functions such as memory-to-memory moves.
- DMA operations can be triggered by on- or off-chip events. Each DMA channel can select one trigger input from 20 sources. Trigger sources include ADC interrupts, Timer interrupts, pin interrupts, and the SCT DMA request lines.
- Priority is user selectable for each channel.
- Continuous priority arbitration.
- Address cache.
- Efficient use of data bus.
- Supports single transfers up to 1,024 words.
- Address increment options allow packing and/or unpacking data.

7.16 Digital serial peripherals

7.16.1 USART

7.16.1.1 Features

- Synchronous mode with master or slave operation. Includes data phase selection and continuous clock option.
- Maximum bit rates of 6.25 Mbit/s in asynchronous mode.
- Maximum supported bit rate of 24 Mbit/s for USART master and slave synchronous modes.
- 7, 8, or 9 data bits and 1 or 2 stop bits.