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LPC5411x

32-bit ARM Cortex-M4/M0+ MCU; 192 KB SRAM; 256 KB flash, Crystal-less USB operation, DMIC subsystem, Flexcomm Interface, 32-bit counter/ timers, SCTimer/PWM, 12-bit 5.0 Msamples/sec ADC, Temperature sensor

Rev. 2.1 — 9 May 2018 Product data sheet

1. General description

The LPC5411x are ARM Cortex-M4 based microcontrollers for embedded applications. These devices include an ARM Cortex-M0+ coprocessor, up to 192 KB of on-chip SRAM, up to 256 KB on-chip flash, full-speed USB device interface with Crystal-less operation, a DMIC subsystem with PDM microphone interface and I2S, five general-purpose timers, one SCTimer/PWM, one RTC/alarm timer, one 24-bit Multi-Rate Timer (MRT), a Windowed Watchdog Timer (WWDT), eight flexible serial communication peripherals (each of which can be a USART, SPI, or I^2C interface), and one 12-bit 5.0 Msamples/sec ADC, and a temperature sensor.

The ARM Cortex-M4 is a 32-bit core that offers system enhancements such as low power consumption, enhanced debug features, and a high level of support block integration. The ARM Cortex-M4 CPU incorporates a 3-stage pipeline, uses a Harvard architecture with separate local instruction and data buses as well as a third bus for peripherals, and includes an internal prefetch unit that supports speculative branching. The ARM Cortex-M4 supports single-cycle digital signal processing and SIMD instructions. A hardware floating-point unit is integrated in the core.

The ARM Cortex-M0+ coprocessor is an energy-efficient and easy-to-use 32-bit core which is code and tool-compatible with the Cortex-M4 core. The Cortex-M0+ coprocessor offers up to 100 MHz performance with a simple instruction set and reduced code size.

2. Features and benefits

- Dual processor cores: ARM Cortex-M4 and ARM Cortex-M0+. Both cores operate up to a maximum frequency of 100 MHz.
- ARM Cortex-M4 core (version r0p1):
  - ARM Cortex-M4 processor, running at a frequency of up to 100 MHz.
  - Floating Point Unit (FPU) and Memory Protection Unit (MPU).
  - ARM Cortex-M4 built-in Nested Vectored Interrupt Controller (NVIC).
  - Non-maskable Interrupt (NMI) input with a selection of sources.
  - Serial Wire Debug (SWD) with six instruction breakpoints, two literal comparators, and four watch points. Includes Serial Wire Output for enhanced debug capabilities.
  - System tick timer.

- ARM Cortex-M0+ core
  - ARM Cortex-M0+ processor, running at a frequency of up to 100 MHz (uses the same clock as Cortex-M4) with a single-cycle multiplier and a fast single-cycle I/O port.
  - ARM Cortex-M0+ built-in Nested Vectored Interrupt Controller (NVIC).
  - Non-maskable Interrupt (NMI) input with a selection of sources.
  - Serial Wire Debug with four breakpoints and two watch points.
  - System tick timer.
- On-chip memory:
  - Up to 256 KB on-chip flash program memory with flash accelerator and 256 byte page erase and write.
  - Up to 192 KB total SRAM consisting of 160 KB contiguous main SRAM and an additional 32 KB SRAM on the I&D buses.
- ROM API support:
  - Flash In-Application Programming (IAP) and In-System Programming (ISP).
  - ROM-based USB drivers (HID, CDC, MSC, and DFU). Flash updates via USB is supported.
  - Supports booting from valid user code in flash, USART, SPI, and I^2C.
  - Legacy, Single, and Dual image boot.
- Serial interfaces:
  - Flexcomm Interface contains eight serial peripherals. Each can be selected by software to be a USART, SPI, or I^2C interface. Two Flexcomm Interfaces also include an I^2S interface. Each Flexcomm Interface includes a FIFO that supports USART, SPI, and I^2S if supported by that Flexcomm Interface. A variety of clocking options are available to each Flexcomm Interface and include a shared fractional baud-rate generator.
  - I^2C-bus interfaces support Fast-mode and Fast-mode Plus with data rates of up to 1Mbit/s and with multiple address recognition and monitor mode. Two sets of true I^2C pads also support high speed mode (3.4 Mbit/s) as a slave.
  - USB 2.0 full-speed device controller with on-chip PHY and dedicated DMA controller supporting crystal-less operation in device mode using software library. See Technical note TN00031 for more details.
- Digital peripherals:
  - DMA controller with 20 channels and 20 programmable triggers, able to access all memories and DMA-capable peripherals.
  - Up to 48 General-Purpose Input/Output (GPIO) pins. Most GPIOs have configurable pull-up/pull-down resistors, programmable open-drain mode, and input inverter.
  - GPIO registers are located on the AHB for fast access.
  - Up to eight GPIOs can be selected as pin interrupts (PINT), triggered by rising, falling or both input edges.
  - Two GPIO grouped interrupts (GINT) enable an interrupt based on a logical (AND/OR) combination of input states.
  - CRC engine.

- Analog peripherals:
  - 12-bit ADC with 12 input channels and with multiple internal and external trigger inputs and sample rates of up to 5.0 MSamples/sec. The ADC supports two independent conversion sequences.
  - Integrated temperature sensor connected to the ADC.
- DMIC subsystem including a dual-channel PDM microphone interface, flexible decimators, 16 entry FIFOs, optional DC locking, hardware voice activity detection, and the option to stream the processed output data to I^2S.
- Timers:
  - Five 32-bit standard general purpose timers/counters, four of which support up to four capture inputs and four compare outputs, PWM mode, and external count input. Specific timer events can be selected to generate DMA requests. The fifth timer does not have external pin connections and may be used for internal timing operations.
  - One SCTimer/PWM with eight input and eight output functions (including capture and match). Inputs and outputs can be routed to or from external pins and internally to or from selected peripherals. Internally, the SCTimer/PWM supports ten captures/matches, ten events, and ten states.
  - 32-bit Real-time clock (RTC) with 1 s resolution running in the always-on power domain. A timer in the RTC can be used for wake-up from all low power modes including deep power-down, with 1 ms resolution.
  - Multiple-channel multi-rate 24-bit timer (MRT) for repetitive interrupt generation at up to four programmable, fixed rates.
  - Windowed Watchdog Timer (WWDT).
- Clock generation:
  - 12 MHz internal Free Running Oscillator (FRO). This oscillator provides a selectable 48 MHz or 96 MHz output, and a 12 MHz output (divided down from the selected higher frequency) that can be used as a system clock. The FRO is trimmed to ±1 % accuracy over the entire voltage and temperature range.
  - External clock input for clock frequencies of up to 25 MHz.
  - Watchdog oscillator (WDTOSC) with a frequency range of 6 kHz to 1.5 MHz.
  - 32.768 kHz low-power RTC oscillator.
  - System PLL allows CPU operation up to the maximum CPU rate without the need for a high-frequency external clock. May be run from the internal FRO 12 MHz output, the external clock input CLKIN, or the RTC oscillator.
  - Clock output function with divider.
  - Frequency measurement unit for measuring the frequency of any on-chip or off-chip clock signal.
- Power control:
  - Programmable PMU (Power Management Unit) to minimize power consumption and to match requirements at different performance levels.
  - Reduced power modes: sleep, deep-sleep, and deep power-down.
  - Wake-up from deep-sleep modes due to activity on the USART, SPI, and I2C peripherals when operating as slaves.

- The Micro-Tick Timer running from the watchdog oscillator can be used to wake-up the device from any reduced power modes.
- Power-On Reset (POR).
- Brown-Out Detect (BOD) with separate thresholds for interrupt and forced reset.

- Single power supply 1.62 V to 3.6 V.
- JTAG boundary scan supported.
- 128 bit unique device serial number for identification.
- Operating temperature range −40 °C to +105 °C.
- Available as WLCSP49 and LQFP64 packages.

3. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
LPC54113J256UK49	WLCSP49	wafer level chip-size package; 49 (7 x 7) bumps; 3.436 x 3.436 x 0.525 mm	-
LPC54114J256UK49	WLCSP49	wafer level chip-size package; 49 (7 x 7) bumps; 3.436 x 3.436 x 0.525 mm	-
LPC54113J128BD64	LQFP64	plastic low profile quad flat package; 64 leads; body 10 × 10 × 1.4 mm	SOT314-2
LPC54113J256BD64	LQFP64	plastic low profile quad flat package; 64 leads; body 10 × 10 × 1.4 mm	SOT314-2
LPC54114J256BD64	LQFP64	plastic low profile quad flat package; 64 leads; body 10 × 10 × 1.4 mm	SOT314-2

3.1 Ordering options

Table 2. Ordering options

Type number	Flash in KB	SRAM in KB					Cortex-M4 with FPU	Cortex-M0+	USB FS	GPIO
		SRAMX	SRAM0	SRAM1	SRAM2	Total				
LPC54113J256UK49	256	32	64	64	32	192	1	0	1	37
LPC54114J256UK49	256	32	64	64	32	192	1	1	1	37
LPC54113J128BD64	128	32	64	-	-	96	1	0	1	48
LPC54113J256BD64	256	32	64	64	32	192	1	0	1	48
LPC54114J256BD64	256	32	64	64	32	192	1	1	1	48

4. Marking

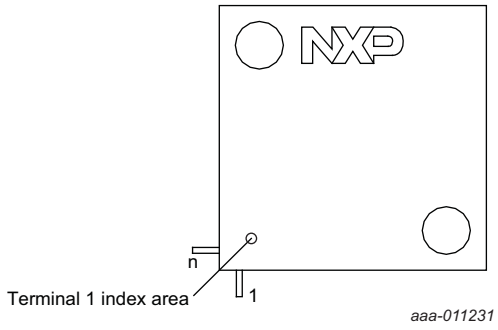


Fig 1. LQFP64 package marking

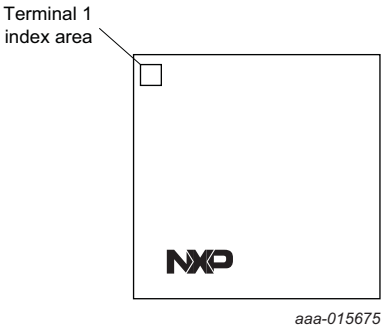


Fig 2. WLCSP49 package marking

The LPC5411x LQFP64 package has the following top-side marking:

- First line: LPC5411xJyyy
  - x: 4 = dual core (M4, M0+)
  - x: 3 = single core (M4)
  - yyy: flash size
- Second line: BD64
- Third line: xxxxxxxxxxxx
- Fourth line: xxxyywwx[R]x
  - yyww: Date code with yy = year and ww = week.
  - xR = Boot code version and device revision.

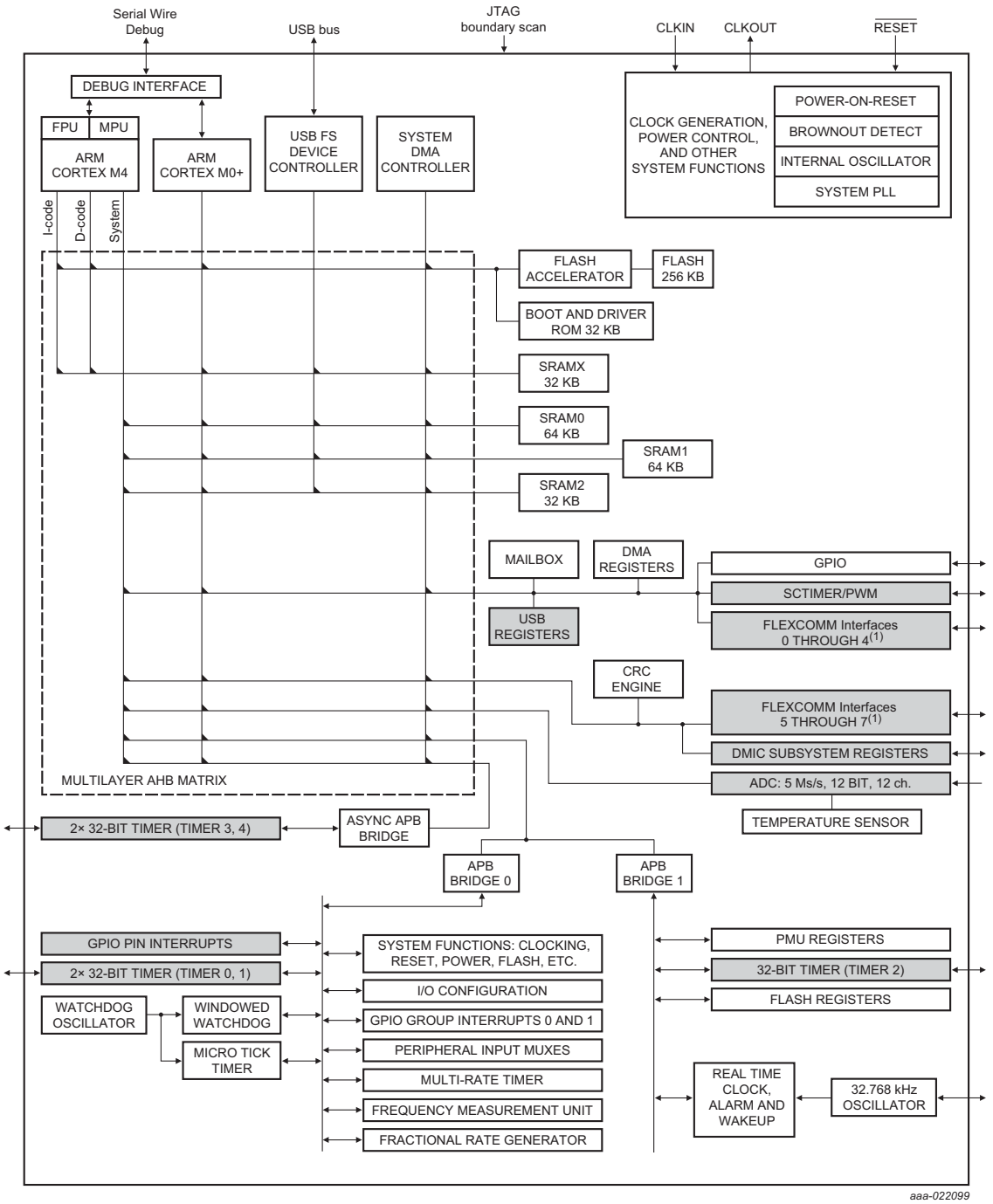
The LPC5411x WLCSP49 package has the following top-side marking:

- First line: LPC5411x
  - x: 4 = dual core (M4, M0+)
  - x: 3 = single core (M4)
- Second line: JxxxUK49
  - xxx: flash size
- Third line: xxxxxxxx
- Fourth line: xxxyyww
  - yyww: Date code with yy = year and ww = week.
- Fifth line: xxxxx
- Sixth line: NXP x[R]x
  - xR = Boot code version and device revision.

Table 3. Device revision table

	Revision description
'0A'	Initial device revision with boot code version 18.0.

5. Block diagram



Each Flexcomm Interface includes USART, SPI, and I^2C functions. Flexcomm Interfaces 6 and 7 each also provide an I2S function. Grey-shaded blocks indicate peripherals that provide DMA requests or are otherwise able to trigger DMA transfers

Fig 3. LPC5411x Block diagram

6. Pinning information

6.1 Pinning

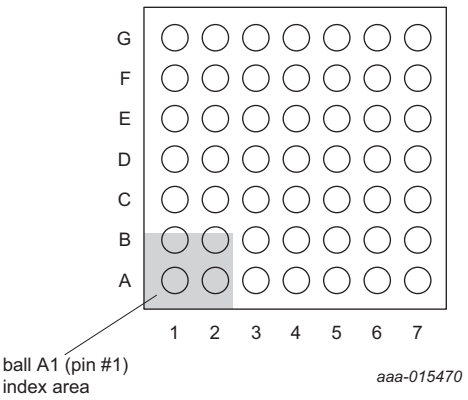


Fig 4. WLCSP49 Pin configuration

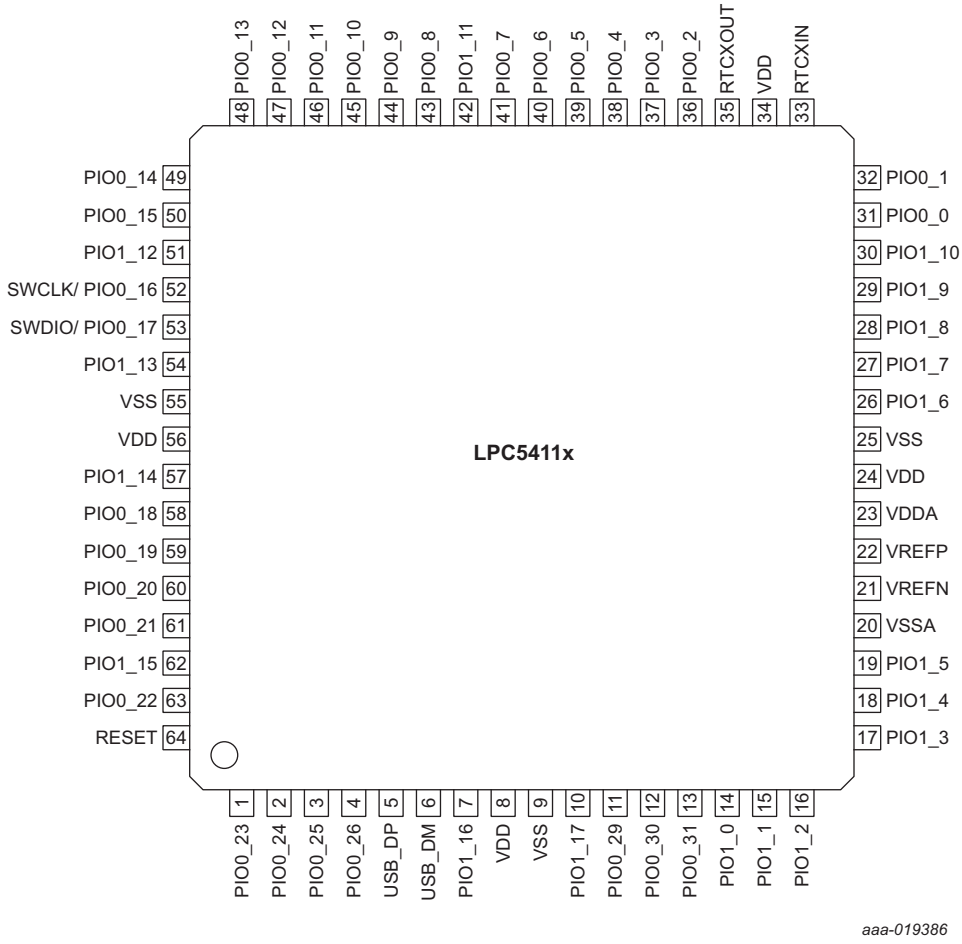


Fig 5. LQFP64 Pin configuration

6.2 Pin description

On the LPC5411x, digital pins are grouped into two ports. Each digital pin may support up to four different digital functions and one analog function, including General Purpose I/O (GPIO).

Table 4. Pin description

Symbol	49-pin	64-pin		Reset state [1]	Type	Description
PIO0_0	A6	31	[2]	PU	I/O	**PIO0_0 —** General-purpose digital input/output pin. **Remark:** In ISP mode, this pin is set to the Flexcomm Interface 0 USART RXD function.
					I/O	**FC0_RXD_SDA_MOSI —** Flexcomm Interface 0: USART RXD, I2C SDA, SPI MOSI.
					I/O	**FC3_CTS_SDA_SSEL0 —** Flexcomm Interface 3: USART CTS, I2C SDA, SPI SSEL0.
					I	**CTimer0_CAP0 —** 32-bit CTimer0 capture input 0.
						R — Reserved.
					O	**SCT0_OUT3 —** SCT0 output 3. PWM output 3.
PIO0_1	B6	32	[2]	PU	I/O	**PIO0_1 —** General-purpose digital input/output pin. **Remark:** In ISP mode, this pin is set to the Flexcomm Interface 0 USART TXD function.
					I/O	**FC0_TXD_SCL_MISO —** Flexcomm Interface 0: USART TXD, I2C SCL, SPI MISO.
					I/O	**FC3_RTS_SCL_SSEL1 —** Flexcomm Interface 3: USART RTS, I2C SCL, SPI SSEL1.
					I	**CTimer0_CAP1 —** 32-bit CTimer0 capture input 1.
						R — Reserved.
					O	**SCT0_OUT1 —** SCT0 output 1. PWM output 1.
PIO0_2	-	36	[2]	PU	I/O	**PIO0_2 —** General-purpose digital input/output pin.
					I/O	**FC0_CTS_SDA_SSEL0 —** Flexcomm Interface 0: USART CTS, I2C SDA, SPI SSEL0.
					I/O	**FC3_SSEL3 —** Flexcomm Interface 3: SPI SSEL3.
					I	**CTimer2_CAP1 —** 32-bit CTimer2 capture input 1.
PIO0_3	-	37	[2]	PU	I/O	**PIO0_3 —** General-purpose digital input/output pin.
					I/O	**FC0_RTS_SCL_SSEL1 —** Flexcomm Interface 0: USART RTS, I2C SCL, SPI SSEL1.
					I/O	**FC2_SSEL2 —** Flexcomm Interface 2: SPI SSEL2.
					O	**CTimer1_MAT3 —** 32-bit CTimer1 match output 3.
PIO0_4	C7	38	[2]	PU	I/O	**PIO0_4 —** General-purpose digital input/output pin. **Remark:** The state of this pin at Reset in conjunction with PIO0_31 and PIO1_6 will determine the boot source for the part or if ISP handler is invoked. See the Boot Process chapter in UM10914 for more details.
					I/O	**FC0_SCK —** Flexcomm Interface 0: USART or SPI clock.
					I/O	**FC3_SSEL2 —** Flexcomm Interface 3: SPI SSEL2.
					I	**CTimer0_CAP2 —** 32-bit CTimer0 capture input 2.

Table 4. Pin description *...continued*

Symbol	49-pin	64-pin		Reset state [1]	Type	Description
PIO0_5	C6	39	[2]	PU	I/O	**PIO0_5 —** General-purpose digital input/output pin.
					I/O	**FC6_RXD_SDA_MOSI_DATA —** Flexcomm Interface 6: USART RXD, I2C SDA, SPI MOSI, I2S data.
					O	**SCT0_OUT6 —** SCT0 output 6. PWM output 6.
					O	**CTimer0_MAT0 —** 32-bit CTimer0 match output 0.
PIO0_6	D7	40	[2]	PU	I/O	**PIO0_6 —** General-purpose digital input/output pin.
					I/O	**FC6_TXD_SCL_MISO_WS —** Flexcomm Interface 6: USART TXD, I2C SCL, SPI MISO, I2S WS.
						R — Reserved.
					O	**CTimer0_MAT1 —** 32-bit CTimer0 match output 1.
						R — Reserved.
					I	**UTICK_CAP0 —** Micro-tick timer capture input 0.
PIO0_7	D6	41	[2]	PU	I/O	**PIO0_7 —** General-purpose digital input/output pin.
					I/O	**FC6_SCK —** Flexcomm Interface 6: USART, SPI, or I2S clock.
					O	**SCT0_OUT0 —** SCT0 output 0. PWM output 0.
					O	**CTimer0_MAT2 —** 32-bit CTimer0 match output 2.
						R — Reserved.
					I	**CTimer0_CAP2 —** 32-bit CTimer0 capture input 2.
PIO0_8	D5	43	[2]	PU	I/O	**PIO0_8 —** General-purpose digital input/output pin.
					I/O	**FC2_RXD_SDA_MOSI —** Flexcomm Interface 2: USART RXD, I2C SDA, SPI MOSI.
					O	**SCT0_OUT1 —** SCT0 output 1. PWM output 1.
					O	**CTimer0_MAT3 —** 32-bit CTimer0 match output 3.
PIO0_9	E7	44	[2]	PU	I/O	**PIO0_9 —** General-purpose digital input/output pin.
					I/O	**FC2_TXD_SCL_MISO —** Flexcomm Interface 2: USART TXD, I2C SCL, SPI MISO.
					O	**SCT0_OUT2 —** SCT0 output 2. PWM output 2.
					I	**CTimer3_CAP0 —** 32-bit CTimer3 capture input 0.
						R — Reserved.
					I/O	**FC3_CTS_SDA_SSEL0 —** Flexcomm Interface 3: USART CTS, I2C SDA, SPI SSEL0.
PIO0_10	E6	45	[2]	PU	I/O	**PIO0_10 —** General-purpose digital input/output pin.
					I/O	**FC2_SCK —** Flexcomm Interface 2: USART or SPI clock.
					O	**SCT0_OUT3 —** SCT0 output 3. PWM output 3.
					O	**CTimer3_MAT0 —** 32-bit CTimer3 match output 0.

Table 4. Pin description *...continued*

Symbol	49-pin	64-pin		Reset state [1]	Type	Description
PIO0_11	E5	46	[2]	PU	I/O	**PIO0_11 —** General-purpose digital input/output pin. In ISP mode, this pin is set to the Flexcomm 3 SPI SCK function.
					I/O	**FC3_SCK —** Flexcomm Interface 3: USART or SPI clock.
					I/O	**FC6_RXD_SDA_MOSI_DATA —** Flexcomm Interface 6: USART RXD, I2C SDA, SPI MOSI, I2S DATA.
					O	**CTimer2_MAT1 —** 32-bit CTimer2 match output 1.
PIO0_12	F7	47	[2]	PU	I/O	**PIO0_12 —** General-purpose digital input/output pin. In ISP mode, this pin is set to the Flexcomm 3 SPI MOSI function.
					I/O	**FC3_RXD_SDA_MOSI —** Flexcomm Interface 3: USART RXD, I2C SDA, SPI MOSI.
					I/O	**FC6_TXD_SCL_MISO_WS —** Flexcomm Interface 6: USART TXD, I2C SCL, SPI MISO, I2S WS.
					O	**CTimer2_MAT3 —** 32-bit CTimer2 match output 3.
PIO0_13	G7	48	[2]	PU	I/O	**PIO0_13 —** General-purpose digital input/output pin. In ISP mode, this pin is set to the Flexcomm 3 SPI MISO function.
					I/O	**FC3_TXD_SCL_MISO —** Flexcomm Interface 3: USART TXD, I2C SCL, SPI MISO.
					O	**SCT0_OUT4 —** SCT0 output 4. PWM output 4.
					O	**CTimer2_MAT0 —** 32-bit CTimer2 match output 0.
PIO0_14/ TCK	F6	49	[2]	PU	I/O	**PIO0_14 —** General-purpose digital input/output pin. In boundary scan mode: TCK (Test Clock In). In ISP mode, this pin is set to the Flexcomm 3 SPI SSELN0 function.
					I/O	**FC3_CTS_SDA_SSEL0 —** Flexcomm Interface 3: USART CTS, I2C SDA, SPI SSEL0.
					O	**SCT0_OUT5 —** SCT0 output 5. PWM output 5.
					O	**CTimer2_MAT1 —** 32-bit CTimer2 match output 1.
						R — Reserved.
					I/O	**FC1_SCK —** Flexcomm Interface 1: USART or SPI clock.
PIO0_15/ TDO	G6	50	[2]	PU	I/O	**PIO0_15 —** General-purpose digital input/output pin. In boundary scan mode: TDO (Test Data Out).
					I/O	**FC3_RTS_SCL_SSEL1 —** Flexcomm Interface 3: USART RTS, I2C SCL, SPI SSEL1.
					I/O	**SWO —** Serial wire trace output.
					O	**CTimer2_MAT2 —** 32-bit CTimer2 match output 2.
						R — Reserved.
					I/O	**FC4_SCK —** Flexcomm Interface 4: USART or SPI clock.

Table 4. Pin description *...continued*

Symbol	49-pin	64-pin		Reset state [1]	Type	Description
SWCLK/ PIO0_16	F5	52	[2]	PU	I/O	**PIO0_16 —** General-purpose digital input/output pin.
					I/O	**FC3_SSEL2 —** Flexcomm Interface 3: SPI SSEL2.
					I/O	**FC6_CTS_SDA_SSEL0 —** Flexcomm Interface 6: USART CTS, I2C SDA, SPI SSEL0.
					O	**CTimer3_MAT1 —** 32-bit CTimer3 match output 1.
						R — Reserved.
					I/O	**SWCLK —** Serial Wire Clock. JTAG Test Clock. This is the default function after booting.
						R — Reserved.
SWDIO/ PIO0_17	G5	53	[2]	PU	I/O	**PIO0_17 —** General-purpose digital input/output pin.
					I/O	**FC3_SSEL3 —** Flexcomm Interface 3: SPI SSEL3.
					I/O	**FC6_RTS_SCL_SSEL1 —** Flexcomm Interface 6: USART RTS, I2C SCL, SPI SSEL1.
					O	**CTimer3_MAT2 —** 32-bit CTimer3 match output 2.
						R — Reserved.
					I/O	**SWDIO —** Serial Wire Debug I/O. This is the default function after booting.
PIO0_18/ $\overline{\text{TRST}}$	G4	58	[2]	PU	I/O	**PIO0_18 —** General-purpose digital input/output pin. In boundary scan mode: $\overline{\text{TRST}}$ (Test Reset).
					I/O	**FC5_TXD_SCL_MISO —** Flexcomm Interface 5: USART TXD, I2C SCL, SPI MISO.
					O	**SCT0_OUT0 —** SCT0 output 0. PWM output 0.
					O	**CTimer0_MAT0 —** 32-bit CTimer0 match output 0.
PIO0_19/ TDI	G3	59	[2]	PU	I/O	**PIO0_19 —** General-purpose digital input/output pin. In boundary scan mode: TDI (Test Data In).
					I/O	**FC5_SCK —** Flexcomm Interface 5: USART or SPI clock.
					O	**SCT0_OUT1 —** SCT0 output 1. PWM output 1.
					O	**CTimer0_MAT1 —** 32-bit CTimer0 match output 1.
PIO0_20/ TMS	F3	60	[2]	PU	I/O	**PIO0_20 —** General-purpose digital input/output pin. In boundary scan mode: TMS (Test Mode Select).
					I/O	**FC5_RXD_SDA_MOSI —** Flexcomm Interface 5: USART RXD, I2C SDA, SPI MOSI.
					I/O	**FC0_SCK —** Flexcomm Interface 0: USART or SPI clock.
					I	**CTimer3_CAP0 —** 32-bit CTimer3 capture input 0.
PIO0_21	E3	61	[2]	PU	I/O	**PIO0_21 —** General-purpose digital input/output pin.
					O	**CLKOUT —** Clock output.
					I/O	**FC0_TXD_SCL_MISO —** Flexcomm Interface 0: USART TXD, I2C SCL, SPI MISO.
					O	**CTimer3_MAT0 —** 32-bit CTimer3 match output 0.

Table 4. Pin description *...continued*

Symbol	49-pin	64-pin		Reset state [1]	Type	Description
PIO0_22	G2	63	[2]	PU	I/O	**PIO0_22 —** General-purpose digital input/output pin.
					I	**CLKIN —** Clock input.
					I/O	**FC0_RXD_SDA_MOSI —** Flexcomm Interface 0: USART RXD, I2C SDA, SPI MOSI.
					O	**CTimer3_MAT3 —** 32-bit CTimer3 match output 3.
PIO0_23	F2	1	[3]	Z	I/O	**PIO0_23 —** General-purpose digital input/output pin. In ISP mode, this pin is set to the Flexcomm 1 I2C SCL function.
					I/O	**FC1_RTS_SCL_SSEL1 —** Flexcomm Interface 1: USART CTS, I2C SCL, SPI SSEL1.
						R — Reserved.
					I	**CTimer0_CAP0 —** 32-bit CTimer0 capture input 0.
						R — Reserved.
					I	**UTICK_CAP1 —** Micro-tick timer capture input 1.
PIO0_24	F1	2	[3]	Z	I/O	**PIO0_24 —** General-purpose digital input/output pin. In ISP mode, this pin is set to the Flexcomm 1 I2C SDA function.
					I/O	**FC1_CTS_SDA_SSEL0 —** Flexcomm Interface 1: USART CTS, I2C SDA, SPI SSEL0.
						R — Reserved.
					I	**CTimer0_CAP1 —** 32-bit CTimer0 capture input 1.
						R — Reserved.
					O	**CTimer0_MAT0 —** 32-bit CTimer0 match output 0.
PIO0_25	E2	3	[3]	Z	I/O	**PIO0_25 —** General-purpose digital input/output pin.
					I/O	**FC4_RTS_SCL_SSEL1 —** Flexcomm Interface 4: USART CTS, I2C SCL, SPI SSEL1.
					I/O	**FC6_CTS_SDA_SSEL0 —** Flexcomm Interface 6: USART CTS, I2C SDA, SPI SSEL0.
					I	**CTimer0_CAP2 —** 32-bit CTimer0 capture input 2.
						R — Reserved.
					I	**CTimer1_CAP1 —** 32-bit CTimer1 capture input 1.
PIO0_26	E1	4	[3]	Z	I/O	**PIO0_26 —** General-purpose digital input/output pin.
					I/O	**FC4_CTS_SDA_SSEL0 —** Flexcomm Interface 4: USART CTS, I2C SDA, SPI SSEL0.
						R — Reserved.
					I	**CTimer0_CAP3 —** 32-bit CTimer0 capture input 3.

Table 4. Pin description *...continued*

Symbol	49-pin	64-pin		Reset state [1]	Type	Description
PIO0_29/ ADC0_0	D3	11	[4]	PU	I/O; AI	**PIO0_29/ADC0_0 —** General-purpose digital input/output pin. ADC input channel 0 if the DIGIMODE bit is set to 0 in the IOCON register for this pin.
					I/O	**FC1_RXD_SDA_MOSI —** Flexcomm Interface 1: USART RXD, I2C SDA, SPI MOSI.
					O	**SCT0_OUT2 —** SCT0 output 2. PWM output 2.
					O	**CTimer0_MAT3 —** 32-bit CTimer0 match output 3.
						R — Reserved.
					I	**CTimer0_CAP1 —** 32-bit CTimer0 capture input 1.
						R — Reserved.
					O	**CTimer0_MAT1 —** 32-bit CTimer0 match output 1.
PIO0_30/ ADC0_1	C1	12	[4]	PU	I/O; AI	**PIO0_30/ADC0_1 —** General-purpose digital input/output pin. ADC input channel 1 if the DIGIMODE bit is set to 0 in the IOCON register for this pin.
					I/O	**FC1_TXD_SCL_MISO —** Flexcomm Interface 1: USART TXD, I2C SCL, SPI MISO.
					O	**SCT0_OUT3 —** SCT0 output 3. PWM output 3.
					O	**CTimer0_MAT2 —** 32-bit CTimer0 match output 2.
						R — Reserved.
					I	**CTimer0_CAP2 —** 32-bit CTimer0 capture input 2.
PIO0_31/ ADC0_2	C2	13	[4]	PU	I/O; AI	**PIO0_31/ADC0_2 —** General-purpose digital input/output pin. ADC input channel 2 if the DIGIMODE bit is set to 0 in the IOCON register for this pin. **Remark:** This pin is also used to invoke ISP mode after device reset. Secondary selection of boot source for ISP mode also uses PIO0_4 and PIO1_6. See the Boot Process chapter in UM10914 for more details.
					O	**PDM0_CLK —** Clock for PDM interface 0, for digital microphone.
					I/O	**FC2_CTS_SDA_SSEL0 —** Flexcomm Interface 2: USART CTS, I2C SDA, SPI SSEL0.
					I	**CTimer2_CAP2 —** 32-bit CTimer2 capture input 2.
						R — Reserved.
					I	**CTimer0_CAP3 —** 32-bit CTimer0 capture input 3.
					O	**CTimer0_MAT3 —** 32-bit CTimer0 match output 3.
PIO1_0/ ADC0_3	C3	14	[4]	PU	I/O; AI	**PIO1_0/ADC0_3 —** General-purpose digital input/output pin. ADC input channel 3 if the DIGIMODE bit is set to 0 in the IOCON register for this pin.
					I	**PDM0_DATA —** Data for PDM interface 0, digital microphone input.
					I/O	**FC2_RTS_SCL_SSEL1 —** Flexcomm Interface 2: USART RTS, I2C SCL, SPI SSEL1.
					O	**CTimer3_MAT1 —** 32-bit CTimer3 match output 1.
						R — Reserved.
					I	**CTimer0_CAP0 —** 32-bit CTimer0 capture input 0.

Table 4. Pin description *...continued*

Symbol	49-pin	64-pin		Reset state [1]	Type	Description
PIO1_1/ ADC0_4	B1	15	[4]	PU	I/O; AI	**PIO1_1/ADC0_4 —** General-purpose digital input/output pin. ADC input channel 4 if the DIGIMODE bit is set to 0 in the IOCON register for this pin.
						R — Reserved.
					I/O	**SWO —** Serial wire trace output.
					O	**SCT0_OUT4 —** SCT0 output 4. PWM output 4.
					I/O	**FC5_SSEL2 —** Flexcomm Interface 5: SPI SSEL2.
					I/O	**FC4_TXD_SCL_MISO —** Flexcomm Interface 4: USART TXD, I2C SCL, SPI MISO.
PIO1_2/ ADC0_5	A1	16	[4]	PU	I/O; AI	**PIO1_2/ADC0_5 —** General-purpose digital input/output pin. ADC input channel 5 if the DIGIMODE bit is set to 0 in the IOCON register for this pin.
					I/O	**MCLK —** MCLK input or output for I2S and/or digital microphone.
					I/O	**FC7_SSEL3 —** Flexcomm Interface 7: SPI SSEL3.
					O	**SCT0_OUT5 —** SCT0 output 5. PWM output 5.
					I/O	**FC5_SSEL3 —** Flexcomm Interface 5: SPI SSEL3.
					I/O	**FC4_RXD_SDA_MOSI —** Flexcomm Interface 4: USART RXD, I2C SDA, SPI MOSI.
PIO1_3/ ADC0_6	B2	17	[4]	PU	I/O; AI	**PIO1_3/ADC0_6 —** General-purpose digital input/output pin. ADC input channel 6 if the DIGIMODE bit is set to 0 in the IOCON register for this pin.
						R — Reserved.
					I/O	**FC7_SSEL2 —** Flexcomm Interface 7: SPI SSEL2.
					O	**SCT0_OUT6 —** SCT0 output 6. PWM output 6.
						R — Reserved.
					I/O	**FC3_SCK —** Flexcomm Interface 3: USART or SPI clock.
					I	**CTimer0_CAP1 —** 32-bit CTimer0 capture input 1.
					O	**USB_UP_LED —** USB port 2 GoodLink LED indicator. It is LOW when the device is configured (non-control endpoints enabled). It is HIGH when the device is not configured or during global suspend.
PIO1_4/ ADC0_7	A2	18	[4]	PU	I/O; AI	**PIO1_4/ADC0_7 —** General-purpose digital input/output pin. ADC input channel 7 if the DIGIMODE bit is set to 0 in the IOCON register for this pin.
					O	**PDM1_CLK —** Clock for PDM interface 1, for digital microphone.
					I/O	**FC7_RTS_SCL_SSEL1 —** Flexcomm Interface 7: USART RTS, I2C SCL, SPI SSEL1.
					O	**SCT0_OUT7 —** SCT0 output 7. PWM output 7.
						R — Reserved.
					I/O	**FC3_TXD_SCL_MISO —** Flexcomm Interface 3: USART TXD, I2C SCL, SPI MISO.
					O	**CTimer0_MAT1 —** 32-bit CTimer0 match output 1.

Table 4. Pin description *...continued*

Symbol	49-pin	64-pin		Reset state [1]	Type	Description
PIO1_5/ ADC0_8	B3	19	[4]	PU	I/O; AI	**PIO1_5/ADC0_8 —** General-purpose digital input/output pin. ADC input channel 8 if the DIGIMODE bit is set to 0 in the IOCON register for this pin.
					I	**PDM1_DATA —** Data for PDM interface 1, digital microphone input. Also PDM clock input in bypass mode.
					I/O	**FC7_CTS_SDA_SSEL0 —** Flexcomm Interface 7: USART CTS, I2C SDA, SPI SSEL0.
					I	**CTimer1_CAP0 —** 32-bit CTimer1 capture input 0.
						R — Reserved.
					O	**CTimer1_MAT3 —** 32-bit CTimer1 match output 3.
						R — Reserved.
					O	**USB_FRAME —** USB start-of-frame signal derived from host signaling.
PIO1_6/ ADC0_9	A5	26	[4]	PU	I/O; AI	**PIO1_6/ADC0_9 —** General-purpose digital input/output pin. ADC input channel 9 if the DIGIMODE bit is set to 0 in the IOCON register for this pin. **Remark:** This pin is also used as part of secondary selection of boot source for ISP mode after device reset, in connection with PIO0_31 and PIO0_4. See the Boot Process chapter in UM10914 for more details.
						R — Reserved.
					I/O	**FC7_SCK —** Flexcomm Interface 7: USART, SPI, or I2S clock.
					I	**CTimer1_CAP2 —** 32-bit CTimer1 capture input 2.
						R — Reserved.
					O	**CTimer1_MAT2 —** 32-bit CTimer1 match output 2.
						R — Reserved.
					I	**USB_VBUS —** Monitors the presence of USB bus power. This signal must be HIGH for USB reset to occur.
PIO1_7/ ADC0_10	B5	27	[4]	PU	I/O; AI	**PIO1_7/ADC0_10 —** General-purpose digital input/output pin. ADC input channel 10 if the DIGIMODE bit is set to 0 in the IOCON register for this pin.
						R — Reserved.
					I/O	**FC7_RXD_SDA_MOSI_DATA —** Flexcomm Interface 7: USART RXD, I2C SDA, SPI MOSI, I2S DATA.
					O	**CTimer1_MAT2 —** 32-bit CTimer1 match output 2.
						R — Reserved.
					I	**CTimer1_CAP2 —** 32-bit CTimer1 capture input 2.
PIO1_8/ ADC0_11	C5	28	[4]	PU	I/O; AI	**PIO1_8/ADC0_11 —** General-purpose digital input/output pin. ADC input channel 11 if the DIGIMODE bit is set to 0 in the IOCON register for this pin.
						R — Reserved.
					I/O	**FC7_TXD_SCL_MISO_WS —** Flexcomm Interface 7: USART TXD, I2C SCL, SPI MISO, I2S WS.
					O	**CTimer1_MAT3 —** 32-bit CTimer1 match output 3.
						R — Reserved.
					I	**CTimer1_CAP3 —** 32-bit CTimer1 capture input 3.

Table 4. Pin description *...continued*

Symbol	49-pin	64-pin		Reset state [1]	Type	Description
PIO1_9	-	29	[2]	PU	I/O	**PIO1_9 —** General-purpose digital input/output pin.
						R — Reserved.
					I/O	**FC3_RXD_SDA_MOSI —** Flexcomm Interface 3: USART RXD, I2C SDA, SPI MOSI.
					I	**CTimer0_CAP2 —** 32-bit CTimer0 capture input 2.
						R — Reserved.
						R — Reserved.
					O	**USB_UP_LED —** USB port 2 GoodLink LED indicator. It is LOW when the device is configured (non-control endpoints enabled). It is HIGH when the device is not configured or during global suspend.
PIO1_10	-	30	[2]	PU	I/O	**PIO1_10 —** General-purpose digital input/output pin.
						R — Reserved.
					I/O	**FC6_TXD_SCL_MISO_WS —** Flexcomm Interface 6: USART TXD, I2C SCL, SPI MISO, I2S WS.
					O	**SCT0_OUT4 —** SCT0 output 4. PWM output 4.
					I/O	**FC1_SCK —** Flexcomm Interface 1: USART or SPI clock.
						R — Reserved.
						R — Reserved.
					I	**USB_FRAME —** USB start-of-frame signal derived from host signaling.
PIO1_11	-	42	[2]	PU	I/O	**PIO1_11 —** General-purpose digital input/output pin.
						R — Reserved.
					I/O	**FC6_RTS_SCL_SSEL1 —** Flexcomm Interface 6: USART RTS, I2C SCL, SPI SSEL1.
					I	**CTimer1_CAP0 —** 32-bit CTimer1 capture input 0.
					I/O	**FC4_SCK —** Flexcomm Interface 4: USART or SPI clock.
						R — Reserved.
						R — Reserved.
					I	**USB_VBUS —** Monitors the presence of USB bus power. This signal must be HIGH for USB reset to occur.
PIO1_12	-	51	[2]	PU	I/O	**PIO1_12 —** General-purpose digital input/output pin.
						R — Reserved.
					I/O	**FC5_RXD_SDA_MOSI —** Flexcomm Interface 5: USART RXD, I2C SDA, SPI MOSI.
					O	**CTimer1_MAT0 —** 32-bit CTimer1 match output 0.
					I/O	**FC7_SCK —** Flexcomm Interface 7: USART, SPI, or I2S clock.
					I	**UTICK_CAP2 —** Micro-tick timer capture input 2.

Table 4. Pin description *...continued*

Symbol	49-pin	64-pin		Reset state [1]	Type	Description
PIO1_13	-	54	[2]	PU	I/O	**PIO1_13 —** General-purpose digital input/output pin.
						R — Reserved.
					I/O	**FC5_TXD_SCL_MISO —** Flexcomm Interface 5: USART TXD, I2C SCL, SPI MISO.
					O	**CTimer1_MAT1 —** 32-bit CTimer1 match output 1.
					I/O	**FC7_RXD_SDA_MOSI_DATA —** Flexcomm Interface 7: USART RXD, I2C SDA, SPI MOSI, I2S DATA.
PIO1_14	-	57	[2]	PU	I/O	**PIO1_14 —** General-purpose digital input/output pin.
						R — Reserved.
					I/O	**FC2_RXD_SDA_MOSI —** Flexcomm Interface 2: USART RXD, I2C SDA, SPI MOSI.
					O	**SCT0_OUT7 —** SCT0 output 7. PWM output 7.
					I/O	**FC7_TXD_SCL_MISO_WS —** Flexcomm Interface 7: USART TXD, I2C SCL, SPI MISO, I2S WS.
PIO1_15	-	62	[2]	PU	I/O	**PIO1_15 —** General-purpose digital input/output pin.
					O	**PDM0_CLK —** Clock for PDM interface 0, for digital microphone.
					O	**SCT0_OUT5 —** SCT0 output 5. PWM output 5.
					I	**CTimer1_CAP3 —** 32-bit CTimer1 capture input 3.
					I/O	**FC7_CTS_SDA_SSEL0 —** Flexcomm Interface 7: USART CTS, I2C SDA, SPI SSEL0.
PIO1_16	-	7	[2]	PU	I/O	**PIO1_16 —** General-purpose digital input/output pin.
					I	**PDM0_DATA —** Data for PDM interface 0, digital microphone input.
					O	**CTimer0_MAT0 —** 32-bit CTimer0 match output 0.
					I	**CTimer0_CAP0 —** 32-bit CTimer0 capture input 0.
					I/O	**FC7_RTS_SCL_SSEL1 —** Flexcomm Interface 7: USART RTS, I2C SCL, SPI SSEL1.
PIO1_17	-	10	[2]	PU	I/O	**PIO1_17 —** General-purpose digital input/output pin.
						R — Reserved.
						R — Reserved.
						R — Reserved.
					I/O	**MCLK —** MCLK input or output for I2S and/or digital microphone.
					I	**UTICK_CAP3 —** Micro-tick timer capture input 3.
USB_DP	D2	5	[6]	F	I/O	USB0 bidirectional D+ line.
USB_DM	D1	6	[6]	F	I/O	USB0 bidirectional D- line.
RESETN	G1	64	[5]	PU	I	External reset input: A LOW on this pin resets the device, causing I/O ports and peripherals to take on their default states, and processor execution to begin at address 0. Wakes up the part from deep power-down mode.
RTCXIN	A7	33		-	-	RTC oscillator input.
RTCXOUT	B7	35		-	-	RTC oscillator output.
VREFP	B4	22		-	-	ADC positive reference voltage.

Table 4. Pin description *…continued*

Symbol	49-pin	64-pin		Reset state [1]	Type	Description
VREFN	-	21		-	-	ADC negative reference voltage.
V_{DDA}	A4	23		-	-	Analog supply voltage.
V_{DD}	C4, F4	8, 24, 34, 56		-	-	Single 1.62 V to 3.6 V power supply powers internal digital functions and I/Os.
V_{SS}	D4, E4	9, 25, 55		-	-	Ground.
V_{SSA}	A3	20		-	-	Analog ground.

[1] PU = input mode, pull-up enabled (pull-up resistor pulls up pin to V_{DD}). Z = high impedance; pull-up or pull-down disabled, AI = analog input, I = input, O = output, F = floating. Reset state reflects the pin state at reset without boot code operation. For pin states in the different power modes, see Section 6.2.2 “Pin states in different power modes”. For termination on unused pins, see Section 6.2.1 “Termination of unused pins”.

[2] 5 V tolerant pad with programmable glitch filter (5 V tolerant if V_{DD} present; if V_{DD} not present, do not exceed 3.6 V); provides digital I/O functions with TTL levels and hysteresis; normal drive strength. See Figure 31. Pulse width of spikes or glitches suppressed by input filter is from 3 ns to 16 ns (simulated value).

[3] True open-drain pin. I2C-bus pins compliant with the I2C-bus specification for I2C standard mode, I2C Fast-mode, and I2C Fast-mode Plus. The pin requires an external pull-up to provide output functionality. When power is switched off, this pin is floating and does not disturb the I2C lines. Open-drain configuration applies to all functions on this pin.

[4] 5 V tolerant pin providing standard digital I/O functions with configurable modes, configurable hysteresis, and analog input. When configured as an analog input, the digital section of the pin is disabled, and the pin is not 5 V tolerant.

[5] Reset pad.5 V tolerant pad with glitch filter with hysteresis. Pulse width of spikes or glitches suppressed by input filter is from 3 ns to 20 ns (simulated value)

[6] 5 V tolerant transparent analog pad.

6.2.1 Termination of unused pins

Table 5 shows how to terminate pins that are **not** used in the application. In many cases, unused pins should be connected externally or configured correctly by software to minimize the overall power consumption of the part.

Unused pins with GPIO function should be configured as outputs set to LOW with their internal pull-up disabled. To configure a GPIO pin as output and drive it LOW, select the GPIO function in the IOCON register, select output in the GPIO DIR register, and write a 0 to the GPIO PORT register for that pin. Disable the pull-up in the pin's IOCON register.

In addition, it is recommended to configure all GPIO pins that are not bonded out on smaller packages as outputs driven LOW with their internal pull-up disabled.

Table 5. Termination of unused pins

Pin	Default state[1]	Recommended termination of unused pins
$\overline{\text{RESET}}$	I; PU	The $\overline{\text{RESET}}$ pin can be left unconnected if the application does not use it.
all PIOn_m (not open-drain)	I; PU	Can be left unconnected if driven LOW and configured as GPIO output with pull-up disabled by software.
PIOn_m (I2C open-drain)	IA	Can be left unconnected if driven LOW and configured as GPIO output by software.
USB_DP	F	If USB interface is not used, pin can be left unconnected except in deep power-down mode where it must be externally pulled low.
USB_DM	F	If USB interface is not used, pin can be left unconnected except in deep power-down mode where it must be externally pulled low.
RTCXIN	-	Connect to ground. When grounded, the RTC oscillator is disabled.
RTCXOUT	-	Can be left unconnected.
VREFP	-	Tie to V_{DD}.
VREFN	-	Tie to V_{SS}.
V_{DDA}	-	Tie to V_{DD}.
V_{SSA}	-	Tie to V_{SS}.

[1] I = Input, IA = Inactive (no pull-up/pull-down enabled), PU = Pull-Up enabled, F = Floating

6.2.2 Pin states in different power modes

Table 6. Pin states in different power modes

Pin	Active	Sleep	Deep-sleep	Deep power-down
PIOn_m pins (not I2C)	As configured in the IOCON[1]. Default: internal pull-up enabled.			Floating.
PIO0_23 to PIO0_26 (open-drain I2C-bus pins)	As configured in the IOCON[1].			Floating.
$\overline{\text{RESET}}$	Reset function enabled. Default: input, internal pull-up enabled.			

[1] Default and programmed pin states are retained in sleep and deep-sleep modes.

7. Functional description

7.1 Architectural overview

The ARM Cortex-M4 includes three AHB-Lite buses, one system bus and the I-code and D-code buses. One bus is dedicated for instruction fetch (I-code), and one bus is dedicated for data access (D-code). The use of two core buses allows for simultaneous operations if concurrent operations target different devices.

The LPC5411x uses a multi-layer AHB matrix to connect the ARM Cortex-M4 buses and other bus masters to peripherals in a flexible manner that optimizes performance by allowing peripherals that are on different slave ports of the matrix to be accessed simultaneously by different bus masters.

7.2 ARM Cortex-M4 processor

The ARM Cortex-M4 is a general purpose, 32-bit microprocessor, which offers high performance and very low power consumption. The ARM Cortex-M4 offers many new features, including a Thumb-2 instruction set, low interrupt latency, hardware multiply and divide, interruptable/continuable multiple load and store instructions, automatic state save and restore for interrupts, tightly integrated interrupt controller with wake-up interrupt controller, and multiple core buses capable of simultaneous accesses.

A 3-stage pipeline is employed so that all parts of the processing and memory systems can operate continuously. Typically, while one instruction is being executed, its successor is being decoded, and a third instruction is being fetched from memory.

7.3 ARM Cortex-M4 integrated Floating Point Unit (FPU)

The FPU fully supports single-precision add, subtract, multiply, divide, multiply and accumulate, and square root operations. It also provides conversions between fixed-point and floating-point data formats, and floating-point constant instructions.

The FPU provides floating-point computation functionality that is compliant with the ANSI/IEEE Std 754-2008, IEEE Standard for Binary Floating-Point Arithmetic, referred to as the IEEE 754 standard.

7.4 ARM Cortex-M0+ co-processor

The ARM Cortex-M0+ co-processor offers high performance and very low power consumption. This processor uses a 2-stage pipeline von Neumann architecture and a small but powerful instruction set providing high-end processing hardware. The processor includes a single-cycle multiplier, an NVIC with 32 interrupts, and a separate system tick timer.

7.5 Memory Protection Unit (MPU)

The Cortex-M4 includes a Memory Protection Unit (MPU) which can be used to improve the reliability of an embedded system by protecting critical data within the user application.

The MPU allows separating processing tasks by disallowing access to each other's data, disabling access to memory regions, allowing memory regions to be defined as read-only and detecting unexpected memory accesses that could potentially break the system.

The MPU separates the memory into distinct regions and implements protection by preventing disallowed accesses. The MPU supports up to eight regions each of which can be divided into eight subregions. Accesses to memory locations that are not defined in the MPU regions, or not permitted by the region setting, will cause the Memory Management Fault exception to take place.

7.6 Nested Vectored Interrupt Controller (NVIC) for Cortex-M4

The NVIC is an integral part of the Cortex-M4. The tight coupling to the CPU allows for low interrupt latency and efficient processing of late arriving interrupts.

7.6.1 Features

- Controls system exceptions and peripheral interrupts.
- 40 vectored interrupt slots.
- Eight programmable interrupt priority levels, with hardware priority level masking.
- Relocatable vector table using Vector Table Offset Register (VTOR).
- Non-Maskable Interrupt (NMI).
- Software interrupt generation.

7.6.2 Interrupt sources

Each peripheral device has one interrupt line connected to the NVIC but may have several interrupt flags.

7.7 Nested Vectored Interrupt Controller (NVIC) for Cortex-M0+

The NVIC is an integral part of the Cortex-M0+. The tight coupling to the CPU allows for low interrupt latency and efficient processing of late arriving interrupts.

7.7.1 Features

- Controls system exceptions and peripheral interrupts.
- 32 vectored interrupt slots.
- Four programmable interrupt priority levels, with hardware priority level masking.
- Relocatable vector table using VTOR.
- Non-Maskable Interrupt (NMI).
- Software interrupt generation.

7.7.2 Interrupt sources

Each peripheral device has one interrupt line connected to the NVIC but may have several interrupt flags.

7.8 System Tick timer (SysTick)

The ARM Cortex-M4 and ARM Cortex-M0+ cores include a system tick timer (SysTick) that is intended to generate a dedicated SYSTICK exception. The clock source for the SysTick can be the system clock or the SYSTICK clock.

7.9 On-chip static RAM

The LPC5411x supports up to192 KB SRAM with separate bus master access for higher throughput and individual power control for low-power operation.

7.10 On-chip flash

The LPC5411x supports up to 256 KB of on-chip flash memory.

7.11 On-chip ROM

The 32 KB on-chip ROM contains the boot loader and the following Application Programming Interfaces (API):

- In-System Programming (ISP) and In-Application Programming (IAP) support for flash programming.
- ROM-based USB drivers (HID, CDC, MSC, and DFU). Flash updates via USB is supported.
- Supports booting from valid user code in flash, USART, SPI, and I^2C.
- Legacy, Single, and Dual image boot.

7.12 Memory mapping

The LPC5411x incorporates several distinct memory regions. The APB peripheral area is 64 KB in size and is divided to allow for up to 32 peripherals. Each peripheral is allocated 4 KB of space simplifying the address decoding.

Figure 6 shows the overall map of the entire address space from the user program viewpoint following reset.