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LPC546xx

32-bit ARM Cortex-M4 microcontroller; up to 512 KB flash and 200 kB SRAM; High-speed USB device/host + PHY; Full-speed USB device/host; Ethernet AVB; LCD; EMC; SPIFI; CAN FD, SDIO; SHA; 12-bit 5 Msamples/s ADC; DMIC subsystem

Rev. 2.5 — 20 June 2018 Product data sheet

1. General description

The LPC546xx is a family of ARM Cortex-M4 based microcontrollers for embedded applications featuring a rich peripheral set with very low power consumption and enhanced debug features.

The ARM Cortex-M4 is a 32-bit core that offers system enhancements such as low power consumption, enhanced debug features, and a high level of support block integration. The ARM Cortex-M4 CPU incorporates a 3-stage pipeline, uses a Harvard architecture with separate local instruction and data buses as well as a third bus for peripherals, and includes an internal prefetch unit that supports speculative branching. The ARM Cortex-M4 supports single-cycle digital signal processing and SIMD instructions. A hardware floating-point processor is integrated into the core.

The LPC546xx family includes up to 512 KB of flash, 200 KB of on-chip SRAM, up to 16 kB of EEPROM memory, a quad SPI Flash Interface (SPIFI) for expanding program memory, one high-speed and one full-speed USB host and device controller, Ethernet AVB, LCD controller, Smart Card Interfaces, SD/MMC, CAN FD, an External Memory Controller (EMC), a DMIC subsystem with PDM microphone interface and I^2S, five general-purpose timers, SCTimer/PWM, RTC/alarm timer, Multi-Rate Timer (MRT), a Windowed Watchdog Timer (WWDT), ten flexible serial communication peripherals (USART, SPI, I^2S, I^2C interface), Secure Hash Algorithm (SHA), 12-bit 5.0 Msamples/sec ADC, and a temperature sensor.

2. Features and benefits

- ARM Cortex-M4 core (version r0p1):
  - ARM Cortex-M4 processor, running at a frequency of up to 220 MHz.
  - The LPC5460x/61x devices operate at CPU frequencies of up to 180 MHz. The LPC54628 device operates at CPU frequencies of up to 220 MHz.
  - Floating Point Unit (FPU) and Memory Protection Unit (MPU).
  - ARM Cortex-M4 built-in Nested Vectored Interrupt Controller (NVIC).
  - Non-maskable Interrupt (NMI) input with a selection of sources.
  - Serial Wire Debug (SWD) with six instruction breakpoints, two literal comparators, and four watch points. Includes Serial Wire Output and ETM Trace for enhanced debug capabilities, and a debug timestamp counter.
  - System tick timer.

- On-chip memory:
  - Up to 512 KB on-chip flash program memory with flash accelerator and 256 byte page erase and write.
  - Up to 200 KB total SRAM consisting of 160 KB contiguous main SRAM and an additional 32 KB SRAM on the I&D buses. 8 KB of SRAM bank intended for USB traffic.
  - 16 KB of EEPROM.
- ROM API support:
  - Flash In-Application Programming (IAP) and In-System Programming (ISP).
  - ROM-based USB drivers (HID, CDC, MSC, and DFU). Flash updates via USB.
  - Booting from valid user code in flash, USART, SPI, and I^2C.
  - Legacy, Single, and Dual image boot.
  - OTP API for programming OTP memory.
  - Random Number Generator (RNG) API.
- Serial interfaces:
  - Flexcomm Interface contains up to ten serial peripherals. Each Flexcomm Interface can be selected by software to be a USART, SPI, or I^2C interface. Two Flexcomm Interfaces also include an I^2S interface. Each Flexcomm Interface includes a FIFO that supports USART, SPI, and I^2S if supported by that Flexcomm Interface. A variety of clocking options are available to each Flexcomm Interface and include a shared fractional baud-rate generator.
  - I^2C-bus interfaces support Fast-mode and Fast-mode Plus with data rates of up to 1Mbit/s and with multiple address recognition and monitor mode. Two sets of true I^2C pads also support High Speed Mode (3.4 Mbit/s) as a slave.
  - Two ISO 7816 Smart Card Interfaces with DMA support.
  - USB 2.0 high-speed host/device controller with on-chip high-speed PHY.
  - USB 2.0 full-speed host/device controller with on-chip PHY and dedicated DMA controller supporting crystal-less operation in device mode using software library. See Technical note TN00032 for more details.
  - SPIFI with XIP feature uses up to four data lines to access off-chip SPI/DSPI/QSPI flash memory at a much higher rate than standard SPI or SSP interfaces.
  - Ethernet MAC with MII/RMII interface with Audio Video Bridging (AVB) support and dedicated DMA controller.
  - Two CAN FD modules with dedicated DMA controller.
- Digital peripherals:
  - DMA controller with 30 channels and up to 24 programmable triggers, able to access all memories and DMA-capable peripherals.
  - LCD Controller supporting both Super-Twisted Nematic (STN) and Thin-Film Transistor (TFT) displays. It has a dedicated DMA controller, selectable display resolution (up to 1024 x 768 pixels), and supports up to 24-bit true-color mode.
  - External Memory Controller (EMC) provides support for asynchronous static memory devices such as RAM, ROM and flash, in addition to dynamic memories such as single data rate SDRAM with an SDRAM clock of up to 100 MHz. EMC bus width (bit) on TFBGA180, TFBGA100, and LQFP100 and packages supports up to 8/16 data line wide static memory, in addition to dynamic memories, such as, SDRAM (2 banks only) with an SDRAM clock of up to 100 MHz.
  - Secured digital input/output (SD/MMC and SDIO) card interface with DMA support.

- CRC engine block can calculate a CRC on supplied data using one of three standard polynomials with DMA support.
- Up to 171 General-Purpose Input/Output (GPIO) pins.
- GPIO registers are located on the AHB for fast access. The DMA supports GPIO ports.
- Up to eight GPIOs can be selected as Pin Interrupts (PINT), triggered by rising, falling or both input edges.
- Two GPIO Grouped Interrupts (GINT) enable an interrupt based on a logical (AND/OR) combination of input states.
- CRC engine.

- Analog peripherals:
  - 12-bit ADC with 12 input channels and with multiple internal and external trigger inputs and sample rates of up to 5.0 MSamples/sec. The ADC supports two independent conversion sequences.
  - Integrated temperature sensor connected to the ADC.
- DMIC subsystem including a dual-channel PDM microphone interface, flexible decimators, 16 entry FIFOs, optional DC locking, hardware voice activity detection, and the option to stream the processed output data to I^2S.
- Timers:
  - Five 32-bit general purpose timers/counters, four of which support up to four capture inputs and four compare outputs, PWM mode, and external count input. Specific timer events can be selected to generate DMA requests. The fifth timer does not have external pin connections and may be used for internal timing operations.
  - SCTimer/PWM with 8 input and 10 output functions (including capture and match). Inputs and outputs can be routed to/from external pins and internally to or from selected peripherals. Internally, the SCTimer/PWM supports 10 match/captures, 10 events, and 10 states.
  - 32-bit Real-time clock (RTC) with 1 s resolution running in the always-on power domain. A timer in the RTC can be used for wake-up from all low power modes including deep power-down, with 1 ms resolution.
  - Multiple-channel multi-rate 24-bit timer (MRT) for repetitive interrupt generation at up to four programmable, fixed rates.
  - Windowed Watchdog Timer (WWDT).
  - Repetitive Interrupt Timer (RIT) for debug time stamping and for general purpose use.
- Security features:
  - enhanced Code Read Protection (eCRP) to protect user code.
  - OTP memory for ECRP settings, and user application specific data.
  - Secure Hash Algorithm (SHA1/SHA2) module with dedicated DMA controller.
- Clock generation:
  - 12 MHz internal Free Running Oscillator (FRO). This oscillator provides a selectable 48 MHz or 96 MHz output, and a 12 MHz output (divided down from the selected higher frequency) that can be used as a system clock. The FRO is trimmed to ±1 % accuracy over the entire voltage and temperature range.
  - External clock input for clock frequencies of up to 25 MHz.
  - Crystal oscillator with an operating range of 1 MHz to 25 MHz.

- Watchdog Oscillator (WDTOSC) with a frequency range of 6 kHz to 1.5 MHz.
- 32.768 kHz low-power RTC oscillator.
- System PLL allows CPU operation up to the maximum CPU rate and can run from the main oscillator, the internal FRO, the watchdog oscillator or the 32.768 KHz RTC oscillator.
- Two additional PLLs for USB clock and audio subsystem.
- Independent clocks for the SPIFI interface, ADC, USBs, and the audio subsystem.
- Clock output function with divider.
- Frequency measurement unit for measuring the frequency of any on-chip or off-chip clock signal.

- Power control:
  - Programmable PMU (Power Management Unit) to minimize power consumption and to match requirements at different performance levels.
  - Reduced power modes: sleep, deep-sleep, and deep power-down.
  - Wake-up from deep-sleep modes due to activity on the USART, SPI, and I2C peripherals when operating as slaves.
  - Ultra-low power Micro-tick Timer, running from the Watchdog oscillator that can be used to wake up the device from low power modes.
  - Power-On Reset (POR).
  - Brown-Out Detect (BOD) with separate thresholds for interrupt and forced reset.
- Single power supply 1.71 V to 3.6 V.
- Power-On Reset (POR).
- Brown-Out Detect (BOD) with separate thresholds for interrupt and forced reset.
- JTAG boundary scan supported.
- 128 bit unique device serial number for identification.
- Operating temperature range −40 °C to +105 °C.
- Available in TFBGA180, TFBGA100, LQFP208, and LQFP100 packages.

3. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
LPC54605J256ET180	TFBGA180	thin fine-pitch ball grid array package; 180 balls; body 12 ´ 12 ´ 0.8 mm	SOT570-3
LPC54605J512ET180	TFBGA180	thin fine-pitch ball grid array package; 180 balls; body 12 ´ 12 ´ 0.8 mm	SOT570-3
LPC54605J256BD100	LQFP100	plastic low profile quad flat package; 100 leads; body 14 × 14 × 1.4 mm	SOT407-1
LPC54605J512BD100	LQFP100	plastic low profile quad flat package; 100 leads; body 14 × 14 × 1.4 mm	SOT407-1
LPC54605J256ET100	TFBGA100	plastic thin fine-pitch ball grid array package; 100 balls; body 9 × 9 × 0.7 mm	SOT926-1
LPC54605J512ET100	TFBGA100	plastic thin fine-pitch ball grid array package; 100 balls; body 9 × 9 × 0.7 mm	SOT926-1
LPC54606J256ET100	TFBGA100	plastic thin fine-pitch ball grid array package; 100 balls; body 9 × 9 × 0.7 mm	SOT926-1
LPC54606J256BD100	LQFP100	plastic low profile quad flat package; 100 leads; body 14 × 14 × 1.4 mm	SOT407-1
LPC54606J256ET180	TFBGA180	thin fine-pitch ball grid array package; 180 balls; body 12 ´ 12 ´ 0.8 mm	SOT570-3
LPC54606J512ET100	TFBGA100	plastic thin fine-pitch ball grid array package; 100 balls; body 9 × 9 × 0.7 mm	SOT926-1
LPC54606J512BD100	LQFP100	plastic low profile quad flat package; 100 leads; body 14 × 14 × 1.4 mm	SOT407-1
LPC54606J512BD208	LQFP208	plastic low profile quad flat package; 208 leads; body 28 × 28 × 1.4 mm	SOT459-1
LPC54607J256ET180	TFBGA180	thin fine-pitch ball grid array package; 180 balls; body 12 ´ 12 ´ 0.8 mm	SOT570-3
LPC54607J512ET180	TFBGA180	thin fine-pitch ball grid array package; 180 balls; body 12 ´ 12 ´ 0.8 mm	SOT570-3
LPC54607J256BD208	LQFP208	plastic low profile quad flat package; 208 leads; body 28 × 28 × 1.4 mm	SOT459-1
LPC54608J512ET180	TFBGA180	thin fine-pitch ball grid array package; 180 balls; body 12 ´ 12 ´ 0.8 mm	SOT570-3
LPC54608J512BD208	LQFP208	plastic low profile quad flat package; 208 leads; body 28 × 28 × 1.4 mm	SOT459-1
LPC54616J256ET180	TFBGA180	thin fine-pitch ball grid array package; 180 balls; body 12 ´ 12 ´ 0.8 mm	SOT570-3
LPC54616J512ET100	TFBGA100	plastic thin fine-pitch ball grid array package; 100 balls; body 9 × 9 × 0.7 mm	SOT926-1
LPC54616J512BD100	LQFP100	plastic low profile quad flat package; 100 leads; body 14 × 14 × 1.4 mm	SOT407-1
LPC54616J512BD208	LQFP208	plastic low profile quad flat package; 208 leads; body 28 × 28 × 1.4 mm	SOT459-1
LPC54618J512ET180	TFBGA180	thin fine-pitch ball grid array package; 180 balls; body 12 ´ 12 ´ 0.8 mm	SOT570-3
LPC54618J512BD208	LQFP208	plastic low profile quad flat package; 208 leads; body 28 × 28 × 1.4 mm	SOT459-1
LPC54628J512ET180	TFBGA180	thin fine-pitch ball grid array package; 180 balls; body 12 ´ 12 ´ 0.8 mm	SOT570-3

3.1 Ordering options

Table 2. Ordering options

Type number	Package Name	Frequency/MHz	Flash/kB	SRAM/kB	FS USB	HS USB	Ethernet AVB	Classic CAN	CAN FD	LCD	Flexcomm Interface	EMC data bus width (bit)	GPIO	SHA
LPC54628 devices (HS/FS USB, Ethernet, CAN FD, CAN 2.0, LCD, SHA)														
LPC54628J512ET180	TFBGA180	220	512	200	yes	yes	yes	yes	yes	yes	10	8/16	145	yes
LPC54618 devices (HS/FS USB, Ethernet, CAN FD, CAN 2.0, LCD)														
LPC54618J512ET180	TFBGA180	180	512	200	yes	yes	yes	yes	yes	yes	10	8/16	145	no
LPC54618J512BD208	LQFP208	180	512	200	yes	yes	yes	yes	yes	yes	10	8/16/32	171	no
LPC54616 devices (HS/FS USB, Ethernet, CAN FD, CAN 2.0)														
LPC54616J256ET180	TFBGA180	180	256	136	yes	yes	yes	yes	yes	no	10	8/16	145	no
LPC54616J512BD208	LQFP208	180	512	200	yes	yes	yes	yes	yes	no	10	8/16/32	171	no
LPC54616J512ET100	TFBGA100	180	512	200	yes	yes	yes	yes	yes	no	9	8/16	64	no
LPC54616J512BD100	LQFP100	180	512	200	yes	yes	yes	yes	yes	no	9	8/16	64	no
LPC54608 devices (HS/FS USB, Ethernet, CAN 2.0, LCD)														
LPC54608J512ET180	TFBGA180	180	512	200	yes	yes	yes	yes	no	yes	10	8/16	145	no
LPC54608J512BD208	LQFP208	180	512	200	yes	yes	yes	yes	no	yes	10	8/16/32	171	no
LPC54607 devices (HS/FS USB, LCD)														
LPC54607J256ET180	TFBGA180	180	256	136	yes	yes	no	no	no	yes	10	8/16	145	no
LPC54607J512ET180	TFBGA180	180	512	200	yes	yes	no	no	no	yes	10	8/16	145	no
LPC54607J256BD208	LQFP208	180	256	136	yes	yes	no	no	no	yes	10	8/16/32	171	no
LPC54606 devices (HS/FS USB, Ethernet, CAN 2.0)														
LPC54606J256ET180	TFBGA180	180	256	136	yes	yes	yes	yes	no	no	10	8/16	145	no
LPC54606J512BD208	LQFP208	180	512	200	yes	yes	yes	yes	no	no	10	8/16/32	171	no
LPC54606J256ET100	TFBGA100	180	256	136	yes	yes	yes	yes	no	no	9	8/16	64	no
LPC54606J512ET100	TFBGA100	180	512	200	yes	yes	yes	yes	no	no	9	8/16	64	no
LPC54606J256BD100	LQFP100	180	256	136	yes	yes	yes	yes	no	no	9	8/16	64	no
LPC54606J512BD100	LQFP100	180	512	200	yes	yes	yes	yes	no	no	9	8/16	64	no
LPC54605 devices (HS/FS USB)														
LPC54605J256ET180	TFBGA180	180	256	136	yes	yes	no	no	no	no	10	8/16	145	no
LPC54605J512ET180	TFBGA180	180	512	200	yes	yes	no	no	no	no	10	8/16	145	no
LPC54605J256BD100	LQFP100	180	256	136	yes	yes	no	no	no	no	9	8/16	64	no
LPC54605J512BD100	LQFP100	180	512	200	yes	yes	no	no	no	no	9	8/16	64	no
LPC54605J256ET100	TFBGA100	180	256	136	yes	yes	no	no	no	no	9	8/16	64	no
LPC54605J512ET100	TFBGA100	180	512	200	yes	yes	no	no	no	no	9	8/16	64	no

4. Marking

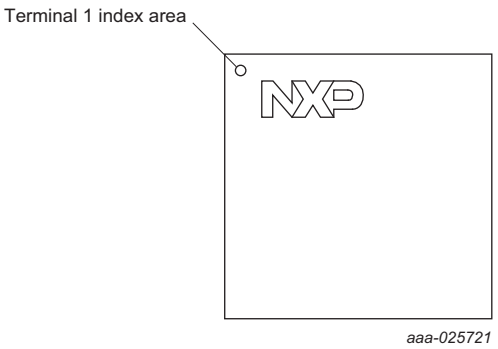

Fig 1. TFBGA180 and TFBGA100 package markings

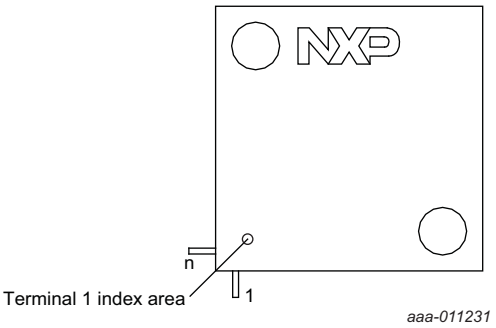

Fig 2. LQFP208 package marking

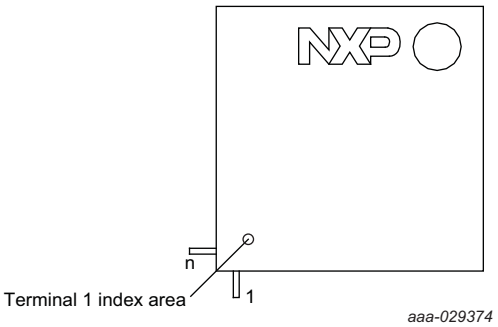

Fig 3. LQFP100 package marking

The LPC546xx TFBGA180 and TFBGA100 packages have the following top-side marking:

- First line: LPC546xxJyyy
  - yyy: flash size
- Second line: ET180 or ET100
- Third line: xxxxxxxxxxxx
- Fourth line: xxxyywwx[R]x
  - yyww: Date code with yy = year and ww = week.
  - xR = boot code version and device revision.

The LPC546xx LQFP208 and LQFP100 packages have the following top-side marking:

- First line: LPC546xxJyyy
  - yyy: flash size
- Second line: BD208 or BD100
- Third line: xxxxxxxxxxxx
- Fourth line: xxxyywwx[R]x

– yyww: Date code with yy = year and ww = week.
– xR = Boot code version and device revision.

Table 3. Device revision table

Revision identifier (R)	Revision description
1A	Initial device revision with Boot ROM version 19.1

5. Block diagram

Figure 4 shows the LPC546xx block diagram. In this figure, orange shaded blocks support general purpose DMA and yellow shaded blocks include dedicated DMA control.

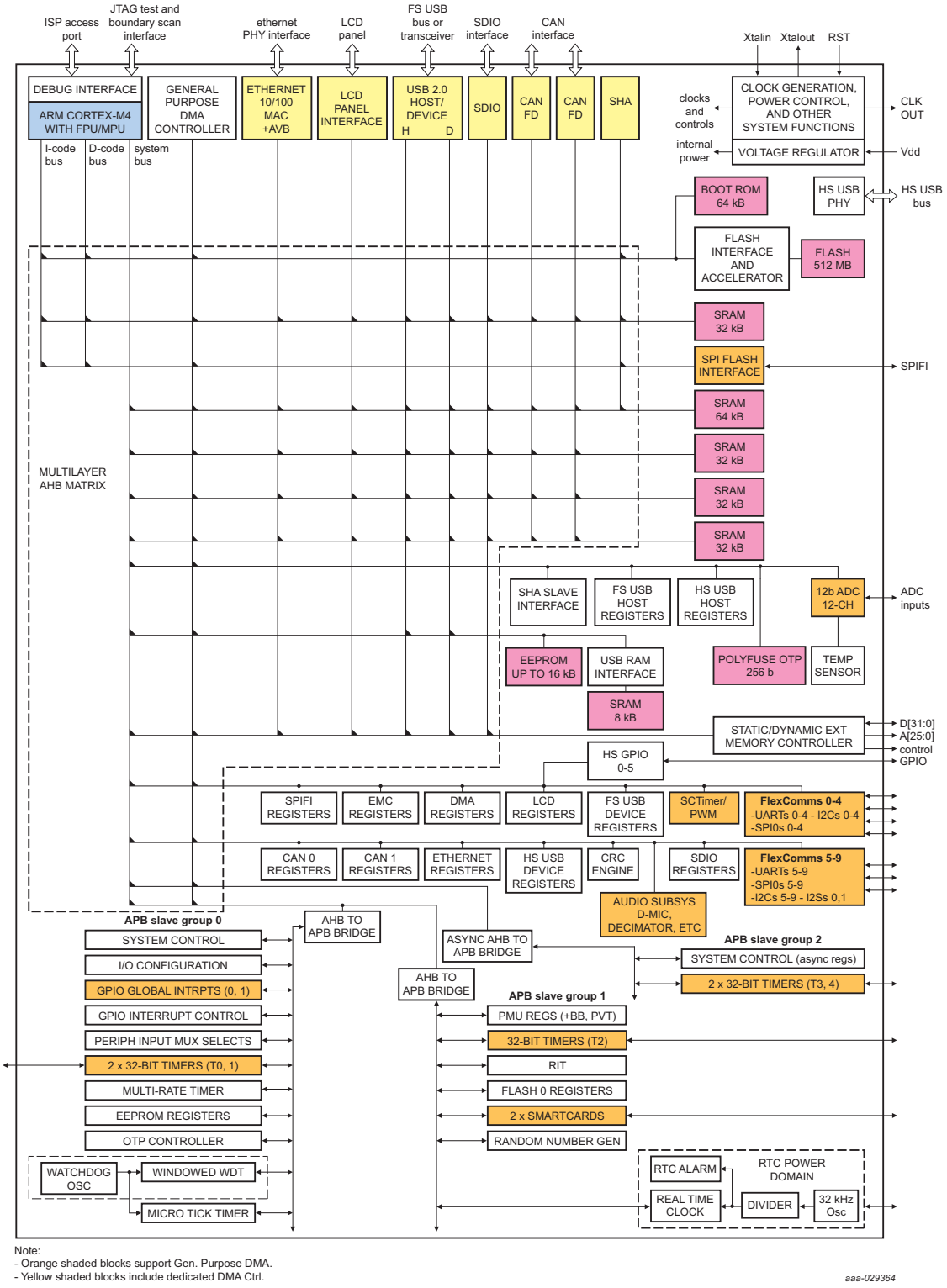

Fig 4. LPC546xx Block diagram

6. Pinning information

6.1 Pinning

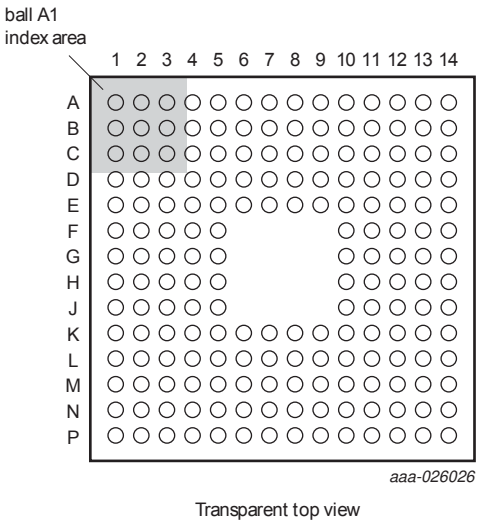

Fig 5. TFBGA 180 Pin configuration

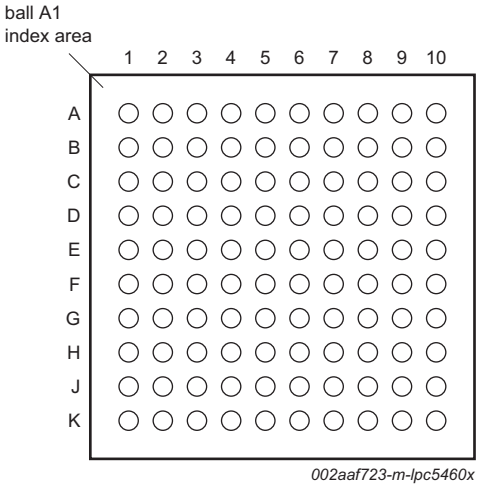

Fig 6. TFBGA 100 Pin configuration

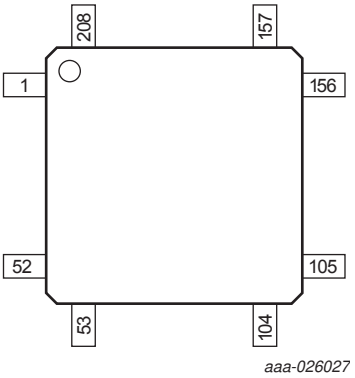

Fig 7. LQFP 208 Pin configuration

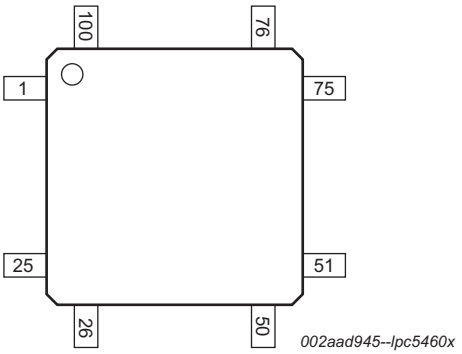

Fig 8. LQFP 100 Pin configuration

6.2 Pin description

On the LPC546xx, digital pins are grouped into several ports. Each digital pin can support several different digital functions (including General Purpose I/O (GPIO)) and an additional analog function.

Table 4. Pin description

Symbol	100-pin, TFBGA	180-pin, TFBGA	208-pin, LQFP	100-pin, LQFP		Reset state [1]	Type	Description
PIO0_0	C4	D6	196	93	[2]	PU	I/O	**PIO0_0 —** General-purpose digital input/output pin. **Remark:** In ISP mode, this pin is set to the Flexcomm 3 SPI SCK function.
							I	**CAN1_RD —** Receiver input for CAN 1.
							I/O	**FC3_SCK —** Flexcomm 3: USART or SPI clock.
							O	**CTimer_MAT0 —** Match output 0 from Timer 0.
							I	**SCT0_GPI0 —** Pin input 0 to SCTimer/PWM.
							O	**PDM0_CLK —** Clock for PDM interface 0, for digital microphone.
PIO0_1	A1	A1	207	100	[2]	PU	I/O	**PIO0_1 —** General-purpose digital input/output pin. **Remark:** In ISP mode, this pin is set to the Flexcomm 3 SPI SSEL0 function.
							O	**CAN1_TD —** Transmitter output for CAN 1.
							I/O	**FC3_CTS_SDA_SSEL0 —** Flexcomm 3: USART clear-to-send, I2C data I/O, SPI Slave Select 0.
							I	**CT0_CAP0 —** Capture input 0 to Timer 0.
							I	**SCT0_GPI1 —** Pin input 1 to SCTimer/PWM.
							I	**PDM0_DATA —** Data for PDM interface 0 (digital microphone).
PIO0_2/ TRST	A7	E9	174	83	[2]	PU	I/O	**PIO0_2 —** General-purpose digital input/output pin. In boundary scan mode: TRST (Test Reset). **Remark:** In ISP mode, this pin is set to the Flexcomm 3 SPI MISO function.
							I/O	**FC3_TXD_SCL_MISO —** Flexcomm 3: USART transmitter, I2C clock, SPI master-in/slave-out data.
							I	**CT0_CAP1 —** Capture input 1 to Timer 0.
							O	**SCT0_OUT0 —** SCTimer/PWM output 0.
							I	**SCT0_GPI[2] —** Pin input 2 to SCTimer/PWM.
							I/O	**EMC_D[0] —** External Memory interface data [0].

Table 4. Pin description *...continued*

Symbol	100-pin, TFBGA	180-pin, TFBGA	208-pin, LQFP	100-pin, LQFP		Reset state [1]	Type	Description
PIO0_3/ TCK	A6	A10	178	85	[2]	PU	I/O	**PIO0_3 —** General-purpose digital input/output pin. In boundary scan mode: TCK (Test Clock In). **Remark:** In ISP mode, this pin is set to the Flexcomm 3 SPI MOSI function.
							I/O	**FC3_RXD_SDA_MOSI —** Flexcomm 3: USART receiver, I2C data I/O, SPI master-out/slave-in data.
							O	**CT0_MAT1 —** Match output 1 from Timer 0.
							O	**SCT0_OUT1 —** SCTimer/PWM output 1.
							I	**SCT0_GPI3 —** Pin input 3 to SCTimer/PWM.
								R — Reserved.
							I/O	**EMC_D[1] —** External Memory interface data [1].
PIO0_4/ TMS	B6	C8	185	87	[2]	PU	I/O	**PIO0_4 —** General-purpose digital input/output pin. In boundary scan mode: TMS (Test Mode Select). **Remark:** The state of this pin at Reset in conjunction with PIO0_5 and PIO0_6 will determine the boot source for the part or if ISP handler is invoked. See the Boot Process chapter in UM10912 for more details.
							I	**CAN0_RD —** Receiver input for CAN 0.
							I/O	**FC4_SCK —** Flexcomm 4: USART or SPI clock.
							I	**CT3_CAP0 —** Capture input 0 to Timer 3.
							I	**SCT0_GPI4 —** Pin input 4 to SCTimer/PWM.
								R — Reserved.
							I/O	**EMC_D[2] —** External Memory interface data [2].
							O	**ENET_MDC —** Ethernet management data clock.
PIO0_5/ TDI	A5	E7	189	89	[2]	PU	I/O	**PIO0_5 —** General-purpose digital input/output pin. In boundary scan mode: TDI (Test Data In). **Remark:** The state of this pin at Reset in conjunction with PIO0_4 and PIO0_6 will determine the boot source for the part or if ISP handler is invoked. See the Boot Process chapter in UM10912 for more details.
							O	**CAN0_TD —** Transmitter output for CAN 0.
							I/O	**FC4_RXD_SDA_MOSI —** Flexcomm 4: USART receiver, I2C data I/O, SPI master-out/slave-in data.
							O	**CT3_MAT0 —** Match output 0 from Timer 3.
							I	**SCT0_GPI5 —** Pin input 5 to SCTimer/PWM.
								R — Reserved.
							I/O	**EMC_D[3] —** External Memory interface data [3].
							I/O	**ENET_MDIO —** Ethernet management data I/O.

Table 4. Pin description *...continued*

Symbol	100-pin, TFBGA	180-pin, TFBGA	208-pin, LQFP	100-pin, LQFP		Reset state [1]	Type	Description
PIO0_6/ TDO	A4	A5	191	90	[2]	PU	I/O	**PIO0_6 —** General-purpose digital input/output pin. In boundary scan mode: TDO (Test Data Out). **Remark:** The state of this pin at Reset in conjunction with PIO0_4 and PIO0_5 will determine the boot source for the part or if ISP handler is invoked. See the Boot Process chapter in UM10912 for more details.
							I/O	**FC3_SCK —** Flexcomm 3: USART or SPI clock.
							I	**CT3_CAP1 —** Capture input 1 to Timer 3.
							O	**CT4_MAT0 —** Match output 0 from Timer 4.
							I	**SCT0_GPI6 —** Pin input 6 to SCTimer/PWM.
								R — Reserved.
							I/O	**EMC_D[4] —** External Memory interface data [4].
							I	**ENET_RX_DV —** Ethernet receive data valid.
PIO0_7	F9	H12	125	61	[2]	PU	I/O	**PIO0_7 —** General-purpose digital input/output pin.
							I/O	**FC3_RTS_SCL_SSEL1 —** Flexcomm 3: USART request-to-send, I2C clock, SPI slave select 1.
							O	**SD_CLK —** SD/MMC clock.
							I/O	**FC5_SCK —** Flexcomm 5: USART or SPI clock.
							I/O	**FC1_SCK —** Flexcomm 1: USART or SPI clock.
							O	**PDM1_CLK —** Clock for PDM interface 1, for digital microphone.
							I/O	**EMC_D[5] —** External Memory interface data [5].
							I	**ENET_RX_CLK —** Ethernet Receive Clock (MII interface) or Ethernet Reference Clock (RMII interface).
PIO0_8	E9	H10	133	64	[2]	PU	I/O	**PIO0_8 —** General-purpose digital input/output pin.
							I/O	**FC3_SSEL3 —** Flexcomm 3: SPI slave select 3.
							I/O	**SD_CMD —** SD/MMC card command I/O.
							I/O	**FC5_RXD_SDA_MOSI —** Flexcomm 5: USART receiver, I2C data I/O, SPI master-out/slave-in data.
							O	**SWO —** Serial Wire Debug trace output.
							I	**PDM1_DATA —** Data for PDM interface 1 (digital microphone).
							I/O	**EMC_D[6] —** External Memory interface data [6].

Table 4. Pin description *...continued*

Symbol	100-pin, TFBGA	180-pin, TFBGA	208-pin, LQFP	100-pin, LQFP		Reset state [1]	Type	Description
PIO0_9	E10	G12	136	65	[2]	PU	I/O	**PIO0_9 —** General-purpose digital input/output pin.
							I/O	**FC3_SSEL2 —** Flexcomm 3: SPI slave select 2.
							O	**SD_POW_EN —** SD/MMC card power enable.
							I/O	**FC5_TXD_SCL_MISO —** Flexcomm 5: USART transmitter, I2C clock, SPI master-in/slave-out data.
								R — Reserved.
							I/O	**SCI1_IO —** SmartCard Interface 1 data I/O.
							I/O	**EMC_D[7] —** External Memory interface data [7].
PIO0_10/ ADC0_0	J1	P2	50	23	[4]	PU	I/O; AI	**PIO0_10/ADC0_0 —** General-purpose digital input/output pin. ADC input channel 0 if the DIGIMODE bit is set to 0 in the IOCON register for this pin.
							I/O	**FC6_SCK —** Flexcomm 6: USART, SPI, or I2S clock.
							I	**CT2_CAP2 —** Capture input 2 to Timer 2.
							O	**CT2_MAT0 —** Match output 0 from Timer 2.
							I/O	**FC1_TXD_SCL_MISO —** Flexcomm 1: USART transmitter, I2C clock, SPI master-in/slave-out data.
								R — Reserved.
							O	**SWO —** Serial Wire Debug trace output.
PIO0_11/ ADC0_1	K1	L3	51	24	[4]	PU	I/O; AI	**PIO0_11/ADC0_1 —** General-purpose digital input/output pin. ADC input channel 1 if the DIGIMODE bit is set to 0 in the IOCON register for this pin.
							I/O	**FC6_RXD_SDA_MOSI_DATA —** Flexcomm 6: USART receiver, I2C data I/O, SPI master-out/slave-in data, I2S data I/O.
							O	**CT2_MAT2 —** Match output 2 from Timer 2.
							I	**FREQME_GPIO_CLK_A —** Frequency Measure pin clock input A.
								R — Reserved.
								R — Reserved.
							I	**SWCLK —** Serial Wire Debug clock. This is the default function after booting.

Table 4. Pin description *...continued*

Symbol	100-pin, TFBGA	180-pin, TFBGA	208-pin, LQFP	100-pin, LQFP		Reset state [1]	Type	Description
PIO0_12/ ADC0_2	J2	M3	52	25	[4]	PU	I/O; AI	**PIO0_12/ADC0_2 —** General-purpose digital input/output pin. ADC input channel 2 if the DIGIMODE bit is set to 0 in the IOCON register for this pin.
							I/O	**FC3_TXD_SCL_MISO —** Flexcomm 3: USART transmitter, I2C clock, SPI master-in/slave-out data.
								R — Reserved.
							I	**FREQME_GPIO_CLK_B —** Frequency Measure pin clock input B.
							I	**SCT0_GPI7 —** Pin input 7 to SCTimer/PWM.
								R — Reserved.
							I/O	**SWDIO —** Serial Wire Debug I/O. This is the default function after booting.
PIO0_13	C10	F11	141	67	[3]	Z	I/O	**PIO0_13 —** General-purpose digital input/output pin. **Remark:** In ISP mode, this pin is set to the Flexcomm 1 I2C SDA function.
							I/O	**FC1_CTS_SDA_SSEL0 —** Flexcomm 1: USART clear-to-send, I2C data I/O, SPI Slave Select 0.
							I	**UTICK_CAP0 —** Micro-tick timer capture input 0.
							I	**CT0_CAP0 —** Capture input 0 to Timer 0.
							I	**SCT0_GPI0 —** Pin input 0 to SCTimer/PWM.
								R — Reserved.
								R — Reserved.
							I	**ENET_RXD0 —** Ethernet receive data 0.
PIO0_14	D9	E13	144	69	[3]	Z	I/O	**PIO0_14 —** General-purpose digital input/output pin. **Remark:** In ISP mode, this pin is set to the Flexcomm 1 I2C SCL function.
							I/O	**FC1_RTS_SCL_SSEL1 —** Flexcomm 1: USART request-to-send, I2C clock, SPI slave select 1.
							I	**UTICK_CAP1 —** Micro-tick timer capture input 1.
							I	**CT0_CAP1 —** Capture input 1 to Timer 0.
							I	**SCT0_GPI1 —** Pin input 1 to SCTimer/PWM.
								R — Reserved.
								R — Reserved.
							I	**ENET_RXD1 —** Ethernet receive data 1.

Table 4. Pin description *...continued*

Symbol	100-pin, TFBGA	180-pin, TFBGA	208-pin, LQFP	100-pin, LQFP		Reset state [1]	Type	Description
PIO0_15/ ADC0_3	K2	L4	53	26	[4]	PU	I/O; AI	**PIO0_15/ADC0_3 —** General-purpose digital input/output pin. ADC input channel 3 if the DIGIMODE bit is set to 0 in the IOCON register for this pin.
							I/O	**FC6_CTS_SDA_SSEL0 —** Flexcomm 6: USART clear-to-send, I2C data I/O, SPI Slave Select 0.
							I	**UTICK_CAP2 —** Micro-tick timer capture input 2.
							I	**CT4_CAP0 —** Capture input 4 to Timer 0.
							O	**SCT0_OUT2 —** SCTimer/PWM output 2.
								R — Reserved.
							O	**EMC_WEN —** External memory interface Write Enable (active low).
							O	**ENET_TX_EN —** Ethernet transmit enable (RMII/MII interface).
PIO0_16/ ADC0_4	H3	M4	54	27	[4]	PU	I/O; AI	**PIO0_16/ADC0_4 —** General-purpose digital input/output pin. ADC input channel 4 if the DIGIMODE bit is set to 0 in the IOCON register for this pin.ws
							I/O	**FC4_TXD_SCL_MISO —** Flexcomm 4: USART transmitter, I2C clock, SPI master-in/slave-out data.
							O	**CLKOUT —** Output of the CLKOUT function.
							I	**CT1_CAP0 —** Capture input 0 to Timer 1.
								R — Reserved.
								R — Reserved.
							O	**EMC_CSN[0] —** External memory interface static chip select 0 (active low).
							O	**ENET_TXD0 —** Ethernet transmit data 0.
PIO0_17	B10	E14	146	70	[2]	PU	I/O	**PIO0_17 —** General-purpose digital input/output pin.
							I/O	**FC4_SSEL2 —** Flexcomm 4: SPI slave select 2.
							I	**SD_CARD_DET_N —** SD/MMC card detect (active low).
							I	**SCT0_GPI7 —** Pin input 7 to SCTimer/PWM.
							O	**SCT0_OUT0 —** SCTimer/PWM output 0.
								R — Reserved.
							O	**EMC_OEN —** External memory interface output enable (active low)
							O	**ENET_TXD1 —** Ethernet transmit data 1.

Table 4. Pin description *...continued*

Symbol	100-pin, TFBGA	180-pin, TFBGA	208-pin, LQFP	100-pin, LQFP		Reset state [1]	Type	Description
PIO0_18	C9	C14	150	72	[2]	PU	I/O	**PIO0_18 —** General-purpose digital input/output pin.
							I/O	**FC4_CTS_SDA_SSEL0 —** Flexcomm 4: USART clear-to-send, I2C data I/O, SPI Slave Select 0.
							I	**SD_WR_PRT —** SD/MMC write protect.
							O	**CT1_MAT0 —** Match output 0 from Timer 1.
							O	**SCT0_OUT1 —** SCTimer/PWM output 1.
							O	**SCI1_SCLK —** SmartCard Interface 1 clock.
							O	**EMC_A[0] —** External memory interface address 0.
PIO0_19	C5	C6	193	91	[2]	PU	I/O	**PIO0_19 —** General-purpose digital input/output pin.
							I/O	**FC4_RTS_SCL_SSEL1 —** Flexcomm 4: USART request-to-send, I2C clock, SPI slave select 1.
							I	**UTICK_CAP0 —** Micro-tick timer capture input 0.
							O	**CT0_MAT2 —** Match output 2 from Timer 0.
							O	**SCT0_OUT2 —** SCTimer/PWM output 2.
								R — Reserved.
							O	**EMC_A[1] —** External memory interface address 1.
							I/O	**FC7_TXD_SCL_MISO_WS —** Flexcomm 7: USART transmitter, I2C clock, SPI master-in/slave-out data I/O, I2S word-select/frame.
PIO0_20	C8	D13	153	74	[2]	PU	I/O	**PIO0_20 —** General-purpose digital input/output pin.
							I/O	**FC3_CTS_SDA_SSEL0 —** Flexcomm 3: USART clear-to-send, I2C data I/O, SPI Slave Select 0.
							O	**CT1_MAT1 —** Match output 1 from Timer 1.
							I	**CT3_CAP3 —** Capture input 3 to Timer 3.
							I	**SCT0_GPI2 —** Pin input 2 to SCTimer/PWM.
							I/O	**SCI0_IO —** SmartCard Interface 0 data I/O.
							O	**EMC_A[2] —** External memory interface address 2.
							I/O	**FC7_RXD_SDA_MOSI_DATA —** Flexcomm 7: USART receiver, I2C data I/O, SPI master-out/slave-in data, I2S data I/O.
PIO0_21	B9	C13	158	77	[2]	PU	I/O	**PIO0_21 —** General-purpose digital input/output pin.
							I/O	**FC3_RTS_SCL_SSEL1 —** Flexcomm 3: USART request-to-send, I2C clock, SPI slave select 1.
							I	**UTICK_CAP3 —** Micro-tick timer capture input 3.
							O	**CT3_MAT3 —** Match output 3 from Timer 3.
							I	**SCT0_GPI3 —** Pin input 3 to SCTimer/PWM.
							O	**SCI0_SCLK —** SmartCard Interface 0 clock.
							O	**EMC_A[3] —** External memory interface address 3.
							I/O	**FC7_SCK —** Flexcomm 7: USART, SPI, or I2S clock.

Table 4. Pin description *...continued*

Symbol	100-pin, TFBGA	180-pin, TFBGA	208-pin, LQFP	100-pin, LQFP		Reset state [1]	Type	Description
PIO0_22	B8	B12	163	80	[2][8]	PU	I/O	**PIO0_22 —** General-purpose digital input/output pin.
							I/O	**FC6_TXD_SCL_MISO_WS —** Flexcomm 6: USART transmitter, I2C clock, SPI master-in/slave-out data I/O, I2S word-select/frame.
							I	**UTICK_CAP1 —** Micro-tick timer capture input 1.
							I	**CT3_CAP3 —** Capture input 3 to Timer 3.
							O	**SCT0_OUT3 —** SCTimer/PWM output 3.
								R — Reserved.
								R — Reserved.
							I	**USB0_VBUS —** Monitors the presence of USB0 bus power.
PIO0_23/ ADC0_11	K5	N7	71	35	[4]	PU	I/O; AI	**PIO0_23/ADC0_11 —** General-purpose digital input/output pin. ADC input channel 11 if the DIGIMODE bit is set to 0 in the IOCON register for this pin.
							I/O	**MCLK —** MCLK input or output for I2S and/or digital microphone.
							O	**CT1_MAT2 —** Match output 2 from Timer 1.
							O	**CT3_MAT3 —** Match output 3 from Timer 3.
							O	**SCT0_OUT4 —** SCTimer/PWM output 4.
								R — Reserved.
							I/O	**SPIFI_CSN —** SPI Flash Interface chip select (active low).
PIO0_24	J5	M7	76	38	[2]	PU	I/O	**PIO0_24 —** General-purpose digital input/output pin.
							I/O	**FC0_RXD_SDA_MOSI —** Flexcomm 0: USART receiver, I2C data I/O, SPI master-out/slave-in data.
							I/O	**SD_D[0] —** SD/MMC data 0.
							I	**CT2_CAP0 —** Capture input 0 to Timer 2.
							I	**SCT0_GPI0 —** Pin input 0 to SCTimer/PWM.
								R — Reserved.
							I/O	**SPIFI_IO0 —** Data bit 0 for the SPI Flash Interface.
PIO0_25	J6	K8	83	40	[2]	PU	I/O	**PIO0_25 —** General-purpose digital input/output pin.
							I/O	**FC0_TXD_SCL_MISO —** Flexcomm 0: USART transmitter, I2C clock, SPI master-in/slave-out data.
							I/O	**SD_D[1] —** SD/MMC data 1.
							I	**CT2_CAP1 —** Capture input 1 to Timer 2.
							I	**SCT0_GPI1 —** Pin input 1 to SCTimer/PWM.
								R — Reserved.
							I/O	**SPIFI_IO1 —** Data bit 1 for the SPI Flash Interface.

Table 4. Pin description *...continued*

Symbol	100-pin, TFBGA	180-pin, TFBGA	208-pin, LQFP	100-pin, LQFP		Reset state [1]	Type	Description
PIO0_26	H10	M13	110	56	[2]	PU	I/O	**PIO0_26 —** General-purpose digital input/output pin.
							I/O	**FC2_RXD_SDA_MOSI —** Flexcomm 2: USART receiver, I2C data I/O, SPI master-out/slave-in data.
							O	**CLKOUT —** Output of the CLKOUT function.
							I	**CT3_CAP2 —** Capture input 2 to Timer 3.
							O	**SCT0_OUT5 —** SCTimer/PWM output 5.
							O	**PDM0_CLK —** Clock for PDM interface 0, for digital microphone.
							O	**SPIFI_CLK —** Clock output for the SPI Flash Interface.
							I	**USB0_IDVALUE —** Indicates to the transceiver whether connected as an A-device (USB0_ID LOW) or B-device (USB0_ID HIGH).
PIO0_27	H7	L9	87	42	[2]	PU	I/O	**PIO0_27 —** General-purpose digital input/output pin.
							I/O	**FC2_TXD_SCL_MISO —** Flexcomm 2: USART transmitter, I2C clock, SPI master-in/slave-out data.
								R — Reserved.
							O	**CT3_MAT2 —** Match output 2 from Timer 3.
							O	**SCT0_OUT6 —** SCTimer/PWM output 6.
							I	**PDM0_DATA —** Data for PDM interface 0 (digital microphone).
							I/O	**SPIFI_IO3 —** Data bit 3 for the SPI Flash Interface.
PIO0_28	J7	M9	91	44	[2]	PU	I/O	**PIO0_28 —** General-purpose digital input/output pin.
							I/O	**FC0_SCK —** Flexcomm 0: USART or SPI clock.
								R — Reserved.
							I	**CT2_CAP3 —** Capture 3 input to Timer 2.
							O	**SCT0_OUT7 —** SCTimer/PWM output 7.
							O	**TRACEDATA[3] —** Trace data bit 3.
							I/O	**SPIFI_IO2 —** Data bit 2 for the SPI Flash Interface.
							I	**USB0_OVERCURRENTN —** USB0 bus overcurrent indicator (active low).
PIO0_29	B7	B13	167	82	[2]	PU	I/O	**PIO0_29 —** General-purpose digital input/output pin. **Remark:** In ISP mode, this pin is set to the Flexcomm 0 USART RXD function.
							I/O	**FC0_RXD_SDA_MOSI —** Flexcomm 0: USART receiver, I2C data I/O, SPI master-out/slave-in data.
								R — Reserved.
							O	**CT2_MAT3 —** Match output 3 from Timer 2.
							O	**SCT0_OUT8 —** SCTimer/PWM output 8.
							O	**TRACEDATA[2] —** Trace data bit 2.

Table 4. Pin description *...continued*

Symbol	100-pin, TFBGA	180-pin, TFBGA	208-pin, LQFP	100-pin, LQFP		Reset state [1]	Type	Description
PIO0_30	A2	A2	200	95	[2]	PU	I/O	**PIO0_30 —** General-purpose digital input/output pin. **Remark:** In ISP mode, this pin is set to the Flexcomm 0 USART TXD function.
							I/O	**FC0_TXD_SCL_MISO —** Flexcomm 0: USART transmitter, I2C clock, SPI master-in/slave-out data.
								R — Reserved.
							O	**CT0_MAT0 —** Match output 0 from Timer 0.
							O	**SCT0_OUT9 —** SCTimer/PWM output 9.
							O	**TRACEDATA[1] —** Trace data bit 1.
PIO0_31/ ADC0_5	K3	M5	55	28	[4]	PU	I/O; AI	**PIO0_31/ADC0_5 —** General-purpose digital input/output pin. ADC input channel 5 if the DIGIMODE bit is set to 0 in the IOCON register for this pin.
							I/O	**FC0_CTS_SDA_SSEL0 —** Flexcomm 0: USART clear-to-send, I2C data I/O, SPI Slave Select 0.
							I/O	**SD_D[2] —** SD/MMC data 2.
							O	**CT0_MAT1 —** Match output 1 from Timer 0.
							O	**SCT0_OUT3 —** SCTimer/PWM output 3.
							O	**TRACEDATA[0] —** Trace data bit 0.
PIO1_0/ ADC0_6	J3	N3	56	29	[4]	PU	I/O; AI	**PIO1_0/ADC0_6 —** General-purpose digital input/output pin. ADC input channel 6 if the DIGIMODE bit is set to 0 in the IOCON register for this pin.
							I/O	**FC0_RTS_SCL_SSEL1 —** Flexcomm 0: USART request-to-send, I2C clock, SPI slave select 1.
							I/O	**SD_D[3] —** SD/MMC data 3.
							I	**CT0_CAP2 —** Capture 2 input to Timer 0.
							I	**SCT0_GPI4 —** Pin input 4 to SCTimer/PWM.
							O	**TRACECLK —** Trace clock.
PIO1_1	J10	K12	109	55	[2]	PU	I/O	**PIO1_1/ —** General-purpose digital input/output pin.
							I/O	**FC3_RXD_SDA_MOSI —** Flexcomm 3: USART receiver, I2C data I/O, SPI master-out/slave-in data.
								R — Reserved.
							I	**CT0_CAP3 —** Capture 3 input to Timer 0.
							I	**SCT0_GPI5 —** Pin input 5 to SCTimer/PWM.
								R — Reserved.
								R — Reserved.
							I	**USB1_OVERCURRENTN —** USB1 bus overcurrent indicator (active low).

Table 4. Pin description *...continued*

Symbol	100-pin, TFBGA	180-pin, TFBGA	208-pin, LQFP	100-pin, LQFP		Reset state [1]	Type	Description
PIO1_2	G9	L14	117	58	[2]	PU	I/O	**PIO1_2 —** General-purpose digital input/output pin.
							O	**CAN0_TD —** Transmitter output for CAN0.
								R — Reserved.
							O	**CT0_MAT3 —** Match output 3 from Timer0.
							I	**SCT0_GPI6 —** Pin input 6 to SCTimer/PWM.
							O	**PDM1_CLK —** Clock for PDM interface 1, for digital microphone.
								R — Reserved.
							O	**USB1_PORTPWRN —** USB1 VBUS drive indicator (Indicates VBUS must be driven).
PIO1_3	F10	J13	120	60	[2]	PU	I/O	**PIO1_3 —** General-purpose digital input/output pin.
							I	**CAN0_RD —** Receiver input for CAN0.
								R — Reserved.
								R — Reserved.
							O	**SCT0_OUT4 —** SCTimer/PWM output 4.
							I	**PDM1_DATA —** Data for PDM interface 1 (digital microphone).
							O	**USB0_PORTPWRN —** USB0 VBUS drive indicator (Indicates VBUS must be driven).
PIO1_4	C3	D4	3	3	[2]	PU	I/O	**PIO1_4 —** General-purpose digital input/output pin.
							I/O	**FC0_SCK —** Flexcomm 0: USART or SPI clock.
							I/O	**SD_D[0] —** SD/MMC data 0.
							O	**CT2_MAT1 —** Match output 1 from Timer 2.
							O	**SCT0_OUT0 —** SCTimer/PWM output 0.
							I	**FREQME_GPIO_CLK_A —** Frequency Measure pin clock input A.
							I/O	**EMC_D[11]) —** External Memory interface data [11].
PIO1_5	C2	E4	5	4	[2]	PU	I/O	**PIO1_5 —** General-purpose digital input/output pin.
							I/O	**FC0_RXD_SDA_MOSI —** Flexcomm 0: USART receiver, I2C data I/O, SPI master-out/slave-in data.
							I/O	**SD_D[2] —** SD/MMC data 2.
							O	**CT2_MAT0 —** Match output 0 from Timer 2.
							I	**SCT0_GPI0 —** Pin input 0 to SCTimer/PWM.
								R — Reserved.
							O	**EMC_A[4] —** External memory interface address 4.

Table 4. Pin description *...continued*

Symbol	100-pin, TFBGA	180-pin, TFBGA	208-pin, LQFP	100-pin, LQFP		Reset state [1]	Type	Description
PIO1_6	F1	G4	30	15	[2]	PU	I/O	**PIO1_6 —** General-purpose digital input/output pin.
							I/O	**FC0_TXD_SCL_MISO —** Flexcomm 0: USART transmitter, I2C clock, SPI master-in/slave-out data.
							I/O	**SD_D[3] —** SD/MMC data 3.
							O	**CT2_MAT1 —** Match output 1 from Timer 2.
							I	**SCT0_GPI3 —** Pin input 3 to SCTimer/PWM.
								R — Reserved.
							O	**EMC_A[5] —** External memory interface address 5.
PIO1_7	H1	N1	38	18	[2]	PU	I/O	**PIO1_7 —** General-purpose digital input/output pin.
							I/O	**FC0_RTS_SCL_SSEL1 —** Flexcomm 0: USART request-to-send, I2C clock, SPI slave select 1.
							I/O	**SD_D[1] —** SD/MMC data 1.
							O	**CT2_MAT2 —** Match output 2 from Timer 2.
							I	**SCT0_GPI4 —** Pin input 4 to SCTimer/PWM.
								R — Reserved.
							O	**EMC_A[6] —** External memory interface address 6.
PIO1_8	H5	P8	72	36	[2]	PU	I/O	**PIO1_8 —** General-purpose digital input/output pin.
							I/O	**FC0_CTS_SDA_SSEL0 —** Flexcomm 0: USART clear-to-send, I2C data I/O, SPI Slave Select 0.
							O	**SD_CLK —** SD/MMC clock.
								R — Reserved.
							O	**SCT0_OUT1 —** SCTimer/PWM output 1.
							I/O	**FC4_SSEL2 —** Flexcomm 4: SPI slave select 2.
							O	**EMC_A[7] —** External memory interface address 7.
PIO1_9	K7	K6	78	39	[2]	PU	I/O	**PIO1_9 —** General-purpose digital input/output pin.
							O	**ENET_TXD0 —** Ethernet transmit data 0.
							I/O	**FC1_SCK —** Flexcomm 1: USART or SPI clock.
							I	**CT1_CAP0 —** Capture 0 input to Timer 1.
							O	**SCT0_OUT2 —** SCTimer/PWM output 2.
							I/O	**FC4_CTS_SDA_SSEL0 —** Flexcomm 4: USART clear-to-send, I2C data I/O, SPI Slave Select 0.
							O	**EMC_CASN —** External memory interface column access strobe (active low).

Table 4. Pin description *...continued*

Symbol	100-pin, TFBGA	180-pin, TFBGA	208-pin, LQFP	100-pin, LQFP		Reset state [1]	Type	Description
PIO1_10	H6	N9	84	41	[2]	PU	I/O	**PIO1_10 —** General-purpose digital input/output pin.
							O	**ENET_TXD1 —** Ethernet transmit data 1.
							I/O	**FC1_RXD_SDA_MOSI —** Flexcomm 1: USART receiver, I2C data I/O, SPI master-out/slave-in data.
							O	**CT1_MAT0 —** Match output 0 from Timer 1.
							O	**SCT0_OUT3 —** SCTimer/PWM output 3.
								R — Reserved.
							O	**EMC_RASN —** External memory interface row address strobe (active low).
PIO1_11	B4	B4	198	94	[2][8]	PU	I/O	**PIO1_11 —** General-purpose digital input/output pin.
							O	**ENET_TX_EN —** Ethernet transmit enable (RMII/MII interface).
							I/O	**FC1_TXD_SCL_MISO —** Flexcomm 1: USART transmitter, I2C clock, SPI master-in/slave-out data.
							I	**CT1_CAP1 —** Capture 1 input to Timer 1.
							I	**USB0_VBUS —** Monitors the presence of USB0 bus power.
								R — Reserved.
							O	**EMC_CLK[0] —** External memory interface clock 0.
PIO1_12	F8	K9	128	62	[2]	PU	I/O	**PIO1_12 —** General-purpose digital input/output pin.
							I	**ENET_RXD0 —** Ethernet receive data 0.
							I/O	**FC6_SCK —** Flexcomm 6: USART, SPI, or I2S clock.
							O	**CT1_MAT1 —** Match output 1 from Timer 1.
							O	**USB0_PORTPWRN —** USB0 VBUS drive indicator (Indicates VBUS must be driven).
							O	**EMC_DYCSN[0] —** External Memory interface SDRAM chip select 0 (active low).
PIO1_13	D10	G10	139	66	[2]	PU	I/O	**PIO1_13 —** General-purpose digital input/output pin.
							I	**ENET_RXD1 —** Ethernet receive data 1.
							I/O	**FC6_RXD_SDA_MOSI_DATA —** Flexcomm 6: USART receiver, I2C data I/O, SPI master-out/slave-in data, I2S data I/O.
							I	**CT1_CAP2 —** Capture 2 input to Timer 1.
							I	**USB0_OVERCURRENTN —** USB0 bus overcurrent indicator (active low).
							O	**USB0_FRAME —** USB0 frame toggle signal.
							O	**EMC_DQM[0] —** External memory interface data mask 0.