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LPC804

32-bit Arm® Cortex®-M0+ microcontroller; up to 32 KB flash and 4 KB SRAM; 12-bit ADC; Comparator; 10-bit DAC; Capacitive Touch Interface; Programmable Logic Unit

Rev. 1.4 — 12 July 2018 Product data sheet

1. General description

The LPC804 are an Arm Cortex-M0+ based, low-cost 32-bit MCU family operating at CPU frequencies of up to 15 MHz. The LPC804 supports 32 KB of flash memory and 4 KB of SRAM.

The peripheral complement of the LPC804 includes a CRC engine, two I^2C-bus interfaces, up to two USARTs, one SPI interface, Capacitive Touch Interface (Cap Touch), one multi-rate timer, self-wake-up timer, one general purpose 32-bit counter/timer, one 12-bit ADC, one 10-bit DAC, one analog comparator, function-configurable I/O ports through a switch matrix, an input pattern match engine, Programmable Logic Unit (PLU), and up to 30 general-purpose I/O pins.

For additional documentation related to the LPC804 parts, see Section 19.

2. Features and benefits

- System:
  - Arm Cortex-M0+ processor (revision r0p1), running at frequencies of up to 15 MHz with single-cycle multiplier and fast single-cycle I/O port.
  - Arm Cortex-M0+ built-in Nested Vectored Interrupt Controller (NVIC).
  - System tick timer.
  - AHB multilayer matrix.
  - Serial Wire Debug (SWD) with four break points and two watch points. JTAG boundary scan (BSDL) supported.
- Memory:
  - Up to 32 KB on-chip EEPROM based flash programming memory.
  - Code Read Protection (CRP).
  - 4 KB SRAM.
- Dual I/O power (LPC804M111JDH24):
  - Independent supplies on each package side permitting level-shifting signals from one off-chip voltage domain to another and/or interfacing directly to off-chip peripherals operating at different supply levels.
  - The switch matrix provides level shifter functionality to allow up to two selected signals to be routed from user-selected pins in one voltage domain to selected pins in the alternate domain. This feature can also be used on a single supply device if voltage level shifting is not required.
- ROM API support:
  - Boot loader.

- Supports Flash In-Application Programming (IAP).
- Supports In-System Programming (ISP) through USART.
- On-chip ROM APIs for integer divide.
- Free Running Oscillator (FRO) API.

- Digital peripherals:
  - High-speed GPIO interface connected to the Arm Cortex-M0+ I/O bus with up to 30 General-Purpose I/O (GPIO) pins with configurable pull-up/pull-down resistors, programmable open-drain mode, and input inverter. GPIO direction control supports independent set/clear/toggle of individual bits.
  - High-current source output driver (20 mA) on five pins.
  - GPIO interrupt generation capability with boolean pattern-matching feature on eight GPIO inputs.
  - Switch matrix for flexible configuration of each I/O pin function.
  - CRC engine.
  - Capacitive Touch Interface.
  - Programmable Logic Unit (PLU) to create small combinatorial and/or sequential logic networks including simple state machines.
- Timers:
  - One 32-bit general purpose counter/timer, with four match outputs and three capture inputs. Supports PWM mode, and external count
  - Four channel Multi-Rate Timer (MRT) for repetitive interrupt generation at up to four programmable, fixed rates.
  - Self-Wake-up Timer (WKT) clocked from either Free Running Oscillator (FRO), a low-power, low-frequency internal oscillator, or an external clock input.
  - Windowed Watchdog timer (WWDT).
- Analog peripherals:
  - One 12-bit ADC with up to 12 input channels with multiple internal and external trigger inputs and with sample rates of up to 480 Ksamples/s. The ADC supports two independent conversion sequences.
  - Comparator with five input pins and external or internal reference voltage.
  - One 10-bit DAC.
- Serial peripherals:
  - Two USART interfaces with pin functions assigned through the switch matrix and one fractional baud rate generators.
  - One SPI controllers with pin functions assigned through the switch matrix.
  - Two I^2C-bus interface. It supports data rates up to 400 kbit/s on standard digital pins.
- Clock generation:
  - Free Running Oscillator (FRO). This oscillator provides a selectable 9 MHz, 12 MHz and 15 MHz outputs that can be used as a system clock. The FRO is trimmed to ±1 % accuracy over the entire voltage and temperature range of 0 C to 70 C.
  - 1 MHz low power oscillator can be used as a clock source.
  - Clock output function with divider that can reflect all internal clock sources.
- Power control:
  - Reduced power modes: sleep mode, deep-sleep mode, power-down mode, and deep power-down mode.

- Wake-up from deep-sleep and power-down modes on activity on USART, SPI, and I^2C peripherals.
- Wake-up from deep power-down mode on multiple pins.
- Timer-controlled self wake-up from sleep, deep-sleep, and power-down modes.
- Power-On Reset (POR).
- Brownout detect (BOD).

- Unique device serial number for identification.
- Single power supply (1.71 V to 3.6 V).
- Operating temperature range -40 °C to +105 °C.
- Available in WLCSP20, TSSOP20, TSSOP24, and HVQFN33 packages.

3. Applications

- Sensor gateways
- Industrial
- Gaming controllers
- 8/16-bit applications
- Consumer
- Climate control
- Simple motor control
- Portables and wearables
- Lighting
- Motor control
- Fire and security applications

4. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
LPC804M101JDH20	TSSOP20	plastic thin shrink small outline package; 20 leads; body width 4.4 mm	SOT360-1
LPC804M101JDH24	TSSOP24	plastic thin shrink small outline package; 24 leads; body width 4.4 mm	SOT355-1
LPC804M111JDH24	TSSOP24	plastic thin shrink small outline package; 24 leads; body width 4.4 mm	SOT355-1
LPC804M101JHI33	HVQFN33	HVQFN: plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 5 × 5 × 0.85 mm	SOT617-11
LPC804UK	WLCSP20	wafer level chip-size package; 20 (5 × 4) bumps; 2.50 ×1.84 × 0.5 mm	SOT1397-8

4.1 Ordering options

Table 2. Ordering options

Type number	Flash/KB	SRAM/KB	USART	I2C	SPI	DAC	Capacitive Touch	PLU	GPIO	Dual I/O power supply	Package
LPC804M101JDH20	32	4	2	2	1	-	yes	yes	17	-	TSSOP20
LPC804M101JDH24	32	4	2	2	1	1	yes	yes	21	-	TSSOP24
LPC804M111JDH24	32	4	2	2	1	1	yes	yes	20	yes	TSSOP24
LPC804M101JHI33	32	4	2	2	1	1	yes	yes	30	-	HVQFN33
LPC804UK	32	4	2	2	1	-	yes	yes	17	-	WLCSP20

5. Marking

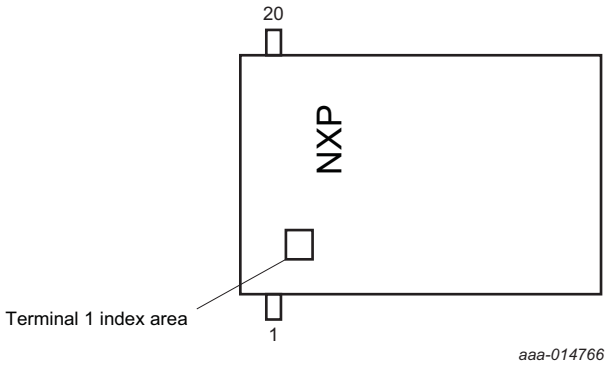


Fig 1. TSSOP20 and TSSOP24 package markings

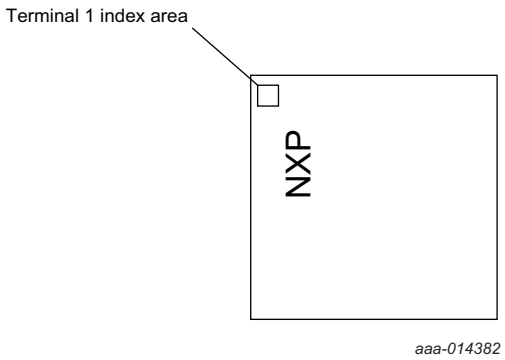


Fig 2. HVQFN33 package marking

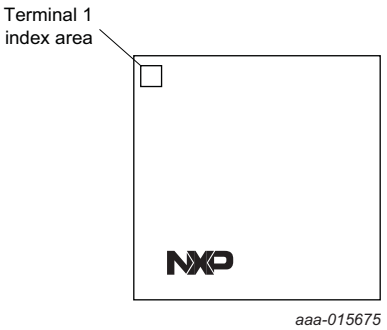


Fig 3. WLCSP20 package marking

The LPC804 HVQFN33 packages have the following top-side marking::

- First line: LPC804M1
- Second line: xxxx
- Third line: yywwx[R]
  - yyww: Date code with yy = year and ww = week.
  - xR = Boot code version and device revision.

The LPC804 TSSOP20 packages typically have the following top-side marking:

- First line: LPC804
- Second line: M101
- Third line: xxxx
- Fourth line: xxywwx[R]
  - yww: Date code with y = year and ww = week.
  - xR = Boot code version and device revision.

The LPC804 TSSOP24 packages have the following top-side marking:

- First line: LPC804
- Second line: xxxx
- Third line: ywwx[R]
  - yww: Date code with y = year and ww = week.
  - xR = Boot code version and device revision.
- Fourth line: M1y1J
  - y: 0 or 1

The LPC804 WLCSP20 packages have the following top-side marking:

- First line: LPC804
- Second line: xxxxx
- Third line: xyywwx[R]
  - yyww: Date code with ww = week and yy = year.
  - xR = Boot code version and device revision.
- Fourth line: xxx - yyy

Table 3. Device revision table

Revision identifier (R)	Revision description
1A	Initial device revision with Boot ROM version 13.1
1B	Initial device revision with Boot ROM version 13.1

6. Block diagram

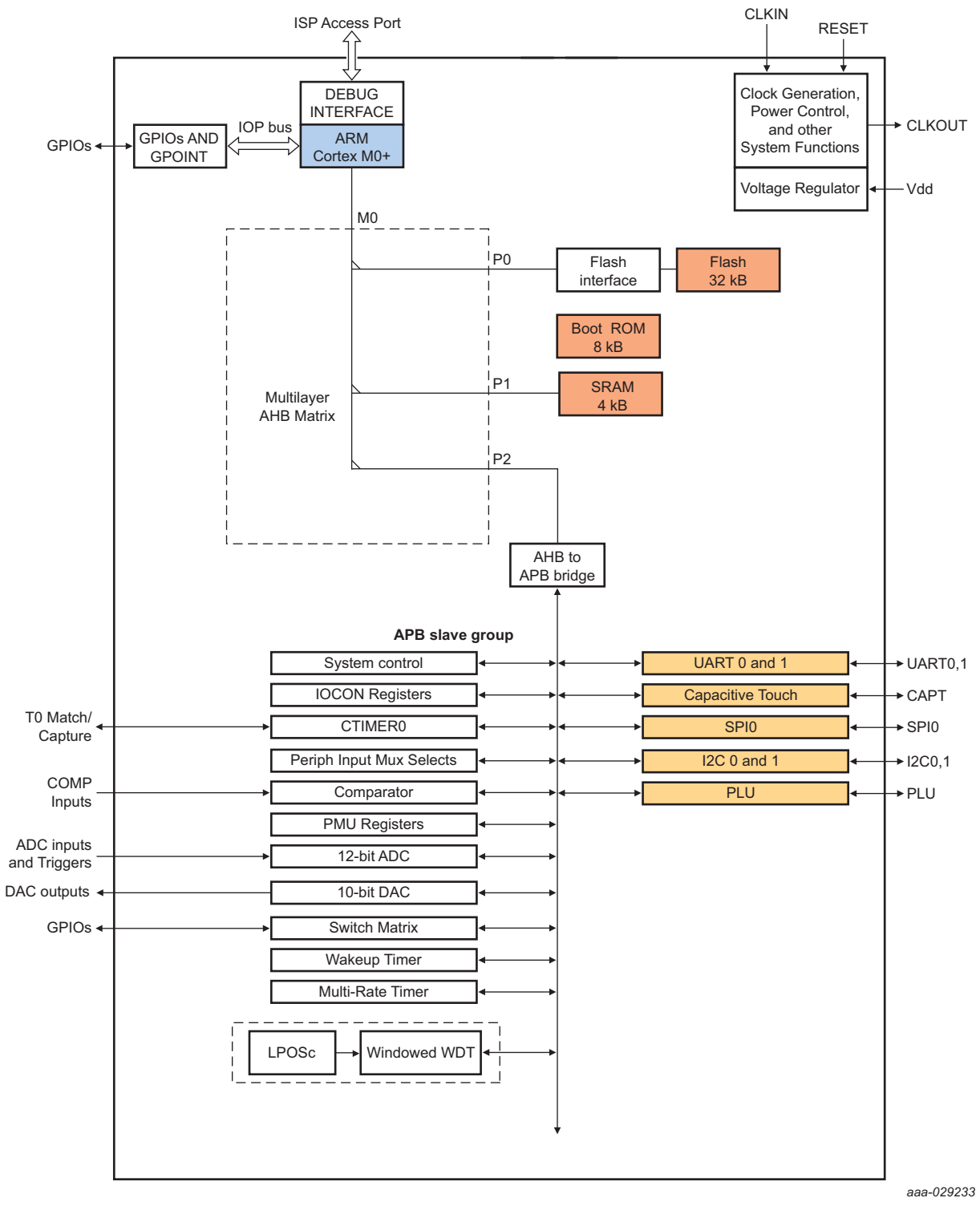


Fig 4. LPC804 block diagram

7. Pinning information

7.1 Pinning

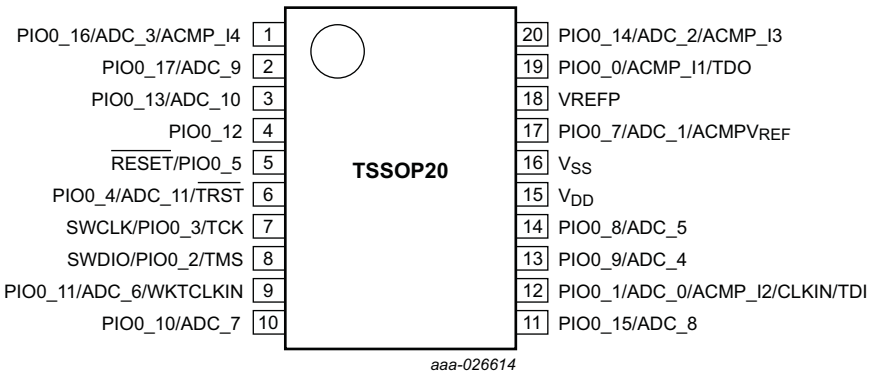


Fig 5. Pin configuration TSSOP20 package

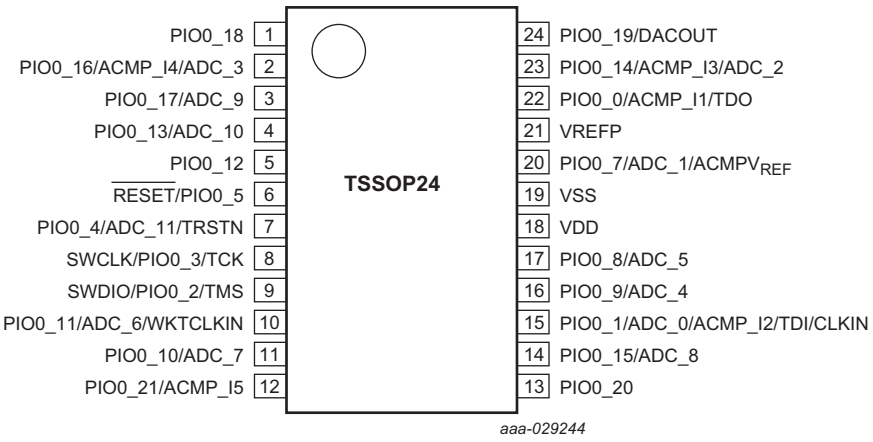


Fig 6. Pin configuration TSSOP24 - 1 package (LPC804M101JDH24 - single supply device)

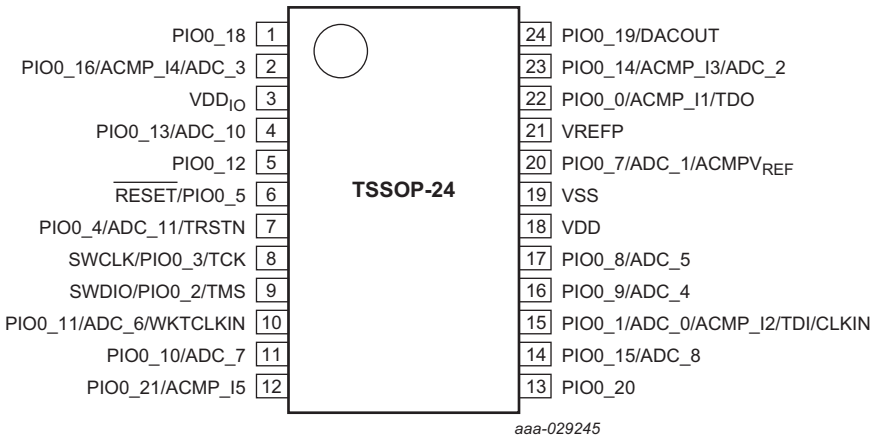
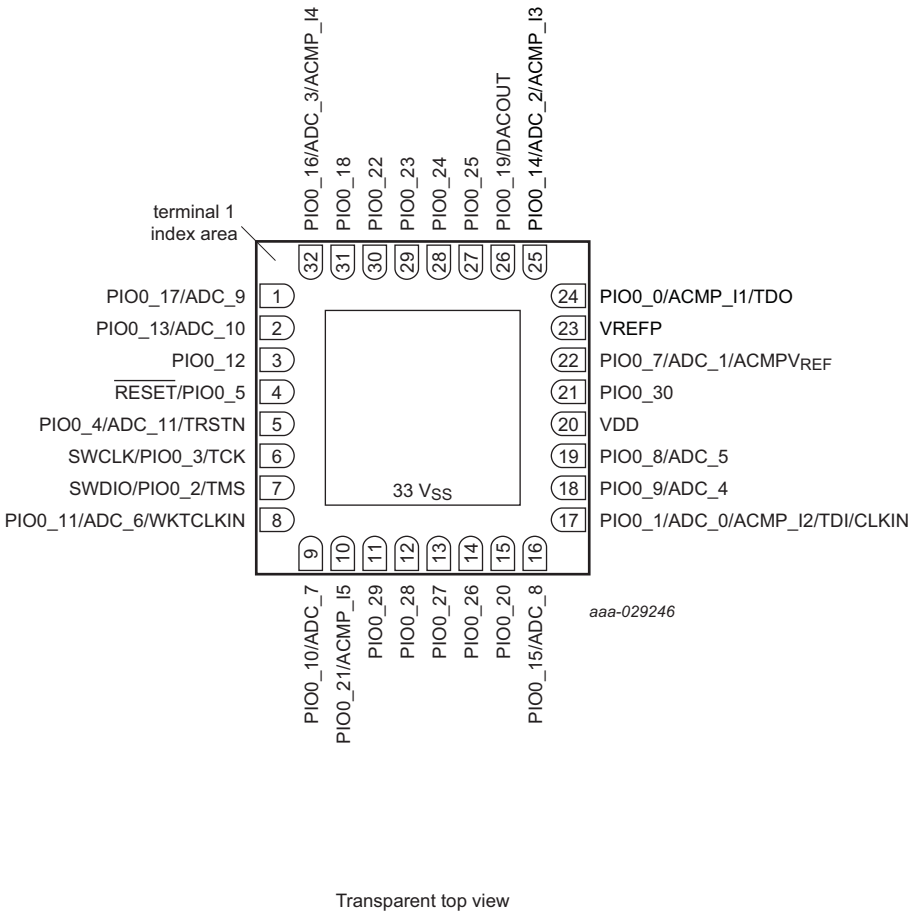


Fig 7. Pin configuration TSSOP24 - 2 package with VDDIO (LPC804M111JDH20 - dual supply device)



Transparent top view

Fig 8. Pin configuration HVQFN33 package

7.2 Pin description

Table 4 shows the pin functions that are fixed to specific pins on each package. These fixed-pin functions are selectable through the switch matrix between GPIO and the comparator, ADC, SWD, and RESET pins. By default, the GPIO function is selected except on pins PIO0_2, PIO0_3, and PIO0_5. JTAG functions are available in boundary scan mode only.

Movable functions for the I2C, USART, SPI, CTimer pins, Capacitive Touch, and other peripherals can be assigned through the switch matrix to any pin that is not power or ground in place of the pin's fixed functions.

The following exceptions apply:

Do not assign more than one output to any pin. However, an output and/or one or more inputs can be assigned to a pin. Once any function is assigned to a pin, the pin's GPIO functionality is disabled.

Eight GPIO pins trigger a wake-up from deep power-down mode. If the part must wake up from deep power-down mode via an external pin, do not assign any movable function to this pin. The GPIO pins should be pulled HIGH externally before entering deep power-down mode. A LOW-going pulse as short as 50 ns causes the chip to exit deep power-down mode and wakes up the part.

The JTAG functions TDO, TDI, TCK, TMS, and TRST are selected on pins PIO0_0 to PIO0_4 by hardware when the part is in boundary scan mode.

PIO0_2, PIO0_3, PIO0_12, PIO0_18, and PIO0_20 are the high drive output pins. PIO0_4, PIO0_8, PIO0_9, PIO0_10, PIO0_11, PIO0_13, PIO0_15, and PIO0_17 are the WAKEUP pins.

Table 4. Pin description

Symbol	TSSOP24-1	TSSOP24-2	TSSOP20	HVQFN33	WLCSP20		Reset state[1]	Type	Description
PIO0_0/ACMP_I1/TDO	22	22	19	24	D3	[2]	I; PU	IO	**PIO0_0 —** General-purpose port 0 input/output 0. In ISP mode, this is the U0_RXD pin (for single supply devices). In boundary scan mode: TDO (Test Data Out).
								A	**ACMP_I1 —** Analog comparator input 1.
PIO0_1/ADC_0/ACMP_I2/ TDI/CLKIN	15	15	12	17	A4	[2]	I; PU	IO	**PIO0_1 —** General-purpose port 0 input/output 1. In boundary scan mode: TDI (Test Data In).
								A	**ACMP_I2 —** Analog comparator input 2.
								I	**CLKIN —** External clock input.
SWDIO/PIO0_2/ TMS	9	9	8	7	B2	[3]	I; PU	IO	**SWDIO —** Serial Wire Debug I/O. SWDIO is enabled by default on this pin. In boundary scan mode: TMS (Test Mode Select).
								I/O	**PIO0_2 —** General-purpose port 0 input/output 2.
SWCLK/PIO0_3/ TCK	8	8	7	6	B1	[3]	I; PU	I	**SWCLK —** Serial Wire Clock. SWCLK is enabled by default on this pin. In boundary scan mode: TCK (Test Clock).
								IO	**PIO0_3 —** General-purpose port 0 input/output 3.
PIO0_4/ADC_11/ TRSTN	7	7	6	5	C2	[2]	I; PU	IO	**PIO0_4 —** General-purpose port 0 input/output 4. In ISP mode, this pin is the U0_TXD pin (for single supply devices). In boundary scan mode: $\overline{\text{TRST}}$ (Test Reset).
								A	**ADC_11 —** ADC input 11.
$\overline{\text{RESET}}$/PIO0_5	6	6	5	4	C1	[5]	I; PU	IO	**$\overline{\text{RESET}}$ —** External reset input: A LOW-going pulse as short as 50 ns on this pin resets the device, causing I/O ports and peripherals to take on their default states, and processor execution to begin at address 0. The $\overline{\text{RESET}}$ pin can be left unconnected or be used as a GPIO or for any movable function if an external $\overline{\text{RESET}}$ function is not needed.
								I	**PIO0_5 —** General-purpose port 0 input/output 5.

Table 4. Pin description

Symbol	TSSOP24-1	TSSOP24-2	TSSOP20	HVQFN33	WLCSP20		Reset state[1]	Type	Description
PIO0_7/ADC_1/ $ACMPV_{REF}$	20	20	17	22	D4	[2]	I; PU	IO	**PIO0_7 —** General-purpose port 0 input/output 7.
								A	**ADC_1 —** ADC input 1.
									$ACMPV_{REF}$ — Alternate reference voltage for the analog comparator.
PIO0_8/ADC_5	17	17	14	19	C3	[2]	I; PU	IO	**PIO0_8 —** General-purpose port 0 input/output 8. In ISP mode, this is the U0_RXD pin (for dual supply devices).
								A	**ADC_5 —** ADC input 5.
PIO0_9/ADC_4	16	16	13	18	B3	[2]	I; PU	IO	**PIO0_9 —** General-purpose port 0 input/output 9. In ISP mode, this is the U0_TXD pin (for dual supply devices).
								A	**ADC_4 —** ADC input 4.
PIO0_10/ADC_7	11	11	10	9	A2	[2]	Inactive	I; F	**PIO0_10 —** General-purpose port 0 input/output 10.
									ADC_7 — ADC input 7.
PIO0_11/ADC_6/ WKTCLKIN	10	10	9	8	A1	[2]	Inactive	I; F	**PIO0_11 —** General-purpose port 0 input/output 11.
									ADC_6 — ADC input 6.
									WKTCKLKIN — This pin can host an external clock for the self-wake-up timer. To use the pin as a self-wake-up timer clock input, select the external clock in the wake-up timer CTRL register. The external clock input is active in sleep, deep-sleep, and power-down modes.
PIO0_12	5	5	4	3	D1	[3]	I; PU	IO	**PIO0_12 —** General-purpose port 0 input/output 12. ISP entry pin. A LOW level on this pin during reset starts the ISP command handler.
PIO0_13/ADC_10	4	4	3	2	D2	[2]	I; PU	IO	**PIO0_13 —** General-purpose port 0 input/output 13.
								A	**ADC_10 —** ADC input 10.
PIO0_14/ACMP_3/ ADC_2	23	23	20	25	E3	[2]	I; PU	IO	**PIO0_14 —** General-purpose port 0 input/output 14.
								A	**ACMP_I3 —** Analog comparator common input 3.
								A	**ADC_2 —** ADC input 2.
PIO0_15/ADC_8	14	14	11	16	A3	[4]	I; PU	IO	**PIO0_15 —** General-purpose port 0 input/output 15.
									ADC_8 — ADC input 8.

Table 4. Pin description

Symbol	TSSOP24-1	TSSOP24-2	TSSOP20	HVQFN33	WLCSP20		Reset state[1]	Type	Description
PIO0_16/ACMP_I4/ ADC_3	2	2	1	32	E2	[3]	I; PU	IO	**PIO0_16 —** General-purpose port 0 input/output 16.
									ACMP_I4 — Analog comparator common input 4.
									ADC_3 — ADC input 3.
PIO0_17/ADC_9	3	-	2	1	E1	[2]	I; PU	IO	**PIO0_17 —** General-purpose port 0 input/output 17.
								A	**ADC_9 —** ADC input 9.
PIO0_18	1	1	-	31	-	[3]	I; PU	IO	**PIO0_18 —** General-purpose port 0 input/output 18.
PIO0_19/DACOUT	24	24	-	26	-	[2]	I; PU	IO	**PIO0_19 —** General-purpose port 0 input/output 19.
								A	**DACOUT —** DAC output.
PIO0_20	13	13	-	15	-	[3]	I; PU	IO	**PIO0_20 —** General-purpose port 0 input/output 20.
PIO0_21/ACMP_I5	12	12	-	10	-	[3]	I; PU	IO	**PIO0_21 —** General-purpose port 0 input/output 21.
									ACMP_15 — Analog comparator common input 5.
PIO0_22	-	-	-	30	-	[3]	I; PU	IO	**PIO0_22 —** General-purpose port 0 input/output 22.
PIO0_23	-	-	-	29	-	[3]	I; PU	IO	**PIO0_23 —** General-purpose port 0 input/output 23.
PIO0_24	-	-	-	28	-	[3]	I; PU	IO	**PIO0_24 —** General-purpose port 0 input/output 24.
PIO0_25	-	-	-	27	-	[3]	I; PU	IO	**PIO0_25 —** General-purpose port 0 input/output 25.
PIO0_26	-	-	-	14	-	[3]	I; PU	IO	**PIO0_26 —** General-purpose port 0 input/output 26.
PIO0_27	-	-	-	13	-	[3]	I; PU	IO	**PIO0_27 —** General-purpose port 0 input/output 27.
PIO0_28	-	-	-	12	-	[3]	I; PU	IO	**PIO0_28 —** General-purpose port 0 input/output 28.
PIO0_29	-	-	-	11	-	[3]	I; PU	IO	**PIO0_29 —** General-purpose port 0 input/output 29.
PIO0_30	-	-	-	21	-	[3]	I; PU	IO	**PIO0_30 —** General-purpose port 0 input/output 30.
VREFP	21	21	18	23	E4			A	**VREFP —** ADC positive reference voltage. Must be equal or lower than V_{DD}.

Table 4. Pin description

Symbol	TSSOP24-1	TSSOP24-2	TSSOP20	HVQFN33	WLCSP20		Reset state[1]	Type	Description
V_{DD}	18	18	15	20	B4		-	-	If VDDIO is present, VDD is the supply voltage for the I/Os on the right side of the package and the core voltage regulator. If VDDIO is not present, VDD also supplies voltage to the I/Os on the left side of the package.
VDD_{IO}	-	3	-	-	-		-	-	If present, it is the supply voltage for the I/Os on the left side of the package.
V_{SS}	19		16	33[8]	C4		-	-	Ground.

[1] Pin state at reset for default function: I = Input; AI = Analog Input; O = Output; PU = internal pull-up enabled (pins pulled up to full V_{DD} level); IA = inactive, no pull-up/down enabled; F = floating. For pin states in the different power modes, see Section 15.5 “Pin states in different power modes”. For termination on unused pins, see Section 15.4 “Termination of unused pins”.

[2] 5 V tolerant pin providing standard digital I/O functions with configurable modes, configurable hysteresis, and analog input. When configured as an analog input, the digital section of the pin is disabled, and the pin is not 5 V tolerant.

[3] 5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors and configurable hysteresis; includes high-current output driver.

[4] 5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors and configurable hysteresis.

[5] See Figure 16 for the reset pad configuration. This pin includes a 20 ns glitch filter (active in all power modes). $\overline{\text{RESET}}$ functionality is not available in deep power-down mode. Use the WAKEUP pin to reset the chip and wake up from deep power-down mode.

[6] The WKTCLKIN function is enabled in the PINENABLE0 register in the PMU. See the LPC804 user manual.

[7] The digital part of this pin is 3 V tolerant pin due to special analog functionality. Pin provides standard digital I/O functions with configurable modes, configurable hysteresis, and an analog input. When configured as an analog input, the digital section of the pin is disabled.

[8] Thermal pad for HVQFN33.

8. Movable functions

Movable functions for the I2C, USART, SPI, CTimer pins, Capacitive Touch, and other peripherals can be assigned through the switch matrix to any pin that is not power or ground in place of the fixed functions of the pin.

Table 5. Movable functions (assign to pins PIO0_0 to PIO0_5, PIO0_7 to PIO0_30 through switch matrix)

Function name	Type	Description
Ux_TXD	O	Transmitter output for USART0 to USART1.
Ux_RXD	I	Receiver input for USART0 to USART1.
$\overline{\text{Ux\_RTS}}$	O	Request To Send output for USART0.
$\overline{\text{Ux\_CTS}}$	I	Clear To Send input for USART0.
Ux_SCLK	I/O	Serial clock input/output for USART0 to USART1 in synchronous mode.
SPIx_SCK	I/O	Serial clock for SPI0.
SPIx_MOSI	I/O	Master Out Slave In for SPI0.
SPIx_MISO	I/O	Master In Slave Out for SPI0.
SPIx_SSEL0	I/O	Slave select 0 for SPI0.
SPIx_SSEL1	I/O	Slave select 1 for SPI0.
I2Cx_SDA	I/O	I^2C0 and I^2C1 bus data input/output.
I2Cx_SCL	I/O	I^2C0 and I^2C1 bus clock input/output.
ACMP_O	O	Analog comparator output.
CLKOUT	O	Clock output.
GPIO_INT_BMAT	O	Output of the pattern match engine.
T0_MAT0	O	Timer Match channel 0.
T0_MAT1	O	Timer Match channel 1.
T0_MAT2	O	Timer Match channel 2.
T0_MAT3	O	Timer Match channel 3.
T0_CAP0	I	Timer Capture channel 0.
T0_CAP1	I	Timer Capture channel 1.
T0_CAP2	I	Timer Capture channel 2.
CAPT_X0	O	CAPT_X0 function.
CAPT_X1	O	CAPT_X1 function.
CAPT_X2	O	CAPT_X2 function.
CAPT_X3	O	CAPT_X3 function.
CAPT_X4	O	CAPT_X4 function.
CAPT_YL	O	CAPT_YL function.
CAPT_YH	O	CAPT_YH function.
LVLSHFT_IN0	I	Level shift input 0.
LVLSHFT_IN1	I	Level shift input 1.
LVLSHFT_OUT0	O	Level shift output 0.
LVLSHFT_OUT1	O	Level shift output 1.

9. Functional description

9.1 Arm Cortex-M0+ core

The Arm Cortex-M0+ core runs at an operating frequency of up to 15 MHz using a two-stage pipeline. The core revision is r0p1.

Integrated in the core are the NVIC and Serial Wire Debug with four breakpoints and two watchpoints. The Arm Cortex-M0+ core supports a single-cycle I/O enabled port for fast GPIO access.

The core includes a single-cycle multiplier and a system tick timer.

9.2 On-chip flash program memory

The LPC804 contain up to 32 KB of on-chip EEPROM based flash program memory.

9.3 On-chip SRAM

The LPC804 contain a total of 4 KB on-chip static RAM data memory.

9.4 On-chip ROM

The on-chip ROM contains the bootloader:

- Boot loader.
- Supports Flash In-Application Programming (IAP).
- Supports In-System Programming (ISP) through USART.
- On-chip ROM APIs for integer divide.
- Free Running Oscillator (FRO) API.

9.5 Memory map

The LPC804 incorporates several distinct memory regions. Figure 9 shows the overall map of the entire address space from the user program viewpoint following reset. The interrupt vector area supports address remapping.

The Arm private peripheral bus includes the Arm core registers for controlling the NVIC, the system tick timer (SysTick), and the reduced power modes.

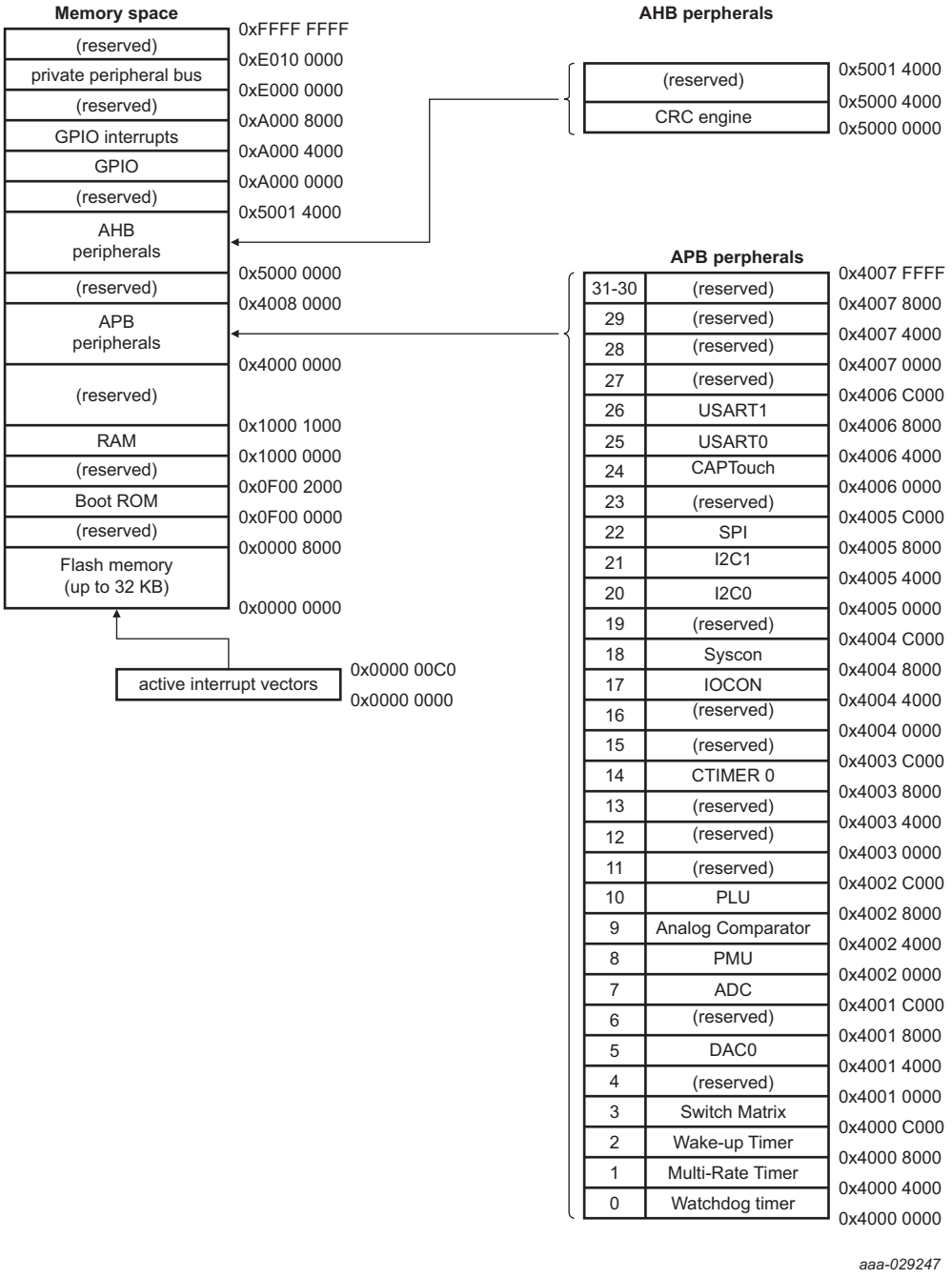


Fig 9. LPC804 Memory mapping

9.6 Nested Vectored Interrupt Controller (NVIC)

The Nested Vectored Interrupt Controller (NVIC) is part of the Cortex-M0+. The tight coupling to the CPU allows for low interrupt latency and efficient processing of late arriving interrupts.

9.6.1 Features

- Nested Vectored Interrupt Controller is a part of the Arm Cortex-M0+.
- Tightly coupled interrupt controller provides low interrupt latency.
- Controls system exceptions and peripheral interrupts.
- Supports 32 vectored interrupts.
- In the LPC804, the NVIC supports vectored interrupts for each of the peripherals and the eight pin interrupts.
- Four programmable interrupt priority levels with hardware priority level masking.
- Software interrupt generation using the Arm exceptions SVCall and PendSV.
- Supports NMI.

9.6.2 Interrupt sources

Each peripheral device has at least one interrupt line connected to the NVIC but can have several interrupt flags. Individual interrupt flags can also represent more than one interrupt source.

9.7 System tick timer

The Arm Cortex-M0+ includes a 24-bit system tick timer (SysTick) that is intended to generate a dedicated SysTick exception at a fixed time interval (typically 10 ms).

9.8 I/O configuration

The IOCON block controls the configuration of the I/O pins. Each digital or mixed digital/analog pin with the PIO0_n designator in Table 4 can be configured as follows:

- Enable or disable the weak internal pull-up and pull-down resistors.
- Select a pseudo open-drain mode. The input cannot be pulled up above V_{DD}. The pins are not 5 V tolerant when V_{DD} is grounded.
- Program the input glitch filter with different filter constants using one of the IOCON divided clock signals (IOCONCLKCDIV, see Figure 12 “LPC804 clock generation”). You can also bypass the glitch filter.
- Invert the input signal.
- Hysteresis can be enabled or disabled.
- The switch matrix setting enables the analog input mode on pins with analog and digital functions. Enabling the analog mode disconnects the digital functionality.
- The LPC804 uses a dual voltage I/O feature. The pins on one side of the package are supplied by VDDIO and the pins on the other side are supplied by VDD. Each of these two supplies can be connected to different voltages within the allowed Vdd range. This feature allows the device to level-shift signals from one off-chip voltage domain to another.

- The switch matrix provides level shifter functionality to allow up to two selected signals to be routed from user-selected pins in one voltage domain to selected pins in the alternate domain. This feature can also be used on a single supply device if voltage level shifting is not required.

Remark: The functionality of each I/O pin is flexible and is determined entirely through the switch matrix. See Section 9.9 for details.

9.8.1 Standard I/O pad configuration

Figure 10 shows the possible pin modes for standard I/O pins with analog input function:

- Digital output driver with configurable open-drain output.
- Digital input: Weak pull-up resistor (PMOS device) enabled/disabled.
- Digital input: Weak pull-down resistor (NMOS device) enabled/disabled.
- Digital input: Repeater mode enabled/disabled.
- Digital input: Programmable input digital filter selectable on all pins.
- Analog input: Selected through the switch matrix.

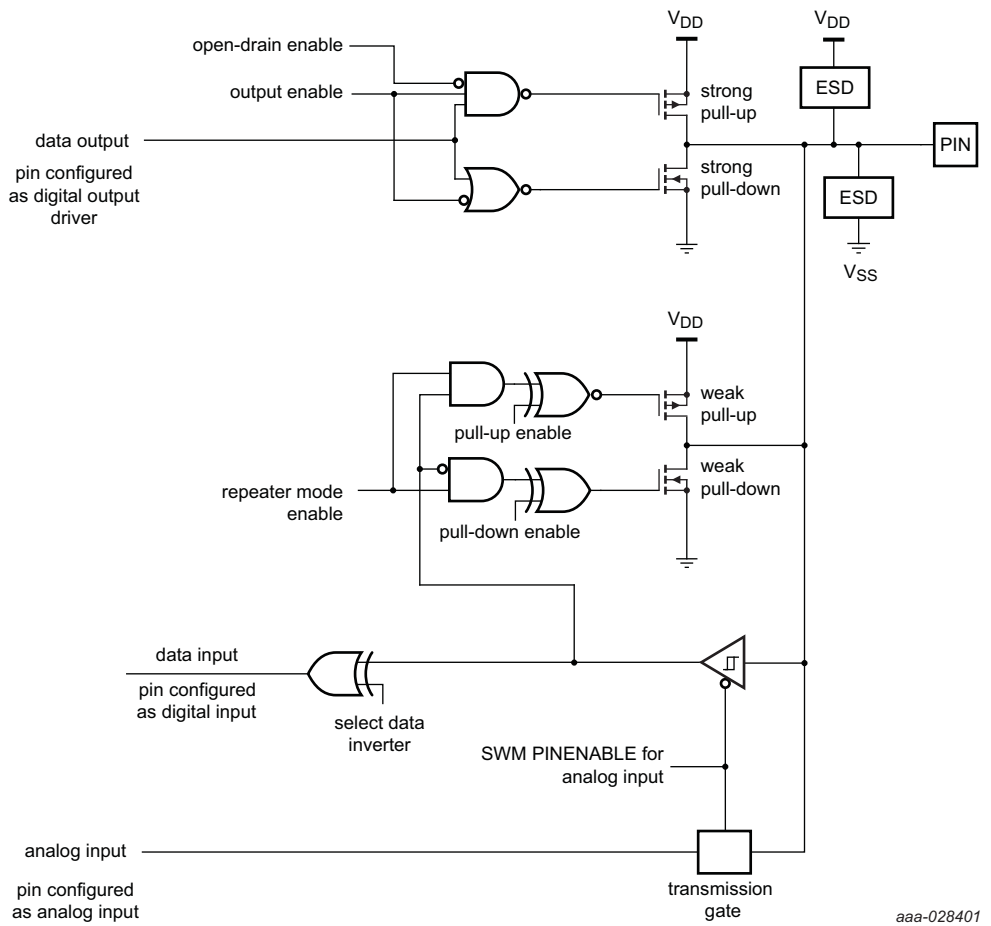


Fig 10. Standard I/O pad configuration

9.9 Switch Matrix (SWM)

The switch matrix controls the function of each digital or mixed analog/digital pin in a highly flexible way by allowing to connect many functions like the USART, SPI, CTimer, Capacitive Touch, and I2C functions to any pin that is not power or ground. These functions are called movable functions and are listed in Table 5.

Functions that need specialized pads can be enabled or disabled through the switch matrix. These functions are called fixed-pin functions and cannot move to other pins. The fixed-pin functions are listed in Section 7.2 “Pin description”. If a fixed-pin function is disabled, any other movable function can be assigned to this pin.

9.10 Fast General-Purpose parallel I/O (GPIO)

Device pins that are not connected to a specific peripheral function are controlled by the GPIO registers. Pins may be dynamically configured as inputs or outputs. Multiple outputs can be set or cleared in one write operation.

LPC804 use accelerated GPIO functions:

- GPIO registers are on the Arm Cortex-M0+ IO bus for fastest possible single-cycle I/O timing, allowing GPIO toggling with rates of up to 7 MHz.
- An entire port value can be written in one instruction.
- Mask, set, and clear operations are supported for the entire port.

All GPIO port pins are fixed-pin functions that are enabled or disabled on the pins by the switch matrix. Therefore each GPIO port pin is assigned to one specific pin and cannot be moved to another pin. Except for pins SWDIO/PIO0_2, SWCLK/PIO0_3, and RESET/PIO0_5, the switch matrix enables the GPIO port pin function by default.

9.10.1 Features

- Bit level port registers allow a single instruction to set and clear any number of bits in one write operation.
- Direction control of individual bits.
- All I/O default to GPIO inputs with internal pull-up resistors enabled after reset.
- Pull-up/pull-down configuration, repeater, and open-drain modes can be programmed through the IOCON block for each GPIO pin (see Figure 10).
- Direction (input/output) can be set and cleared individually.
- Pin direction bits can be toggled.

9.11 Pin interrupt

The pin interrupt block configures up to eight pins from all digital pins for providing eight external interrupts connected to the NVIC.

Any digital pin, independently of the function selected through the switch matrix, can be configured through the SYSCON block as input to the pin interrupt. The registers that control the pin interrupt are on the IO+ bus for fast single-cycle access.

9.11.1 Features

- Pin interrupts
  - Up to eight pins can be selected from all digital pins as edge- or level-sensitive interrupt requests. Each request creates a separate interrupt in the NVIC.
  - Edge-sensitive interrupt pins can interrupt on rising or falling edges or both.
  - Level-sensitive interrupt pins can be HIGH- or LOW-active.
  - Pin interrupts can wake up the LPC804 from sleep mode, deep-sleep mode, and power-down mode.

9.12 USART0/1

All USART functions are movable functions and are assigned to pins through the switch matrix.

9.12.1 Features

- Maximum bit rates of 1.875 Mbit/s in asynchronous mode and 10 Mbit/s in synchronous mode for USART functions connected to all digital pins.
- 7, 8, or 9 data bits and 1 or 2 stop bits
- Synchronous mode with master or slave operation. Includes data phase selection and continuous clock option.
- Multiprocessor/multidrop (9-bit) mode with software address compare. (RS-485 possible with software address detection and transceiver direction control.)
- Parity generation and checking: odd, even, or none.
- One transmit and one receive data buffer.
- RTS/CTS for hardware signaling for automatic flow control. Software flow control can be performed using Delta CTS detect, Transmit Disable control, and any GPIO as an RTS output.
- Received data and status can optionally be read from a single register
- Break generation and detection.
- Receive data is 2 of 3 sample "voting". Status flag set when one sample differs.
- Built-in Baud Rate Generator.
- A fractional rate divider is shared among all UARTs.
- Interrupts available for Receiver Ready, Transmitter Ready, Receiver Idle, change in receiver break detect, Framing error, Parity error, Overrun, Underrun, Delta CTS detect, and receiver sample noise detected.
- Separate data and flow control loopback modes for testing.
- Baud rate clock can also be output in asynchronous mode.

9.13 SPI0

All SPI functions are movable functions and are assigned to pins through the switch matrix.

9.13.1 Features

- Maximum data rates of up to 15 Mbit/s in master mode and up to 20 Mbit/s in slave mode for SPI functions connected to all digital pins.
- Data frames of 1 to 16 bits supported directly. Larger frames supported by software.
- Master and slave operation.
- Data can be transmitted to a slave without the need to read incoming data, which can be useful while setting up an SPI memory.
- Control information can optionally be written along with data, which allows very versatile operation, including “any length” frames.
- One Slave Select input/output with selectable polarity and flexible usage.

Remark: Texas Instruments SSI and National Microwire modes are not supported.

9.14 I^2C-bus interface (I^2C0 and I^2C1)

The I^2C-bus is bidirectional for inter-IC control using only two wires: a serial clock line (SCL) and a serial data line (SDA). Each device is recognized by a unique address and can operate as either a receiver-only device (e.g., an LCD driver) or a transmitter with the capability to both receive and send information (such as memory). Transmitters and/or receivers can operate in either master or slave mode, depending on whether the chip has to initiate a data transfer or is only addressed. The I^2C is a multi-master bus and can be controlled by more than one bus master.

9.14.1 Features

- I^2C0 and I^2C1 support standard and fast mode with data rates of up to 400 kbit/s.
- Independent Master, Slave, and Monitor functions.
- Supports both Multi-master and Multi-master with Slave functions.
- Multiple I^2C slave addresses supported in hardware.
- One slave address can be selectively qualified with a bit mask or an address range in order to respond to multiple I^2C bus addresses.
- 10-bit addressing supported with software assist.
- Supports SMBus.

9.15 Capacitive Touch Interface

The Capacitive Touch interface is designed to handle up to five capacitive buttons in different sensor configurations, such as slider, and button matrix. It operates in sleep, deep sleep, and power-down modes, allowing very low power performance.

The Capacitive Touch module measures the change in capacitance of an electrode plate when an earth-ground connected object (for example, finger) is brought within close proximity.

9.16 CTimer

9.16.1 General-purpose 32-bit timers/external event counter

The LPC804 has one general-purpose 32-bit timer/counter.

The timer/counter is designed to count cycles of the system derived clock or an externally-supplied clock. It can optionally generate interrupts or perform other actions at specified timer values, based on four match registers. The timer/counter also includes three capture inputs to trap the timer value when an input signal transitions, optionally generating an interrupt.

9.16.1.1 Features

- A 32-bit timer/counter with a programmable 32-bit prescaler.
- Counter or timer operation.
- Up to three 32-bit captures can take a snapshot of the timer value when an input signal transitions. A capture event may also optionally generate an interrupt. The number of capture inputs for each timer that are actually available on device pins can vary by device.
- Four 32-bit match registers that allow:
  - Continuous operation with optional interrupt generation on match.
  - Stop timer on match with optional interrupt generation.
  - Reset timer on match with optional interrupt generation.
  - Shadow registers are added for glitch-free PWM output.
- For each timer, up to 4 external outputs corresponding to match registers with the following capabilities (the number of match outputs for each timer that are actually available on device pins can vary by device):
  - Set LOW on match.
  - Set HIGH on match.
  - Toggle on match.
  - Do nothing on match.
- The timer and prescaler may be configured to be cleared on a designated capture event. This feature permits easy pulse width measurement by clearing the timer on the leading edge of an input pulse and capturing the timer value on the trailing edge.
- Up to 4 match registers can be configured for PWM operation, allowing up to 3 single edged controlled PWM outputs. (The number of match outputs for each timer that are actually available on device pins can vary by device.)

9.17 Multi-Rate Timer (MRT)

The Multi-Rate Timer (MRT) provides a repetitive interrupt timer with two channels. Each channel can be programmed with an independent time interval, and each channel operates independently from the other channels.

9.17.1 Features

- 31-bit interrupt timer
- Two channels independently counting down from individually set values
- Bus stall, repeat and one-shot interrupt modes

9.18 Windowed WatchDog Timer (WWDT)

The watchdog timer resets the controller if software fails to service the watchdog timer periodically within a programmable time window.

9.18.1 Features

- Internally resets chip if not periodically reloaded during the programmable time-out period.
- Optional windowed operation requires reload to occur between a minimum and maximum time period, both programmable.
- Optional warning interrupt can be generated at a programmable time prior to watchdog time-out.
- Enabled by software but requires a hardware reset or a watchdog reset/interrupt to be disabled.
- Incorrect feed sequence causes reset or interrupt if enabled.
- Flag to indicate watchdog reset.
- Programmable 24-bit timer with internal prescaler.
- Selectable time period from ($T_{cy(WDCLK)} \times 256 \times 4$) to ($T_{cy(WDCLK)} \times 2^{24} \times 4$) in multiples of $T_{cy(WDCLK)} \times 4$.
- The WatchDog Clock (WDCLK) is generated by the dedicated watchdog oscillator (WDOSC).

9.19 Self-Wake-up Timer (WKT)

The self-wake-up timer is a 32-bit, loadable down counter. Writing any non-zero value to this timer automatically enables the counter and launches a count-down sequence. When the counter is used as a wake-up timer, this write can occur prior to entering a reduced power mode.

9.19.1 Features

- 32-bit loadable down counter. Counter starts automatically when a count value is loaded. Time-out generates an interrupt/wake up request.
- The WKT supports three clock sources: an external clock on the WKTCLKIN pin, the low-power oscillator, and the FRO. The low-power oscillator can be used as the clock source in sleep, deep-sleep, and power-down modes.
- The WKT can be used for waking up the part from any reduced power mode or for general-purpose timing.

9.20 Programmable Logic Unit (PLU)

The PLU is comprised of 26 5-input LUT elements. Each LUT element contains a 32-bit truth table (look-up table) register and a 32:1 multiplexer. During operation, the five LUT inputs control the select lines of the multiplexer. This structure allows any desired logical combination of the five LUT inputs.

9.20.1 Features

- The PLU is used to create small combinatorial and/or sequential logic networks including simple state machines.
- The PLU is comprised of an array of 26 inter-connectable, 5-input Look-up Table (LUT) elements, and four flip-flops.
- Eight primary outputs can be selected using a multiplexer from among all of the LUT outputs and the four flip-flops.
- An external clock to drive the four flip-flops must be applied to the PLU_CLKIN pin if a sequential network is implemented.
- Programmable logic can be used to drive on-chip inputs/triggers through external pin-to-pin connections.
- A tool suite is provided to facilitate programming of the PLU to implement the logic network described in a Verilog RTL design.

Remark: PLU cannot be used to wake-up from sleep, deep-sleep, power-down, and deep power-down modes.

9.21 Analog comparator (ACMP)

The analog comparator with selectable hysteresis can compare voltage levels on external pins and internal voltages.

After power-up and after switching the input channels of the comparator, the output of the voltage ladder must be allowed to settle to its stable value before it can be used as a comparator reference input. Settling times are given in Table 27.

The analog comparator output is a movable function and is assigned to a pin through the switch matrix. The comparator inputs and the voltage reference are enabled through the switch matrix.