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LPC81xM

32-bit ARM® Cortex®-M0+ microcontroller; up to 16 kB flash and 4 kB SRAM

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1. General description

The LPC81xM are an ARM Cortex-M0+ based, low-cost 32-bit MCU family operating at CPU frequencies of up to 30 MHz. The LPC81xM support up to 16 kB of flash memory and 4 kB of SRAM.

The peripheral complement of the LPC81xM includes a CRC engine, one I2C-bus interface, up to three USARTs, up to two SPI interfaces, one multi-rate timer, self wake-up timer, and state-configurable timer, one comparator, function-configurable I/O ports through a switch matrix, an input pattern match engine, and up to 18 general-purpose I/O pins.

2. Features and benefits

- System:
  - ARM Cortex-M0+ processor, running at frequencies of up to 30 MHz with single-cycle multiplier and fast single-cycle I/O port.
  - ARM Cortex-M0+ built-in Nested Vectored Interrupt Controller (NVIC).
  - System tick timer.
  - Serial Wire Debug (SWD) and JTAG boundary scan modes supported.
  - Micro Trace Buffer (MTB) supported.
- Memory:
  - Up to 16 kB on-chip flash programming memory with 64 Byte page write and erase.
  - Up to 4 kB SRAM.
- ROM API support:
  - Boot loader.
  - USART drivers.
  - I2C drivers.
  - Power profiles.
  - Flash In-Application Programming (IAP) and In-System Programming (ISP).
- Digital peripherals:
  - High-speed GPIO interface connected to the ARM Cortex-M0+ IO bus with up to 18 General-Purpose I/O (GPIO) pins with configurable pull-up/pull-down resistors, programmable open-drain mode, input inverter, and glitch filter.
  - High-current source output driver (20 mA) on four pins.
  - High-current sink driver (20 mA) on two true open-drain pins.
  - GPIO interrupt generation capability with boolean pattern-matching feature on eight GPIO inputs.
  - Switch matrix for flexible configuration of each I/O pin function.

◆ State Configurable Timer/PWM (SCTimer/PWM) with input and output functions (including capture and match) assigned to pins through the switch matrix.

◆ Multiple-channel multi-rate timer (MRT) for repetitive interrupt generation at up to four programmable, fixed rates.

◆ Self Wake-up Timer (WKT) clocked from either the IRC or a low-power, low-frequency internal oscillator.

◆ CRC engine.

◆ Windowed Watchdog timer (WWDT).

■ Analog peripherals:

◆ Comparator with internal and external voltage references with pin functions assigned or enabled through the switch matrix.

■ Serial interfaces:

◆ Three USART interfaces with pin functions assigned through the switch matrix.

◆ Two SPI controllers with pin functions assigned through the switch matrix.

◆ One I^2C-bus interface with pin functions assigned through the switch matrix.

■ Clock generation:

◆ 12 MHz internal RC oscillator trimmed to 1.5 % accuracy that can optionally be used as a system clock.

◆ Crystal oscillator with an operating range of 1 MHz to 25 MHz.

◆ Programmable watchdog oscillator with a frequency range of 9.4 kHz to 2.3 MHz.

◆ 10 kHz low-power oscillator for the WKT.

◆ PLL allows CPU operation up to the maximum CPU rate without the need for a high-frequency crystal. May be run from the system oscillator, the external clock input CLKIN, or the internal RC oscillator.

◆ Clock output function with divider that can reflect the crystal oscillator, the main clock, the IRC, or the watchdog oscillator.

■ Power control:

◆ Integrated PMU (Power Management Unit) to minimize power consumption.

◆ Reduced power modes: Sleep mode, Deep-sleep mode, Power-down mode, and Deep power-down mode.

◆ Wake-up from Deep-sleep and Power-down modes on activity on USART, SPI, and I2C peripherals.

◆ Timer-controlled self wake-up from Deep power-down mode.

◆ Power-On Reset (POR).

◆ Brownout detect.

■ Unique device serial number for identification.

■ Single power supply.

■ Operating temperature range −40 °C to 105 °C except for the DIP8 package, which is available for a temperature range of −40 °C to 85 °C.

■ Available as DIP8, TSSOP16, SO20, TSSOP20, and XSON16 package.

3. Applications

■ 8/16-bit applications

■ Consumer

■ Climate control

■ Lighting

■ Motor control

■ Fire and security applications

4. Ordering information

Table 1.   Ordering information

Type number	Package		Version
	Name	**Description**	
LPC810M021FN8	DIP8	plastic dual in-line package; 8 leads (300 mil)	SOT097-2
LPC811M001JDH16	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1
LPC812M101JDH16	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1
LPC812M101JD20	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1
LPC812M101JDH20	TSSOP20	plastic thin shrink small outline package; 20 leads; body width 4.4 mm	SOT360-1
LPC812M101JTB16	XSON16	plastic extremely thin small outline package; no leads; 16 terminals; body 2.5 × 3.2 × 0.5 mm	SOT1341-1

4.1   Ordering options

Table 2.   Ordering options

Type number	Flash/kB	SRAM/kB	USART	I^{2}C-bus	SPI	Comparator	GPIO	Package
LPC810M021FN8	4	1	2	1	1	1	6	DIP8
LPC811M001JDH16	8	2	2	1	1	1	14	TSSOP16
LPC812M101JDH16	16	4	3	1	2	1	14	TSSOP16
LPC812M101JD20	16	4	2	1	1	1	18	SO20
LPC812M101JDH20	16	4	3	1	2	1	18	TSSOP20
LPC812M101JTB16	16	4	3	1	2	1	14	XSON16

5. Marking

The LPC81xM devices typically have the following top-side marking:

LPC81x

xxxxx

xxxxxxxx

xxYWWxR[x]

The last two letters in the last line (field 'xR') identify the boot code version and device revision.

Table 3.   Device revision table

Revision identifier (xR)	Revision description
'1A'	Initial device revision with boot code version 13.1
'2A'	Device revision with boot code version 13.2
'4C'	Device revision with boot code version 13.4

Field 'Y' states the year the device was manufactured. Field 'WW' states the week the device was manufactured during that year.

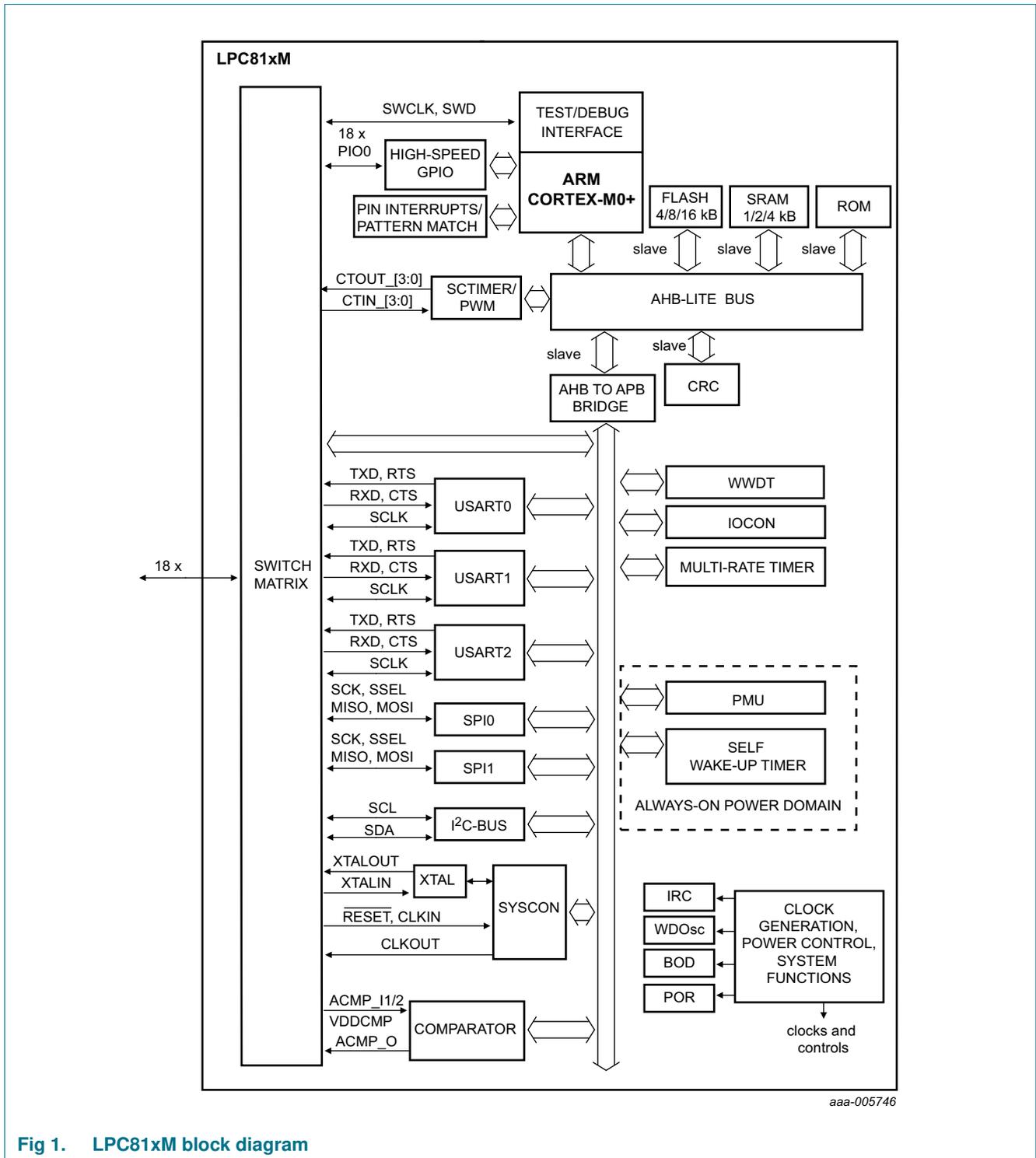**Remark:** On the TSSOP16 package, the last line includes only the date code xxYWW.

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6. Block diagram

Fig 1.   LPC81xM block diagram

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7. Pinning information

7.1 Pinning

RESET/PIO0_5 — 1 | DIP8 | 8 — PIO0_0/ACMP_I1/TDO
PIO0_4/WAKEUP/TRST — 2 | | 7 — V_{SS}
SWCLK/PIO0_3/TCK — 3 | | 6 — V_{DD}
SWDIO/PIO0_2/TMS — 4 | | 5 — PIO0_1/ACMP_I2/CLKIN/TDI

aaa-005747
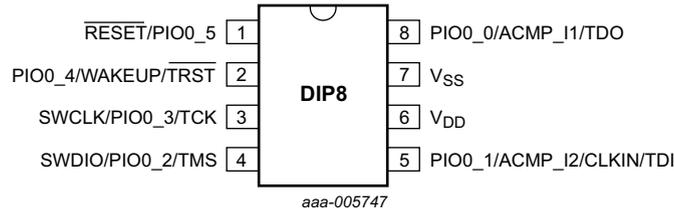
Fig 2. Pin configuration DIP8 package (LPC810M021JN8)

PIO0_13 — 1 | TSSOP16 | 16 — PIO0_0/ACMP_I1/TDO
PIO0_12 — 2 | | 15 — PIO0_6/VDDCMP
RESET/PIO0_5 — 3 | | 14 — PIO0_7
PIO0_4/WAKEUP/TRST — 4 | | 13 — V_{SS}
SWCLK/PIO0_3/TCK — 5 | | 12 — V_{DD}
SWDIO/PIO0_2/TMS — 6 | | 11 — PIO0_8/XTALIN
PIO0_11 — 7 | | 10 — PIO0_9/XTALOUT
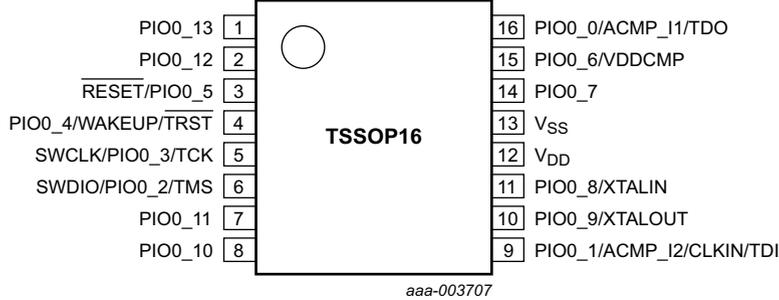PIO0_10 — 8 | | 9 — PIO0_1/ACMP_I2/CLKIN/TDI

aaa-003707

Fig 3. Pin configuration TSSOP16 package (LPC811M001JDH16 and LPC812M101JDH16)

PIO0_17 — 1 | SO20 | 20 — PIO0_14
PIO0_13 — 2 | | 19 — PIO0_0/ACMP_I1/TDO
PIO0_12 — 3 | | 18 — PIO0_6/VDDCMP
RESET/PIO0_5 — 4 | | 17 — PIO0_7
PIO0_4/WAKEUP/TRST — 5 | | 16 — V_{SS}
SWCLK/PIO0_3/TCK — 6 | | 15 — V_{DD}
SWDIO/PIO0_2/TMS — 7 | | 14 — PIO0_8/XTALIN
PIO0_11 — 8 | | 13 — PIO0_9/XTALOUT
PIO0_10 — 9 | | 12 — PIO0_1/ACMP_I2/CLKIN/TDI
PIO0_16 — 10 | | 11 — PIO0_15

aaa-003756

Fig 4. Pin configuration SO20 package (LPC812M101JD20)

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Fig 5.   Pin configuration TSSOP20 package (LPC812M101JDH20)
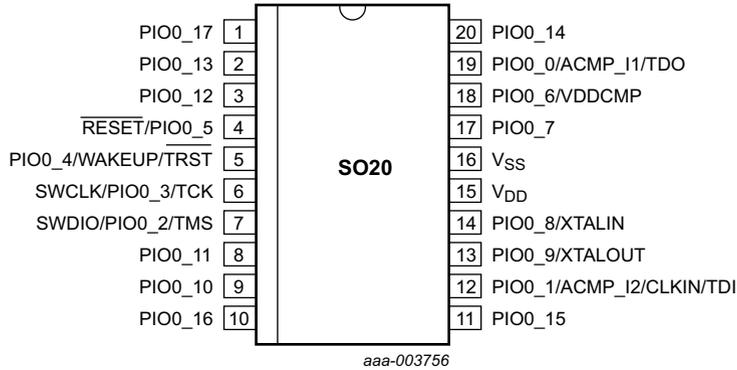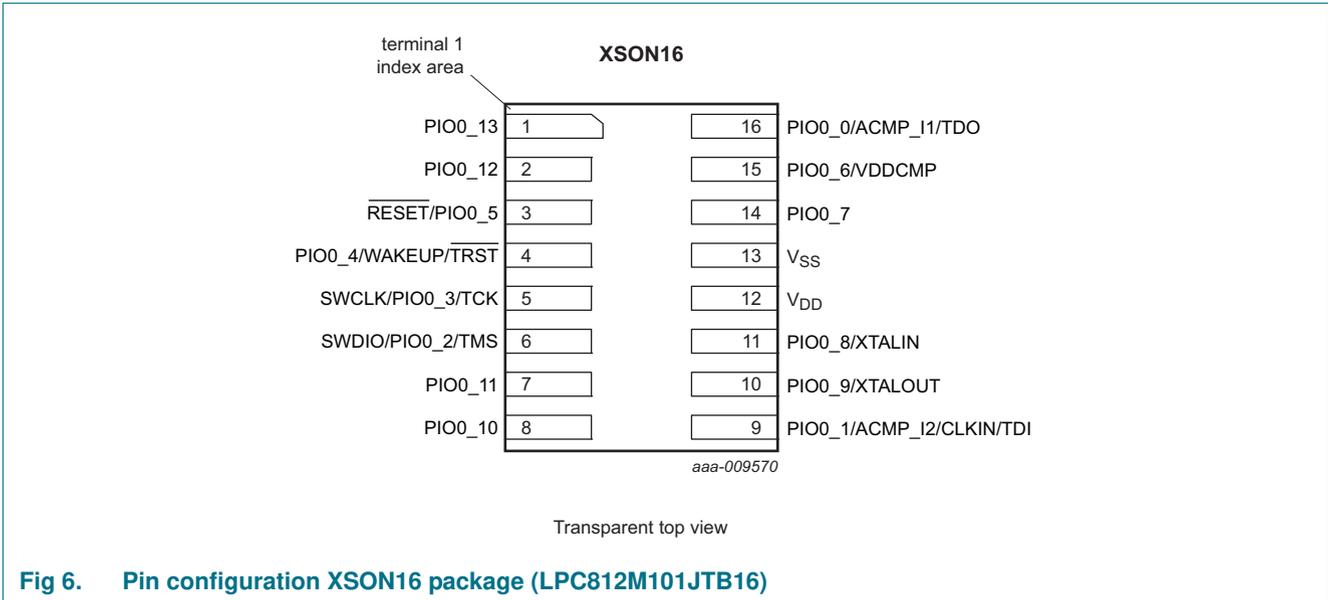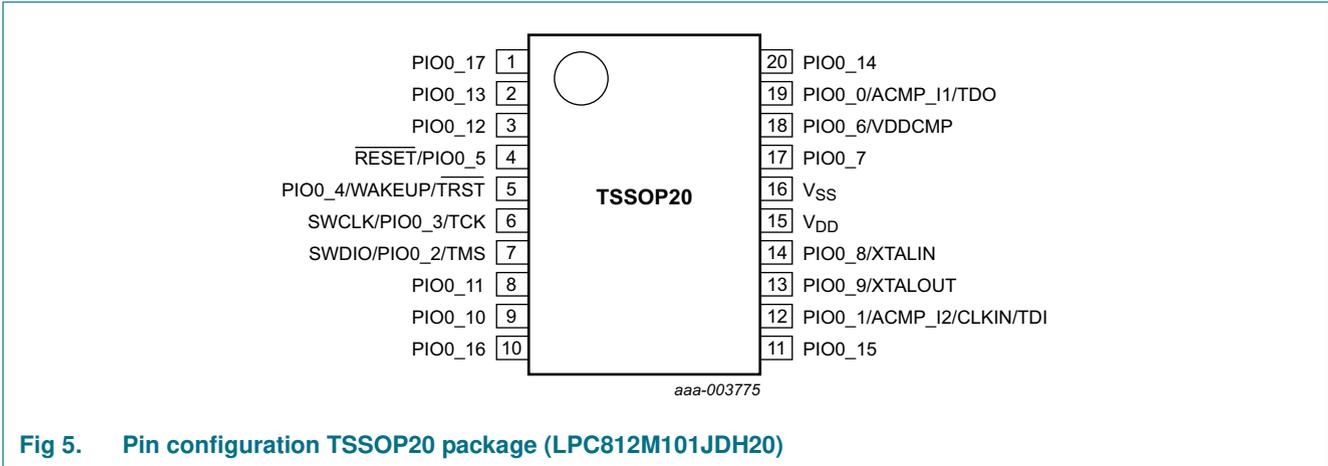

Transparent top view

Fig 6.   Pin configuration XSON16 package (LPC812M101JTB16)

7.2 Pin description

The pin description consists of two parts showing pin functions that are fixed to a certain package pin (see Table 4) and showing pin functions that can be assigned to any pin on the package through the switch matrix (see Table 5).

The pin description table in Table 4 shows the pin functions that are fixed to specific pins on each package. These fixed-pin functions are selectable between GPIO and the comparator inputs, SWD, RESET, and the XTAL pins. By default, the GPIO function is selected except on pins PIO0_2, PIO0_3, and PIO0_5. JTAG functions are available in boundary scan mode only.

Table 5 shows the the I2C, USART, SPI, and SCT pin functions, which can be assigned through the switch matrix to any pin that is not power or ground in place of the pin's fixed functions.

The following exceptions apply:

For full I2C-bus compatibility, assign the I2C functions to the open-drain pins PIO0_11 and PIO0_10.

Do not assign more than one output to any pin. However, more than one input can be assigned to a pin. Once any function is assigned to a pin, the pin's GPIO functionality is disabled.

Pin PIO0_4 triggers a wake-up from Deep power-down mode. If you need to wake up from Deep power-down mode via an external pin, do not assign any movable function to this pin.

The JTAG functions TDO, TDI, TCK, TMS, and TRST are selected on pins PIO0_0 to PIO0_4 by hardware when the part is in boundary scan mode.

Table 4.   Pin description table (fixed pins)

Symbol	SO20/ TSSOP20	TSSOP16	XSON16	DIP8		Type	Reset state [1]	Description
PIO0_0/ACMP_I1/ TDO	19	16	16	8	[5]	I/O	I; PU	**PIO0_0 —** General purpose digital input/output port 0 pin 0. In ISP mode, this is the USART0 receive pin U0_RXD. In boundary scan mode: TDO (Test Data Out).
						AI	-	**ACMP_I1 —** Analog comparator input 1.
PIO0_1/ACMP_I2/ CLKIN/TDI	12	9	9	5	[5]	I/O	I; PU	**PIO0_1 —** General purpose digital input/output pin. In boundary scan mode: TDI (Test Data In). ISP entry pin on chip versions 1A and 2A and on the DIP8 package (see Table 6). For these chip versions and packages, a LOW level on this pin during reset starts the ISP command handler. See PIO0_12 for all other packages.
						AI	-	**ACMP_I2 —** Analog comparator input 2.
						I	-	**CLKIN —** External clock input.

Table 4. **Pin description table (fixed pins)**

Symbol	SO20/ TSSOP20	TSSOP16	XSON16	DIP8		Type	Reset state [1]	Description
SWDIO/PIO0_2/TMS	7	6	6	4	[2]	I/O	I; PU	**SWDIO** — Serial Wire Debug I/O. SWDIO is enabled by default on this pin. In boundary scan mode: TMS (Test Mode Select).
						I/O	-	**PIO0_2** — General purpose digital input/output pin.
SWCLK/PIO0_3/ TCK	6	5	5	3	[2]	I/O	I; PU	**SWCLK** — Serial Wire Clock. SWCLK is enabled by default on this pin. In boundary scan mode: TCK (Test Clock).
						I/O	-	**PIO0_3** — General purpose digital input/output pin.
PIO0_4/WAKEUP/ $\overline{TRST}$	5	4	4	2	[6]	I/O	I; PU	**PIO0_4** — General purpose digital input/output pin. In ISP mode, this is the USART0 transmit pin U0_TXD. In boundary scan mode: $\overline{TRST}$ (Test Reset). This pin triggers a wake-up from Deep power-down mode. If you need to wake up from Deep power-down mode via an external pin, do not assign any movable function to this pin. This pin should be pulled HIGH externally before entering Deep power-down mode. A LOW-going pulse as short as 50 ns causes the chip to exit Deep power-down mode and wakes up the part.
$\overline{RESET}$/PIO0_5	4	3	3	1	[4]	I/O	I; PU	**RESET** — External reset input: A LOW-going pulse as short as 50 ns on this pin resets the device, causing I/O ports and peripherals to take on their default states, and processor execution to begin at address 0. In deep power-down mode, this pin must be pulled HIGH externally. The $\overline{RESET}$ pin can be left unconnected or be used as a GPIO or for any movable function if an external $\overline{RESET}$ function is not needed and the Deep power-down mode is not used.
						I	-	**PIO0_5** — General purpose digital input/output pin.
PIO0_6/VDDCMP	18	15	15	-	[9]	I/O	I; PU	**PIO0_6** — General purpose digital input/output pin.
						AI	-	**VDDCMP** — Alternate reference voltage for the analog comparator.
PIO0_7	17	14	14	-	[2]	I/O	I; PU	**PIO0_7** — General purpose digital input/output pin.
PIO0_8/XTALIN	14	11	11	-	[8]	I/O	I; PU	**PIO0_8** — General purpose digital input/output pin.
						I	-	**XTALIN** — Input to the oscillator circuit and internal clock generator circuits. Input voltage must not exceed 1.95 V.
PIO0_9/XTALOUT	13	10	10	-	[8]	I/O	I; PU	**PIO0_9** — General purpose digital input/output pin.
						O	-	**XTALOUT** — Output from the oscillator circuit.
PIO0_10	9	8	8	-	[3]	I	IA	**PIO0_10** — General purpose digital input/output pin. Assign I2C functions to this pin when true open-drain pins are needed for a signal compliant with the full I2C specification.
PIO0_11	8	7	7	-	[3]	I	IA	**PIO0_11** — General purpose digital input/output pin. Assign I2C functions to this pin when true open-drain pins are needed for a signal compliant with the full I2C specification.

Table 4.   Pin description table (fixed pins)

Symbol	SO20/ TSSOP20	TSSOP16	XSON16	DIP8		Type	Reset state [1]	Description
PIO0_12	3	2	2	-	[2]	I/O	I; PU	**PIO0_12 —** General purpose digital input/output pin. ISP entry pin on the SO20/TSSOP20/TSSOP16/XSON16 packages starting with chip version 4C (see Table 6). A LOW level on this pin during reset starts the ISP command handler. See pin PIO0_1 for the DIP8 package and chip versions 1A and 2A.
PIO0_13	2	1	1	-	[2]	I/O	I; PU	**PIO0_13 —** General purpose digital input/output pin.
PIO0_14	20	-	-	-	[7]	I/O	I; PU	**PIO0_14 —** General purpose digital input/output pin.
PIO0_15	11	-	-	-	[7]	I/O	I; PU	**PIO0_15 —** General purpose digital input/output pin.
PIO0_16	10	-	-	-	[7]	I/O	I; PU	**PIO0_16 —** General purpose digital input/output pin.
PIO0_17	1	-	-	-	[7]	I/O	I; PU	**PIO0_17 —** General purpose digital input/output pin.
V_{DD}	15	12	12	6		-	-	3.3 V supply voltage.
V_{SS}	16	13	13	7		-	-	Ground.

[1]   Pin state at reset for default function: I = Input; AI = Analog Input; O = Output; PU = internal pull-up enabled (pins pulled up to full V_{DD} level); IA = inactive, no pull-up/down enabled.

[2]   5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors and configurable hysteresis; includes high-current output driver.

[3]   True open-drain pin. I2C-bus pins compliant with the I2C-bus specification for I2C standard mode, I2C Fast-mode, and I2C Fast-mode Plus. Do not use this pad for high-speed applications such as SPI or USART. The pin requires an external pull-up to provide output functionality. When power is switched off, this pin is floating and does not disturb the I2C lines. Open-drain configuration applies to all functions on this pin.

   Remark: If this pin is not available on the package, prevent it from internally floating as follows: Set bits 10 and 11 in the GPIO DIR0 register to 1 to enable the output driver and write 1 to bits 10 and 11 in the GPIO CLR0 register to drive the outputs LOW internally.

[4]   See Figure 11 for the reset pad configuration. $\overline{RESET}$ functionality is not available in Deep power-down mode. Use the WAKEUP pin to reset the chip and wake up from Deep power-down mode. An external pull-up resistor is required on this pin for the Deep power-down mode.

[5]   5 V tolerant pin providing standard digital I/O functions with configurable modes, configurable hysteresis, and analog input. When configured as an analog input, the digital section of the pin is disabled, and the pin is not 5 V tolerant.

[6]   5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors and configurable hysteresis. In Deep power-down mode, pulling this pin LOW wakes up the chip. The wake-up pin function can be disabled and the pin can be used for other purposes, if the WKT low power oscillator is enabled for waking up the part from Deep power-down mode.

[7]   5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors and configurable hysteresis.

[8]   5 V tolerant pin providing standard digital I/O functions with configurable modes, configurable hysteresis, and analog I/O for the system oscillator. When configured as an analog I/O, the digital section of the pin is disabled, and the pin is not 5 V tolerant.

[9]   The digital part of this pin is 3 V tolerant pin due to special analog functionality. Pin provides standard digital I/O functions with configurable modes, configurable hysteresis, and an analog input. When configured as an analog input, the digital section of the pin is disabled.

Table 5.   Movable functions (assign to pins PIO0_0 to PIO_17 through switch matrix)

Function name	Type	Description
U0_TXD	O	Transmitter output for USART0.
U0_RXD	I	Receiver input for USART0.
$\overline{U0\_RTS}$	O	Request To Send output for USART0.
$\overline{U0\_CTS}$	I	Clear To Send input for USART0.

Table 5. **Movable functions (assign to pins PIO0_0 to PIO_17 through switch matrix)**

Function name	Type	Description
U0_SCLK	I/O	Serial clock input/output for USART0 in synchronous mode.
U1_TXD	O	Transmitter output for USART1.
U1_RXD	I	Receiver input for USART1.
U1_RTS	O	Request To Send output for USART1.
U1_CTS	I	Clear To Send input for USART1.
U1_SCLK	I/O	Serial clock input/output for USART1 in synchronous mode.
U2_TXD	O	Transmitter output for USART2.
U2_RXD	I	Receiver input for USART2.
U2_RTS	O	Request To Send output for USART2.
U2_CTS	I	Clear To Send input for USART2.
U2_SCLK	I/O	Serial clock input/output for USART2 in synchronous mode.
SPI0_SCK	I/O	Serial clock for SPI0.
SPI0_MOSI	I/O	Master Out Slave In for SPI0.
SPI0_MISO	I/O	Master In Slave Out for SPI0.
SPI0_SSEL	I/O	Slave select for SPI0.
SPI1_SCK	I/O	Serial clock for SPI1.
SPI1_MOSI	I/O	Master Out Slave In for SPI1.
SPI1_MISO	I/O	Master In Slave Out for SPI1.
SPI1_SSEL	I/O	Slave select for SPI1.
CTIN_0	I	SCT input 0.
CTIN_1	I	SCT input 1.
CTIN_2	I	SCT input 2.
CTIN_3	I	SCT input 3.
CTOUT_0	O	SCT output 0.
CTOUT_1	O	SCT output 1.
CTOUT_2	O	SCT output 2.
CTOUT_3	O	SCT output 3.
I2C0_SCL	I/O	I2C-bus clock input/output (open-drain if assigned to pin PIO0_10). High-current sink only if assigned to PIO0_10 and if I2C Fast-mode Plus is selected in the I/O configuration register.
I2C0_SDA	I/O	I2C-bus data input/output (open-drain if assigned to pin PIO0_11). High-current sink only if assigned to pin PIO0_11 and if I2C Fast-mode Plus is selected in the I/O configuration register.
ACMP_O	O	Analog comparator digital output.
CLKOUT	O	Clock output.
GPIO_INT_BMAT	O	Output of the pattern match engine.

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Table 6. **Pin location in ISP mode**

ISP entry pin	USART RXD	USART TXD	Marking	Boot loader version	Package
PIO0_1	PIO0_0	PIO0_4	1A	v 13.1	TSSOP20; SO20; TSSOP16; DIP8; XSON16
PIO0_1	PIO0_0	PIO0_4	2A	v 13.2	TSSOP20; SO20; TSSOP16; DIP8; XSON16
PIO0_1	PIO0_0	PIO0_4	4C and later	v 13.4 and later	DIP8
PIO0_12	PIO0_0	PIO0_4	4C and later	v 13.4 and later	TSSOP20; SO20; TSSOP16; XSON16

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8. Functional description

8.1 ARM Cortex-M0+ core

The ARM Cortex-M0+ core runs at an operating frequency of up to 30 MHz using a two-stage pipeline. Integrated in the core are the NVIC and Serial Wire Debug with four breakpoints and two watchpoints. The ARM Cortex-M0+ core supports a single-cycle I/O enabled port for fast GPIO access.

The core includes a single-cycle multiplier and a system tick timer.

8.2 On-chip flash program memory

The LPC81xM contain up to 16 kB of on-chip flash program memory. The flash memory supports a 64 Byte page size with page write and erase.

8.3 On-chip SRAM

The LPC81xM contain a total of up to 4 kB on-chip static RAM data memory.

8.4 On-chip ROM

The 8 kB on-chip ROM contains the boot loader and the following Application Programming Interfaces (API):

- In-System Programming (ISP) and In-Application Programming (IAP) support for flash programming
- Power profiles for configuring power consumption and PLL settings
- USART driver API routines
- I^2C-bus driver API routines

8.5 Nested Vectored Interrupt Controller (NVIC)

The Nested Vectored Interrupt Controller (NVIC) is an integral part of the Cortex-M0+. The tight coupling to the CPU allows for low interrupt latency and efficient processing of late arriving interrupts.

8.5.1 Features

- Controls system exceptions and peripheral interrupts.
- On the LPC81xM, the NVIC supports 32 vectored interrupts including up to 8 external interrupt inputs selectable from all GPIO pins.
- Four programmable interrupt priority levels with hardware priority level masking.
- Software interrupt generation using the ARM exceptions SVCall and PendSV.
- Relocatable interrupt vector table using vector table offset register.

8.5.2 Interrupt sources

Each peripheral device has one interrupt line connected to the NVIC but may have several interrupt flags. Individual interrupt flags may also represent more than one interrupt source.

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Up to eight pins, regardless of the selected function, can be programmed to generate an interrupt on a level, a rising or falling edge, or both. The interrupt generating pins can be selected from all digital or mixed digital/analog pins. The pin interrupt/pattern match block controls the edge or level detection mechanism.

8.6 System tick timer

The ARM Cortex-M0+ includes a 24-bit system tick timer (SysTick) that is intended to generate a dedicated SysTick exception at a fixed time interval (typically 10 ms).

8.7 Memory map

The LPC81xM incorporates several distinct memory regions. Figure 7 shows the overall map of the entire address space from the user program viewpoint following reset. The interrupt vector area supports address remapping.

The ARM private peripheral bus includes the ARM core registers for controlling the NVIC, the system tick timer (SysTick), and the reduced power modes.
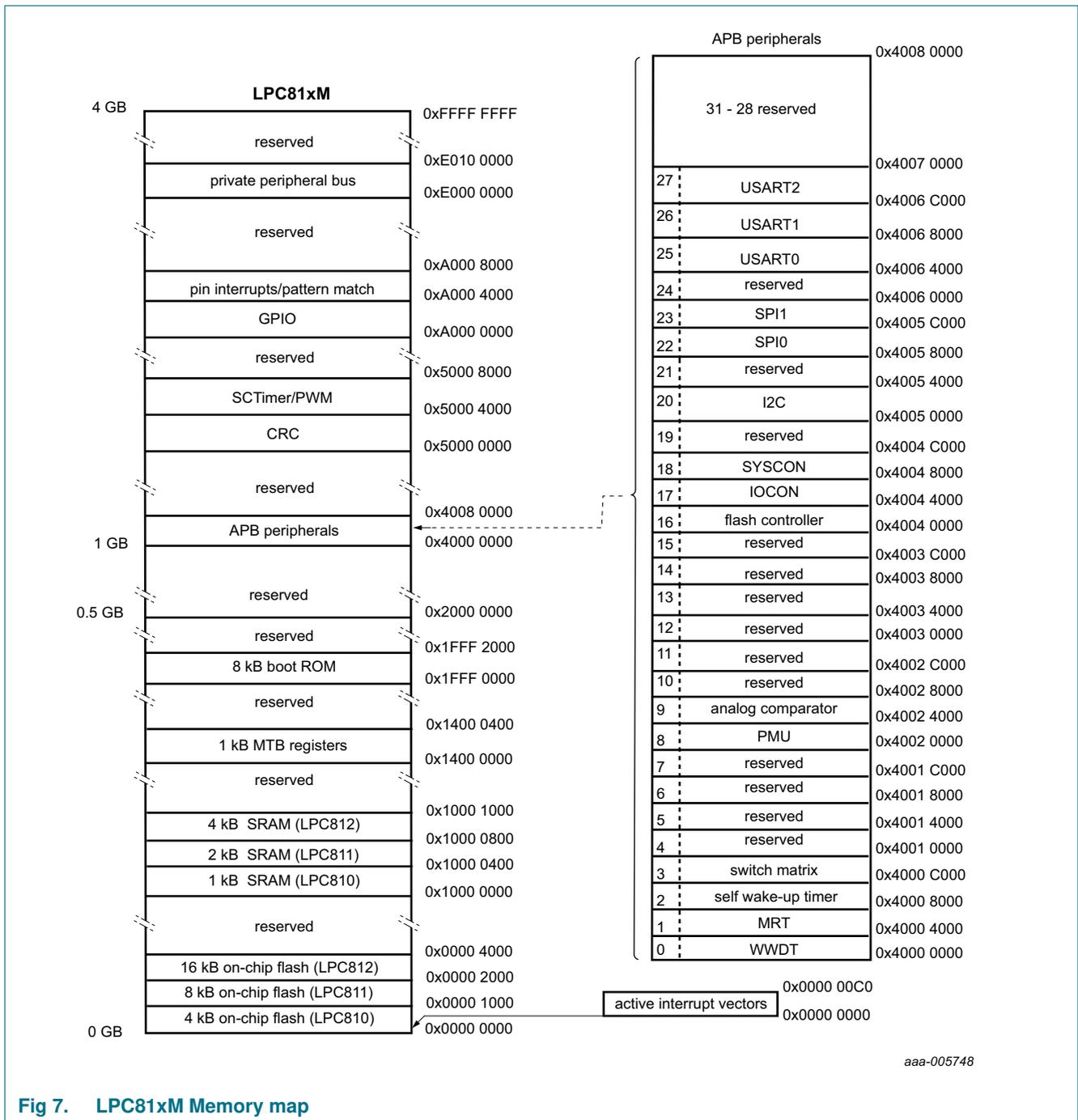
Fig 7.   LPC81xM Memory map

8.8   I/O configuration

The IOCON block controls the configuration of the I/O pins. Each digital or mixed digital/analog pin with the PIO0_n designator (except the true open-drain pins PIO0_10 and PIO0_11) in Table 4 can be configured as follows:

- Enable or disable the weak internal pull-up and pull-down resistors.

- Select a pseudo open-drain mode. The input cannot be pulled up above V_{DD}. This pin is not 5 V tolerant when $V_{DD} = 0$.

- Program the input glitch filter with different filter constants using one of the IOCON divided clock signals (IOCONCLKCDIV, see Figure 10 "LPC81xM clock generation"). You can also bypass the glitch filter.

- Invert the input signal.

- Hysteresis can be enabled or disabled.

- For pins PIO0_10 and PIO0_11, select the I2C-mode and output driver for standard digital operation, for I2C standard and fast modes, or for I2C Fast mode+.

- On mixed digital/analog pins, enable the analog input mode. Enabling the analog mode disconnects the digital functionality.

Remark: The functionality of each I/O pin is flexible and is determined entirely through the switch matrix. See Section 8.9 for details.

8.8.1 Standard I/O pad configuration

Figure 8 shows the possible pin modes for standard I/O pins with analog input function:

- Digital output driver with configurable open-drain output
- Digital input: Weak pull-up resistor (PMOS device) enabled/disabled
- Digital input: Weak pull-down resistor (NMOS device) enabled/disabled
- Digital input: Repeater mode enabled/disabled
- Digital input: Input glitch filter selectable on all pins
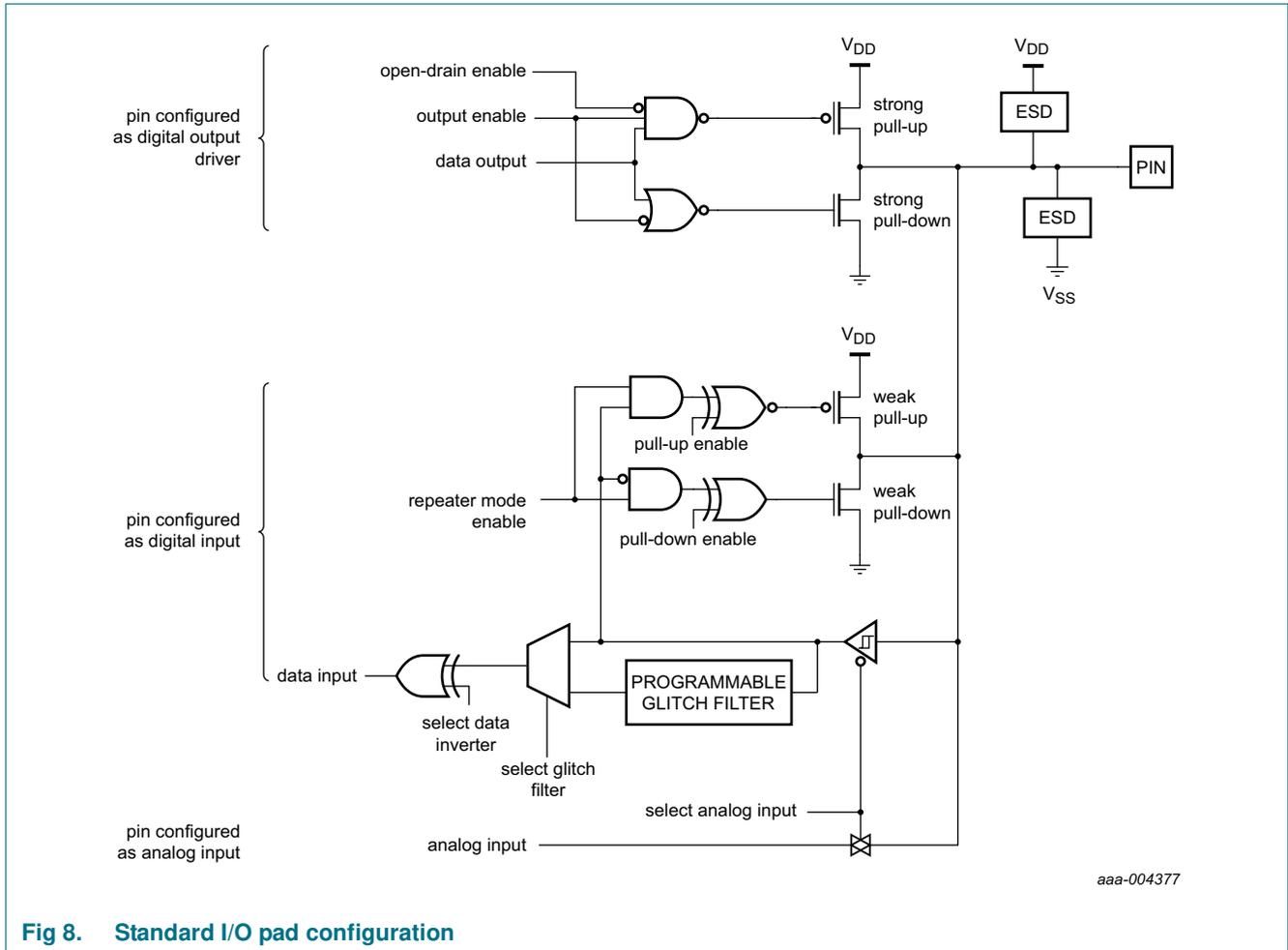- Analog input

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Fig 8.   Standard I/O pad configuration

8.9 Switch Matrix (SWM)

The switch matrix controls the function of each digital or mixed analog/digital pin in a highly flexible way by allowing to connect many functions like the USART, SPI, SCT, and I2C functions to any pin that is not power or ground. These functions are called movable functions and are listed in Table 5.

Functions that need specialized pads like the oscillator pins XTALIN and XTALOUT can be enabled or disabled through the switch matrix. These functions are called fixed-pin functions and cannot move to other pins. The fixed-pin functions are listed in Table 4. If a fixed-pin function is disabled, any other movable function can be assigned to this pin.

8.10 Fast General-Purpose parallel I/O (GPIO)

Device pins that are not connected to a specific peripheral function are controlled by the GPIO registers. Pins may be dynamically configured as inputs or outputs. Multiple outputs can be set or cleared in one write operation.

LPC81xM use accelerated GPIO functions:

- GPIO registers are located on the ARM Cortex M0+ IO bus for fastest possible single-cycle I/O timing, allowing GPIO toggling with rates of up to 15 MHz.

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- An entire port value can be written in one instruction.

- Mask, set, and clear operations are supported for the entire port.

All GPIO port pins are fixed-pin functions that are enabled or disabled on the pins by the switch matrix. Therefore each GPIO port pin is assigned to one specific pin and cannot be moved to another pin. Except for pins SWDIO/PIO0_2, SWCLK/PIO0_3, and RESET/PIO0_5, the switch matrix enables the GPIO port pin function by default.

8.10.1 Features

- Bit level port registers allow a single instruction to set and clear any number of bits in one write operation.

- Direction control of individual bits.

- All I/O default to inputs with internal pull-up resistors enabled after reset - except for the I^{2}C-bus true open-drain pins PIO0_2 and PIO0_3.

- Pull-up/pull-down configuration, repeater, and open-drain modes can be programmed through the IOCON block for each GPIO pin (see Figure 8).

-

8.11 Pin interrupt/pattern match engine

The pin interrupt block configures up to eight pins from all digital pins for providing eight external interrupts connected to the NVIC.

The pattern match engine can be used, in conjunction with software, to create complex state machines based on pin inputs.

Any digital pin, independently of the function selected through the switch matrix, can be configured through the SYSCON block as input to the pin interrupt or pattern match engine. The registers that control the pin interrupt or pattern match engine are located on the IO+ bus for fast single-cycle access.

8.11.1 Features

- Pin interrupts

  - Up to eight pins can be selected from all digital pins as edge- or level-sensitive interrupt requests. Each request creates a separate interrupt in the NVIC.

  - Edge-sensitive interrupt pins can interrupt on rising or falling edges or both.

  - Level-sensitive interrupt pins can be HIGH- or LOW-active.

  - Pin interrupts can wake up the LPC81xM from sleep mode, deep-sleep mode, and power-down mode.

- Pin interrupt pattern match engine

  - Up to eight pins can be selected from all digital pins to contribute to a boolean expression. The boolean expression consists of specified levels and/or transitions on various combinations of these pins.

  - Each minterm (product term) comprising the specified boolean expression can generate its own, dedicated interrupt request.

  - Any occurrence of a pattern match can be programmed to also generate an RXEV notification to the ARM CPU. The RXEV signal can be connected to a pin.

– The pattern match engine does not facilitate wake-up.

8.12 USART0/1/2

Remark: USART0 and USART1 are available on all LPC800 parts. USART2 is available on parts LPC812M101JTB16, LPC812M101JDH16, and LPC812M101JDH20 only.

All USART functions are movable functions and are assigned to pins through the switch matrix.

8.12.1 Features

- Maximum bit rates of 1.875 Mbit/s in asynchronous mode and 10 Mbit/s in synchronous mode for USART functions connected to all digital pins except PIO0_10 and PIO0_11.
- 7, 8, or 9 data bits and 1 or 2 stop bits
- Synchronous mode with master or slave operation. Includes data phase selection and continuous clock option.
- Multiprocessor/multidrop (9-bit) mode with software address compare. (RS-485 possible with software address detection and transceiver direction control.)
- Parity generation and checking: odd, even, or none.
- One transmit and one receive data buffer.
- RTS/CTS for hardware signaling for automatic flow control. Software flow control can be performed using Delta CTS detect, Transmit Disable control, and any GPIO as an RTS output.
- Received data and status can optionally be read from a single register
- Break generation and detection.
- Receive data is 2 of 3 sample "voting". Status flag set when one sample differs.
- Built-in Baud Rate Generator.
- A fractional rate divider is shared among all UARTs.
- Interrupts available for Receiver Ready, Transmitter Ready, Receiver Idle, change in receiver break detect, Framing error, Parity error, Overrun, Underrun, Delta CTS detect, and receiver sample noise detected.
- Separate data and flow control loopback modes for testing.
- Supported by on-chip ROM API.

8.13 SPI0/1

Remark: SPI0 is available on all LPC800 parts. SPI1 is available on parts LPC812M101JDH16 and LPC812M101JDH20 only.

All SPI functions are movable functions and are assigned to pins through the switch matrix.

8.13.1 Features

- Maximum data rates of 30 Mbit/s in master mode and 25 Mbit/s in slave mode for SPI functions connected to all digital pins except PIO0_10 and PIO0_11.

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- Data frames of 1 to 16 bits supported directly. Larger frames supported by software.

- Master and slave operation.

- Data can be transmitted to a slave without the need to read incoming data. This can be useful while setting up an SPI memory.

- Control information can optionally be written along with data. This allows very versatile operation, including "any length" frames.

- One Slave Select input/output with selectable polarity and flexible usage.

Remark: Texas Instruments SSI and National Microwire modes are not supported.

8.14 I2C-bus interface

The I^{2}C-bus is bidirectional for inter-IC control using only two wires: a serial clock line (SCL) and a serial data line (SDA). Each device is recognized by a unique address and can operate as either a receiver-only device (e.g., an LCD driver) or a transmitter with the capability to both receive and send information (such as memory). Transmitters and/or receivers can operate in either master or slave mode, depending on whether the chip has to initiate a data transfer or is only addressed. The I^{2}C is a multi-master bus and can be controlled by more than one bus master connected to it.

The I2C-bus functions are movable functions and can be assigned through the switch matrix to any pin. However, only the true open-drain PIO0_10 and PIO0_11 provide the electrical characteristics to support the full I2C-bus specification (see Ref. 1).

8.14.1 Features

- Supports standard and fast mode with data rates of up to 400 kbit/s.

- Independent Master, Slave, and Monitor functions.

- Supports both Multi-master and Multi-master with Slave functions.

- Multiple I^{2}C slave addresses supported in hardware.

- One slave address can be selectively qualified with a bit mask or an address range in order to respond to multiple I^{2}C bus addresses.

- 10-bit addressing supported with software assist.

- Supports SMBus.

- Supported by on-chip ROM API.

- If the I2C functions are connected to the true open-drain pins (PIO0_10 and PIO0_11), the I2C supports the full I2C-bus specification:

  - Fail-safe operation: When the power to an I^{2}C-bus device is switched off, the SDA and SCL pins connected to the I^{2}C-bus are floating and do not disturb the bus.

  - Supports Fast-mode Plus with bit rates up to 1 Mbit/s.

8.15 State-Configurable Timer/PWM (SCTimer/PWM)

The state configurable timer (SCTimer/PWM or SCT) can perform basic 16-bit and 32-bit timer/counter functions with match outputs and external and internal capture inputs. In addition, the SCTimer/PWM can employ up to two different programmable states, which can change under the control of events, to provide complex timing patterns.

All inputs and outputs of the SCTimer/PWM are movable functions and are assigned to pins through the switch matrix.

8.15.1 Features

- Two 16-bit counters or one 32-bit counter.
- Counters clocked by bus clock or selected input.
- Up counters or up-down counters.
- State variable allows sequencing across multiple counter cycles.
- The following conditions define an event: a counter match condition, an input (or output) condition, a combination of a match and/or and input/output condition in a specified state, and the count direction.
- Events control outputs, interrupts, and the SCT states.
    - Match register 0 can be used as an automatic limit.
    - In bi-directional mode, events can be enabled based on the count direction.
    - Match events can be held until another qualifying event occurs.
- Selected events can limit, halt, start, or stop a counter.
- Supports:
    - 4 inputs
    - 4 outputs
    - 5 match/capture registers
    - 6 events
    - 2 states

8.16 Multi-Rate Timer (MRT)

The Multi-Rate Timer (MRT) provides a repetitive interrupt timer with four channels. Each channel can be programmed with an independent time interval, and each channel operates independently from the other channels.

8.16.1 Features

- 31-bit interrupt timer
- Four channels independently counting down from individually set values
- Bus stall, repeat and one-shot interrupt modes

8.17 Windowed WatchDog Timer (WWDT)

The watchdog timer resets the controller if software fails to periodically service it within a programmable time window.

8.17.1 Features

- Internally resets chip if not periodically reloaded during the programmable time-out period.
- Optional windowed operation requires reload to occur between a minimum and maximum time period, both programmable.

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- Optional warning interrupt can be generated at a programmable time prior to watchdog time-out.
- Enabled by software but requires a hardware reset or a watchdog reset/interrupt to be disabled.
- Incorrect feed sequence causes reset or interrupt if enabled.
- Flag to indicate watchdog reset.
- Programmable 24-bit timer with internal prescaler.
- Selectable time period from ($T_{cy(WDCLK)} \times 256 \times 4$) to ($T_{cy(WDCLK)} \times 2^{24} \times 4$) in multiples of $T_{cy(WDCLK)} \times 4$.
- The Watchdog Clock (WDCLK)is generated by a the dedicated watchdog oscillator (WDOSC).

8.18 Self Wake-up Timer (WKT)

The self wake-up timer is a 32-bit, loadable down-counter. Writing any non-zero value to this timer automatically enables the counter and launches a count-down sequence. When the counter is used as a wake-up timer, this write can occur just prior to entering a reduced power mode.

8.18.1 Features

- 32-bit loadable down-counter. Counter starts automatically when a count value is loaded. Time-out generates an interrupt/wake up request.
- The WKT resides in a separate, always-on power domain.
- The WKT supports two clock sources: the low-power oscillator and the IRC. The low-power oscillator is located in the always-on power domain, so it can be used as the clock source in Deep power-down mode.
- The WKT can be used for waking up the part from any reduced power mode, including Deep power-down mode, or for general-purpose timing.

8.19 Analog comparator (ACMP)

The analog comparator with selectable hysteresis can compare voltage levels on external pins and internal voltages.

After power-up and after switching the input channels of the comparator, the output of the voltage ladder must be allowed to settle to its stable value before it can be used as a comparator reference input. Settling times are given in Table 23.

The analog comparator output is a movable function and is assigned to a pin through the switch matrix. The comparator inputs and the voltage reference are enabled or disabled on pins PIO0_0 and PIO0_1 through the switch matrix.
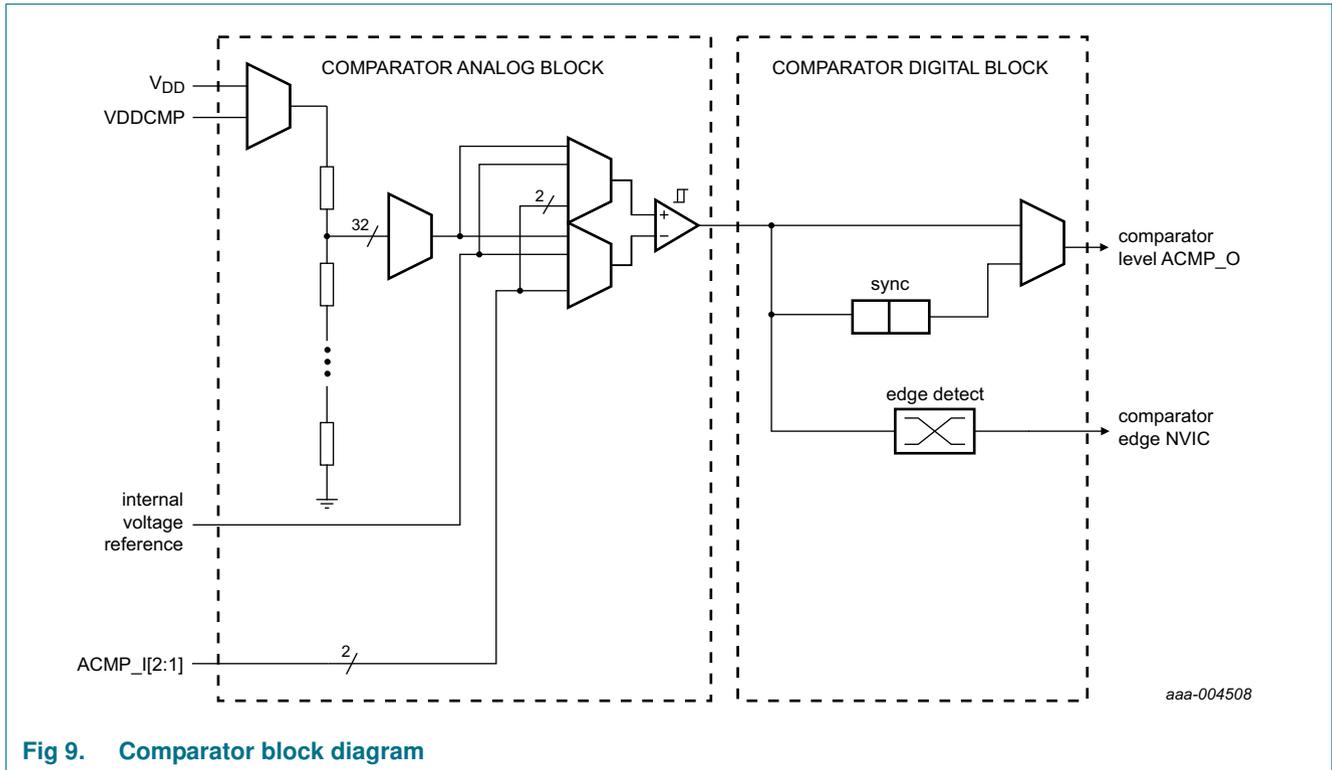
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Fig 9.   Comparator block diagram

8.19.1 Features

- Selectable 0 mV, 10 mV ($\pm$ 5 mV), and 20 mV ($\pm$ 10 mV), 40 mV ($\pm$ 20 mV) input hysteresis.

- Two selectable external voltages (V_{DD} or VDDCMP on pin PIO0_6); fully configurable on either positive or negative input channel.

- Internal voltage reference from band gap selectable on either positive or negative input channel.

- 32-stage voltage ladder with the internal reference voltage selectable on either the positive or the negative input channel.

- Voltage ladder source voltage is selectable from an external pin or the main 3.3 V supply voltage rail.

- Voltage ladder can be separately powered down for applications only requiring the comparator function.

- Interrupt output is connected to NVIC.

- Comparator level output is connected to output pin ACMP_O.

- The comparator output can be routed internally to the SCT input through the switch matrix.

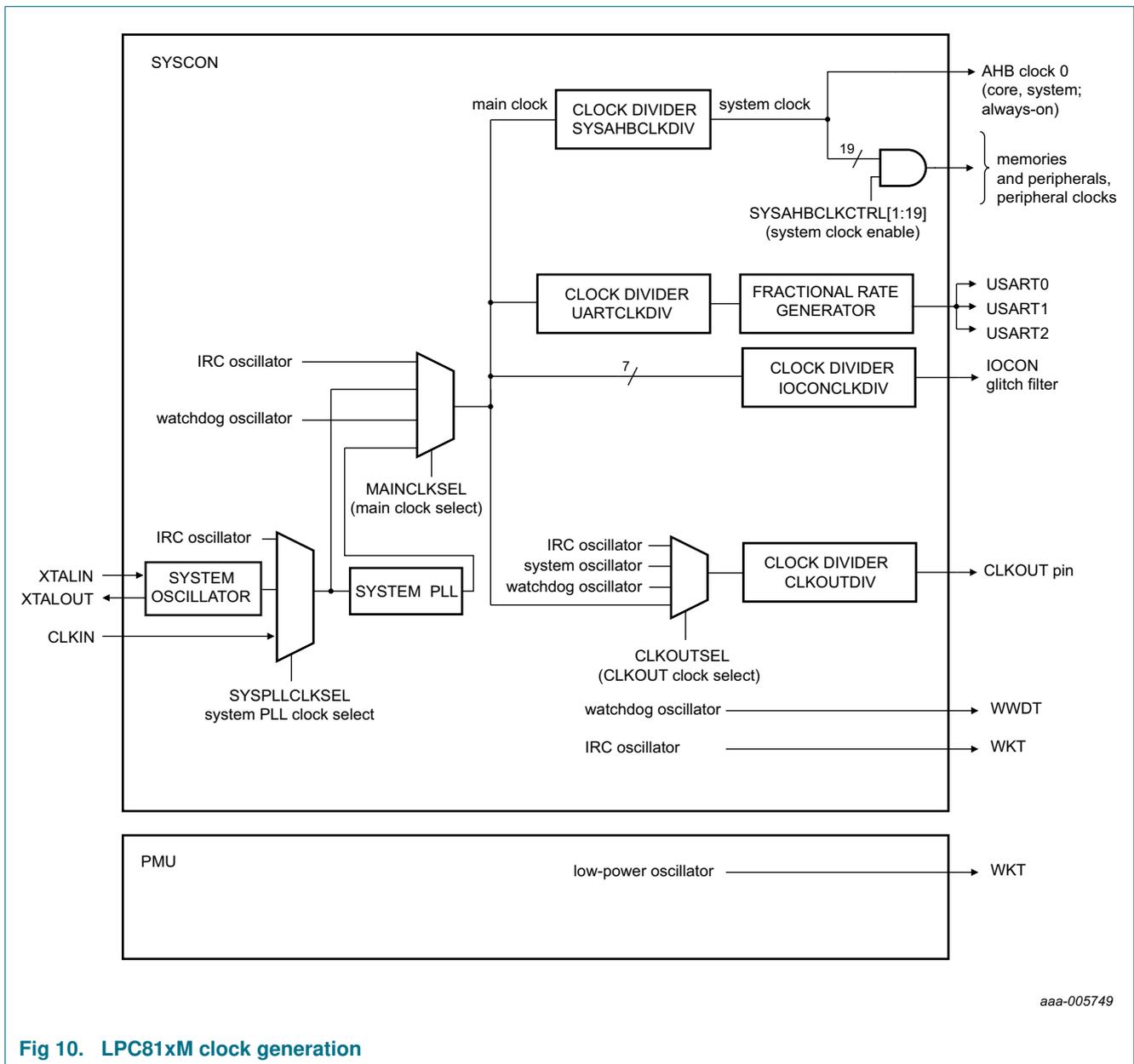## 8.20 Clocking and power control

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Fig 10. LPC81xM clock generation

8.20.1 Crystal and internal oscillators

The LPC81xM include four independent oscillators:

1. The crystal oscillator (SysOsc) operating at frequencies between 1 MHz and 25 MHz.

2. The internal RC Oscillator (IRC) with a fixed frequency of 12 MHz, trimmed to 1% accuracy.

3. The internal low-power, low-frequency Oscillator with a nominal frequency of 10 kHz with 40% accuracy for use with the self wake-up timer.

4. The dedicated Watchdog Oscillator (WDOsc) with a programmable nominal frequency between 9.4 kHz and 2.3 MHz with 40% accuracy.

Each oscillator, except the low-frequency oscillator, can be used for more than one purpose as required in a particular application.

Following reset, the LPC81xM will operate from the IRC until switched by software. This allows systems to operate without any external crystal and the bootloader code to operate at a known frequency.

See Figure 10 for an overview of the LPC81xM clock generation.

8.20.1.1 Internal RC Oscillator (IRC)

The IRC may be used as the clock source for the WWDT, and/or as the clock that drives the PLL and subsequently the CPU. The nominal IRC frequency is 12 MHz. The IRC is trimmed to 1.5 % accuracy over the entire voltage and temperature range.

The IRC can be used as a clock source for the CPU with or without using the PLL. The IRC frequency can be boosted to a higher frequency, up to the maximum CPU operating frequency, by the system PLL.

Upon power-up or any chip reset, the LPC81xM use the IRC as the clock source. Software may later switch to one of the other available clock sources.

8.20.1.2 Crystal Oscillator (SysOsc)

The crystal oscillator can be used as the clock source for the CPU, with or without using the PLL.

The SysOsc operates at frequencies of 1 MHz to 25 MHz. This frequency can be boosted to a higher frequency, up to the maximum CPU operating frequency, by the system PLL.

8.20.1.3 Internal Low-power Oscillator and Watchdog Oscillator (WDOsc)

The nominal frequency of the WDOsc is programmable between 9.4 kHz and 2.3 MHz. The frequency spread over silicon process variations is ± 40%.

The WDOsc is a dedicated oscillator for the windowed WWDT.

The internal low-power 10 kHz (± 40% accuracy) oscillator serves a the clock input to the WKT. This oscillator can be configured to run in all low power modes.

8.20.2 Clock input

An external clock source can be supplied on the selected CLKIN pin. When selecting a clock signal for the CLKIN pin, follow the specifications for digital I/O pins in Table 9 "Static characteristics" and Table 16 "Dynamic characteristics: I/O pins[1]".

An 1.8 V external clock source can be supplied on the XTALIN pins to the system oscillator limiting the voltage of this signal ((see Section 14.2).

The maximum frequency for both clock signals is 25 MHz.

8.20.3 System PLL

The PLL accepts an input clock frequency in the range of 10 MHz to 25 MHz. The input frequency is multiplied up to a high frequency with a Current Controlled Oscillator (CCO). The multiplier can be an integer value from 1 to 32. The CCO operates in the range of 156 MHz to 320 MHz, so there is an additional divider in the loop to keep the CCO within its frequency range while the PLL is providing the desired output frequency. The output