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LPC84x

32-bit Arm® Cortex®-M0+ microcontroller; up to 64 KB flash and 16 KB SRAM; FAIM memory; 12-bit ADC; 10-bit DACs; Comparator; Capacitive Touch Interface

Rev. 1.7 — 27 February 2018 Product data sheet

1. General description

The LPC84x are an Arm Cortex-M0+ based, low-cost 32-bit MCU family operating at CPU frequencies of up to 30 MHz. The LPC84x support up to 64 KB of flash memory and 16 KB of SRAM.

The peripheral complement of the LPC84x includes a CRC engine, four I^2C-bus interfaces, up to five USARTs, up to two SPI interfaces, Capacitive Touch Interface, one multi-rate timer, self-wake-up timer, SCTimer/PWM, one general purpose 32-bit counter/timer, a DMA, one 12-bit ADC, two 10-bit DACs, one analog comparator, function-configurable I/O ports through a switch matrix, an input pattern match engine, and up to 54 general-purpose I/O pins.

For additional documentation related to the LPC84x parts, see Section 18.

2. Features and benefits

- System:
  - Arm Cortex-M0+ processor (revision r0p1), running at frequencies of up to 30 MHz with single-cycle multiplier and fast single-cycle I/O port.
  - Arm Cortex-M0+ built-in Nested Vectored Interrupt Controller (NVIC).
  - System tick timer.
  - AHB multilayer matrix.
  - Serial Wire Debug (SWD) with four break points and two watch points. JTAG boundary scan (BSDL) supported.
  - Micro Trace Buffer (MTB).
- Memory:
  - Up to 64 KB on-chip flash programming memory with 64 Byte page write and erase.
  - Fast Initialization Memory (FAIM) allowing the user to configure chip behavior on power-up.
  - Code Read Protection (CRP)
  - Up to 16 KB SRAM consisting of two 8 KB contiguous SRAM banks. One 8 KB of SRAM can be used for MTB.
  - Bit-band addressing supported to permit atomic operations to modify a single bit.
- ROM API support:
  - Boot loader.
  - Supports Flash In-Application Programming (IAP).

- Supports In-System Programming (ISP) through USART, SPI, and I^2C.
- FAIM API.
- FRO API.
- On-chip ROM APIs for integer divide.

- Digital peripherals:
  - High-speed GPIO interface connected to the Arm Cortex-M0+ I/O bus with up to 54 General-Purpose I/O (GPIO) pins with configurable pull-up/pull-down resistors, programmable open-drain mode, input inverter, and digital filter. GPIO direction control supports independent set/clear/toggle of individual bits.
  - High-current source output driver (20 mA) on four pins.
  - High-current sink driver (20 mA) on two true open-drain pins.
  - GPIO interrupt generation capability with boolean pattern-matching feature on eight GPIO inputs.
  - Switch matrix for flexible configuration of each I/O pin function.
  - CRC engine.
  - DMA with 25 channels and 13 trigger inputs.
  - Capacitive Touch Interface.
- Timers:
  - One SCTimer/PWM with five input and seven output functions (including capture and match) for timing and PWM applications. Inputs and outputs can be routed to or from external pins and internally to or from selected peripherals. Internally, the SCTimer/PWM supports 8 match/captures, 8 events, and 8 states.
  - One 32-bit general purpose counter/timer, with four match outputs and three capture inputs. Supports PWM mode, external count, and DMA.
  - Four channel Multi-Rate Timer (MRT) for repetitive interrupt generation at up to four programmable, fixed rates.
  - Self-Wake-up Timer (WKT) clocked from either Free Running Oscillator (FRO), a low-power, low-frequency internal oscillator, or an external clock input in the always-on power domain.
  - Windowed Watchdog timer (WWDT).
- Analog peripherals:
  - One 12-bit ADC with up to 12 input channels with multiple internal and external trigger inputs and with sample rates of up to 1.2 Msamples/s. The ADC supports two independent conversion sequences.
  - Comparator with five input pins and external or internal reference voltage.
  - Two 10-bit DACs.
- Serial peripherals:
  - Five USART interfaces with pin functions assigned through the switch matrix and two fractional baud rate generators.
  - Two SPI controllers with pin functions assigned through the switch matrix.
  - Four I^2C-bus interfaces. One I^2C supports Fast-mode Plus with 1 Mbit/s data rates on two true open-drain pins and listen mode. Three I^2Cs support data rates up to 400 kbit/s on standard digital pins.
- Clock generation:

- Free Running Oscillator (FRO). This oscillator provides a selectable 18 MHz, 24 MHz, and 30 MHz outputs that can be used as a system clock. Also, these outputs can be divided down to 1.125 MHz, 1.5 MHz, 1.875 MHz, 9 MHz, 12 MHz, and 15 MHz for system clock. The FRO is trimmed to ±1 % accuracy over the entire voltage and temperature range of 0 C to 70 C.
- Low power boot at 1.5 MHz using FAIM memory.
- External clock input for clock frequencies of up to 25 MHz.
- Crystal oscillator with an operating range of 1 MHz to 25 MHz.
- Low power oscillator can be used as a clock source to the watchdog timer.
- Programmable watchdog oscillator with a frequency range of 9.4 kHz to 2.3 MHz.
- PLL allows CPU operation up to the maximum CPU rate without the need for a high-frequency crystal. May be run from the system oscillator, the external clock input, or the internal FRO.
- Clock output function with divider that can reflect all internal clock sources.

- Power control:
  - Reduced power modes: sleep mode, deep-sleep mode, power-down mode, and deep power-down mode.
  - Wake-up from deep-sleep and power-down modes on activity on USART, SPI, and I2C peripherals.
  - Timer-controlled self wake-up from deep power-down mode.
  - Power-On Reset (POR).
  - Brownout detect (BOD).
- Unique device serial number for identification.
- Single power supply (1.8 V to 3.6 V).
- Operating temperature range -40 °C to +105 °C.
- Available in LQFP64, LQFP48, HVQFN48, and HVQFN33 packages.

3. Applications

- Sensor gateways
- Industrial
- Gaming controllers
- 8/16-bit applications
- Consumer
- Climate control
- Simple motor control
- Portables and wearables
- Lighting
- Motor control
- Fire and security applications

4. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
LPC845M301JBD64	LQFP64	Plastic low profile quad flat package; 64 leads; body 10× 10 × 1.4 mm	SOT314-2
LPC845M301JBD48	LQFP48	Plastic low profile quad flat package; 48 leads; body 7× 7 × 1.4 mm	SOT313-2
LPC845M301JHI48	HVQFN48	HVQFN: plastic thermal enhanced very thin quad flat package; no leads; 48 terminals; body 7× 7 × 0.85 mm	SOT619-1
LPC845M301JHI33	HVQFN33	HVQFN: plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 5 × 5 × 0.85 mm	SOT617-11
LPC844M201JBD64	LQFP64	Plastic low profile quad flat package; 64 leads; body 10× 10 × 1.4 mm	SOT314-2
LPC844M201JBD48	LQFP48	Plastic low profile quad flat package; 48 leads; body 7× 7 × 1.4 mm	SOT313-2
LPC844M201JHI48	HVQFN48	HVQFN: plastic thermal enhanced very thin quad flat package; no leads; 48 terminals; body 7 × 7 × 0.85 mm	SOT619-1
LPC844M201JHI33	HVQFN33	HVQFN: plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 5 × 5 × 0.85 mm	SOT617-11

4.1 Ordering options

Table 2. Ordering options

Type number	Flash/KB	SRAM/KB	USART	I^2C	SPI	DAC	Capacitive Touch	GPIO	Package
LPC845M301JBD64	64	16	5	4	2	2	yes	54	LQFP64
LPC845M301JBD48	64	16	5	4	2	2	yes	42	LQFP48
LPC845M301JHI48	64	16	5	4	2	2	yes	42	HVQFN48
LPC845M301JHI33	64	16	5	4	2	1	-	29	HVQFN33
LPC844M201JBD64	64	8	2	2	2	-	-	54	LQFP64
LPC844M201JBD48	64	8	2	2	2	-	-	42	LQFP48
LPC844M201JHI48	64	8	2	2	2	-	-	42	HVQFN48
LPC844M201JHI33	64	8	2	2	2	-	-	29	HVQFN33

5. Marking

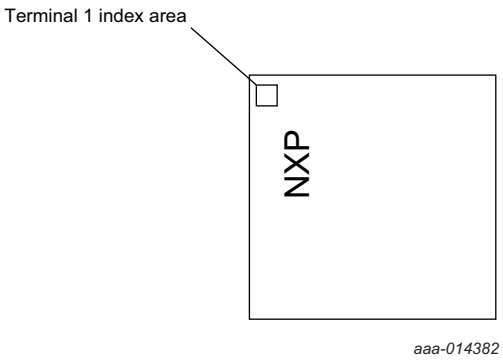


Fig 1. HVQFN48, HVQFN33 package marking

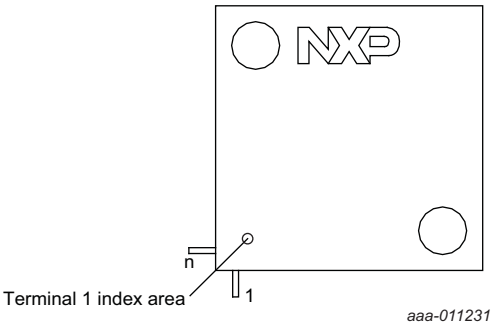


Fig 2. LQFP64, LQFP48 package marking

The LPC84x LQFP64 and LQFP48 packages have the following top-side marking:

- First line: LPC84xMy01
  - y: 3 or 2
- Second line: xxxxxx
- Third line: xxxyywwx[R]x
  - yyww: Date code with yy = year and ww = week.
  - xR = Boot code version and device revision.

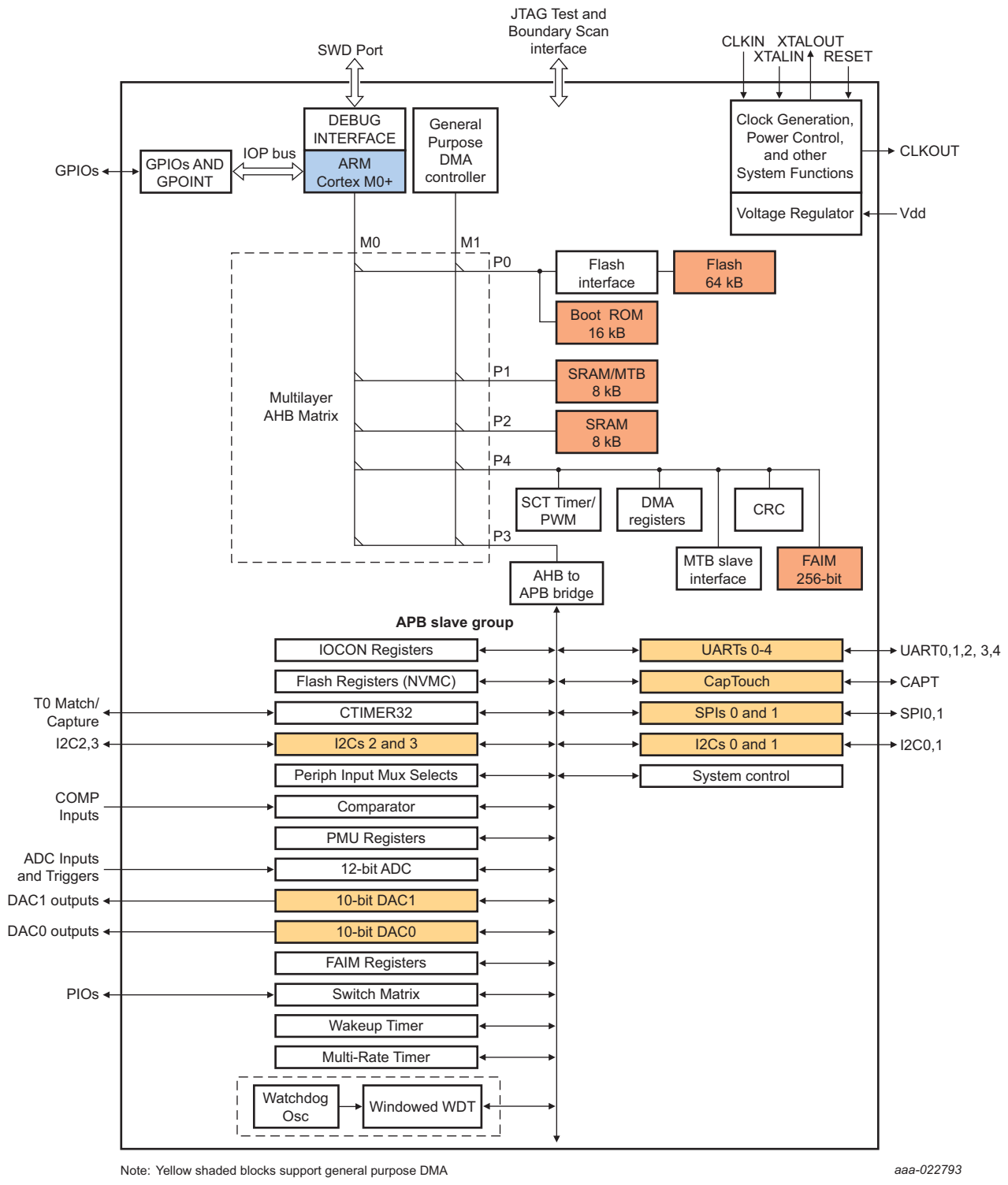
The LPC84x HVQFN48 and HVQFN33 packages have the following top-side marking:

- First line: LPC84xMy01
  - y: 3 or 2
- Second line: xxxxxx
- Third line: xxxyywwx[R]x
  - yyww: Date code with yy = year and ww = week.
  - xR = Boot code version and device revision.

Table 3. Device revision table

Revision identifier (R)	Revision description
1A	Initial device revision with Boot ROM version 13.1

6. Block diagram



Gray-shaded blocks show peripherals that can provide hardware triggers or fixed DMA requests for DMA transfers.

Fig 3. LPC84x block diagram

7. Pinning information

7.1 Pinning

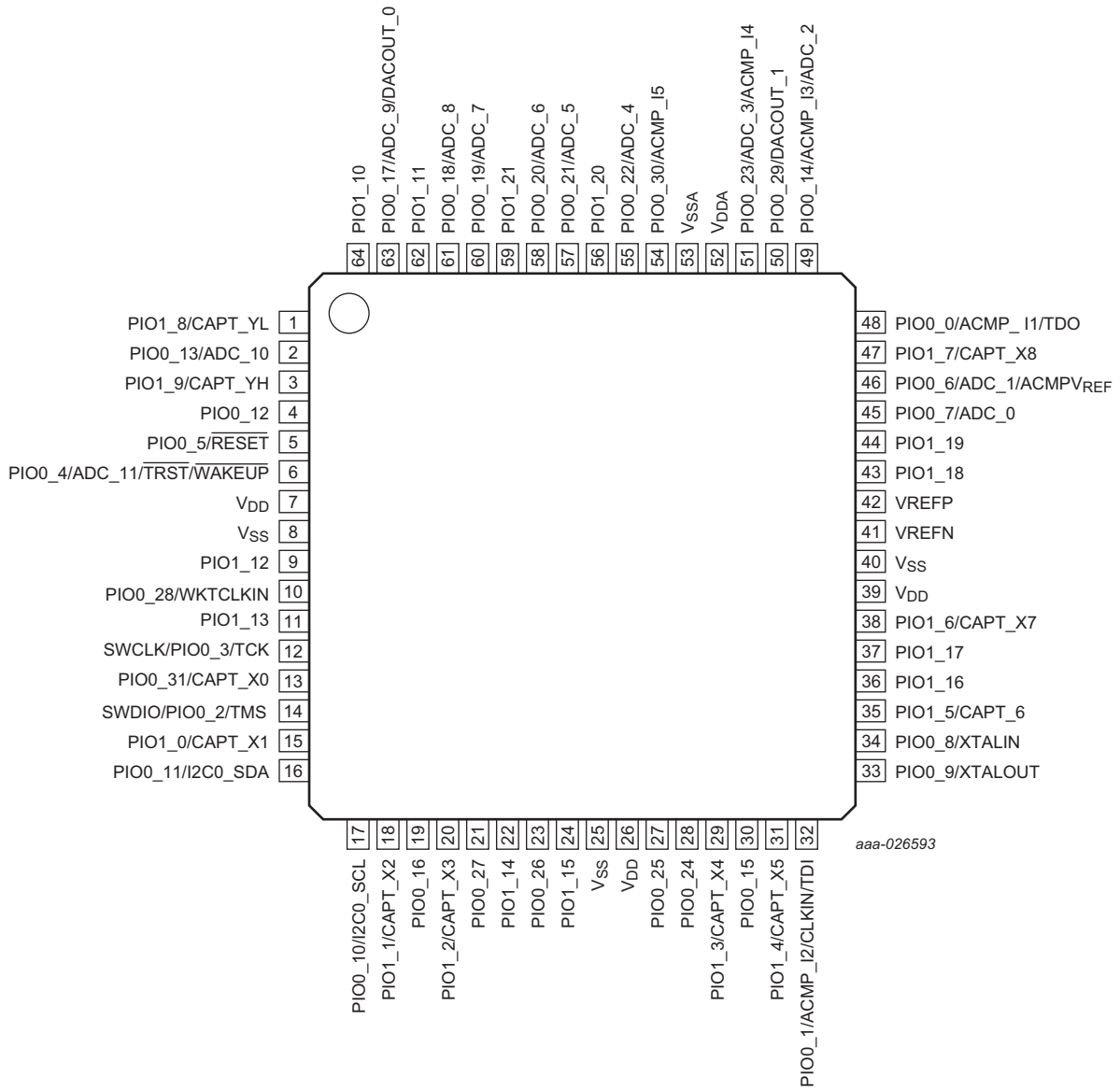


Fig 4. Pin configuration LQFP64 package

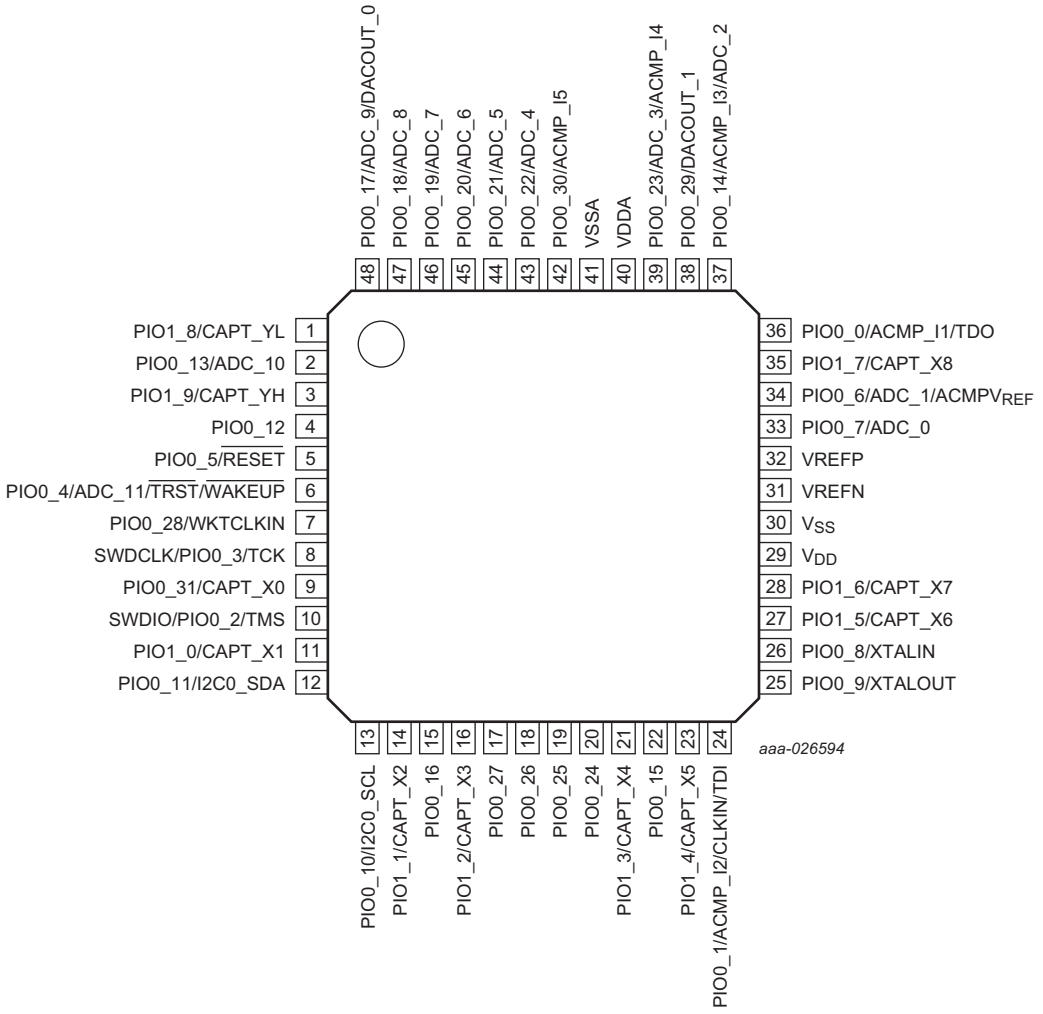


Fig 5. Pin configuration LQFP48 package

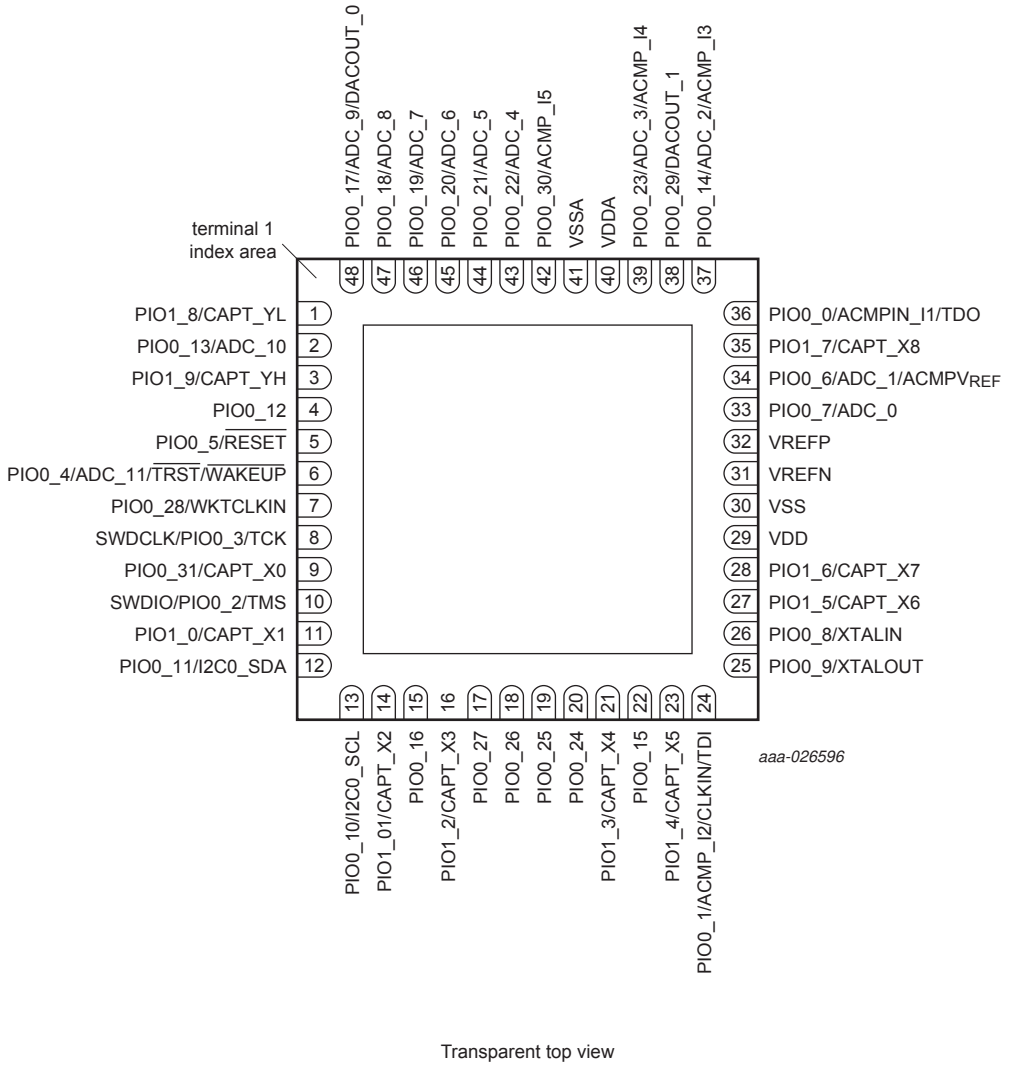


Fig 6. Pin configuration HVQFN48 package

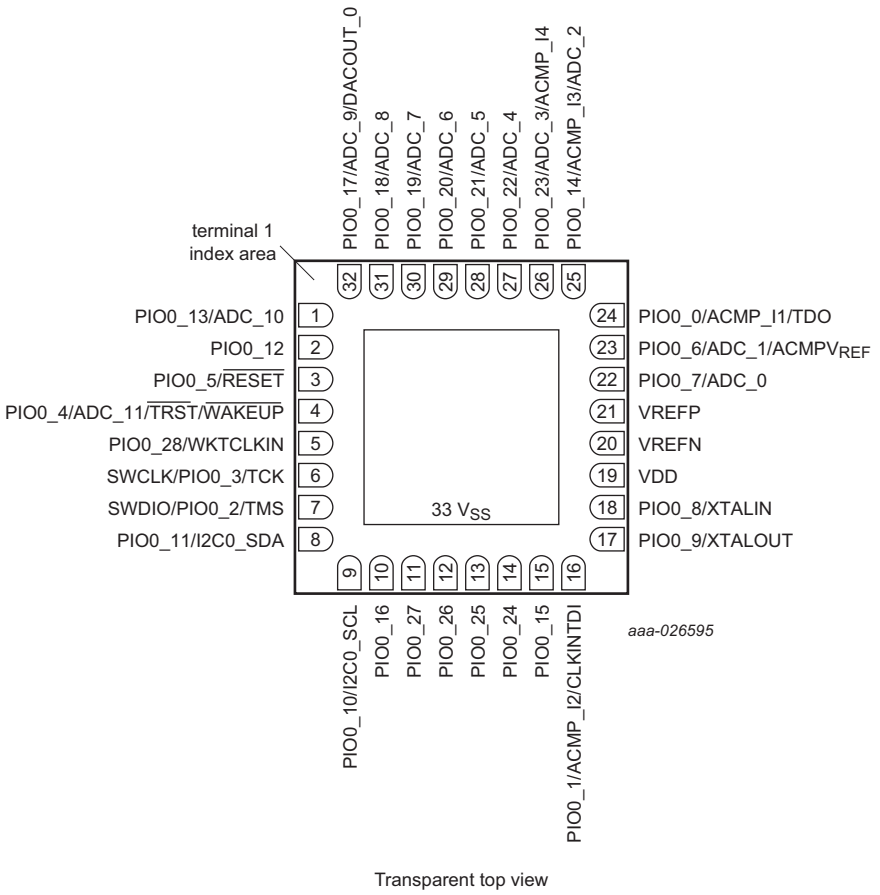


Fig 7. Pin configuration HVQFN33 package

7.2 Pin description

The pin description table shows the pin functions that are fixed to specific pins on each package. See Table 4. These fixed-pin functions are selectable through the switch matrix between GPIO and the comparator, ADC, SWD, RESET, and the XTAL pins. By default, the GPIO function is selected except on pins PIO0_2, PIO0_3, and PIO0_5. JTAG functions are available in boundary scan mode only.

Movable functions for the I^2C, USART, SPI, CTimer, SCT pins, and other peripherals can be assigned through the switch matrix to any pin that is not power or ground in place of the pin's fixed functions.

The following exceptions apply:

Do not assign more than one output to any pin. However, an output and/or one or more inputs can be assigned to a pin. Once any function is assigned to a pin, the pin's GPIO functionality is disabled.

Pin PIO0_4 triggers a wake-up from deep power-down mode. If the part must wake up from deep power-down mode via an external pin, do not assign any movable function to this pin.

PIO0_10 and PIO_11 are high current source pins while PIO0_2, PIO0_3, PIO0_12, and PIO0_16 are high drive output pins.

The JTAG functions TDO, TDI, TCK, TMS, and $\overline{\text{TRST}}$ are selected on pins PIO0_0 to PIO0_4 by hardware when the part is in boundary scan mode.

Table 4. Pin description

Symbol	LQFP64	LQFP48	HVQFN48	HVQFN33		Reset state[1]	Type	Description
PIO0_0/ACMP_I1/ TDO	48	36	36	24	[2]	I; PU	IO	**PIO0_0 —** General-purpose port 0 input/output 0. In boundary scan mode: TDO (Test Data Out).
							A	**ACMP_I1 —** Analog comparator input 1.
PIO0_1/ACMP_I2/ CLKIN/TDI	32	24	24	16	[2]	I; PU	IO	**PIO0_1 —** General-purpose port 0 input/output 1. In boundary scan mode: TDI (Test Data In).
							A	**ACMP_I2 —** Analog comparator input 2.
							I	**CLKIN —** External clock input.
SWDIO/PIO0_2/ TMS	14	10	10	7	[4]	I; PU	IO	**SWDIO —** Serial Wire Debug I/O. SWDIO is enabled by default on this pin. In boundary scan mode: TMS (Test Mode Select).
							I/O	**PIO0_2 —** General-purpose port 0 input/output 2.
SWCLK/PIO0_3/ TCK	12	8	8	6	[4]	I; PU	I	**SWCLK —** Serial Wire Clock. SWCLK is enabled by default on this pin. In boundary scan mode: TCK (Test Clock).
							IO	**PIO0_3 —** General-purpose port 0 input/output 3.
PIO0_4/ADC_11/ TRSTN/WAKEUP	6	6	6	4	[3]	I; PU	IO	**PIO0_4 —** General-purpose port 0 input/output 4. In boundary scan mode: $\overline{\text{TRST}}$ (Test Reset). This pin triggers a wake-up from deep power-down mode. If the part must wake up from deep power-down mode via the $\overline{\text{WAKEUP}}$ pin, do not assign any movable function to this pin and must be externally pulled HIGH before entering deep power-down mode. A LOW-going pulse as short as 50 ns causes the chip to exit deep power-down mode and wakes up the part. The $\overline{\text{WAKEUP}}$ pin can be left unconnected or be used as a GPIO or for any movable function if an external $\overline{\text{WAKEUP}}$ function is not needed.
							A	**ADC_11 —** ADC input 11.

Table 4. Pin description

Symbol	LQFP64	LQFP48	HVQFN48	HVQFN33		Reset state[1]	Type	Description
RESET/PIO0_5	5	5	5	3	[7]	I; PU	I	**RESET —** External reset input: A LOW-going pulse (minimum 20 ns to maximum 50 ns) on this pin resets the device, causing I/O ports and peripherals to take on their default states, and processor execution to begin at address 0. This pin triggers a wake-up from deep power-down mode. If the part must wake up from deep power-down mode via the RESET pin, do not assign any movable function to this pin and must be externally pulled HIGH before entering deep power-down mode. The RESET pin can be left unconnected or be used as a GPIO or for any movable function if an external RESET function is not needed.
							IO	**PIO0_5 —** General-purpose port 0 input/output 5.
PIO0_6/ADC_1/ $ACMPV_{REF}$	46	34	34	23	[10]	I; PU	IO	**PIO0_6 —** General-purpose port 0 input/output 6.
							A	**ADC_1 —** ADC input 1.
							A	**$ACMPV_{REF}$ —** Alternate reference voltage for the analog comparator.
PIO0_7/ADC_0	45	33	33	22	[2]	I; PU	IO	**PIO0_7 —** General-purpose port 0 input/output 7.
							A	**ADC_0 —** ADC input 0.
PIO0_8/XTALIN	34	26	26	18	[8]	I; PU	IO	**PIO0_8 —** General-purpose port 0 input/output 8.
							A	**XTALIN —** Input to the oscillator circuit and internal clock generator circuits. Input voltage must not exceed 1.95 V in slave mode. See Section 14.2.2 "XTAL input".
PIO0_9/XTALOUT	33	25	25	17	[8]	I; PU	IO	**PIO0_9 —** General-purpose port 0 input/output 9.
							A	**XTALOUT —** Output from the oscillator circuit.
PIO0_10/I2C0_SCL	17	13	13	9	[6]	Inactive	I; F	**PIO0_10 —** General-purpose port 0 input/output 10 (open-drain).
								I2C0_SCL — Open-drain I^2C-bus clock input/output. High-current sink if I^2C Fast-mode Plus is selected in the I/O configuration register.
PIO0_11/I2C0_SDA	16	12	12	8	[6]	Inactive	I; F	**PIO0_11 —** General-purpose port 0 input/output 11 (open-drain).
								I2C0_SDA — Open-drain I^2C-bus data input/output. High-current sink if I^2C Fast-mode Plus is selected in the I/O configuration register.
PIO0_12	4	4	4	2	[4]	I; PU	IO	**PIO0_12 —** General-purpose port 0 input/output 12. ISP entry pin. A LOW level on this pin during reset starts the ISP command handler.
PIO0_13/ADC_10	2	2	2	1	[2]	I; PU	IO	**PIO0_13 —** General-purpose port 0 input/output 13.
							A	**ADC_10 —** ADC input 10.

Table 4. Pin description

Symbol	LQFP64	LQFP48	HVQFN48	HVQFN33		Reset state[1]	Type	Description
PIO0_14/ ACMP_I3/ADC_2	49	37	37	25	[2]	I; PU	IO	**PIO0_14 —** General-purpose port 0 input/output 14.
							A	**ACMP_I3 —** Analog comparator common input 3.
							A	**ADC_2 —** ADC input 2.
PIO0_15	30	22	22	15	[5]	I; PU	IO	**PIO0_15 —** General-purpose port 0 input/output 15.
PIO0_16	19	15	15	10	[4]	I; PU	IO	**PIO0_16 —** General-purpose port 0 input/output 16.
PIO0_17/ADC_9/ DACOUT_0	63	48	48	32	[2]	I; PU	IO	**PIO0_17 —** General-purpose port 0 input/output 17.
							A	**ADC_9 —** ADC input 9.
							A	**DACOUT_0 —** DAC Output 0.
PIO0_18/ADC_8	61	47	47	31	[2]	I; PU	IO	**PIO0_18 —** General-purpose port 0 input/output 18.
							A	**ADC_8 —** ADC input 8.
PIO0_19/ADC_7	60	46	46	30	[2]	I; PU	IO	**PIO0_19 —** General-purpose port 0 input/output 19.
							A	**ADC_7 —** ADC input 7.
PIO0_20/ADC_6	58	45	45	29	[2]	I; PU	IO	**PIO0_20 —** General-purpose port 0 input/output 20.
							A	**ADC_6 —** ADC input 6.
PIO0_21/ADC_5	57	44	44	28	[2]	I; PU	IO	**PIO0_21 —** General-purpose port 0 input/output 21.
							A	**ADC_5 —** ADC input 5.
PIO0_22/ADC_4	55	43	43	27	[2]	I; PU	IO	**PIO0_22 —** General-purpose port 0 input/output 22.
							A	**ADC_4 —** ADC input 4.
PIO0_23/ADC_3/ ACMP_I4	51	39	39	26	[2]	I; PU	IO	**PIO0_23 —** General-purpose port 0 input/output 23.
							A	**ADC_3 —** ADC input 3.
							A	**ACMP_I4 —** Analog comparator common input 4.
PIO0_24	28	20	20	14	[5]	I; PU	IO	**PIO0_24 —** General-purpose port 0 input/output 24. In ISP mode, this is the U0_RXD pin.
PIO0_25	27	19	19	13	[5]	I; PU	IO	**PIO0_25 —** General-purpose port 0 input/output 25. In ISP mode, this pin is the U0_TXD pin.
PIO0_26	23	18	18	12	[5]	I; PU	IO	**PIO0_26 —** General-purpose port 0 input/output 26.
PIO0_27	21	17	17	11	[5]	I; PU	IO	**PIO0_27 —** General-purpose port 0 input/output 27.
PIO0_28/ WKTCLKIN	10	7	7	5	[3]	I; PU	IO	**PIO0_28 —** General-purpose port 0 input/output 28. This pin can host an external clock for the self-wake-up timer. To use the pin as a self-wake-up timer clock input, select the external clock in the wake-up timer CTRL register. The external clock input is active in all power modes, including deep power-down.
PIO0_29/ DACOUT_1	50	38	38	-	[5]	I; PU	IO	**PIO0_29 —** General-purpose port 0 input/output 29.
							A	**DACOUT_1 —** DAC output 1.
PIO0_30/ACMP_I5	54	42	42	-	[5]	I; PU	IO	**PIO0_30 —** General-purpose port 0 input/output 30.
							A	**ACMP_I5 —** Analog comparator common input 5.

Table 4. Pin description

Symbol	LQFP64	LQFP48	HVQFN48	HVQFN33		Reset state[1]	Type	Description
PIO0_31/CAPT_X0	13	9	9	-	[5]	I; PU	IO	**PIO0_31 —** General-purpose port 0 input/output 31.
								CAPT_X0 — Capacitive Touch X sensor 0.
PIO1_0/CAPT_X1	15	11	11	-	[5]	I; PU	IO	**PIO1_0 —** General-purpose port 1 input/output 0.
								CAPT_X1 — Capacitive Touch X sensor 1.
PIO1_1/CAPT_X2	18	14	14	-	[5]	I; PU	IO	**PIO1_1 —** General-purpose port 1 input/output 1.
								CAPT_X2 — Capacitive Touch X sensor 2.
PIO1_2/CAPT_X3	20	16	16	-	[5]	I; PU	IO	**PIO1_2 —** General-purpose port 1 input/output 2.
								CAPT_X3 — Capacitive Touch X sensor 3.
PIO1_3/CAPT_X4	29	21	21	-	[5]	I; PU	IO	**PIO1_3 —** General-purpose port 1 input/output 3.
								CAPT_X4 — Capacitive Touch X sensor 4.
PIO1_4/CAPT_X5	31	23	23	-	[5]	I; PU	IO	**PIO1_4 —** General-purpose port 1 input/output 4.
								CAPT_X5 — Capacitive Touch X sensor 5.
PIO1_5/CAPT_X6	35	27	27	-	[5]	I; PU	IO	**PIO1_5 —** General-purpose port 1 input/output 5.
								CAPT_X6 — Capacitive Touch X sensor 6.
PIO1_6/CAPT_X7	38	28	28	-	[5]	I; PU	IO	**PIO1_6 —** General-purpose port 1 input/output 6.
								CAPT_X7 — Capacitive Touch X sensor 7.
PIO1_7/CAPT_X8	47	35	35	-	[5]	I; PU	IO	**PIO1_7 —** General-purpose port 1 input/output 7.
								CAPT_X8 — Capacitive Touch X sensor 8.
PIO1_8/CAPT_YL	1	1	1	-	[5]	I; PU	IO	**PIO1_8 —** General-purpose port 1 input/output 8.
								CAPT_YL — Capacitive Touch Y Low.
PIO1_9/CAPT_YH	3	3	3	-	[5]	I; PU	IO	**PIO1_9 —** General-purpose port 1 input/output 9.
								CAPT_YH — Capacitive Touch Y High.
PIO1_10	64	-	-	-	[5]	I; PU	IO	**PIO1_10 —** General-purpose port 1 input/output 10.
PIO1_11	62	-	-	-	[5]	I; PU	IO	**PIO1_11 —** General-purpose port 1 input/output 11.
PIO1_12	9	-	-	-	[5]	I; PU	IO	**PIO1_12 —** General-purpose port 1 input/output 12.
PIO1_13	11	-	-	-	[5]	I; PU	IO	**PIO1_13 —** General-purpose port 1 input/output 13.
PIO1_14	22	-	-	-	[5]	I; PU	IO	**PIO1_14 —** General-purpose port 1 input/output 14.
PIO1_15	24	-	-	-	[5]	I; PU	IO	**PIO1_15 —** General-purpose port 1 input/output 15.
PIO1_16	36	-	-	-	[5]	I; PU	IO	**PIO1_16 —** General-purpose port 1 input/output 16.
PIO1_17	37	-	-	-	[5]	I; PU	IO	**PIO1_17 —** General-purpose port 1 input/output 17.
PIO1_18	43	-	-	-	[5]	I; PU	IO	**PIO1_18 —** General-purpose port 1 input/output 18.
PIO1_19	44	-	-	-	[5]	I; PU	IO	**PIO1_19 —** General-purpose port 1 input/output 19.
PIO1_20	56	-	-	-	[5]	I; PU	IO	**PIO1_20 —** General-purpose port 1 input/output 20.
PIO1_21	59	-	-	-	[5]	I; PU	IO	**PIO1_21 —** General-purpose port 1 input/output 21.
V_{DD}	7;26;39	29	29	19		-	-	Supply voltage for the I/O pad ring, the and core voltage regulator.
V_{DDA}	52	40	40					Analog supply voltage.
V_{SS}	8;25;40	30	30	33[11]		-	-	Ground.

Table 4. Pin description

Symbol	LQFP64	LQFP48	HVQFN48	HVQFN33		Reset state[1]	Type	Description
V_{SSA}	53	41	41					Analog ground.
VREFN	41	31	31	20		-	-	ADC negative reference voltage.
VREFP	42	32	32	21		-	-	ADC positive reference voltage. Must be equal or lower than V_{DDA}.

[1] Pin state at reset for default function: I = Input; AI = Analog Input; O = Output; PU = internal pull-up enabled (pins pulled up to full V_{DD} level); IA = inactive, no pull-up/down enabled; F = floating. For pin states in the different power modes, see Section 14.6 “Pin states in different power modes”. For termination on unused pins, see Section 14.5 “Termination of unused pins”.

[2] 5 V tolerant pin providing standard digital I/O functions with configurable modes, configurable hysteresis, and analog input. When configured as an analog input, the digital section of the pin is disabled, and the pin is not 5 V tolerant.

[3] 5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors and configurable hysteresis. This pin is active in deep power-down mode and includes a 20 ns glitch filter (active in all power modes). In deep power-down mode, pulling the $\overline{\text{WAKEUP}}$ pin LOW wakes up the chip. The wake-up pin function can be disabled and the pin can be used for other purposes, if the WKT low-power oscillator is enabled for waking up the part from deep power-down mode. See Table 20 “Dynamic characteristics: WKTCLKIN pin” for the WKTCLKIN input.

[4] 5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors and configurable hysteresis; includes high-current output driver.

[5] 5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors and configurable hysteresis.

[6] True open-drain pin. I^2C-bus pins compliant with the I^2C-bus specification for I^2C standard mode, I^2C Fast-mode, and I^2C Fast-mode Plus. Do not use this pad for high-speed applications such as SPI or USART. The pin requires an external pull-up to provide output functionality. When power is switched off, this pin is floating and does not disturb the I2C lines. Open-drain configuration applies to all functions on this pin.

[7] See Figure 14 for the reset pad configuration. This pin includes a 20 ns glitch filter (active in all power modes). $\overline{\text{RESET}}$ functionality is available in deep power-down mode. Use the $\overline{\text{WAKEUP}}$ pin to reset the chip and wake up from deep power-down mode.

[8] 5 V tolerant pin providing standard digital I/O functions with configurable modes, configurable hysteresis, and analog I/O for the system oscillator. When configured for XTALIN and XTALOUT, the digital section of the pin is disabled, and the pin is not 5 V tolerant.

[9] The WKTCLKIN function is enabled in the DPDCTRL register in the PMU. See the LPC84x user manual.

[10] The digital part of this pin is 3 V tolerant pin due to special analog functionality. Pin provides standard digital I/O functions with configurable modes, configurable hysteresis, and an analog input. When configured as an analog input, the digital section of the pin is disabled.

[11] Thermal pad for HVQFN33.

Table 5. Movable functions (assign to pins PIO0_0 to PIO0_31, PIO1_0 to PIO1_21 through switch matrix)

Function name	Type	Description
Ux_TXD	O	Transmitter output for USART0 to USART4.
Ux_RXD	I	Receiver input for USART0 to USART4.
$\overline{\text{Ux\_RTS}}$	O	Request To Send output for USART0 to USART4.
$\overline{\text{Ux\_CTS}}$	I	Clear To Send input for USART0 to USART4.
Ux_SCLK	I/O	Serial clock input/output for USART0 to USART4 in synchronous mode.
SPIx_SCK	I/O	Serial clock for SPI0 and SPI1.
SPIx_MOSI	I/O	Master Out Slave In for SPI0 and SPI1.
SPIx_MISO	I/O	Master In Slave Out for SPI0 and SPI1.

Table 5. Movable functions (assign to pins PIO0_0 to PIO0_31, PIO1_0 to PIO1_21 through switch matrix)

Function name	Type	Description
SPIx_SSEL0	I/O	Slave select 0 for SPI0 and SPI1.
SPIx_SSEL1	I/O	Slave select 1 for SPI0 and SPI1.
SPIx_SSEL2	I/O	Slave select 2 for SPI0 and SPI1.
SPIx_SSEL3	I/O	Slave select 3 for SPI0 and SPI1.
SCT_PIN0	I	Pin input 0 to the SCT input multiplexer.
SCT_PIN1	I	Pin input 1 to the SCT input multiplexer.
SCT_PIN2	I	Pin input 2 to the SCT input multiplexer.
SCT_PIN3	I	Pin input 3 to the SCT input multiplexer.
SCT_OUT0	O	SCT output 0.
SCT_OUT1	O	SCT output 1.
SCT_OUT2	O	SCT output 2.
SCT_OUT3	O	SCT output 3.
SCT_OUT4	O	SCT output 4.
SCT_OUT5	O	SCT output 5.
I2Cx_SDA	I/O	I^2C1, I^2C2, and I^2C3 bus data input/output.
I2Cx_SCL	I/O	I^2C1, I^2C2, and I^2C3 bus clock input/output.
ACMP_O	O	Analog comparator output.
CLKOUT	O	Clock output.
GPIO_INT_BMAT	O	Output of the pattern match engine.
T0_MAT0	O	Timer Match channel 0.
T0_MAT1	O	Timer Match channel 1.
T0_MAT2	O	Timer Match channel 2.
T0_MAT3	O	Timer Match channel 3.
T0_CAP0	I	Timer Capture channel 0.
T0_CAP1	I	Timer Capture channel 1.
T0_CAP2	I	Timer Capture channel 2.

8. Functional description

8.1 Arm Cortex-M0+ core

The Arm Cortex-M0+ core runs at an operating frequency of up to 30 MHz using a two-stage pipeline. The core revision is r0p1.

Integrated in the core are the NVIC and Serial Wire Debug with four breakpoints and two watchpoints. The Arm Cortex-M0+ core supports a single-cycle I/O enabled port for fast GPIO access.

The core includes a single-cycle multiplier and a system tick timer.

8.2 On-chip flash program memory

The LPC84x contain up to 64 KB of on-chip flash program memory. The flash memory supports a 64 Byte page size with page write and erase.

8.3 On-chip SRAM

The LPC84x contain a total of 16KB on-chip static RAM data memory in two separate SRAM blocks with one combined clock for both SRAM blocks. One 8 KB of SRAM can be used for MTB.

A bit-band module is added in series with the AHB matrix to allow atomic read-modify-write operations acting on a single bit.

8.4 FAIM memory

The LPC84x includes the FAIM memory and is used to configure the part at start-up. It is 128/256 bits in size and is used to configure the following:

- Clocks and PMU for low-power start-up.
- Low power boot at 1.5 MHz using FAIM memory.
- Pin configuration including direction and pull- up or pull-down.
- Specification of pins to use for ISP entry for each serial peripheral.
- Select whether SWCLK and SWDIO are enabled on reset.

Remark: The FAIM programming voltage range is 3.0 V ≤ Vdd ≤ 3.6 V.

8.5 On-chip ROM

The on-chip ROM contains the bootloader:

- Boot loader.
- Supports Flash In-Application Programming (IAP).
- Supports In-System Programming (ISP) through USART, SPI, and I^2C.
- On-chip ROM APIs for integer divide.
- FAIM API.
- FRO API.

8.6 Memory map

The LPC84x incorporates several distinct memory regions. Figure 8 shows the overall map of the entire address space from the user program viewpoint following reset. The interrupt vector area supports address remapping.

The Arm private peripheral bus includes the Arm core registers for controlling the NVIC, the system tick timer (SysTick), and the reduced power modes.

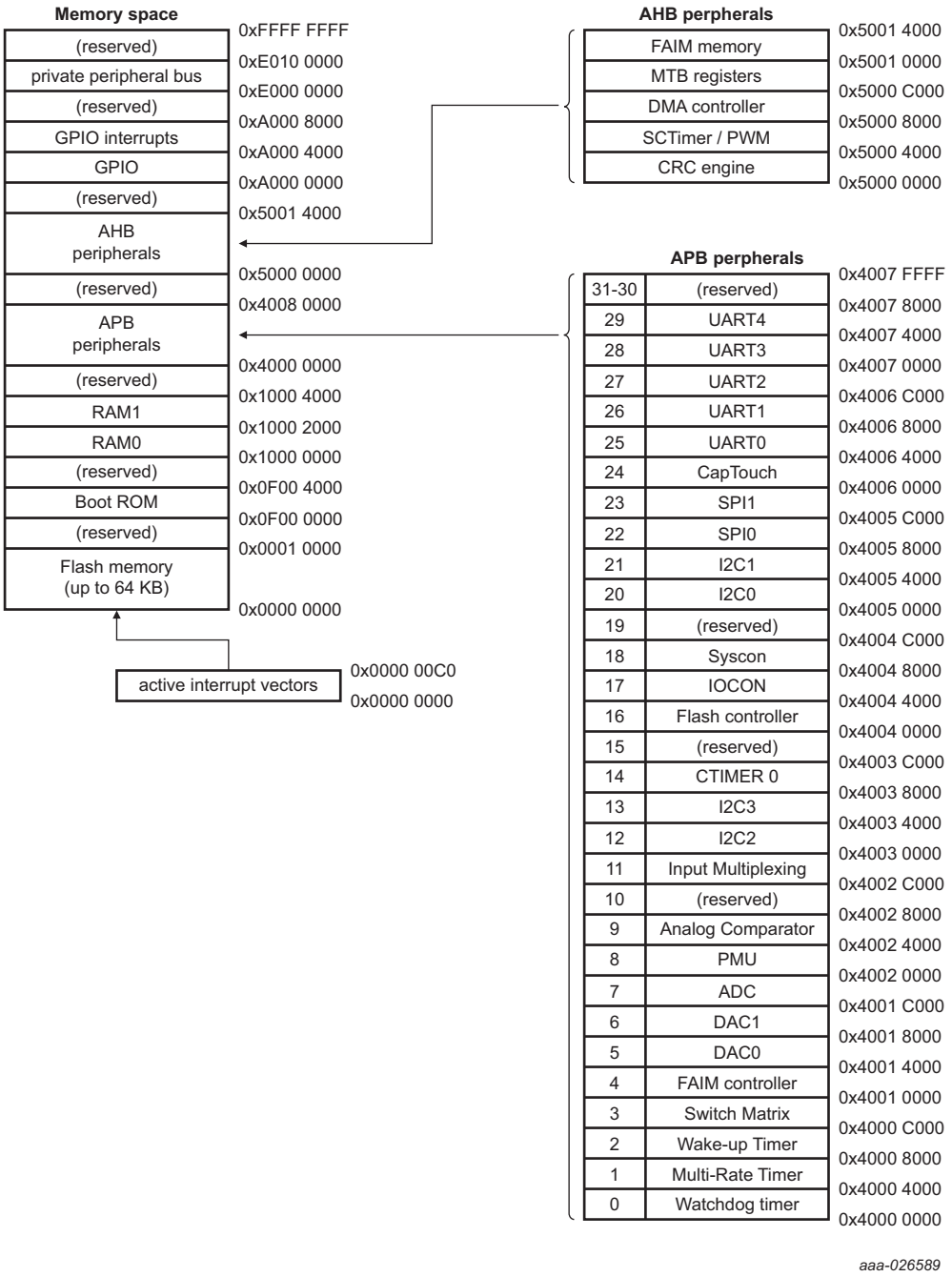


Fig 8. LPC84x AHB Memory mapping

8.7 Nested Vectored Interrupt Controller (NVIC)

The Nested Vectored Interrupt Controller (NVIC) is part of the Cortex-M0+. The tight coupling to the CPU allows for low interrupt latency and efficient processing of late arriving interrupts.

8.7.1 Features

- Nested Vectored Interrupt Controller is a part of the Arm Cortex-M0+.
- Tightly coupled interrupt controller provides low interrupt latency.
- Controls system exceptions and peripheral interrupts.
- Supports 32 vectored interrupts.
- In the LPC84x, the NVIC supports vectored interrupts for each of the peripherals and the eight pin interrupts.
- Four programmable interrupt priority levels with hardware priority level masking.
- Software interrupt generation using the Arm exceptions SVCall and PendSV.
- Supports NMI.

8.7.2 Interrupt sources

Each peripheral device has at least one interrupt line connected to the NVIC but can have several interrupt flags. Individual interrupt flags can also represent more than one interrupt source.

8.8 System tick timer

The Arm Cortex-M0+ includes a 24-bit system tick timer (SysTick) that is intended to generate a dedicated SysTick exception at a fixed time interval (typically 10 ms).

8.9 I/O configuration

The IOCON block controls the configuration of the I/O pins. Each digital or mixed digital/analog pin with the PIO0_n designator (except the true open-drain pins PIO0_10 and PIO0_11) in Table 4 can be configured as follows:

- Enable or disable the weak internal pull-up and pull-down resistors.
- Select a pseudo open-drain mode. The input cannot be pulled up above V_{DD}. The pins are not 5 V tolerant when V_{DD} is grounded.
- Program the input glitch filter with different filter constants using one of the IOCON divided clock signals (IOCONCLKCDIV, see Figure 11 “LPC84x clock generation”). You can also bypass the glitch filter.
- Invert the input signal.
- Hysteresis can be enabled or disabled.
- For pins PIO0_10 and PIO0_11, select the I2C-mode and output driver for standard digital operation, for I2C standard and fast modes, or for I2C Fast mode+.
- The switch matrix setting enables the analog input mode on pins with analog and digital functions. Enabling the analog mode disconnects the digital functionality.

Remark: The functionality of each I/O pin is flexible and is determined entirely through the switch matrix. See Section 8.10 for details.

8.9.1 Standard I/O pad configuration

Figure 9 shows the possible pin modes for standard I/O pins with analog input function:

- Digital output driver with configurable open-drain output.
- Digital input: Weak pull-up resistor (PMOS device) enabled/disabled.
- Digital input: Weak pull-down resistor (NMOS device) enabled/disabled.
- Digital input: Repeater mode enabled/disabled.
- Digital input: Programmable input digital filter selectable on all pins.
- Analog input: Selected through the switch matrix.

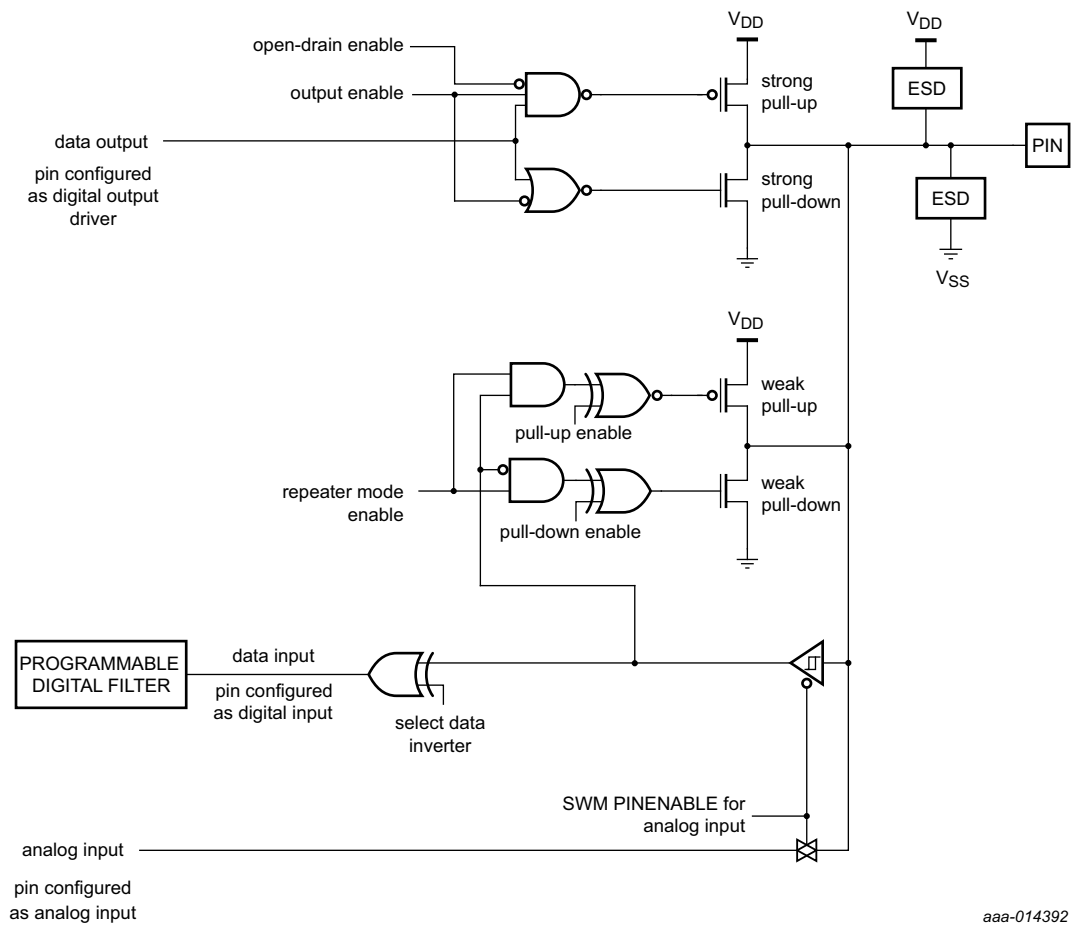


Fig 9. Standard I/O pad configuration

8.10 Switch Matrix (SWM)

The switch matrix controls the function of each digital or mixed analog/digital pin in a highly flexible way by allowing to connect many functions, for example, the USART, SPI, SCTimer/PWM, CTimer, and I^2C functions to any pin that is not power or ground. These functions are called movable functions and are listed in Table 5.

Functions that need specialized pads like the oscillator pins XTALIN and XTALOUT can be enabled or disabled through the switch matrix. These functions are called fixed-pin functions and cannot move to other pins. The fixed-pin functions are listed in Table 4. If a fixed-pin function is disabled, any other movable function can be assigned to this pin.

8.11 Fast General-Purpose parallel I/O (GPIO)

Device pins that are not connected to a specific peripheral function are controlled by the GPIO registers. Pins may be dynamically configured as inputs or outputs. Multiple outputs can be set or cleared in one write operation.

LPC84x use accelerated GPIO functions:

- GPIO registers are on the Arm Cortex-M0+ IO bus for fastest possible single-cycle I/O timing, allowing GPIO toggling with rates of up to 15 MHz.
- An entire port value can be written in one instruction.
- Mask, set, and clear operations are supported for the entire port.

All GPIO port pins are fixed-pin functions that are enabled or disabled on the pins by the switch matrix. Therefore each GPIO port pin is assigned to one specific pin and cannot be moved to another pin. Except for pins SWDIO/PIO0_2, SWCLK/PIO0_3, and RESET/PIO0_5, the switch matrix enables the GPIO port pin function by default.

8.11.1 Features

- Bit level port registers allow a single instruction to set and clear any number of bits in one write operation.
- Direction control of individual bits.
- All I/O default to GPIO inputs with internal pull-up resistors enabled after reset - except for the I^2C-bus true open-drain pins PIO0_10 and PIO0_11.
- Pull-up/pull-down configuration, repeater, and open-drain modes can be programmed through the IOCON block for each GPIO pin (see Figure 9).
- Direction (input/output) can be set and cleared individually.
- Pin direction bits can be toggled.

8.12 Pin interrupt/pattern match engine

The pin interrupt block configures up to eight pins from all digital pins for providing eight external interrupts connected to the NVIC.

The pattern match engine can be used, with software, to create complex state machines based on pin inputs.

Any digital pin, independently of the function selected through the switch matrix, can be configured through the SYSCON block as input to the pin interrupt or pattern match engine. The registers that control the pin interrupt or pattern match engine are on the IO+ bus for fast single-cycle access.

8.12.1 Features

- Pin interrupts
  - Up to eight pins can be selected from all digital pins as edge- or level-sensitive interrupt requests. Each request creates a separate interrupt in the NVIC.
  - Edge-sensitive interrupt pins can interrupt on rising or falling edges or both.
  - Level-sensitive interrupt pins can be HIGH- or LOW-active.
  - Pin interrupts can wake up the LPC84x from sleep mode, deep-sleep mode, and power-down mode.
- Pin interrupt pattern match engine
  - Up to eight pins can be selected from all digital pins to contribute to a boolean expression. The boolean expression consists of specified levels and/or transitions on various combinations of these pins.
  - Each minterm (product term) comprising the specified boolean expression can generate its own, dedicated interrupt request.
  - Any occurrence of a pattern match can be also programmed to generate an RXEV notification to the Arm CPU. The RXEV signal can be connected to a pin.
  - The pattern match engine does not facilitate wake-up.

8.13 DMA controller

The DMA controller can access all memories and the USART, SPI, I^2C, DAC, and Capacitive Touch. DMA transfers can also be triggered by internal events like the ADC interrupts, the pin interrupts (PININT0 and PININT1), the SCTimer DMA requests, CTimer, and the DMA trigger outputs.

8.13.1 Features

- Twenty five channels with each channel connected to peripheral request inputs.
- DMA operations can be triggered by on-chip events or by two pin interrupts. Each DMA channel can select one trigger input from13 sources.
- Priority is user selectable for each channel.
- Continuous priority arbitration.
- Address cache with two entries.
- Efficient use of data bus.
- Supports single transfers up to 1,024 words.
- Address increment options allow packing and/or unpacking data.

8.13.2 DMA trigger input MUX (TRIGMUX)

Each DMA trigger is connected to a programmable multiplexer which connects the trigger input to one of multiple trigger sources. Each multiplexer supports the same trigger sources: the ADC sequence interrupts, the SCT DMA request lines, and pin interrupts PININT0 and PININT1, and the outputs of the DMA triggers 0 and 1 for chaining DMA triggers.

8.14 USART0/1/2/3/4

All USART functions are movable functions and are assigned to pins through the switch matrix.

8.14.1 Features

- Maximum bit rates of 1.875 Mbit/s in asynchronous mode and 10 Mbit/s in synchronous mode for USART functions connected to all digital pins except the open-drain pins.
- 7, 8, or 9 data bits and 1 or 2 stop bits
- Synchronous mode with master or slave operation. Includes data phase selection and continuous clock option.
- Multiprocessor/multidrop (9-bit) mode with software address compare. (RS-485 possible with software address detection and transceiver direction control.)
- Parity generation and checking: odd, even, or none.
- One transmit and one receive data buffer.
- RTS/CTS for hardware signaling for automatic flow control. Software flow control can be performed using Delta CTS detect, Transmit Disable control, and any GPIO as an RTS output.
- Received data and status can optionally be read from a single register
- Break generation and detection.
- Receive data is 2 of 3 sample "voting". Status flag set when one sample differs.
- Built-in Baud Rate Generator.
- A fractional rate divider is shared among all UARTs.
- Interrupts available for Receiver Ready, Transmitter Ready, Receiver Idle, change in receiver break detect, Framing error, Parity error, Overrun, Underrun, Delta CTS detect, and receiver sample noise detected.
- Separate data and flow control loopback modes for testing.
- Baud rate clock can also be output in asynchronous mode.

8.15 SPI0/1

All SPI functions are movable functions and are assigned to pins through the switch matrix.

8.15.1 Features

- Maximum data rates of up to 30 Mbit/s in master mode and up to 18 Mbit/s in slave mode for SPI functions connected to all digital pins except the open-drain pins.

- Data frames of 1 to 16 bits supported directly. Larger frames supported by software.
- Master and slave operation.
- Data can be transmitted to a slave without the need to read incoming data, which can be useful while setting up an SPI memory.
- Control information can optionally be written along with data, which allows very versatile operation, including “any length” frames.
- One Slave Select input/output with selectable polarity and flexible usage.

Remark: Texas Instruments SSI and National Microwire modes are not supported.

8.16 I²C-bus interface (I²C0/1/2/3)

The I²C-bus is bidirectional for inter-IC control using only two wires: a serial clock line (SCL) and a serial data line (SDA). Each device is recognized by a unique address and can operate as either a receiver-only device (for example, an LCD driver) or a transmitter with the capability to both receive and send information (such as memory). Transmitters and/or receivers can operate in either master or slave mode, depending on whether the chip has to initiate a data transfer or is only addressed. The I²C is a multi-master bus and can be controlled by more than one bus master.

The I2C0-bus functions are fixed-pin functions. All other I2C-bus functions for I2C1/2/3 are movable functions and can be assigned through the switch matrix to any pin. However, only the true open-drain pins provide the electrical characteristics to support the full I2C-bus specification (see Ref. 3).

8.16.1 Features

- I2C0 supports Fast-mode Plus with data rates of up to 1 Mbit/s in addition to standard and fast modes on two true open-drain pins.
- True open-drain pins provide fail-safe operation: When the power to an I²C-bus device is switched off, the SDA and SCL pins connected to the I²C0-bus are floating and do not disturb the bus.
- I2C1/2/3 support standard and fast mode with data rates of up to 400 kbit/s.
- Independent Master, Slave, and Monitor functions.
- Supports both Multi-master and Multi-master with Slave functions.
- Multiple I²C slave addresses supported in hardware.
- One slave address can be selectively qualified with a bit mask or an address range in order to respond to multiple I²C bus addresses.
- 10-bit addressing supported with software assist.
- Supports SMBus.

8.17 Capacitive Touch Interface

The Capacitive Touch interface is designed to handle up to nine capacitive buttons in different sensor configurations, such as slider, rotary, and button matrix. It operates in sleep, deep sleep, and power-down modes, allowing very low power performance.

The Capacitive Touch module measures the change in capacitance of an electrode plate when an earth-ground connected object (for example, finger) is brought within close proximity.

8.18 SCTimer/PWM

The SCTimer/PWM can perform basic 16-bit and 32-bit timer/counter functions with match outputs and external and internal capture inputs. In addition, the SCTimer/PWM can employ up to eight different programmable states, which can change under the control of events, to provide complex timing patterns.

The inputs to the SCT are multiplexed between movable functions from the switch matrix and internal connections such as the ADC threshold compare interrupt, the comparator output, and the Arm core signals Arm_TXEV and DEBUG_HALTED. The signal on each SCT input is selected through the INPUT MUX.

All outputs of the SCT are movable functions and are assigned to pins through the switch matrix. One SCT output can also be selected as one of the ADC conversion triggers.

8.18.1 Features

- Each SCTimer/PWM supports:
  - Eight match/capture registers.
  - Eight events.
  - Eight states.
  - Five inputs. The fifth input is hard-wired to a clock source. Each input is configurable through an input multiplexer to use one of four external pins (connected through the switch matrix) or one of four internal sources. The maximum input signal frequency is 25 MHz.
  - Six outputs. Connected to pins through the switch matrix.
- Counter/timer features:
  - Each SCTimer is configurable as two 16-bit counters or one 32-bit counter.
  - Counters can be clocked by the system clock or selected input.
  - Configurable as up counters or up-down counters.
  - Configurable number of match and capture registers. Up to eight match and capture registers total.
  - Upon match create the following events: interrupt; stop, limit, halt the timer or change counting direction; toggle outputs.
  - Counter value can be loaded into capture register triggered by a match or input/output toggle.
- PWM features:
  - Counters can be used with match registers to toggle outputs and create time-proportioned PWM signals.
  - Up to six single-edge or dual-edge PWM outputs with independent duty cycle and common PWM cycle length.
- Event creation features: