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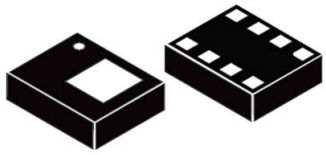
LPS225HB

MEMS pressure sensor: 26 - 126 kPa absolute digital output barometer

Datasheet - production data



HLGA 8L
2.0 x 2.5 x 0.8 (max) mm

Features

- 26 to 126 kPa absolute pressure range
- High-resolution mode: 1 Pa RMS
- Low-power mode: 3.5 Pa RMS
- Current consumption down to 4 µA
- High overpressure capability: 20x full scale
- Embedded temperature compensation
- Embedded 24-bit ADC
- ODR from 1 Hz to 75 Hz
- SPI and I²C interfaces
- Embedded FIFO
- Interrupt functions: Data Ready, FIFO flags, pressure thresholds
- Supply voltage: 1.7 to 3.6 V
- Small and thin package
- ECOPACK® lead-free compliant

Applications

- Altimeters and barometers for portable devices
- GPS applications
- Weather station equipment
- Sport watches

Description

The LPS225HB is an ultra-compact piezoresistive absolute pressure sensor. It includes a monolithic sensing element and an IC interface which communicates a digital signal from the sensing element to the application.

The sensing element, which detects absolute pressure, consists of a suspended membrane inside a single mono-silicon substrate and is manufactured using a dedicated process developed by ST.

The membrane is very small compared to the traditionally built silicon micromachined membranes. Membrane breakage is prevented by an intrinsic mechanical stopper.

The IC interface is manufactured using a standard CMOS process that allows a high level of integration to design a dedicated circuit which is trimmed to better match the characteristics of the sensing element.

The LPS225HB is available in a full-mold, holed LGA package (HLGA). It is guaranteed to operate over a temperature range extending from -40 °C to +85 °C. The package is holed to allow external pressure to reach the sensing element.

Table 1. Device summary

Order code	Temperature range [°C]	Package	Packing
LPS225HBTR	-40 to +85°C	HLGA-8L	Tape and reel

Contents

List of tables

List of figures

1 Block diagram and pin description

Figure 1. Block diagram

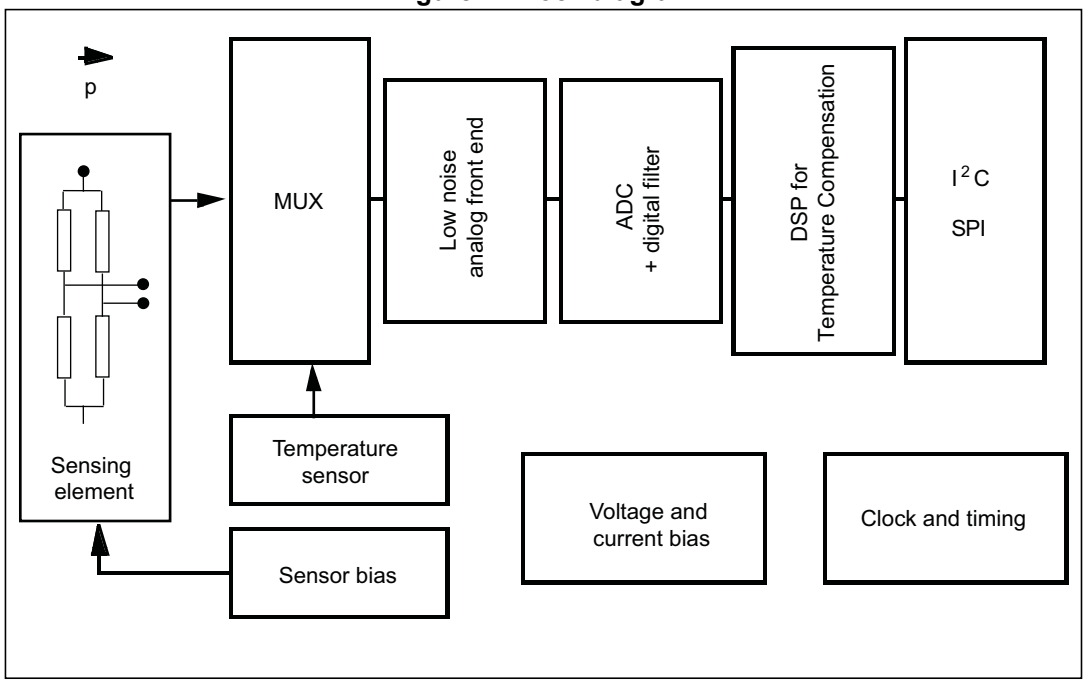


Figure 2. Pin connections

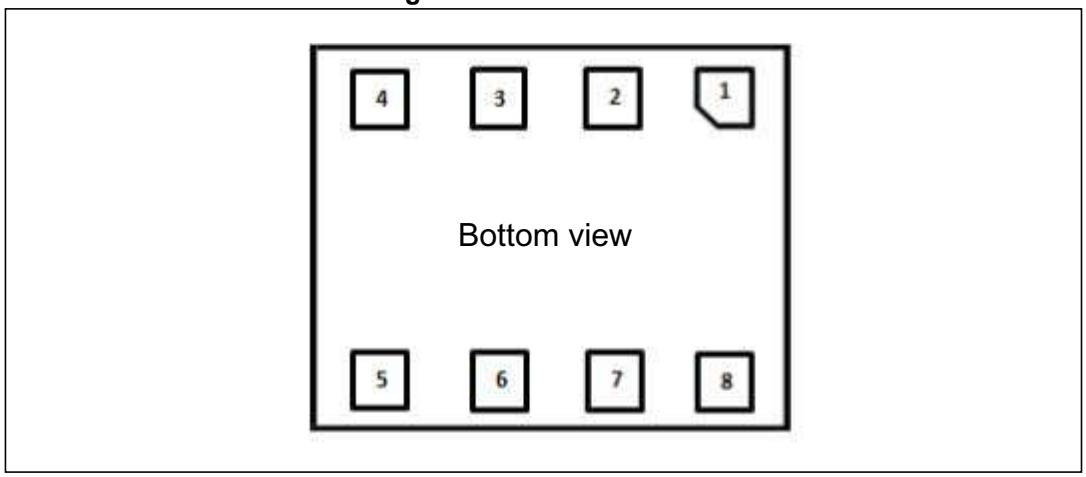


Table 2. Pin description

Pin number	Name	Function
1	GND	0 V supply
2	CS	SPI enable I^2C/SPI mode selection (1: SPI idle mode / I^2C communication enabled; 0: SPI communication mode / I^2C disabled)
3	SDA SDI SDI/SDO	I^2C serial data (SDA) 4-wire SPI serial data input (SDI) 3-wire serial data input/output (SDI/SDO)
4	SCL SPC	I^2C serial clock (SCL) SPI serial port clock (SPC)
5	SDO SA0	4-wire SPI serial data output (SDO) I^2C less significant bit of the device address (SA0)
6	VDD_IO	Power supply for I/O pins
7	INT_DRDY	Interrupt or Data Ready
8	VDD	Power supply

2 Mechanical and electrical specifications

2.1 Mechanical characteristics

VDD = 1.8 V, T = 25 °C, unless otherwise noted.

Table 3. Pressure and temperature sensor characteristics

Symbol	Parameter	Test condition	Min.	Typ.(1)	Max.	Unit
Pressure sensor characteristics						
PT_{op}	Operating temperature range		-40		+85	°C
PT_{full}	Full accuracy temperature range		0		+65	°C
P_{op}	Operating pressure range		260		1260	hPa
P_{bits}	Pressure output data			24		bits
P_{sens}	Pressure sensitivity			4096		LSB/ hPa
P_{AccRel}	Relative accuracy over pressure(2)	P = 800 - 1100 hPa T = 25 °C		±0.1		hPa
P_{AccT}	Absolute accuracy over temperature	P_{op} T = 0 to 65 °C After OPC(3)		±0.1		hPa
		P_{op} T = 0 to 65 °C no OPC (3)		±1		
P_{noise}	RMS pressure sensing noise(4)	with embedded filtering		0.0075		hPa RMS
ODR_{Pres}	Pressure output data rate(5)			1 10 25 50 75		Hz
Temperature sensor characteristics						
T_{op}	Operating temperature range		-40		+85	°C
T_{sens}	Temperature sensitivity			100		LSB/°C
T_{acc}	Temperature absolute accuracy	T = 0 to 65 °C		±1.5		°C
ODR_T	Output temperature data rate(5)			1 10 25 50 75		Hz

1. Typical specifications are not guaranteed.
2. Parameter not tested at final test
3. OPC: One-Point Calibration, see *RPDS_L (18h)*, *RPDS_H (19h)*.
4. Pressure noise RMS evaluated in a controlled environment, based on the average standard deviation of 50 measurements at highest ODR and with LC_EN bit = 0, EN_LPFP = 1, LPFP_CFG = 1.
5. Output data rate is configured acting on ODR[2:0] in *CTRL_REG1 (10h)*.

2.2 Electrical characteristics

VDD = 1.8 V, T = 25 °C, unless otherwise noted.

Table 4. Electrical characteristics

Symbol	Parameter	Test condition	Min.	Typ.(1)	Max.	Unit
VDD	Supply voltage		1.7		3.6	V
VDD_IO	IO supply voltage		1.7		VDD+0.1	V
Idd	Supply current	@ ODR 1Hz		15		µA
IddPdn	Supply current in power-down mode			1		µA

1. Typical specifications are not guaranteed.

2.3 Communication interface characteristics

2.3.1 SPI - serial peripheral interface

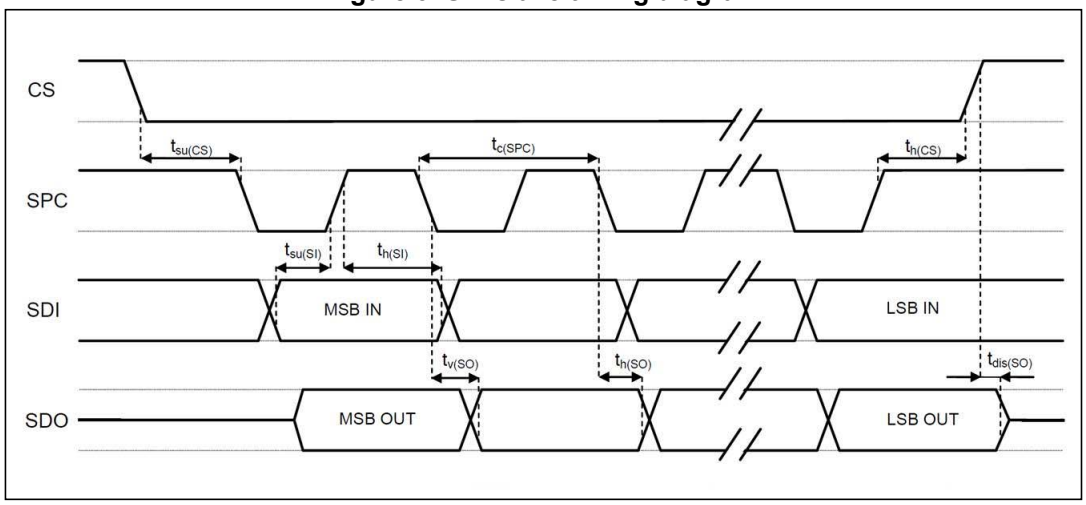
Subject to general operating conditions for Vdd and T_{OP}.

Table 5. SPI slave timing values

Symbol	Parameter	Value(1)		Unit
		Min	Max	
$t_{c(SPC)}$	SPI clock cycle	100		ns
$f_{c(SPC)}$	SPI clock frequency		10	MHz
$t_{su(CS)}$	CS setup time	6		ns
$t_{h(CS)}$	CS hold time	8		
$t_{su(SI)}$	SDI input setup time	5		
$t_{h(SI)}$	SDI input hold time	15		
$t_{v(SO)}$	SDO valid output time		50	
$t_{h(SO)}$	SDO output hold time	9		
$t_{dis(SO)}$	SDO output disable time		50	

1. Values are guaranteed at 10 MHz clock frequency for SPI with both 4 and 3 wires, based on characterization results, not tested in production.

Figure 3. SPI slave timing diagram



Note: Measurement points are done at 0.2·Vdd_IO and 0.8·Vdd_IO, for both ports.

2.3.2 I²C - inter-IC control interface

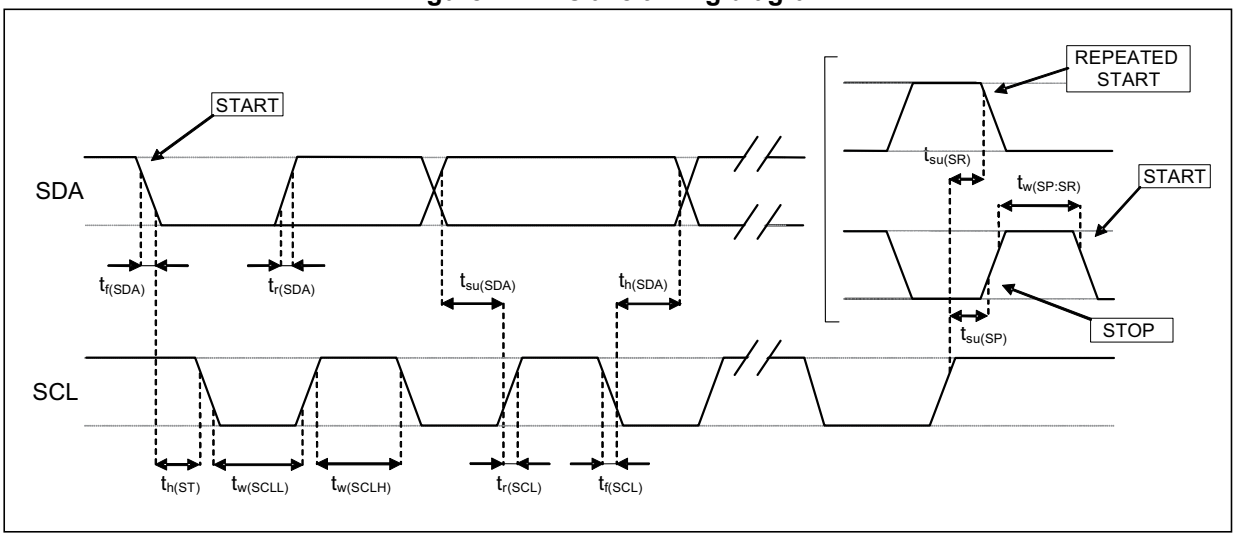
Subject to general operating conditions for Vdd and T_{OP}.

Table 6. I²C slave timing values

Symbol	Parameter (1)	I²C standard mode(1)		I²C fast mode(1)		Unit
		Min	Max	Min	Max	
$f_{(SCL)}$	SCL clock frequency	0	100	0	400	kHz
$t_{w(SCLL)}$	SCL clock low time	4.7		1.3		µs
$t_{w(SCLH)}$	SCL clock high time	4.0		0.6		
$t_{su(SDA)}$	SDA setup time	250		100		ns
$t_{h(SDA)}$	SDA data hold time	0.01	3.45	0	0.9	µs
$t_{r(SDA)}$ $t_{r(SCL)}$	SDA and SCL rise time		1000	$20 + 0.1C_b$(2)	300	ns
$t_{f(SDA)}$ $t_{f(SCL)}$	SDA and SCL fall time		300	$20 + 0.1C_b$(2)	300	
$t_{h(ST)}$	START condition hold time	4		0.6		µs
$t_{su(SR)}$	Repeated START condition setup time	4.7		0.6		
$t_{su(SP)}$	STOP condition setup time	4		0.6		
$t_{w(SP:SR)}$	Bus free time between STOP and START condition	4.7		1.3		

1. Data based on standard I²C protocol requirement, not tested in production.
2. C_b = total capacitance of one bus line, in pF.

Figure 4. I²C slave timing diagram



Note: Measurement points are done at 0.2·Vdd_IO and 0.8·Vdd_IO, for both ports.

2.4 Absolute maximum ratings

Stress above those listed as “Absolute maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 7. Absolute maximum ratings

Symbol	Ratings	Maximum value	Unit
Vdd	Supply voltage	-0.3 to 4.8	V
Vdd_IO	I/O pins supply voltage	-0.3 to 4.8	V
Vin	Input voltage on any control pin	-0.3 to Vdd_IO +0.3	V
P	Overpressure	2	MPa
T_{STG}	Storage temperature range	-40 to +125	°C
ESD	Electrostatic discharge protection	2 (HBM)	kV

Note: Supply voltage on any pin should never exceed 4.8 V.

This device is sensitive to mechanical shock, improper handling can cause permanent damage to the part.

This device is sensitive to electrostatic discharge (ESD), improper handling can cause permanent damage to the part.

3 Functionality

The LPS225HB is a high-resolution, digital output pressure sensor packaged in an HLGA full-mold package. The complete device includes a sensing element based on a piezoresistive Wheatstone bridge approach, and an IC interface which communicates a digital signal from the sensing element to the application.

3.1 Sensing element

An ST proprietary process is used to obtain a mono-silicon µ-sized membrane for MEMS pressure sensors without requiring substrate-to-substrate bonding. When pressure is applied, the membrane deflection induces an imbalance in the Wheatstone bridge piezoresistances whose output signal is converted by the IC interface.

3.2 I^2C interface

The complete measurement chain is composed of a low-noise amplifier which converts the resistance unbalancing of the MEMS sensors (pressure and temperature) into an analog voltage using an analog-to-digital converter.

The pressure and temperature data may be accessed through an I²C/SPI interface, thus making the device particularly suitable for direct interfacing with a microcontroller.

The LPS225HB features a Data-Ready signal which indicates when a new set of measured pressure and temperature data are available, thus simplifying data synchronization in the digital system that uses the device.

3.3 Factory calibration

The IC interface is factory calibrated at three temperatures and two pressures for sensitivity and accuracy.

The trimming values are stored inside the device in a non-volatile structure. When the device is turned on, the trimming parameters are downloaded into the registers to be employed during normal operation which allows the device to be used without requiring any further calibration.

4 FIFO

The LPS225HB embeds 32 slots of 40-bit data FIFO to store the pressure and temperature output values. This allows consistent power saving for the system, since the host processor does not need to continuously poll data from the sensor, but it can wake up only when needed and burst the significant data out from the FIFO. This buffer can work according to seven different modes: Bypass mode, FIFO mode, Stream mode, Dynamic-Stream mode, Stream-to-FIFO mode, Bypass-to-Stream and Bypass-to-FIFO mode. The FIFO buffer is enabled when the FIFO_EN bit in *CTRL_REG2 (11h)* is set to '1' and each mode is selected by the FIFO_MODE[2:0] bits in *FIFO_CTRL (14h)*. Programmable FIFO threshold status, FIFO overrun events and the number of unread samples stored are available in the *FIFO_STATUS (26h)* register and can be set to generate dedicated interrupts on the INT_DRDY pad using the *CTRL_REG3 (12h)* register.

FIFO_STATUS (26h)(FTH_FIFO) goes to '1' when the number of unread samples (*FIFO_STATUS (26h)*(FSS5:0)) is greater than or equal to WTM[4:0] in *FIFO_CTRL (14h)*. If *FIFO_CTRL (14h)*(WTM4:0) is equal to 0, *FIFO_STATUS (26h)*(FTH_FIFO) goes to '0'.

FIFO_STATUS (26h)(OVRN) is equal to '1' if a FIFO slot is overwritten.

FIFO_STATUS (26h)(FSS5:0) contains stored data levels of unread samples; when FSS[5:0] is equal to '000000', FIFO is empty, when FSS[5:0] is equal to '100000', FIFO is full and the unread samples are 32.

To guarantee the switching into and out of FIFO mode, discard the first sample acquired.

4.1 Bypass mode

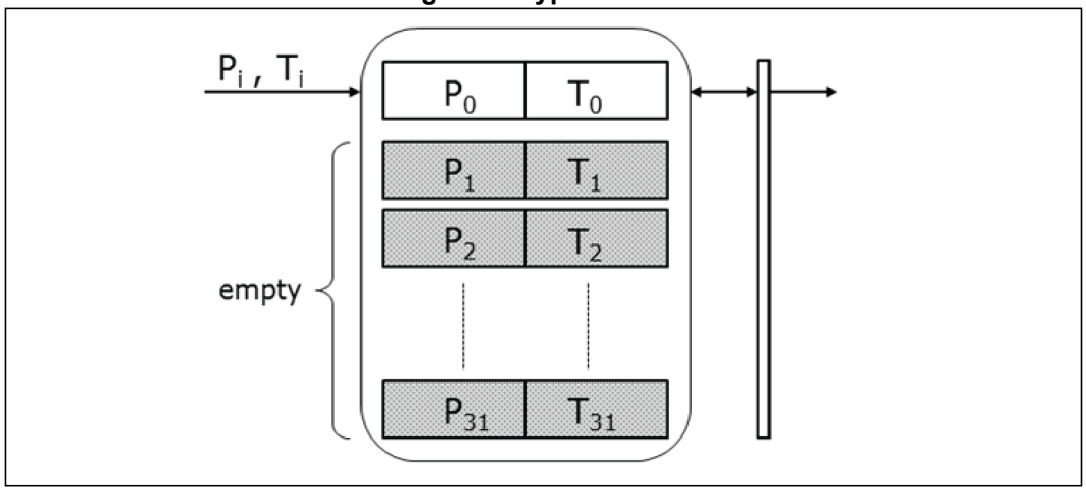
In Bypass mode (*FIFO_CTRL (14h)*(FMODE2:0)=000), the FIFO is not operational and it remains empty.

Bypass mode is also used to reset the FIFO when in FIFO mode.

As described in the next figure, for each channel only the first address is used. When new data is available, the older data is overwritten.

Every time Bypass mode is selected, FIFO content is flushed.

Figure 5. Bypass mode



4.2 FIFO mode

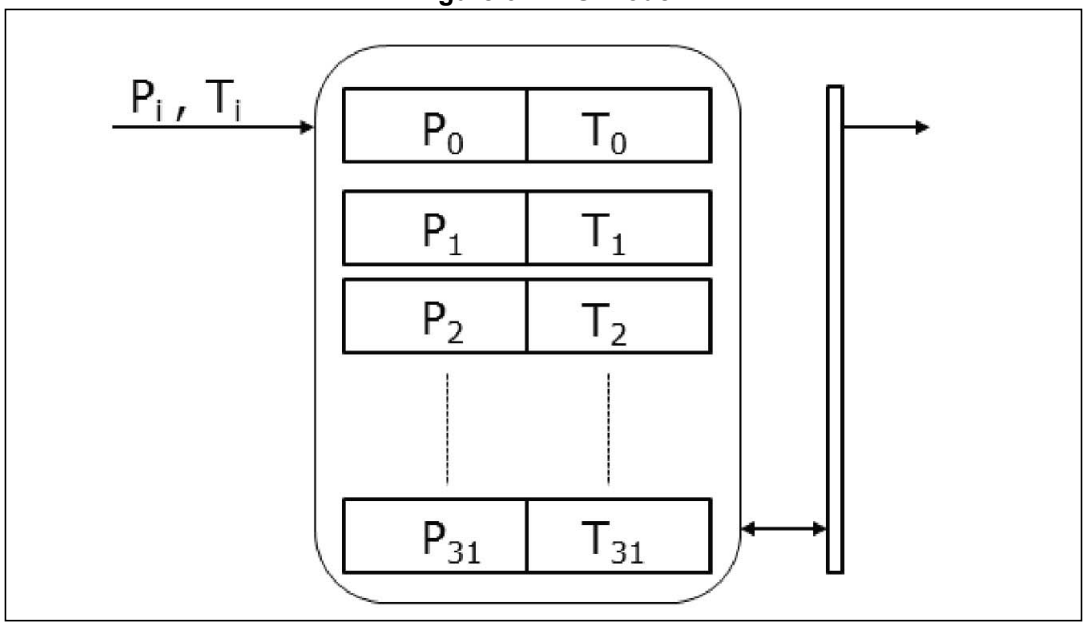
In FIFO mode (*FIFO_CTRL (14h)*(FMODE2:0) = 001) data from the output *PRESS_OUT_XL (28h)*, *PRESS_OUT_L (29h)*, *PRESS_OUT_H (2Ah)* and *TEMP_OUT_L (2Bh)*, *TEMP_OUT_H (2Ch)* are stored in the FIFO until it is overwritten.

To reset FIFO content, in Bypass mode the value '000' must be written in *FIFO_CTRL (14h)*(FMODE2:0). After this reset command, it is possible to restart FIFO mode writing the value '001' in *FIFO_CTRL (14h)*(FMODE2:0).

The FIFO buffer memorizes 32 levels of data but the depth of the FIFO can be resized by setting the *CTRL_REG2 (11h)*(STOP_ON_FTH) bit. If the STOP_ON_FTH bit is set to '1', FIFO depth is limited to *FIFO_CTRL (14h)*(WTM4:0) + 1 data.

A FIFO threshold interrupt can be enabled (F_OVR bit in *CTRL_REG3 (12h)* in order to be raised when the FIFO is filled to the level specified by the WTM4:0 bits of *FIFO_CTRL (14h)*. When a FIFO threshold interrupt occurs, the first data has been overwritten and the FIFO stops collecting data from the input pressure and temperature.

Figure 6. FIFO mode



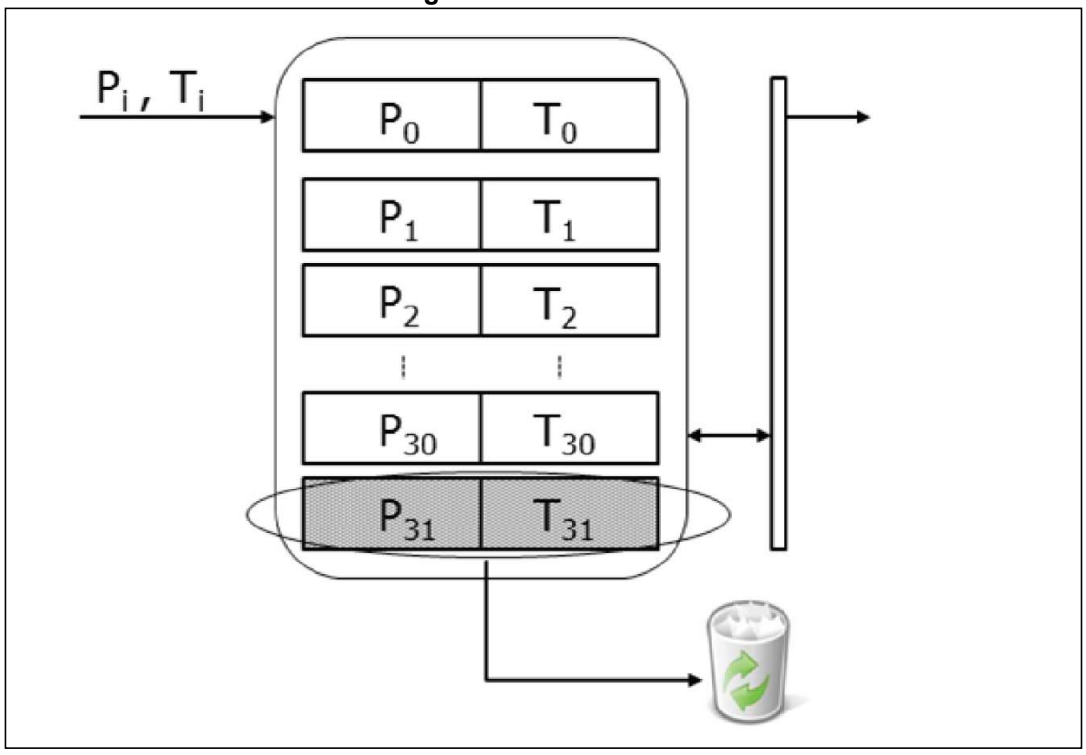
4.3 Stream mode

Stream mode (*FIFO_CTRL (14h)*(FMODE2:0) = 010) provides continuous FIFO update: as new data arrive, the older is discarded.

Once the entire FIFO has been read, the last data read remains in the FIFO and hence once a new sample is acquired, the *FIFO_STATUS (26h)*(FSS5:0) value rises from 0 to 2.

An overrun interrupt can be enabled, *CTRL_REG3 (12h)*(F_OVR) = '1', in order to inform when the FIFO is full and eventually read its content all at once. If an overrun occurs, the oldest sample in FIFO is overwritten, so if the FIFO was empty, the lost sample has already been read.

Figure 7. Stream mode



In the latter case reading all FIFO content before an overrun interrupt has occurred, the first data read is equal to the last already read in the previous burst, so the number of new data available in FIFO depends on the previous reading.

4.4 Dynamic-Stream mode

In Dynamic-Stream mode (*FIFO_CTRL (14h)*(FMODE2:0) = 110) after emptying the FIFO, the first new sample that arrives becomes the first to be read in a subsequent read burst. In this way, the number of new data available in FIFO does not depend on the previous reading.

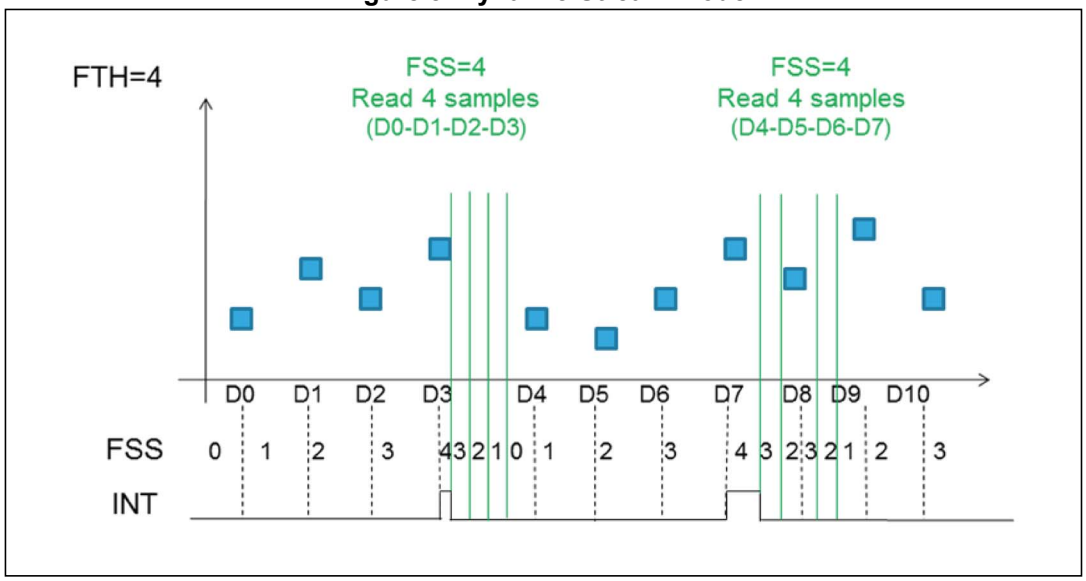
In Dynamic-Stream mode *FIFO_STATUS (26h)*(FSS5:0) is the number of new pressure and temperature samples available in the FIFO buffer.

Stream Mode is intended to be used to read all 32 samples of FIFO within an ODR after receiving an overrun signal.

Dynamic-Stream is intended to be used to read *FIFO_STATUS (26h)*(FSS5:0) samples when it is not possible to guarantee reading data within an ODR.

Also, a FIFO threshold interrupt on the INT_DRDY pad through *CTRL_REG3 (12h)*(F_FTH) can be enabled in order to read data from the FIFO and leave free memory slots for incoming data.

Figure 8. Dynamic-Stream mode



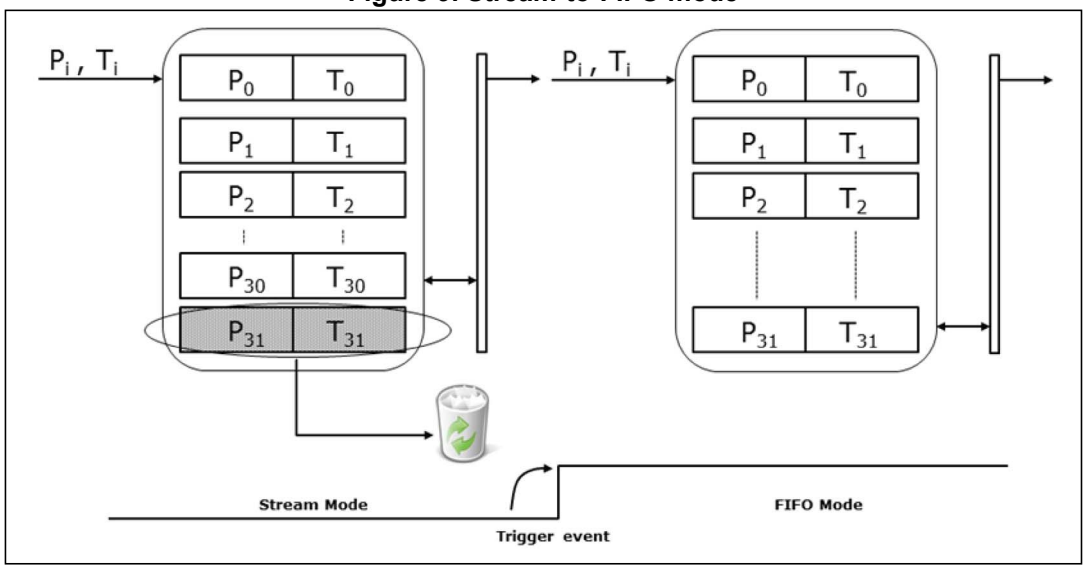
4.5 Stream-to-FIFO mode

In Stream-to-FIFO mode (*FIFO_CTRL (14h)*(FMODE2:0) = 011), FIFO behavior changes according to the INT_SOURCE(IA) bit. When the INT_SOURCE(IA) bit is equal to '1', FIFO operates in FIFO mode. When the INT_SOURCE(IA) bit is equal to '0', FIFO operates in Stream mode.

An interrupt generator can be set to the desired configuration through *INTERRUPT_CFG (0Bh)*.

The *INTERRUPT_CFG (0Bh)*(LIR) bit should be set to '1' in order to have latched interrupt.

Figure 9. Stream-to-FIFO mode



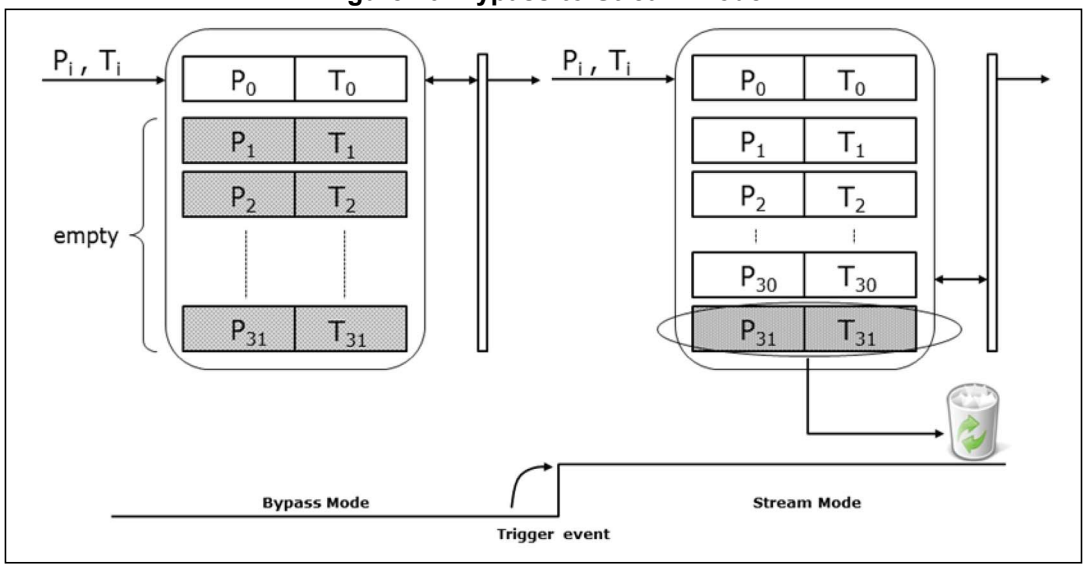
4.6 Bypass-to-Stream mode

In Bypass-to-Stream mode (*FIFO_CTRL (14h)*(FMODE2:0) = '100'), data measurement storage inside FIFO operates in Stream mode when INT_SOURCE(IA) is equal to '1',otherwise FIFO content is reset (Bypass mode).

An interrupt generator can be set to the desired configuration through *INTERRUPT_CFG (0Bh)*.

The *INTERRUPT_CFG (0Bh)*(LIR) bit should be set to '1' in order to have latched interrupt.

Figure 10. Bypass-to-Stream mode



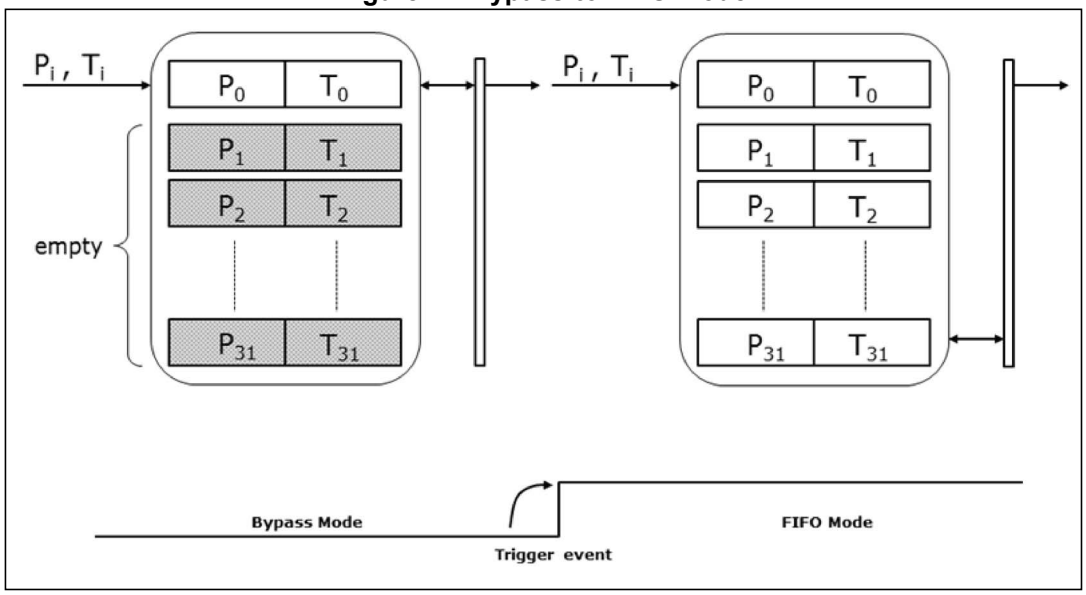
4.7 Bypass-to-FIFO mode

In Bypass-to-FIFO mode (*FIFO_CTRL (14h)*(FMODE2:0) = '111'), data measurement storage inside FIFO operates in FIFO mode when INT_SOURCE(IA) is equal to '1', otherwise FIFO content is reset (Bypass mode).

An interrupt generator can be set to the desired configuration through *INTERRUPT_CFG (0Bh)*.

The *INTERRUPT_CFG (0Bh)*(LIR) bit should be set to '1' in order to have latched interrupt.

Figure 11. Bypass-to-FIFO mode



4.8 Retrieving data from FIFO

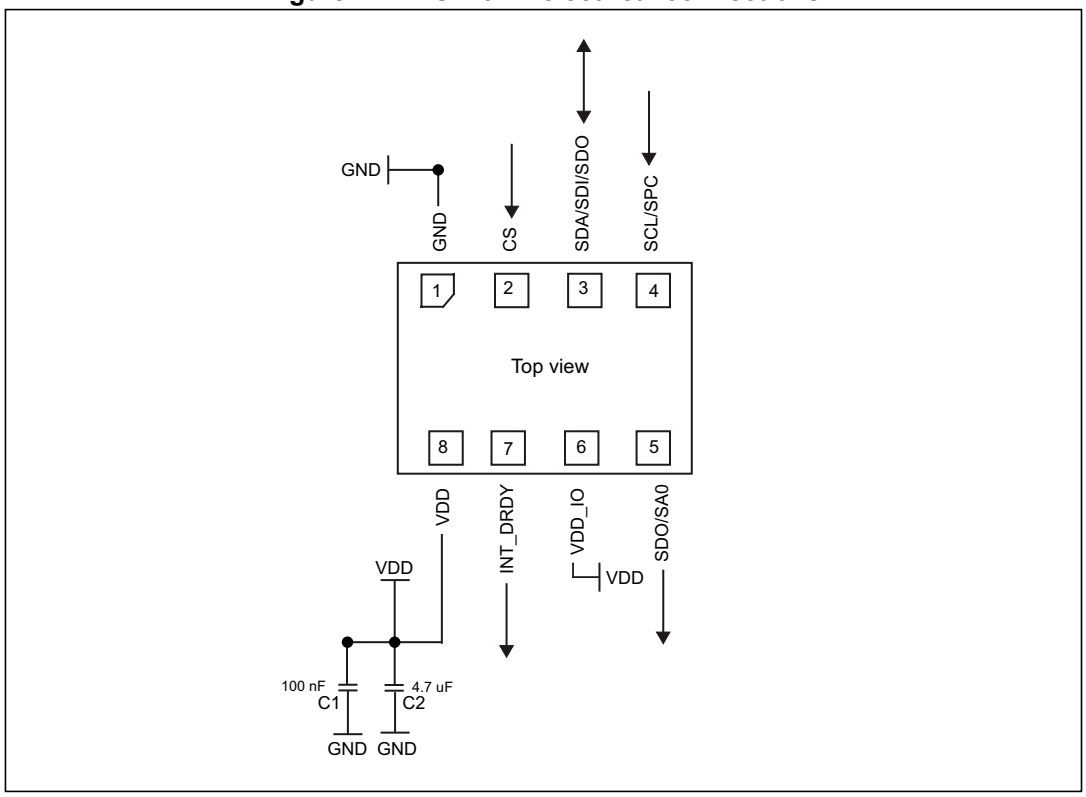
FIFO data is read from PRESS_OUT (Addr. reg 28h, 29h, 2Ah) and TEMP_OUT (Addr. reg 2Bh, 2Ch).

Each time data is read from the FIFO, the oldest data are placed in the *PRESS_OUT_XL (28h)*, *PRESS_OUT_L (29h)*, *PRESS_OUT_H (2Ah)*, *TEMP_OUT_L (2Bh)* and *TEMP_OUT_H (2Ch)* registers and both single-read and read-burst operations can be used.

The device automatically updates the reading address and it rolls back to 28h when register 2Ch is reached. In order to read all FIFO levels in multiple byte reading, 160 bytes (5 output registers by 32 levels) must be read.

5 Application hints

Figure 12. LPS225HB electrical connections



The device core is supplied through the VDD line. Power supply decoupling capacitors (100 nF, 4.7 µF) should be placed as near as possible to the supply pad of the device (common design practice).

The functionality of the device and the measured data outputs are selectable and accessible through the I²C/SPI interface. When using the I²C, CS must be tied high (i.e. connected to VDD_IO).

5.1 Soldering information

The HLGA package is compliant with the ECOPACK® standard and it is qualified for soldering heat resistance according to JEDEC J-STD-020.

6 Digital interfaces

6.1 I²C serial interface

The registers embedded in the LPS225HB may be accessed through both the I²C and SPI serial interfaces. The latter may be SW configured to operate either in 3-wire or 4-wire interface mode.

The serial interfaces are mapped onto the same pads. To select/exploit the I²C interface, the CS line must be tied high (i.e. connected to Vdd_IO).

Table 8. Serial interface pin description

Pin name	Pin description
CS	SPI enable I²C/SPI mode selection (1: SPI idle mode / I²C communication enabled; 0: SPI communication mode / I²C disabled)
SCL/SPC	I²C serial clock (SCL) SPI serial port clock (SPC)
SDA SDI SDI/SDO	I²C serial data (SDA) 4-wire SPI serial data input (SDI) 3-wire serial data input /output (SDI/SDO)
SDO SAO	SPI serial data output (SDO) I²C less significant bit of the device address (SA0)

6.2 I²C serial interface (CS = High)

The LPS225HB I²C is a bus slave. The I²C is employed to write data into registers whose content can also be read back.

The relevant I²C terminology is given in *Table 9*.

Table 9. I²C terminology

Term	Description
Transmitter	The device which sends data to the bus
Receiver	The device which receives data from the bus
Master	The device which initiates a transfer, generates clock signals and terminates a transfer
Slave	The device addressed by the master

There are two signals associated with the I²C bus: the serial clock line (SCL) and the serial data line (SDA). The latter is a bidirectional line used for sending and receiving the data to/from the interface. Both lines have to be connected to Vdd_IO through pull-up resistors.

The I²C interface is compliant with fast mode (400 kHz) I²C standards as well as with the normal mode.

6.2.1 I²C operation

The transaction on the bus is started through a START (ST) signal. A start condition is defined as a HIGH-to-LOW transition on the data line while the SCL line is held HIGH. After this has been transmitted by the master, the bus is considered busy. The next data byte transmitted after the start condition contains the address of the slave in the first 7 bits and the eighth bit tells whether the master is receiving data from the slave or transmitting data to the slave. When an address is sent, each device in the system compares the first seven bits after a start condition with its address. If they match, the device considers itself addressed by the master.

The slave address (SAD) associated to the LPS225HB is 101110xb. The **SDO**/**SA0** pad can be used to modify the less significant bit of the device address. If the SA0 pad is connected to voltage supply, LSb is ‘1’ (address 1011101b), otherwise if the SA0 pad is connected to ground, the LSb value is ‘0’ (address 1011100b). This solution permits to connect and address two different LPS225HB devices to the same I²C lines.

Data transfer with acknowledge is mandatory. The transmitter must release the SDA line during the acknowledge pulse. The receiver must then pull the data line LOW so that it remains stable low during the HIGH period of the acknowledge clock pulse. A receiver which has been addressed is obliged to generate an acknowledge after each byte of data received.

The I²C embedded in the LPS225HB behaves like a slave device and the following protocol must be adhered to. After the start condition (ST) a slave address is sent, once a slave acknowledge (SAK) has been returned, an 8-bit sub-address (SUB) will be transmitted: the 7 LSB represents the actual register address while the MSB enables address auto increment. If the MSb of the SUB field is ‘1’, the SUB (register address) will be automatically increased to allow multiple data read/write.

The slave address is completed with a Read/Write bit. If the bit is ‘1’ (Read), a repeated START (SR) condition must be issued after the two sub-address bytes; if the bit is ‘0’ (Write) the master will transmit to the slave with direction unchanged. *Table 10* explains how the SAD+read/write bit pattern is composed, listing all the possible configurations.

Table 10. SAD+Read/Write patterns

Command	SAD[6:1]	SAD[0] = SA0	R/W	SAD+R/W
Read	101110	0	1	10111001 (B9h)
Write	101110	0	0	10111000 (B8h)
Read	101110	1	1	10111011 (BBh)
Write	101110	1	0	10111010 (BAh)

Table 11. Transfer when master is writing one byte to slave

Master	ST	SAD + W		SUB		DATA		SP
Slave			SAK		SAK		SAK	

Table 12. Transfer when master is writing multiple bytes to slave

Master	ST	SAD + W		SUB		DATA		DATA		SP
Slave			SAK		SAK		SAK		SAK	

Table 13. Transfer when master is receiving (reading) one byte of data from slave

Master	ST	SAD + W		SUB		SR	SAD + R			NMAK	SP
Slave			SAK		SAK			SAK	DATA		

Table 14. Transfer when master is receiving (reading) multiple bytes of data from slave

Master	ST	SAD+W		SUB		SR	SAD+R			MAK		MAK		NMAK	SP
Slave			SAK		SAK			SAK	DATA		DATA		DATA		

Data are transmitted in byte format (DATA). Each data transfer contains 8 bits. The number of bytes transferred per transfer is unlimited. Data is transferred with the most significant bit (MSb) first. If a receiver can't receive another complete byte of data until it has performed some other functions, it can hold the clock line, SCL LOW to force the transmitter into a wait state. Data transfer only continues when the receiver is ready for another byte and releases the data line. If a slave receiver does not acknowledge the slave address (i.e. it is not able to receive because it is performing some real-time function) the data line must be kept HIGH by the slave. The master can then abort the transfer. A LOW-to-HIGH transition on the SDA line while the SCL line is HIGH is defined as a STOP condition. Each data transfer must be terminated by the generation of a STOP (SP) condition.

In order to read multiple bytes incrementing the register address, it is necessary to assert the most significant bit of the sub-address field. In other words, SUB(7) must be equal to 1 while SUB(6-0) represents the address of the first register to be read.

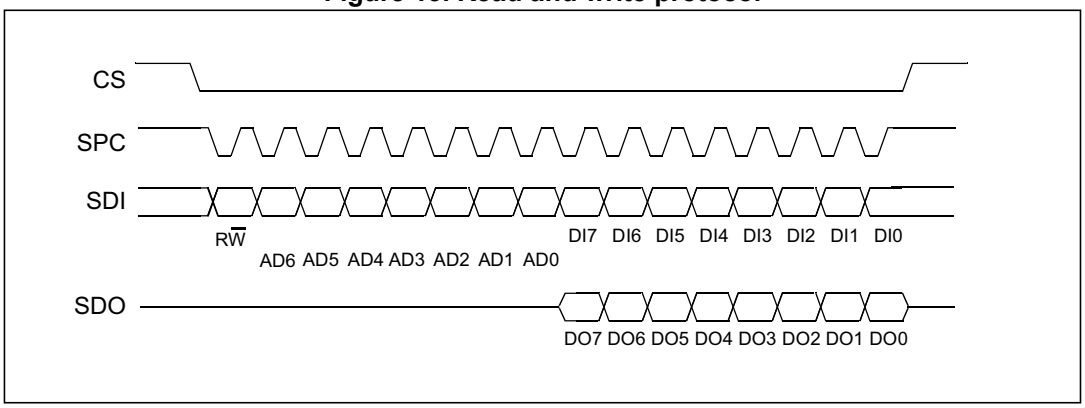
In the presented communication format MAK is Master acknowledge and NMAK is no master acknowledge.

6.3 SPI bus interface

The LPS225HB SPI is a bus slave. The SPI allows writing to and reading from the registers of the device.

The serial interface interacts with the application using 4 wires: **CS**, **SPC**, **SDI** and **SDO**.

Figure 13. Read and write protocol



CS is the serial port enable and it is controlled by the SPI master. It goes low at the start of the transmission and returns to high at the end. **SPC** is the serial port clock and it is controlled by the SPI master. It is stopped high when **CS** is high (no transmission). **SDI** and **SDO** are respectively the serial port data input and output. Those lines are driven at the falling edge of **SPC** and should be captured at the rising edge of **SPC**.

Both the read register and write register commands are completed in 16 clock pulses or in multiples of 8 in the case of multiple read/write bytes. Bit duration is the time between two falling edges of **SPC**. The first bit (bit 0) starts at the first falling edge of **SPC** after the falling edge of **CS** while the last bit (bit 15, bit 23,...) starts at the last falling edge of SPC just before the rising edge of **CS**.

bit 0: R$\overline{W}$ bit. When 0, the data DI(7:0) is written into the device. When 1, the data DO(7:0) from the device is read. In the latter case, the chip will drive **SDO** at the start of bit 8.

bit 1-7: address AD(6:0). This is the address field of the indexed register.

bit 8-15: data DI(7:0) (write mode). This is the data that is written into the device (MSb first).
bit 8-15: data DO(7:0) (read mode). This is the data that is read from the device (MSb first).
In multiple read/write commands further blocks of 8 clock periods are added. When the IF_ADD_INC bit is 0 the address used to read/write data remains the same for every block. When the IF_ADD_INC bit is 1 the address used to read/write data is increased at every block.

The function and the behavior of **SDI** and **SDO** remain unchanged.