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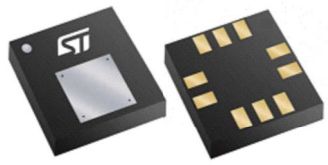
LPS25HB

MEMS pressure sensor: 260-1260 hPa absolute digital output barometer

Datasheet - production data



HLGA-10L
(2.5 x 2.5 x 0.76 mm typ.)

Features

- 260 to 1260 hPa absolute pressure range
- High-resolution mode: 0.01 hPa RMS
- Low power consumption
  - Low-resolution mode: 4 µA
  - Low current & noise mode with FIFO: 4.5 µA
- High overpressure capability: 20x full scale
- Embedded temperature compensation
- 24-bit pressure data output
- ODR from 1 Hz to 25 Hz
- SPI and I^2C interfaces
- Embedded FIFO
- Interrupt functions: Data Ready, FIFO flags, pressure thresholds
- Supply voltage: 1.7 to 3.6 V
- High shock survivability: 10,000 *g*
- ECOPACK® lead-free compliant

Applications

- Altimeter and barometer for portable devices
- Enhanced GPS applications
- Weather station equipment
- Wearable devices

Description

The LPS25HB is a piezoresistive absolute pressure sensor which functions as a digital output barometer. The device comprises a sensing element and an IC interface which communicates through I^2C or SPI from the sensing element to the application.

The sensing element, which detects absolute pressure, consists of a suspended membrane manufactured using a dedicated process developed by ST.

The LPS25HB is available in a full-mold, holed LGA package (HLGA). It is guaranteed to operate over a temperature range extending from -30 to +105 °C. The package is holed to allow external pressure to reach the sensing element.

Table 1. Device summary

Order code	Temperature range [°C]	Package	Packing
LPS25HBTR	-30 to +105 °C	HLGA-10L	Tape and reel

Contents

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List of figures

1 Block diagram and pin description

Figure 1. Block diagram

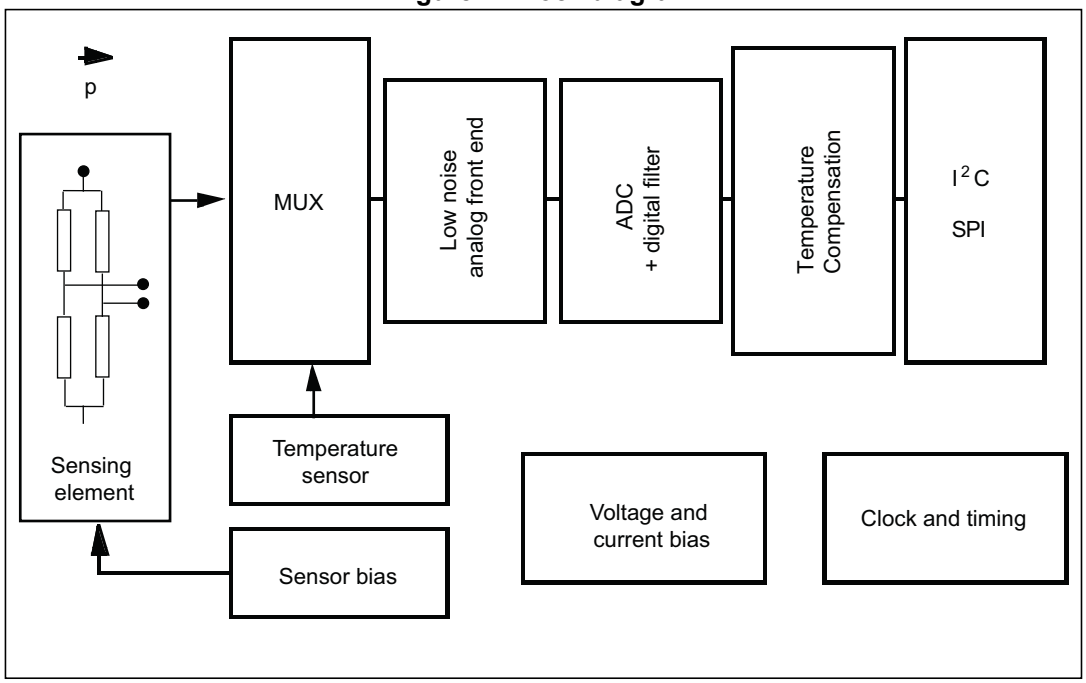


Figure 2. Pin connections (bottom view)

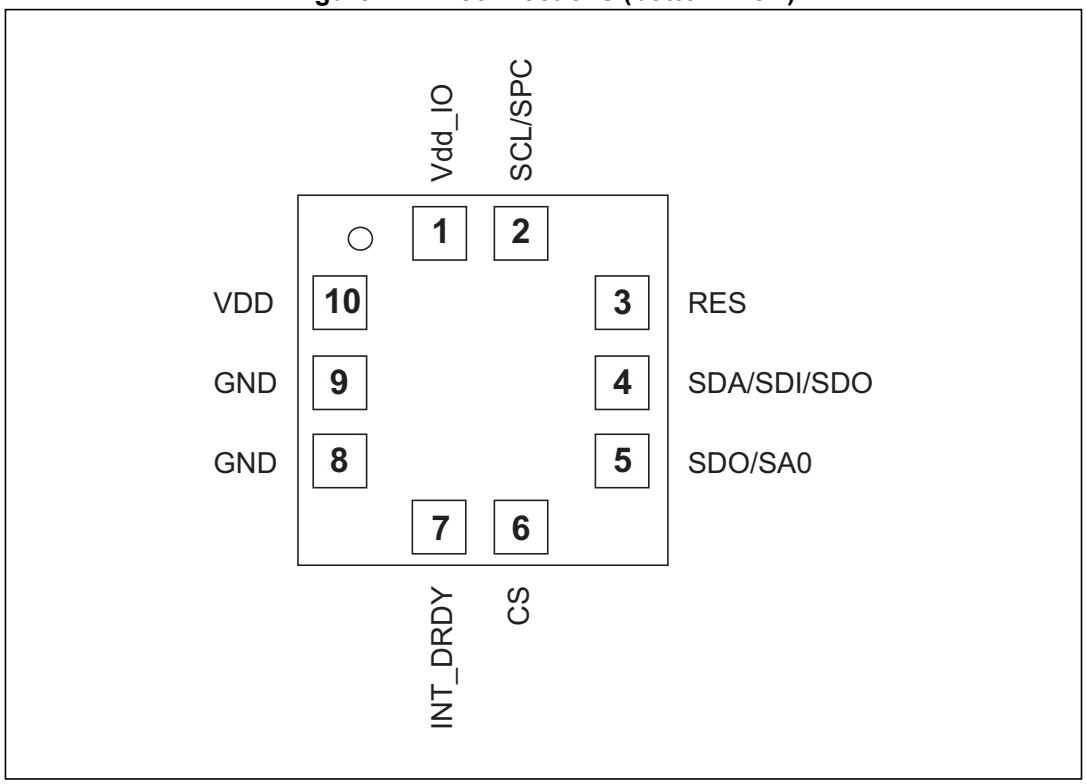


Table 2. Pin description

Pin number	Name	Function
1	Vdd_IO	Power supply for I/O pins
2	SCL SPC	I²C serial clock (SCL) SPI serial port clock (SPC)
3	Reserved	Connect to GND
4	SDA SDI SDI/SDO	I²C serial data (SDA) 4-wire SPI serial data input (SDI) 3-wire serial data input /output (SDI/SDO)
5	SDO SA0	4-wire SPI serial data output (SDO) I²C less significant bit of the device address (SA0)
6	CS	SPI enable I²C/SPI mode selection (1: SPI idle mode / I^2C communication enabled; 0: SPI communication mode / I^2C disabled)
7	INT_DRDY	Interrupt or Data Ready
8	GND	0 V supply
9	GND	0 V supply
10	VDD	Power supply

2 Mechanical and electrical specifications

2.1 Mechanical characteristics

VDD = 1.8 V, T = 25 °C, unless otherwise noted.

Table 3. Pressure and temperature sensor characteristics

Symbol	Parameter	Test condition	Min.	Typ.(1)	Max.	Unit
Pressure sensor characteristics						
PT_{op}	Operating temperature range		-30		+105	°C
PT_{full}	Full accuracy temperature range		0		+80	°C
P_{op}	Operating pressure range		260		1260	hPa
P_{bits}	Pressure output data			24		bits
P_{sens}	Pressure sensitivity			4096		LSB/ hPa
P_{accrel}	Relative accuracy over pressure(2)	P = 800 to 1100 hPa T = 25°C		± 0.1		hPa
P_{accT}	Absolute accuracy pressure over temperature(3)	P = 260 to 1260 hPa T = 20 ~ +60 °C after OPC(4)		± 0.2		hPa
		P = 260 to 1260 hPa T = 0 ~ +80 °C before OPC(4)		± 1		
P_{noise}	Pressure noise(5)	without embedded filtering		0.03		hPa RMS
		with embedded filtering		0.01		
ODR_{Pres}	Pressure output data rate			1 7 12.5 25		Hz
Temperature sensor characteristics						
T_{op}	Operating temperature range		-30		105	°C
T_{bits}	Temperature output data			16		bits
T_{sens}	Temperature sensitivity			480		LSB/°C
Tacc	Absolute accuracy temperature	T= 0 ~ +65 °C		± 2		°C
ORD_T	Temperature output data rate			1 7 12.5 25		Hz

1. Typical specifications are not guaranteed.

2. Characterization data. Parameter not tested at final test.
3. Embedded quadratic compensation.
4. OPC: One Point Calibration in the application.
5. Pressure noise RMS evaluated in a controlled environment based on the average standard deviation of 32 measurements at highest ODR.

2.2 Electrical characteristics

VDD = 1.8 V, T = 25 °C, unless otherwise noted.

Table 4. Electrical characteristics

Symbol	Parameter	Test condition	Min.	Typ.(1)	Max.	Unit
VDD	Supply voltage		1.7		3.6	V
Vdd_IO	IO supply voltage		1.7		VDD + 0.1	V
Idd	Supply current	@ ODR 1 Hz, Low-resolution mode: RES_CONF (10h) = 04h		4		µA
		@ ODR 1 Hz, Low current & noise mode with FIFO: *RES_CONF (10h)* = 05h, *FIFO_CTRL (2Eh)* = DFh, *CTRL_REG2 (21h)* = 50h		4.5		µA
		@ ODR 1 Hz, High-resolution mode: RES_CONF (10h) = 0Fh		25		µA
IddPdn	Supply current in power-down mode			0.5		µA

1. Typical specifications are not guaranteed.

Table 5. DC characteristics

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
DC input characteristics						
Vil	Low-level input voltage (Schmitt buffer)				0.2 * Vdd_IO	V
Vih	High-level input voltage (Schmitt buffer)		0.8 * Vdd_IO			V
DC output characteristics						
Vol	Low-level output voltage		0.2			V
Voh	High-level output voltage				Vdd_IO - 0.2	V

2.3 Communication interface characteristics

2.3.1 SPI - serial peripheral interface

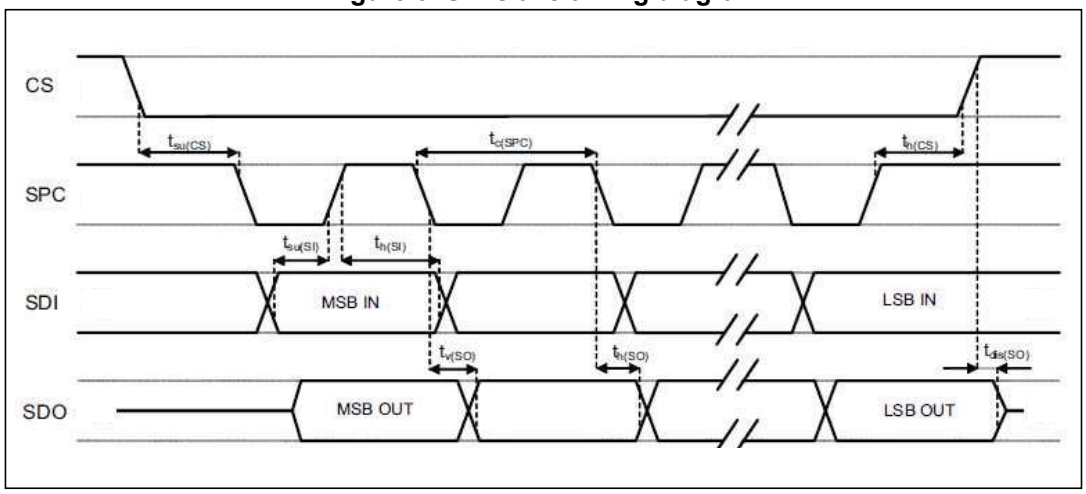
Subject to general operating conditions for Vdd and T_{OP}.

Table 6. SPI slave timing values

Symbol	Parameter	Value(1)		Unit
		Min	Max	
$t_{c(SPC)}$	SPI clock cycle	100		ns
$f_{c(SPC)}$	SPI clock frequency		10	MHz
$t_{su(CS)}$	CS setup time	6		ns
$t_{h(CS)}$	CS hold time	8		
$t_{su(SI)}$	SDI input setup time	5		
$t_{h(SI)}$	SDI input hold time	15		
$t_{v(SO)}$	SDO valid output time		50	
$t_{h(SO)}$	SDO output hold time	9		
$t_{dis(SO)}$	SDO output disable time		50	

1. Values are guaranteed at 10 MHz clock frequency for SPI with both 4 and 3 wires, based on characterization results, not tested in production.

Figure 3. SPI slave timing diagram



Note: Measurement points are done at 0.2·Vdd_IO and 0.8·Vdd_IO, for both ports.

2.3.2 I²C - inter-IC control interface

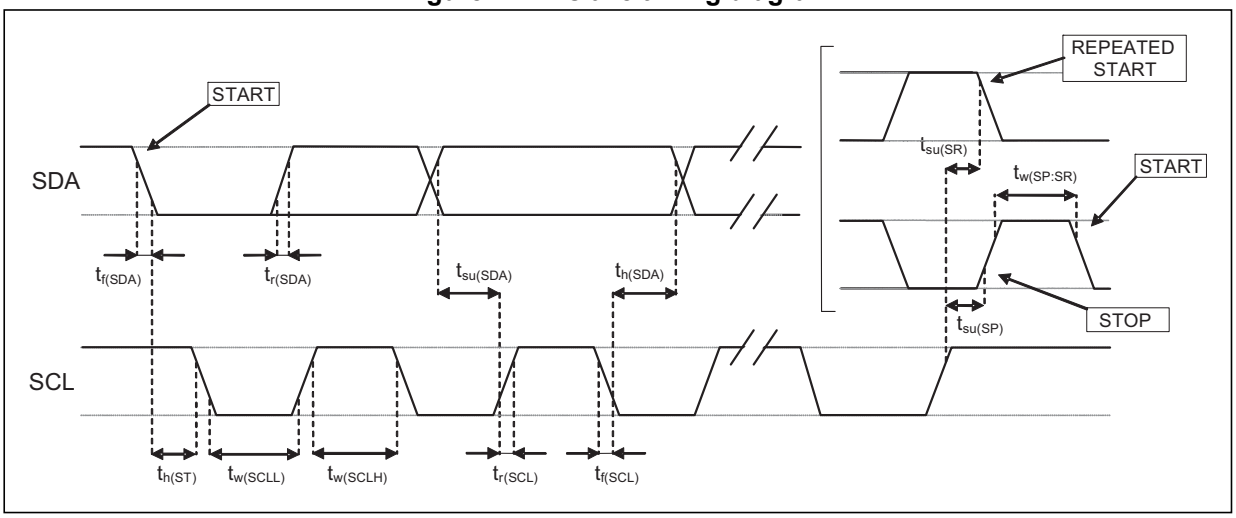
Subject to general operating conditions for Vdd and T_{OP}.

Table 7. I²C slave timing values

Symbol	Parameter (1)	I²C standard		I²C fast mode(1)		Unit
		Min	Max	Min	Max	
$f_{(SCL)}$	SCL clock frequency	0	100	0	400	kHz
$t_{w(SCLL)}$	SCL clock low time	4.7		1.3		µs
$t_{w(SCLH)}$	SCL clock high time	4.0		0.6		
$t_{su(SDA)}$	SDA setup time	250		100		ns
$t_{h(SDA)}$	SDA data hold time	0.01	3.45	0	0.9	µs
$t_{r(SDA)}$ $t_{r(SCL)}$	SDA and SCL rise time		1000	20	300	ns
$t_{f(SDA)}$ $t_{f(SCL)}$	SDA and SCL fall time		300	20x(VDD/5.5)	300	
$t_{h(ST)}$	START condition hold time	4		0.6		µs
$t_{su(SR)}$	Repeated START condition setup time	4.7		0.6		
$t_{su(SP)}$	STOP condition setup time	4		0.6		
$t_{w(SP:SR)}$	Bus free time between STOP and START condition	4.7		1.3		

1. Data based on standard I²C protocol requirement, not tested in production.

Figure 4. I²C slave timing diagram



Note: Measurement points are done at 0.2·Vdd_IO and 0.8·Vdd_IO, for both ports.

2.4 Absolute maximum ratings

Stress above those listed as “Absolute maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 8. Absolute maximum ratings

Symbol	Ratings	Maximum value	Unit
VDD	Supply voltage	-0.3 to 4.8	V
Vdd_IO	I/O pins supply voltage	-0.3 to 4.8	V
Vin	Input voltage on any control pin	-0.3 to Vdd_IO +0.3	V
P	Overpressure	2	MPa
T_{STG}	Storage temperature range	-40 to +125	°C
ESD	Electrostatic discharge protection	2 (HBM)	kV

Note: Supply voltage on any pin should never exceed 4.8 V.

This device is sensitive to mechanical shock, improper handling can cause permanent damage to the part.

This device is sensitive to electrostatic discharge (ESD), improper handling can cause permanent damage to the part.

3 Functionality

The LPS25HB is a high resolution, digital output pressure sensor packaged in an HLGA full-mold package. The complete device includes a sensing element based on a piezoresistive Wheatstone bridge approach, and an IC interface which communicates a digital signal from the sensing element to the application.

3.1 Sensing element

An ST proprietary process is used to obtain a silicon membrane for MEMS pressure sensors. When pressure is applied, the membrane deflection induces an imbalance in the Wheatstone bridge piezoresistances whose output signal is converted by the IC interface.

3.2 I^2C interface

The complete measurement chain is composed of a low-noise amplifier which converts the resistance unbalance of the MEMS sensors (pressure and temperature) into an analog voltage using an analog-to-digital converter.

The pressure and temperature data may be accessed through an I²C/SPI interface thus making the device particularly suitable for direct interfacing with a microcontroller.

The LPS25HB features a Data-Ready signal which indicates when a new set of measured pressure and temperature data are available, thus simplifying data synchronization in the digital system that uses the device.

3.3 Factory calibration

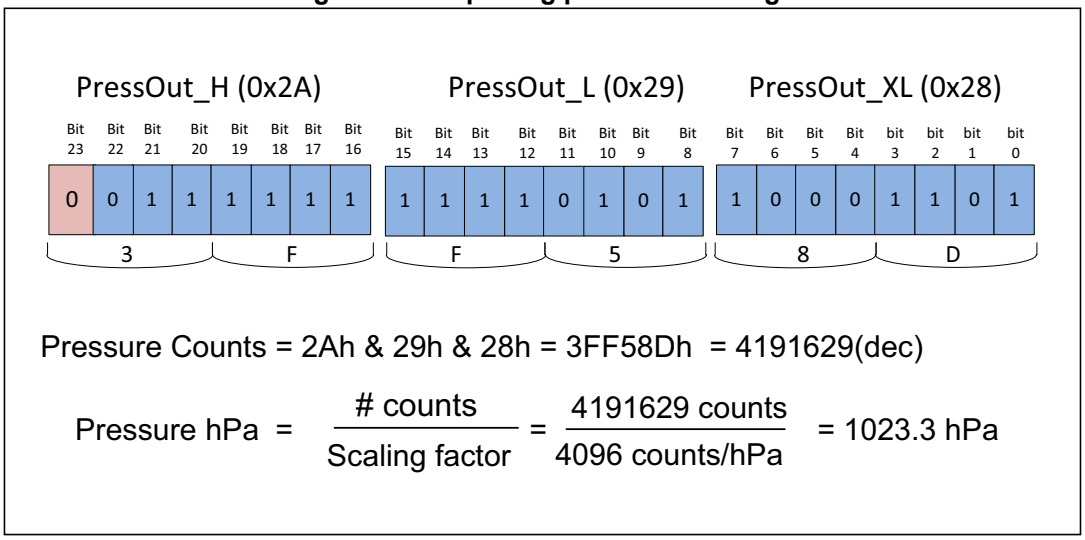
The IC interface is factory calibrated at three temperatures and two pressures for sensitivity and accuracy.

The trimming values are stored inside the device in a non-volatile structure. When the device is turned on, the trimming parameters are downloaded into the registers to be employed during normal operation which allows the device to be used without requiring any further calibration.

3.4 How to interpret pressure readings

The pressure data are stored in 3 registers: *PRESS_OUT_H (2Ah)*, *PRESS_OUT_L (29h)* and *PRESS_OUT_XL (28h)*. The value is expressed as 2's complement. To obtain the pressure in hPa, take the two's complement of the complete word and then divide by 4096 hPa.

Figure 5. Interpreting pressure readings



4 FIFO

The LPS25HB embeds 32-slot data FIFO to store the pressure output values. The FIFO allows consistent power saving for the system, since the host processor does not need to continuously poll data from the sensor, but it can wake up only when needed and burst the significant data out from the FIFO.

This buffer can work according to seven different modes: Bypass mode, FIFO mode, Stream mode, Stream-to-FIFO mode, Bypass-to-Stream mode, Bypass-to-FIFO mode and FIFO Mean mode.

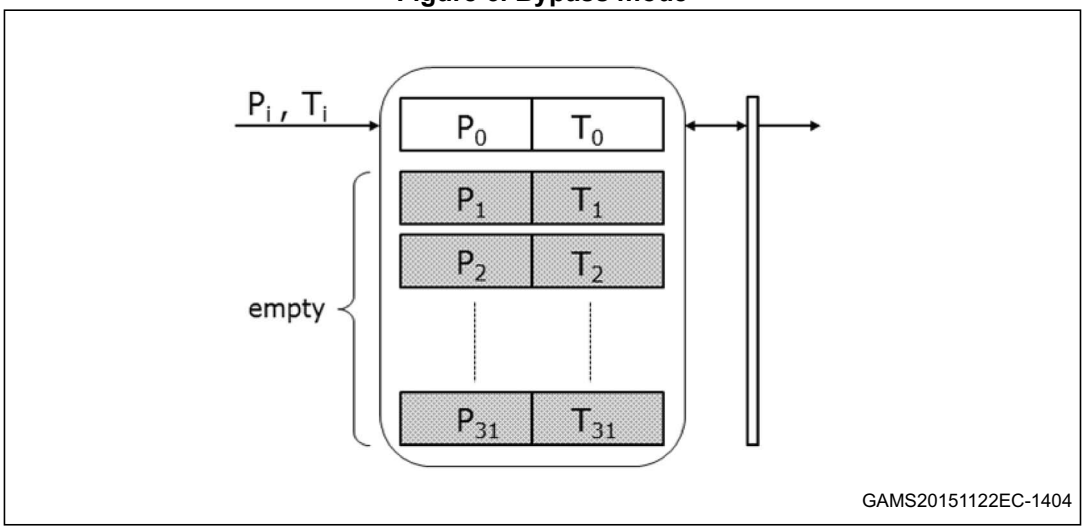
The FIFO buffer is enabled when the FIFO_EN bit in *CTRL_REG2 (21h)* is set to '1' and each mode is selected by the F_MODE[2:0] bits in *FIFO_CTRL (2Eh)*.

FIFO threshold status, FIFO overrun events and the number of unread samples stored are available in the *FIFO_STATUS (2Fh)* register and can be set to generate dedicated interrupts on the INT_DRDY pin in the *CTRL_REG4 (23h)* register.

4.1 Bypass mode

In Bypass mode (F_MODE[2:0] in *FIFO_CTRL (2Eh)* set to '000'), the FIFO is not operational and it remains empty.

Figure 6. Bypass mode



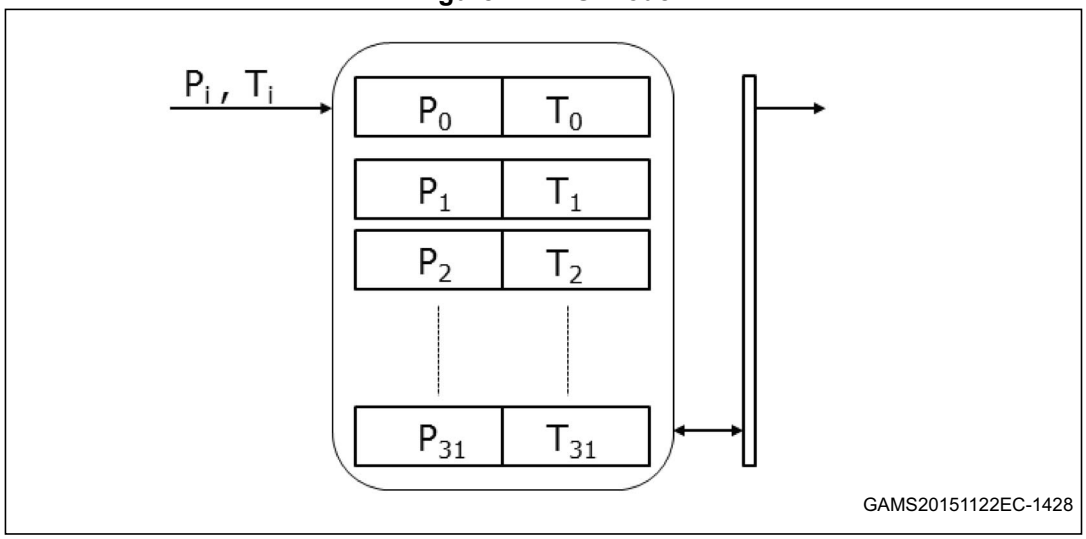
4.2 FIFO mode

In FIFO mode (F_MODE[2:0] in *FIFO_CTRL (2Eh)* set to '001'), the data from *PRESS_OUT_H (2Ah)*, *PRESS_OUT_L (29h)*, and *PRESS_OUT_XL (28h)* are stored in the FIFO.

A watermark interrupt can be enabled (STOP_ON_FTH bit set to '1' in *CTRL_REG2 (21h)*) in order to be raised when the FIFO is filled to the level specified by the WTM_POINT[4:0] bits of *FIFO_CTRL (2Eh)*. The FIFO continues filling until it is full (32 slots of data for pressure output). When full, the FIFO stops collecting data.

The FIFO buffer can store up to 32 levels of data. The FIFO depth can be limited by setting the STOP_ON_FTH bit 5 in *CTRL_REG2 (21h)* to ‘1’ and by selecting a watermark level with the WTM_POINT[4:0] bits in *FIFO_CTRL (2Eh)*.

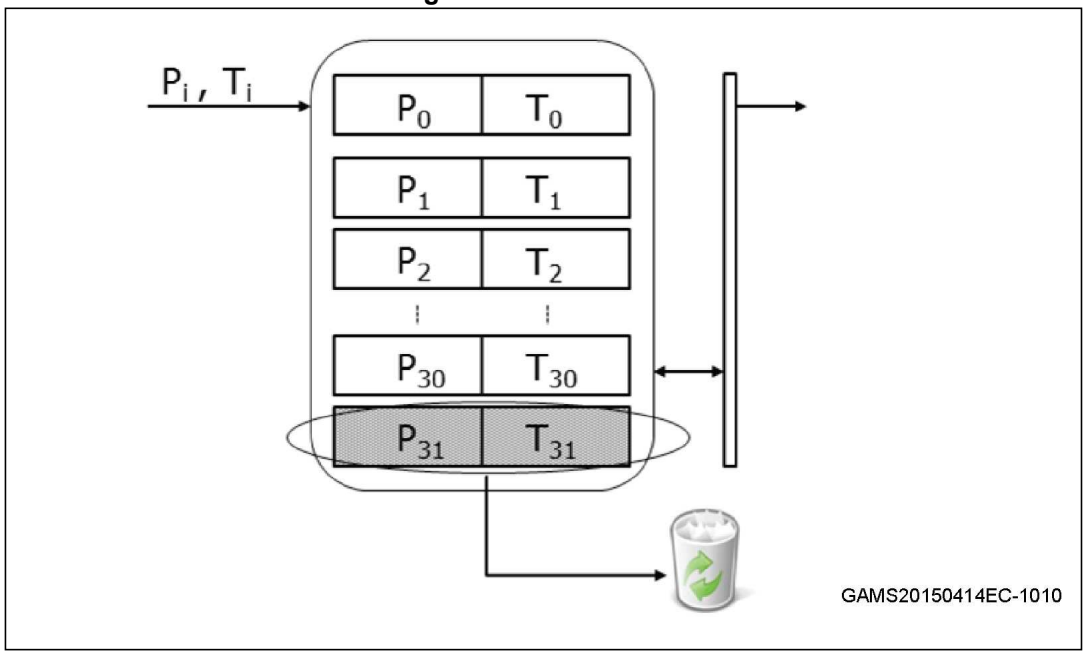
Figure 7. FIFO mode



4.3 Stream mode

In Stream mode (F_MODE[2:0] in *FIFO_CTRL (2Eh)* set to '010'), the data from *PRESS_OUT_H (2Ah)*, *PRESS_OUT_L (29h)*, and *PRESS_OUT_XL (28h)* are stored in the FIFO. The FIFO continues filling until it's full (32 slots of data for pressure output). When full, the FIFO discards the older data as the new arrive. An interrupt can be enabled and set as in FIFO mode.

Figure 8. Stream mode



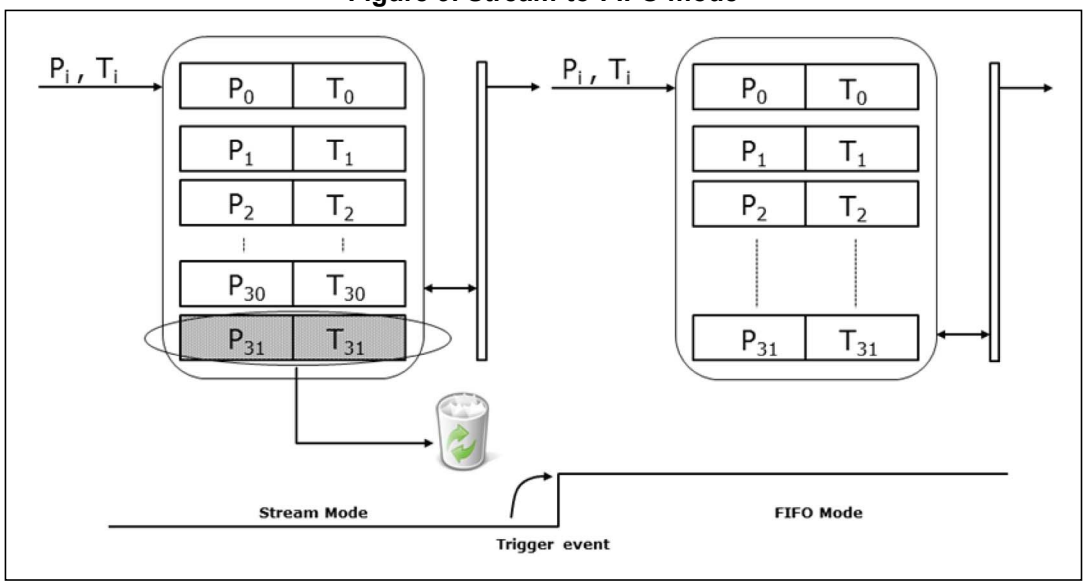
4.4 Stream-to-FIFO mode

In Stream-to-FIFO mode (F_MODE[2:0] in *FIFO_CTRL (2Eh)* set to '011'), the data from *PRESS_OUT_H (2Ah)*, *PRESS_OUT_L (29h)* PRESS_OUT_L (29h) and PRESS_OUT_XL (28h) are stored in the FIFO.

An interrupt can be enabled (STOP_ON_FTH bit set to '1' in *CTRL_REG2 (21h)*) in order to be raised when the FIFO is filled to the level specified by the WTM_POINT[4:0] bits of *FIFO_CTRL (2Eh)*.The FIFO continues filling until it's full (32 slots of data for pressure output). When full, the FIFO discards the older data as the new arrive. Once a trigger event occurs, the FIFO starts operating in FIFO mode. A trigger event can be configured in *INTERRUPT_CFG (24h)*.

The LIR bit in *INTERRUPT_CFG (24h)* should be set to '1' in order to have latched interrupt for triggering and reading the data in FIFO mode.

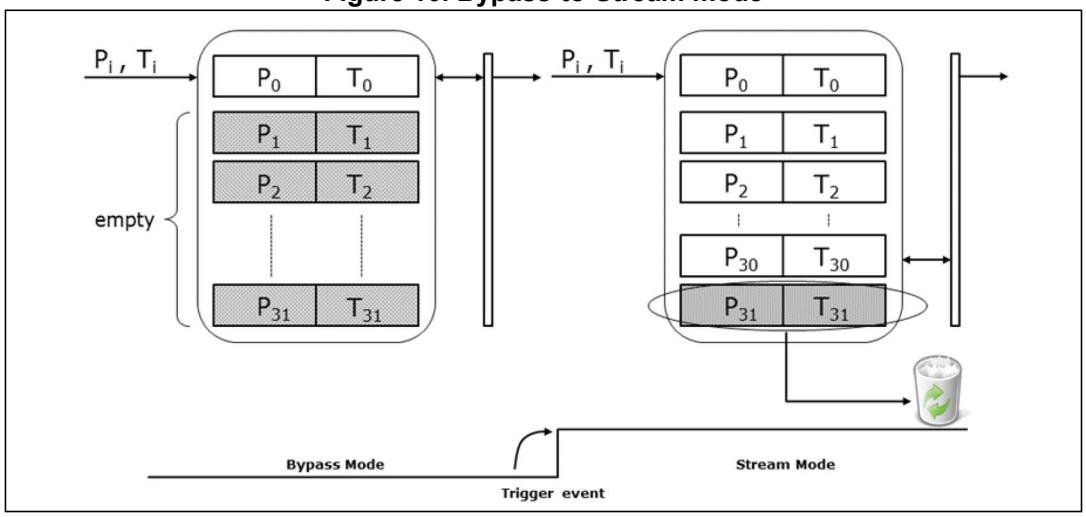
Figure 9. Stream-to-FIFO mode



4.5 Bypass-to-Stream mode

In Bypass-to-Stream mode (F_MODE[2:0] in *FIFO_CTRL (2Eh)* set to '100'), the FIFO is in Bypass mode until a trigger event occurs which is based on the IA bit in *INT_SOURCE (25h)* and the FIFO starts operating in Stream mode. A trigger event can be configured in *INTERRUPT_CFG (24h)*.

Figure 10. Bypass-to-Stream mode



4.6 FIFO Mean mode

In FIFO Mean mode (F_MODE[2:0] in *FIFO_CTRL (2Eh)* set to '110'), the pressure data are not directly sent to the output register but are first stored in the FIFO to calculate the average. In this mode the FIFO is used to implement a moving average of the pressure data with a 2, 4, 8, 16 or 32 sample set by changing the FIFO Mean mode sample size defined by the WTM_POINT[4:0] bits of *FIFO_CTRL (2Eh)* (refer to *Table 9*).

Table 9. Running average sample size

WTM_POINT[4:0]	FIFO Mean mode sample size
00001	2-sample moving average
00011	4-sample moving average
00111	8-sample moving average
01111	16-sample moving average
11111	32-sample moving average

There are two possible ways of providing the output pressure data averaged by FIFO:

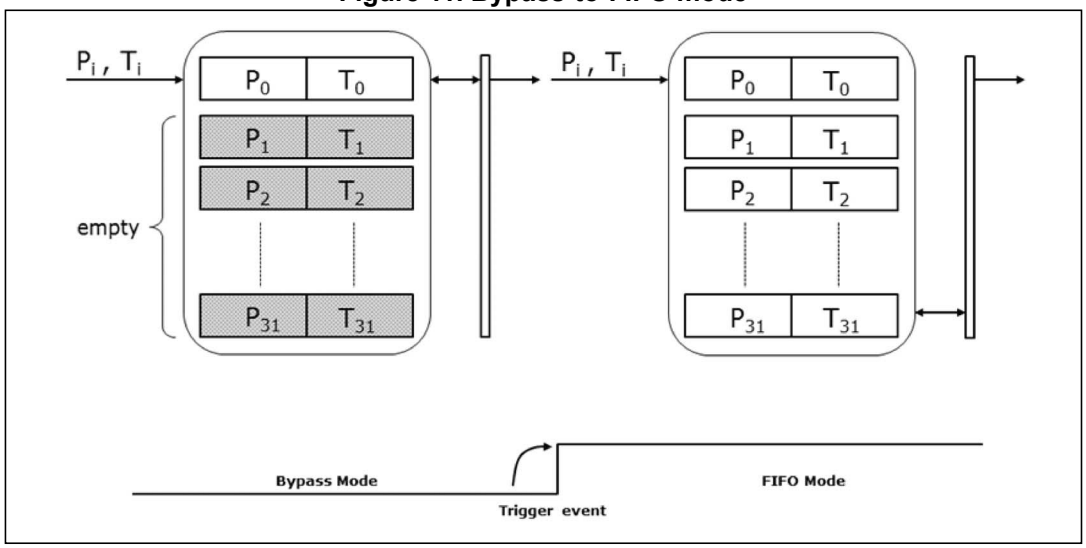
1. If the FIFO_MEAN_DEC bit in *CTRL_REG2 (21h)* is set to '0', the output is at the same ODR of the data coming from the sensor;
2. If the FIFO_MEAN_DEC bit in *CTRL_REG2 (21h)* is set to '1', the output is decimated (@1 Hz when ODR = 4 or 2; @1.04 Hz when ODR=3).

Please note that when using the FIFO Mean mode it is not possible to access the FIFO content.

4.7 Bypass-to-FIFO mode

In Bypass-to-FIFO (F_MODE[2:0] in *FIFO_CTRL (2Eh)* set to '111'), the FIFO is in Bypass mode until a trigger event occurs and the FIFO starts operating in FIFO mode. A trigger event is based on the IA bit in *INT_SOURCE (25h)* and it is configured by *INTERRUPT_CFG (24h)*.

Figure 11. Bypass-to-FIFO mode



4.8 Retrieving data from FIFO

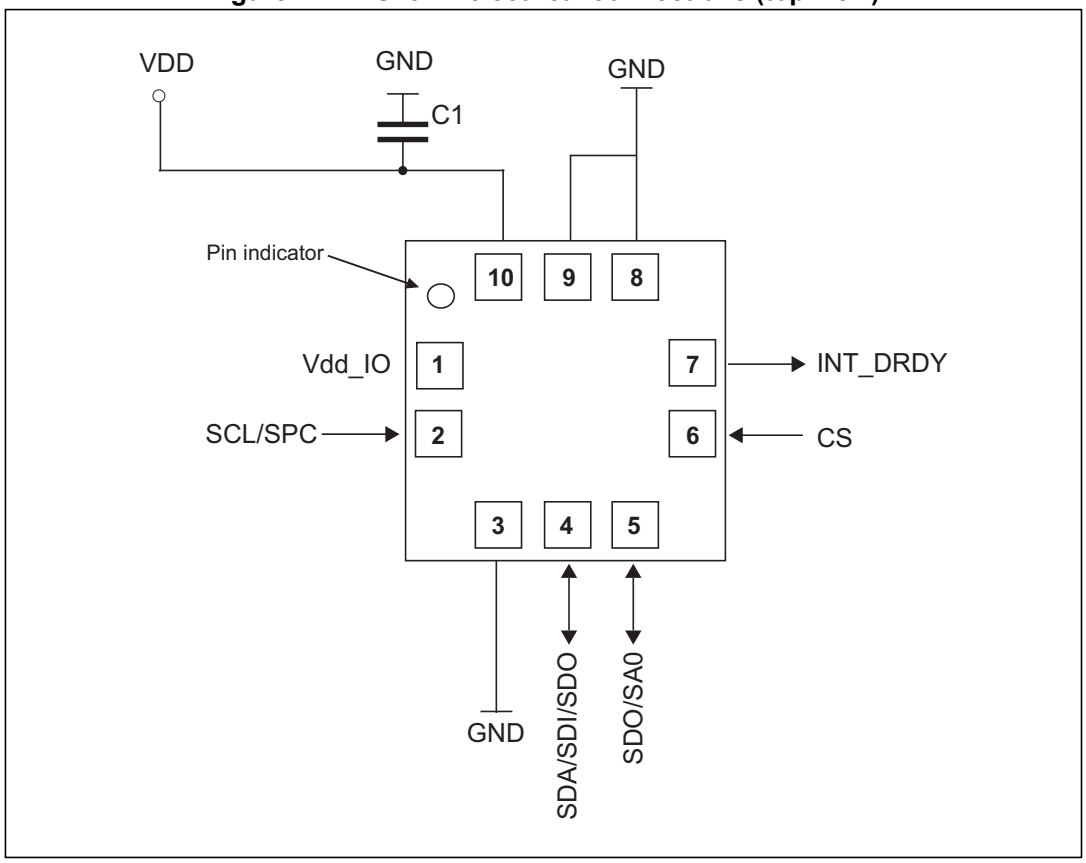
When the FIFO is enabled, FIFO data are read from *PRESS_OUT_H (2Ah)*, *PRESS_OUT_L (29h)*, and *PRESS_OUT_XL (28h)* registers.

Each time data is read from the FIFO, the oldest data are placed in the *PRESS_OUT_H (2Ah)*, *PRESS_OUT_L (29h)* and *PRESS_OUT_XL (28h)* registers and both single-read and read-burst operations can be used.

The reading address is automatically updated by the device and it rolls back to 28h when register 2Ah is reached. In order to read all FIFO levels in a multiple byte reading, 96 bytes (3 output registers by 32 levels) must be read.

5 Application hints

Figure 12. LPS25HB electrical connections (top view)



The device power supply must be provided through the VDD line; the power supply decoupling capacitor C1 (100 nF) must be placed as near as possible to the supply pads of the device. Depending on the application, an additional capacitor of 4.7 µF could be placed on VDD line.

The functionality of the device and the measured data outputs are selectable and accessible through the I²C/SPI interface. When using the I²C, CS must be tied to Vdd_IO.

All the voltage and ground supplies must be present at the same time to have proper behavior of the IC (refer to *Figure 12.*). It is possible to remove VDD while maintaining Vdd_IO without blocking the communication bus, in this condition the measurement chain is powered off.

5.1 Soldering information

The HLGA package is compliant with the ECOPACK® standard and it is qualified for soldering heat resistance according to JEDEC J-STD-020.

The HLGA package is compliant with the ECOPACK®, RoHS and "Green" standard. It is qualified for soldering heat resistance according to JEDEC J-STD-020. Leave "Pin 1 Indicator" unconnected during soldering.

Please refer the technical note TN1198, “Surface mount guidelines for MEMS sensors in HLGA packages” available on *www.st.com* for any additional information

Land pattern and soldering recommendations are available at *www.st.com/mems*.

6 Digital interfaces

6.1 I²C serial interface

The registers embedded in the LPS25HB may be accessed through both the I²C and SPI serial interfaces. The latter may be SW configured to operate either in 3-wire or 4-wire interface mode.

The serial interfaces are mapped onto the same pads. To select/exploit the I²C interface, the CS line must be tied high (i.e. connected to Vdd_IO); to select the SPI interface, the CS line must be tied low (i.e. connected to GND).

Table 10. Serial interface pin description

Pin name	Pin
CS	SPI enable I²C/SPI mode selection (1: I²C mode; 0: SPI enabled
SCL/SPC	I²C serial clock (SCL) SPI serial port clock (SPC)
SDA SDI SDI/SDO	I²C serial data (SDA) 4-wire SPI serial data input (SDI) 3-wire serial data input /output (SDI/SDO)
SDO SAO	SPI serial data output (SDO) I²C less significant bit of the device address (SA0)

6.2 I²C serial interface (CS = High)

The LPS25HB I²C is a bus slave. The I²C is employed to write data into registers whose content can also be read back.

The relevant I²C terminology is given in *Table 9*.

Table 11. I²C terminology

Term	Description
Transmitter	The device which sends data to the bus
Receiver	The device which receives data from the bus
Master	The device which initiates a transfer, generates clock signals and terminates a transfer
Slave	The device addressed by the master

There are two signals associated with the I²C bus: the serial clock line (SCL) and the serial data line (SDA). The latter is a bi-directional line used for sending and receiving the data to/from the interface. Both lines have to be connected to Vdd_IO through pull-up resistors.

The I²C interface is compliant with fast mode (400 kHz) I²C standards as well as with the normal mode.

6.2.1 I²C operation

The transaction on the bus is started through a START (ST) signal. A start condition is defined as a HIGH-to-LOW transition on the data line while the SCL line is held HIGH. After this has been transmitted by the master, the bus is considered busy. The next data byte transmitted after the start condition contains the address of the slave in the first 7 bits and the eighth bit tells whether the master is receiving data from the slave or transmitting data to the slave. When an address is sent, each device in the system compares the first seven bits after a start condition with its address. If they match, the device considers itself addressed by the master.

The slave address (SAD) associated to the LPS25HB is 101110xb. The **SDO**/**SA0** pad can be used to modify the less significant bit of the device address. If the SA0 pad is connected to the voltage supply, LSb is ‘1’ (address 1011101b), otherwise if the SA0 pad is connected to ground, the LSb value is ‘0’ (address 1011100b). This solution permits to connect and address two different LPS25HB devices to the same I²C lines.

Data transfer with acknowledge is mandatory. The transmitter must release the SDA line during the acknowledge pulse. The receiver must then pull the data line LOW so that it remains stable low during the HIGH period of the acknowledge clock pulse. A receiver which has been addressed is obliged to generate an acknowledge after each byte of data received.

The I²C embedded in the LPS25HB behaves like a slave device and the following protocol must be adhered to. After the start condition (ST) a slave address is sent, once a slave acknowledge (SAK) has been returned, an 8-bit sub-address (SUB) will be transmitted: the 7 LSB represents the actual register address while the MSB enables address auto increment. If the MSb of the SUB field is ‘1’, the SUB (register address) will be automatically increased to allow multiple data read/write.

The slave address is completed with a Read/Write bit. If the bit is ‘1’ (Read), a repeated START (SR) condition must be issued after the two sub-address bytes; if the bit is ‘0’ (Write) the master will transmit to the slave with direction unchanged. *Table 12* explains how the SAD+read/write bit pattern is composed, listing all the possible configurations.

Table 12. SAD+Read/Write patterns

Command	SAD[6:1]	SAD[0] = SA0	R/W	SAD+R/W
Read	101110	0	1	10111001 (B9h)
Write	101110	0	0	10111000 (B8h)
Read	101110	1	1	10111011 (BBh)
Write	101110	1	0	10111010 (BAh)

Table 13. Transfer when master is writing one byte to slave

Master	ST	SAD + W		SUB		DATA		SP
Slave			SAK		SAK		SAK	