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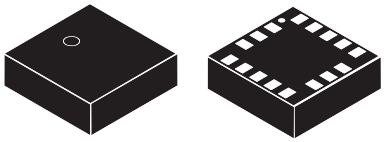
LPS331AP

MEMS pressure sensor: 260-1260 mbar absolute digital output barometer

Datasheet – production data

Features

- 260 to 1260 mbar absolute pressure range
- High-resolution mode: 0.020 mbar RMS
- Low power consumption:
  - Low resolution mode: 5.5 µA
  - High resolution mode: 30 µA
- High overpressure capability: 20x full scale
- Embedded temperature compensation
- Embedded 24-bit ADC
- Selectable ODR from 1 Hz to 25 Hz
- SPI and I^2C interfaces
- Supply voltage: 1.71 to 3.6 V
- High shock survivability: 10,000 *g*
- Small and thin package
- ECOPACK® lead-free compliant



HCLGA-16L
(3 x 3 x 1 mm)

Applications

- Indoor and outdoor navigation
- Enhanced GPS for dead-reckoning
- Altimeter and barometer for portable devices
- Weather station equipment
- Sport watches

Description

The LPS331AP is an ultra compact absolute piezoresistive pressure sensor. It includes a monolithic sensing element and an IC interface able to take the information from the sensing element and to provide a digital signal to the external world.

The sensing element consists of a suspended membrane realized inside a single mono-silicon substrate. It is capable to detecting pressure and is manufactured using a dedicated process developed by ST, called *VENSENS*.

The *VENSENS* process allows to build a mono-silicon membrane above an air cavity with controlled gap and defined pressure. The membrane is very small compared to the traditionally built silicon micromachined membranes. Membrane breakage is prevented by an intrinsic mechanical stopper.

The IC interface is manufactured using a standard CMOS process that allows a high level of integration to design a dedicated circuit which is trimmed to better match the sensing element characteristics.

The LPS331AP is available in a small holed cap land grid array (HCLGA) package and it is guaranteed to operate over a temperature range extending from -40 °C to +85 °C. The package is holed to allow external pressure to reach the sensing element.

Table 1. Device summary

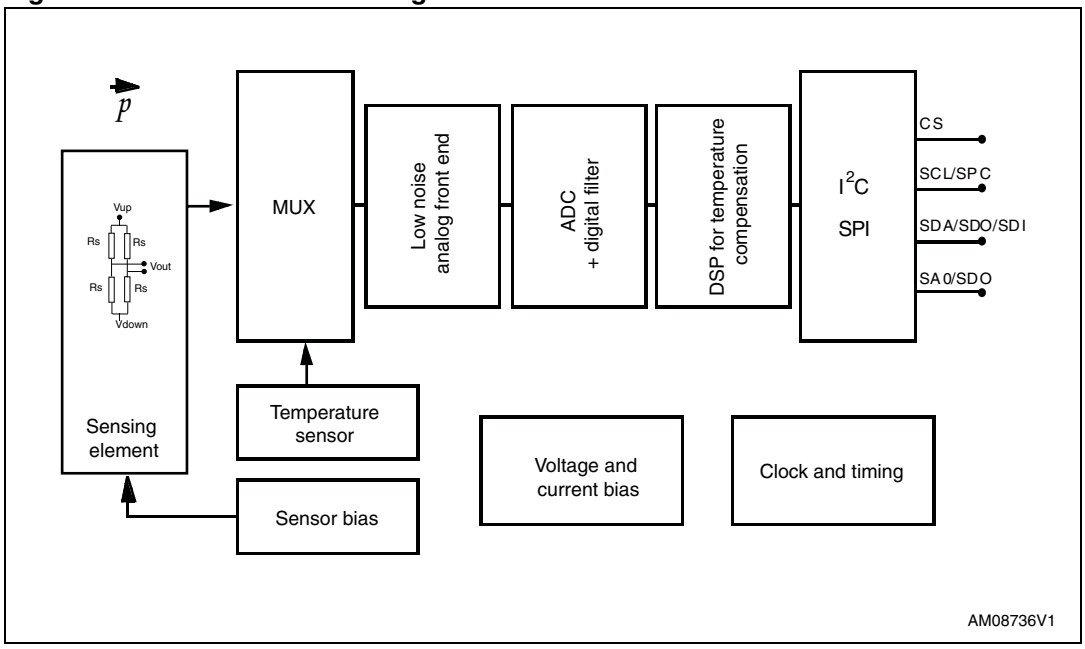
Order codes	Temperature range [°C]	Package	Packing
LPS331APY	-40 to +85	HCLGA-16L	Tray
LPS331APTR			Tape and reel

Contents

1 Block diagram and pin description

1.1 LPS331AP block diagram

Figure 1. LPS331AP block diagram



1.2 Pin description

Figure 2. Pin connection

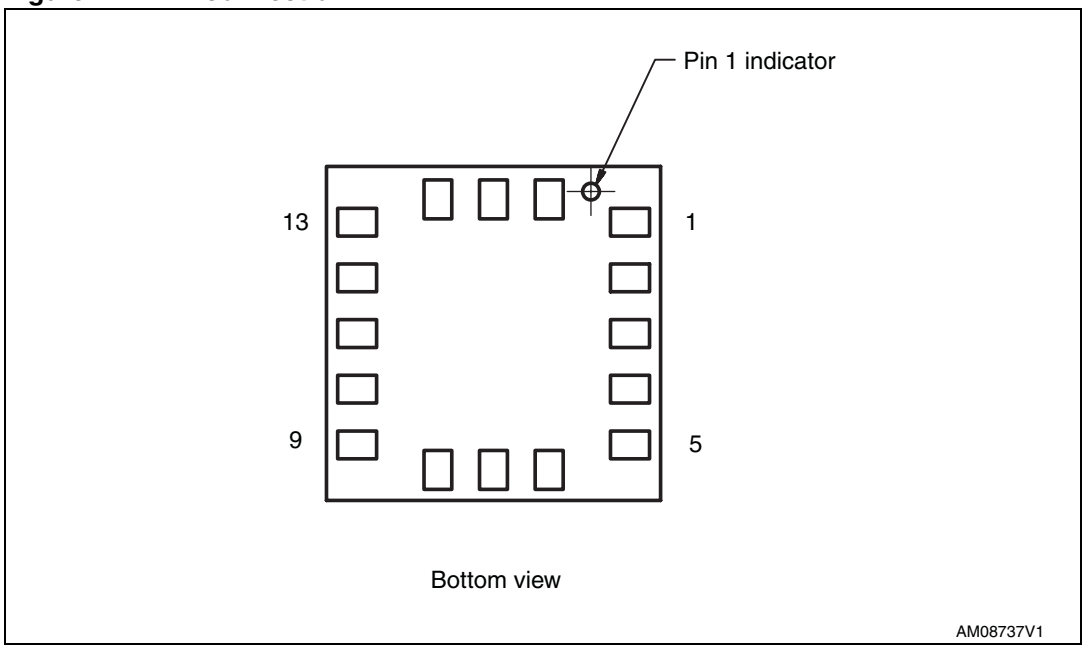


Table 2. Pin description

Pin#	Name	Function
1	Vdd_IO	Power supply for I/O pins
2	NC	Not connected
3	NC	Not connected
4	SCL SPC	I^2C serial clock (SCL) SPI serial port clock (SPC)
5	GND	0 V supply
6	SDA SDI SDO	I^2C serial data (SDA) SPI serial data input (SDI) 3-wire interface serial data output (SDO)
7	SDO SA0	SPI serial data output (SDO) I^2C less significant bit of the device address (SA0)
8	CS	SPI enable I^2C/SPI mode selection (1: I^2C mode; 0: SPI enabled)
9	INT2	Interrupt 2 (or data ready)
10	Reserved	Connect to GND
11	INT1	Interrupt 1 (or data ready)
12	GND	0 V supply
13	GND	0 V supply
14	VDD	Power supply
15	VCCA	Analog power supply
16	GND	0 V supply

2 Mechanical and electrical specifications

Conditions at V_{DD} = 2.5 V, T = 25 °C, unless otherwise noted.

2.1 Mechanical characteristics

Table 3. Mechanical characteristics

Symbol	Parameter	Test condition	Min.	Typ.(1)	Max.	Unit
Top	Operating temperature range		-40	–	85	°C
Tfull	Full accuracy temperature range		0	–	80	°C
Pop	Operating pressure range		260	–	1260	mbar
Pbits	Pressure output data		–	24	–	bits
Pres	Pressure sensitivity		–	4096	–	LSB/ mbar
Paccrel	Relative accuracy over pressure(2)	P = 800 to 1100 mbar T= 25°C	–	±0.1	±0.2	mbar
PaccT	Absolute accuracy pressure over temperature(3)	P = 800 to 1100 mbar T = 0 ~+80 °C	- 3.2	±2	2.6	mbar
Pnoise	Pressure noise		See *Table 17.*			mbar RMS
Tbits	Temperature output data		–	16	–	bits
Tres	Temperature sensitivity		–	480	–	LSB/°C
Tacc	Absolute accuracy temperature	T= 0~+80 °C	–	±2	–	°C

1. Typical specifications are not guaranteed.
2. Characterization data. Parameter not tested at final test
3. Embedded pwl compensation.

2.2 Electrical characteristics

Table 4. Electrical characteristics

Symbol	Parameter	Test condition	Min.	Typ.(1)	Max.	Unit
Vdd	Supply voltage		1.71	–	3.6	V
Vdd_IO	IO supply voltage		1.71	–	3.6	V
Idd	Supply current @ ODRp 1 Hz and ODRt = 1Hz		see *Table 5*			µA
IddPdn	Supply current in power-down mode T = 25 °C		–	0.5	–	µA

1. Typical specifications are not guaranteed.

Table 5. Supply current at ODRp 1 Hz, ODRt 1 Hz

Symbol	RES_CONF (hex)	Min.	Typ.	Max.	Unit
Idd	73	–	5.5	–	µA
	75	–	6.6	–	
	77	–	11.5	–	
	78	–	17.5	–	
	7A	–	30.0	–	

2.3 Absolute maximum ratings

Stress above those listed as “Absolute maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 6. Absolute maximum ratings

Symbol	Ratings	Maximum value	Unit
Vdd	Supply voltage	-0.3 to 4.8	V
Vdd_IO	I/O pins supply voltage	-0.3 to 4.8	V
Vin	Input voltage on any control pin	-0.3 to Vdd_IO +0.3	V
P	Overpressure	20	bar
T_{STG}	Storage temperature range	-40 to +125	°C
ESD	Electrostatic discharge protection	2 (HBM)	kV

Note: Supply voltage on any pin should never exceed 4.8 V.

This is a mechanical shock sensitive device, improper handling can cause permanent damage to the part.

This is an ESD sensitive device, improper handling can cause permanent damage to the part.

3 Functionality

The LPS331AP is a high resolution, digital output pressure sensor packaged in an HCLGA holed package. The complete device includes a sensing element based on a piezoresistive Wheatstone bridge approach, and an IC interface able to take the information from the sensing element to the external world, as a digital signal.

3.1 Sensing element

An ST proprietary process is used to obtain a mono-silicon µ-sized membrane for MEMS pressure sensors, without requiring substrate to substrate bonding. When pressure is applied, the membrane deflection induces an imbalance in the Wheatstone bridge piezoresistances, whose output signal is converted by the IC interface.

Intrinsic mechanical stoppers prevent breakage in case of pressure overstress, ensuring measurement repeatability.

The pressure inside the buried cavity under the membrane is constant and controlled by process parameters.

3.2 IC interface

The complete measurement chain consists of a low-noise capacitive amplifier, which converts the resistive unbalance of the MEMS sensor into an analog voltage signal, and of an analog-to-digital converter, which translates the produced signal into a digital bitstream.

The converter is coupled with a dedicated reconstruction filter which removes the high frequency components of the quantization noise and provides low rate and high resolution digital words.

The pressure data can be accessed through an I^2C/SPI interface making the device particularly suitable for direct interfacing with a microcontroller.

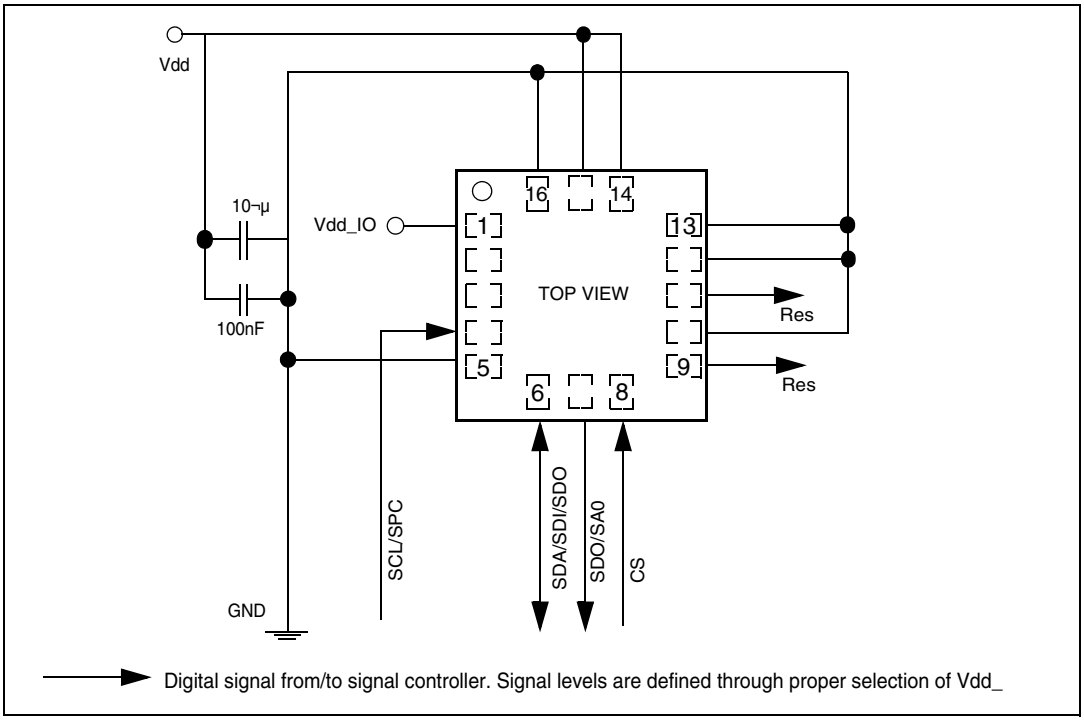
3.3 Factory calibration

The IC interface is factory calibrated at three temperatures and two pressures for sensitivity and accuracy.

The trimming values are stored inside the device by a non-volatile structure. Whenever the device is turned on, the trimming parameters are downloaded into the registers to be employed during normal operation. This allows the user to employ the device without requiring any further calibration.

4 Application hints

Figure 3. LPS331AP electrical connection



The device core is supplied through the Vdd line. Power supply decoupling capacitors (100 nF ceramic, 10 µF aluminum) should be placed as near as possible to the supply pad of the device (common design practice).

The functionality of the device and the measured data outputs are selectable and accessible through the I²C/SPI interface. When using the I²C, CS must be tied high (i.e. connected to Vdd_IO).

4.1 Soldering information

The HCLGA package is compliant with the ECOPACK® standard and it is qualified for soldering heat resistance according to JEDEC J-STD-020.

5 Digital interfaces

5.1 I²C serial interface

The registers embedded in the LPS331AP may be accessed through both the I²C and SPI serial interfaces. The latter may be SW configured to operate either in 3-wire or 4-wire interface mode.

The serial interfaces are mapped onto the same pads. To select/exploit the I²C interface, CS line must be tied high (i.e. connected to Vdd_IO).

Table 7. Serial interface pin description

Pin name	Pin description
CS	SPI enable I²C/SPI mode selection (1: I²C mode; 0: SPI enabled)
SCL/ SPC	I²C serial clock (SCL) SPI serial port clock (SPC)
SDA/ SDI/ SDO	I²C serial data (SDA) SPI serial data input (SDI) 3-wire interface serial data output (SDO)
SA0/ SDO	I²C less significant bit of the device address (SA0) SPI serial data output (SDO)

5.2 I²C serial interface

The LPS331AP I²C is a bus slave. The I²C is employed to write data into registers whose content can also be read back.

The relevant I²C terminology is given in *Table 8.*

Table 8. Serial interface pin description

Term	Description
Transmitter	The device which sends data to the bus
Receiver	The device which receives data from the bus
Master	The device which initiates a transfer, generates clock signals and terminates a transfer
Slave	The device addressed by the master

There are two signals associated with the I²C bus: the serial clock line (SCL) and the serial data line (SDA). The latter is a bi-directional line used for sending and receiving the data to/from the interface. Both lines have to be connected to Vdd_IO through pull-up resistors.

The I²C interface is compliant with fast mode (400 kHz) I²C standards as well as with the normal mode.

5.2.1 I²C operation

The transaction on the bus is started through a START (ST) signal. A start condition is defined as a HIGH to LOW transition on the data line while the SCL line is held HIGH. After this has been transmitted by the master, the bus is considered busy. The next byte of data transmitted after the start condition contains the address of the slave in the first 7 bits and the eighth bit tells whether the master is receiving data from the slave or transmitting data to the slave. When an address is sent, each device in the system compares the first seven bits after a start condition with its address. If they match, the device considers itself addressed by the master.

The slave address (SAD) associated to the LPS331AP is 101110xb. The **SDO**/**SA0** pad can be used to modify the less significant bit of the device address. If the SA0 pad is connected to voltage supply, LSb is '1' (address 1011101b), otherwise if the SA0 pad is connected to ground, the LSb value is '0' (address 1011100b). This solution permits to connect and address two different LPS331APs to the same I²C lines.

Data transfer with acknowledge is mandatory. The transmitter must release the SDA line during the acknowledge pulse. The receiver must then pull the data line LOW so that it remains stable low during the HIGH period of the acknowledge clock pulse. A receiver which has been addressed is obliged to generate an acknowledge after each byte of data received.

The I²C embedded in the LPS331AP behaves like a slave device and the following protocol must be adhered to. After the start condition (ST) a slave address is sent, once a slave acknowledge (SAK) has been returned, a 8-bit sub-address (SUB) will be transmitted: the 7 LSB represents the actual register address while the MSB enables address auto increment. If the MSb of the SUB field is '1', the SUB (register address) will be automatically increased to allow multiple data read/write.

The slave address is completed with a Read/Write bit. If the bit was '1' (Read), a repeated START (SR) condition must be issued after the two sub-address bytes; if the bit is '0' (Write) the master will transmit to the slave with direction unchanged. *Table 9* explains how the SAD+read/write bit pattern is composed, listing all the possible configurations.

Table 9. SAD+Read/Write patterns

Command	SAD[6:1]	SAD[0] = SA0	R/W	SAD+R/W
Read	101110	0	1	10111001 (B9h)
Write	101110	0	0	10111000 (B8h)
Read	101110	1	1	10111011 (BBh)
Write	101110	1	0	10111010 (BAh)

Table 10. Transfer when master is writing one byte to slave

Master	ST	SAD + W		SUB		DATA		SP
Slave			SAK		SAK		SAK	

Table 11. Transfer when master is writing multiple bytes to slave

Master	ST	SAD + W		SUB		DATA		DATA		SP
Slave			SAK		SAK		SAK		SAK	

Table 12. Transfer when master is receiving (reading) one byte of data from slave

Master	ST	SAD + W		SUB		SR	SAD + R			NMAK	SP
Slave			SAK		SAK			SAK	DATA		

Table 13. Transfer when master is receiving (reading) multiple bytes of data from slave

Master	ST	SAD+W		SUB		SR	SAD+R			MAK		MAK		NMAK	SP
Slave			SAK		SAK			SAK	DATA		DATA		DATA		

Data are transmitted in byte format (DATA). Each data transfer contains 8 bits. The number of bytes transferred per transfer is unlimited. Data is transferred with the most significant bit (MSb) first. If a receiver can't receive another complete byte of data until it has performed some other functions, it can hold the clock line, SCL LOW to force the transmitter into a wait state. Data transfer only continues when the receiver is ready for another byte and releases the data line. If a slave receiver does not acknowledge the slave address (i.e. it is not able to receive because it is performing some real time function) the data line must be kept HIGH by the slave. The master can then abort the transfer. A LOW to HIGH transition on the SDA line while the SCL line is HIGH is defined as a STOP condition. Each data transfer must be terminated by the generation of a STOP (SP) condition.

In order to read multiple bytes incrementing the register address, it is necessary to assert the most significant bit of the sub-address field. In other words, SUB(7) must be equal to 1 while SUB(6-0) represents the address of the first register to be read.

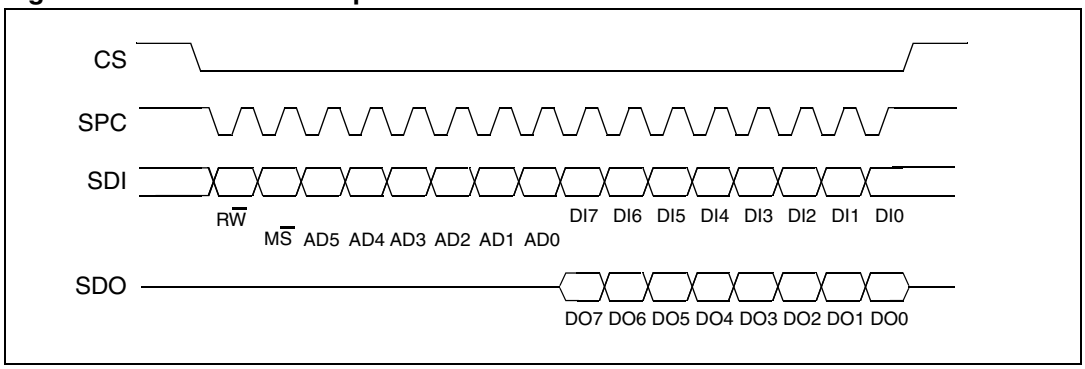
In the presented communication format MAK is Master acknowledge and NMAK is no master acknowledge.

5.3 SPI bus interface

The LPS331AP SPI is a bus slave. The SPI allows to write and read the registers of the device.

The serial interface interacts with the outside world with 4 wires: **CS**, **SPC**, **SDI** and **SDO**.

Figure 4. Read and write protocol



CS is the serial port enable and it is controlled by the SPI master. It goes low at the start of the transmission and returns to high at the end. **SPC** is the serial port clock and it is controlled by the SPI master. It is stopped high when **CS** is high (no transmission). **SDI** and

SDO are respectively the serial port data input and output. Those lines are driven at the falling edge of **SPC** and should be captured at the rising edge of **SPC**.

Both the read register and write register commands are completed in 16 clock pulses or in multiples of 8 in the case of multiple bytes read/write. Bit duration is the time between two falling edges of **SPC**. The first bit (bit 0) starts at the first falling edge of **SPC** after the falling edge of **CS** while the last bit (bit 15, bit 23, ...) starts at the last falling edge of SPC just before the rising edge of **CS**.

bit 0: R$\overline{W}$ bit. When 0, the data DI(7:0) is written into the device. When 1, the data DO(7:0) from the device is read. In the latter case, the chip will drive **SDO** at the start of bit 8.

bit 1: M$\overline{S}$ bit. When 0, the address will remain unchanged in multiple read/write commands. When 1, the address will be auto incremented in multiple read/write commands.

bit 2-7: address AD(5:0). This is the address field of the indexed register.

bit 8-15: data DI(7:0) (write mode). This is the data that is written into the device (MSb first).

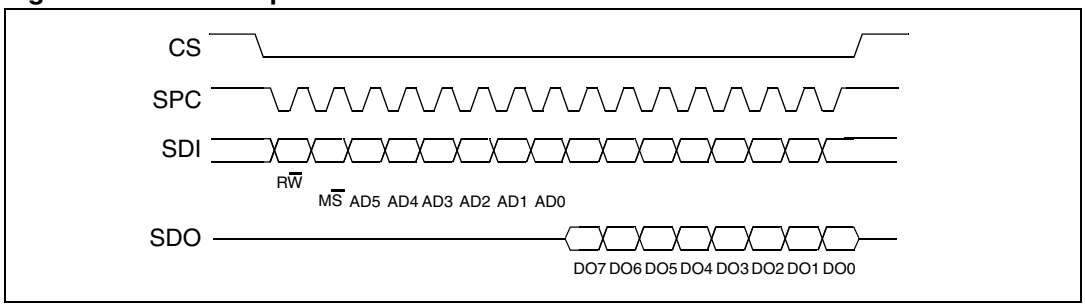
bit 8-15: data DO(7:0) (read mode). This is the data that is read from the device (MSb first).

In multiple read/write commands further blocks of 8 clock periods are added. When the M$\overline{S}$ bit is 0 the address used to read/write data remains the same for every block. When M$\overline{S}$ bit is 1 the address used to read/write data is increased at every block.

The function and the behavior of **SDI** and **SDO** remain unchanged.

5.3.1 SPI read

Figure 5. SPI read protocol



The SPI Read command is performed with 16 clock pulses. The multiple byte read command is performed adding blocks of 8 clock pulses at the previous one.

bit 0: READ bit. The value is 1.

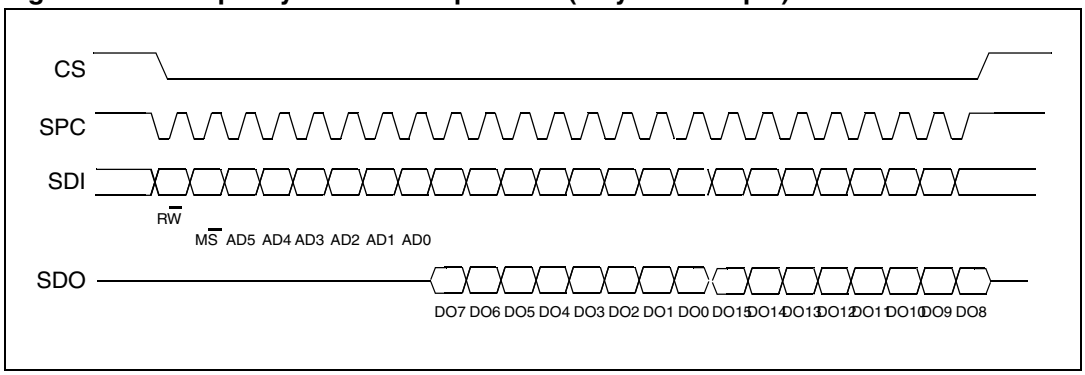
bit 1: M$\overline{S}$ bit. When 0 do not increment address, when 1 increment address in multiple reading.

bit 2-7: address AD(5:0). This is the address field of the indexed register.

bit 8-15: data DO(7:0) (read mode). This is the data that is read from the device (MSb first).

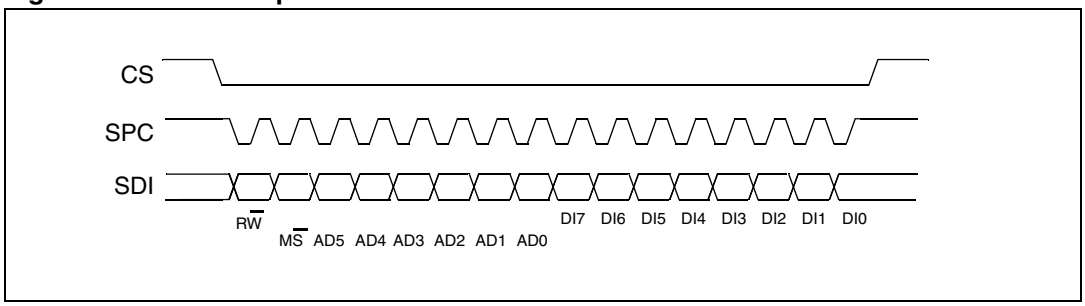
bit 16-... : data DO(...-8). Further data in multiple byte readings.

Figure 6. Multiple bytes SPI read protocol (2 bytes example)



5.3.2 SPI write

Figure 7. SPI write protocol



The SPI Write command is performed with 16 clock pulses. The multiple byte write command is performed adding blocks of 8 clock pulses at the previous one.

bit 0: WRITE bit. The value is 0.

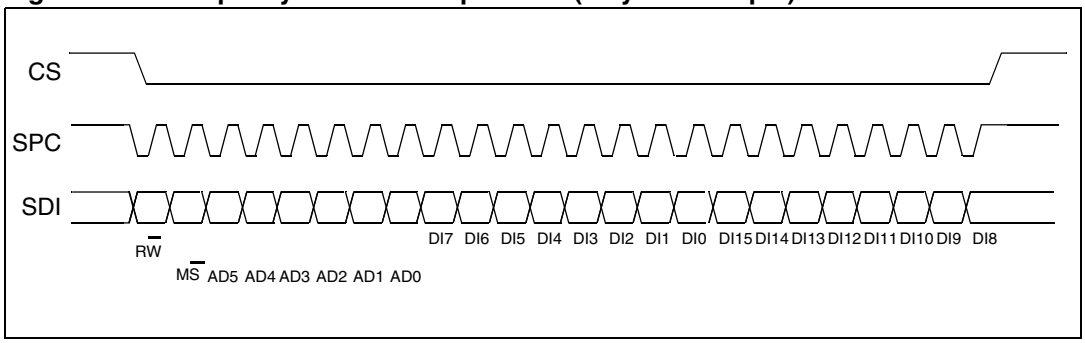
bit 1: MS bit. When 0 do not increment the address, when 1 increment the address in multiple writings.

bit 2 -7: address AD(5:0). This is the address field of the indexed register.

bit 8-15: data DI(7:0) (write mode). This is the data that is written in the device (MSb first).

bit 16-... : data DI(...-8). Further data in multiple byte writings.

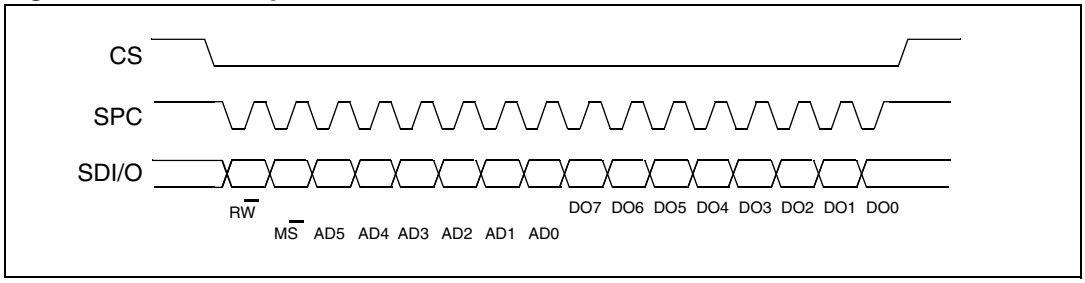
Figure 8. Multiple bytes SPI write protocol (2 bytes example)



5.3.3 SPI read in 3-wires mode

A 3-wires mode is entered by setting to '1' bit SIM (SPI serial interface mode selection) in CTRL_REG4.

Figure 9. SPI read protocol in 3-wires mode



The SPI read command is performed with 16 clock pulses:

bit 0: READ bit. The value is 1.

bit 1: M$\overline{S}$ bit. When 0, do not increment the address, when 1, increment the address in multiple readings.

bit 2-7: address AD(5:0). This is the address field of the indexed register.

bit 8-15: data DO(7:0) (read mode). This is the data that is read from the device (MSb first).

Multiple read command is also available in 3-wires mode.

6 Register mapping

Table 14 provides a list of the 8-bit registers embedded in the device and the related addresses.

Table 14. Registers address map

Name	Type	Register Address		Default	Function and comment
		Hex	Binary		
Reserved (Do not modify)		00-07 0D - 0E			Reserved
REF_P_XL	R/W	08	0001000	00000000	
REF_P_L	R/W	09	0001001	00000000	
REF_P_H	R/W	0A	0001010	00000000	
WHO_AM_I	R	0F	0001111	10111011	Dummy register
RES_CONF	R/W	10	0010000	011111010	
Reserved (Do not modify)		11-1F			Reserved
CTRL_REG1	R/W	20	010 0000	00000000	
CTRL_REG2	R/W	21	010 0001	00000000	
CTRL_REG3	R/W	22	010 0010	00000000	
INT_CFG_REG	R/W	23	0100011	00000000	
INT_SOURCE_REG	R	24	0100100	00000000	
THS_P_LOW_REG	R/W	25	0100101	0000000	
THS_P_HIGH_REG	R/W	26	0100110	0000000	
STATUS_REG	R	27	010 0111	00000000	
PRESS_POUT_XL_REH	R	28	010 1000	output	
PRESS_OUT_L	R	29	010 1001	output	
PRESS_OUT_H	R	2A	010 1010	output	
TEMP_OUT_L	R	2B	010 1011	output	
TEMP_OUT_H	R	2C	010 1100	output	
Reserved (Do not modify)		2D-2F			Reserved
AMP_CTRL	R/W	30	011 0000		Partially reserved

Registers marked as *Reserved* must not be changed. The writing to those registers may cause permanent damages to the device.

The content of the registers that are loaded at boot should not be changed. They contain the factory calibration values. Their content is automatically restored when the device is powered-up.

7 Register description

The device contains a set of registers which are used to control its behavior and to retrieve pressure and temperature data. The register address, made up of 7 bits, is used to identify them and to read/write the data through the serial interface.

REF_P_XL Reference pressure (LSB data)

7	6	5	4	3	2	1	0
REFL7	REFL6	REFL5	REFL4	REFL3	REFL2	REFL1	REFL0

Address: 08h

Type: R/W

Reset: 00h

Description: This reference pressure register contains the lower part of the reference pressure that is sum to the sensor output pressure. The full value is REF_P_XL & REF_P_H & REF_P_L and is represented as 2's complement.

[7:0] REFL7 - REFL0: Reference pressure LSB data. Default value: 00h

REF_P_L Reference pressure (middle part)

16	15	14	13	12	11	10	9
REFL15	REFL14	REFL13	REFL12	REFL11	REFL10	REFL9	REFL8

Address: 09h

Type: R/W

Reset: 00h

Description: This register contains the middle part of the reference pressure that is sum to the sensor output pressure.
The full value is REF_P_XL & REF_P_H & REF_P_L and is represented as 2's complement.

[16:9] REFL15 - REFL8: Default value: 00h

REF_P_H Reference pressure (MSB data)

24	23	22	21	20	19	18	17
REFL23	REFL22	REFL21	REFL20	REFL19	REFL18	REFL17	REFL16

Address: 0Ah

Type: R/W

Reset: 00h

Description: This register contains the higher part of the reference pressure that is sum to the sensor output pressure.
The full value is REF_P_XL & REF_P_H & REF_P_L and is represented as 2's complement.

[24:17] REFL23 - REFL16: Reference pressure MSB data. Default value: 00h.

RES_CONF(10h) Pressure resolution mode

7	6	5	4	3	2	1	0
RFU	AVGT2	AVGT1	AVGT0	AVGP3	AVGP2	AVGP1	AVGP0

Address: 10h

Type: R/W

Reset: 7Ah

Description: AVGP3-AVGP0 allow to select the pressure internal average. AVGT2-AVGT0 allow to select the temperature internal average.
AVGP3-AVGP0 bits can be configured as described in *Table 15*.
AVGT2-AVGT0 bits can be configured as described in *Table 16*.

Table 15. Pressure resolution configuration

AVGP3	AVGP2	AVGP1	AVGP0	Nr. internal average
0	0	0	0	1
0	0	0	1	2
0	0	1	0	4
0	0	1	1	8
0	1	0	0	16
0	1	0	1	32
0	1	1	0	64
0	1	1	1	128
1	0	0	0	256

Table 15. Pressure resolution configuration

AVGP3	AVGP2	AVGP1	AVGP0	Nr. internal average
1	0	0	1	384
1	0	1	0	512(1)

1. Register configuration 7Ah not allowed with ODR = 25Hz/25Hz (Register CTRL_REG1). For ORD 25Hz/25Hz the suggested configuration for RES_CONF is 6Ah.

Table 16. Temperature resolution configuration

AVGT2	AVGT1	AVGT1	Nr. internal average
0	0	0	1
0	0	1	2
0	1	0	4
0	1	1	8
1	0	0	16
1	0	1	32
1	1	0	64
1	1	1	128(1)

1. Register configuration 7Ah not allowed with ODR = 25Hz/25Hz (Register CTRL_REG1). For ORD 25Hz/25Hz the suggested configuration for RES_CONF is 6Ah.

Table 17. Pressure resolution

RES_CONF (hex)	RMS noise(1)	Unit
70	0.450	mbar
71	0.320	
72	0.230	
73	0.160	
74	0.110	
75	0.080	
76	0.060	
77	0.040	
78	0.030	
79	0.025	
7A(2)	0.020	

1. Rms noise is calculated as standard deviation of 10 data points.
2. This configuration is not allowed for ODR = 25Hz/25HZ (register CTRL_REG1). For ORD = 25 Hz/ 25 Hz the suggested configuration for RES_CONF is 6Ah.

WHO_AM_I Device identification

7	6	5	4	3	2	1	0
1	0	1	1	1	0	1	1

Address: 0Fh

Type: R

Description: This read-only register contains the device identifier that, for LPS331AP, is set to BBh.

CTRL_REG1 Control register 1

7	6	5	4	3	2	1	0
PD	ODR2	ODR1	ODR0	DIFF_EN	DBDU	DELTA_EN	SIM

Address: 20h

Type: R/W

Description: Control register.

[7] PD: power down control.
Default value: 0
(0: power-down mode; 1: active mode)

[6:4] ODR2, ODR1, ODR0: output data rate selection.
Default value: 00
(see *Table 18*)

[3] DIFF_EN: Interrupt circuit enable.
Default value: 0
(0: interrupt generation disabled; 1: interrupt circuit enabled)

[2] BDU: block data update.
Default value: 0
(0: continuous update; 1: output registers not updated until MSB and LSB reading)

[1] DELTA_EN: delta pressure enable
(1: delta pressure registers enabled. 0: disable)

[0] SIM: SPI Serial Interface Mode selection.
Default value: 0
(0: 4-wire interface; 1: 3-wire interface)

PD bit allows to turn on the device. The device is in power-down mode when PD = ‘0’ (default value after boot). The device is active when PD is set to ‘1’.

ODR2- ODR1 - ODR0 bits allow to change the output data rates of pressure and temperature samples. The default value is “000” which corresponds to “one shot configuration” for both pressure and temperature output. ODR2, ODR1 and ODR0 bits can be configured as described in *Table 18*.

Note: Before changing the ODR it is necessary to power down the device (CTRL_REG1[7]).

Table 18. Output data rate bit configurations

ODR2	ODR1	ODR0	Pressure output data rate	Temperature output data rate
0	0	0	One shot	One shot
0	0	1	1 Hz	1 Hz
0	1	0	7 Hz	1 Hz
0	1	1	12.5 Hz	1 Hz
1	0	0	25 Hz	1 Hz
1	0	1	7 Hz	7 Hz
1	1	0	12.5 Hz	12.5 Hz
1	1	1	25 Hz	25 Hz

DIFF_EN bit is used to enable the circuitry for the computing of differential pressure output. In default mode (DIF_EN='0') the circuitry is turned off. It is suggested to turn on the circuitry only after the configuration of REF_P_x and THS_P_x.

BDU bit is used to inhibit the output registers update between the reading of upper and lower register parts. In default mode (BDU = '0'), the lower and upper register parts are updated continuously. If it is not sure to read faster than output data rate, it is recommended to set BDU bit to '1'. In this way, after the reading of the lower (upper) register part, the content of that output registers is not updated until the upper (lower) part is read too. This feature avoids reading LSB and MSB related to different samples.

SIM bit selects the SPI serial interface mode. When SIM is '0' (default value) the 4-wire interface mode is selected and data coming from the device are sent to pin #7 (SDO). In 3-wire interface mode, output data are sent to pin #6 (SDI/SDO).

CTRL_REG2 Control register 2

7	6	5	4	3	2	1	0
BOOT	RESERVED				SWRESET	AUTO_ZERO	ONE_SHOT

Address: 21h

Type: R/W

Description: Control register.

[7] BOOT: Reboot memory content. Default value: 0
(0: normal mode; 1: reboot memory content)

[6:3] RESERVED

[2] Software reset. Default value: 0
(0: normal mode; 1: software reset)

[1] Autozero enable. Default value: 0
(0: normal mode; 1: autozero enable)

[0] One shot enable. Default value: 0
(0: waiting for start of conversion; 1: start for a new dataset)

BOOT bit is used to refresh the content of the internal registers stored in the Flash memory block. At the device power-up the content of the Flash memory block is transferred to the internal registers related to trimming functions to permit a good behavior of the device itself. If for any reason, the content of the trimming registers is modified, it is sufficient to use this bit to restore the correct values. When BOOT bit is set to '1' the content of the internal Flash is copied inside the corresponding internal registers and is used to calibrate the device. These values are factory trimmed and they are different for every device. They permit good behavior of the device and normally they should not be changed. At the end of the boot process the BOOT bit is set again to '0'.

BOOT bit takes effect after one ODR clock cycle.

SWRESET is the software reset bit. The device is reset to the power on configuration if the SWRESET bit is set to '1' and BOOT is set to '1'.

AUTO_ZERO, when set to '1', the actual pressure output is copied in the REF_P_H & REF_P_L & REF_P_XL and kept as reference and the PRESS_OUT_H & PRESS_OUT_L & PRESS _OUT_XL is the difference between this reference and the pressure sensor value.

ONE_SHOT bit is used to start a new conversion when ODR1-ODR0 bits in CTRL_REG1 are set to "000". In this situation a single acquisition of temperature and pressure is started when ONE_SHOT bit is set to '1'. At the end of conversion the new data are available in the output registers, the STAUS_REG[0] and STAUS_REG[1] bits are set to '1' and the ONE_SHOT bit comes back to '0' by hardware.

CTRL_REG3 Interrupt control

7	6	5	4	3	2	1	0
INT_H_L	PP_OD	INT2_S3	INT2_S2	INT2_S1	INT1_S3	INT1_S2	INT1S1

Address: 22h

Type: R/W

Description: Control register.

[7] INT_H_L: Interrupt active high, low. Default value: 0
(0: active high; 1: active low)

[6] PP_OD: Push-pull/open drain selection on interrupt pads. Default value: 0
(0: push-pull; 1: open drain)

[5:3] INT2_S3, INT2_S2, INT2_S1: data signal on INT2 pad control bits. Default value: 00
(see *Table 19.*)

[2:0 INT1_S3, INT1_S2, INT1_S1: data signal on INT1 pad control bits. Default value: 00
(see *Table 19.*)

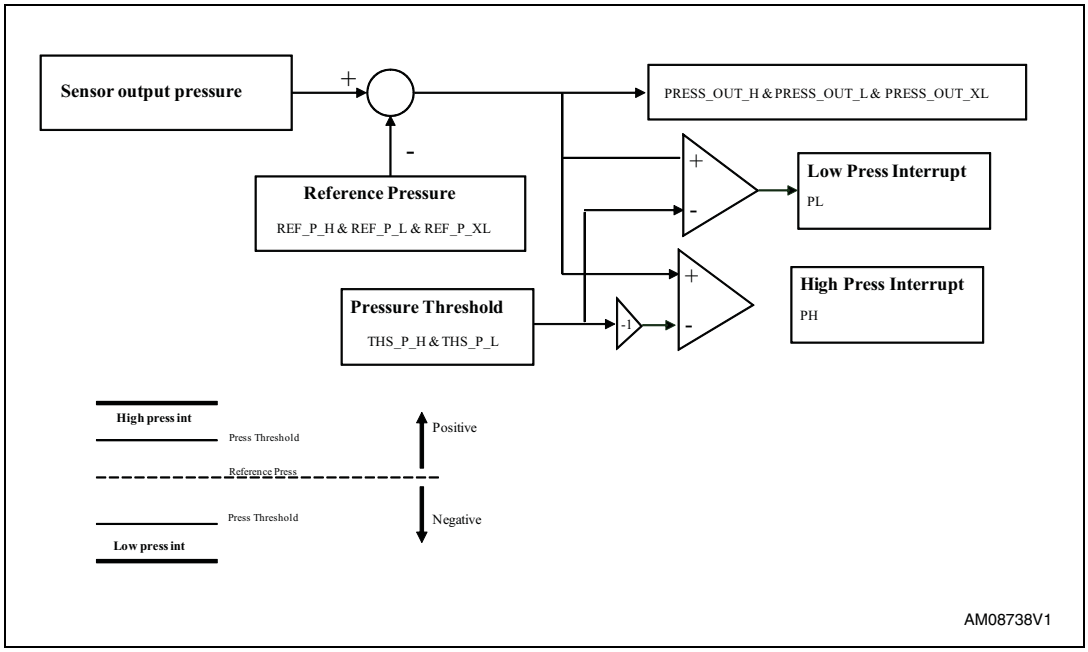
Table 19. Interrupt configurations

INT1(2)_S3	INT1(2)_S2	INT1(2)S1	INT1(2) pin
0	0	0	GND
0	0	1	Pressure high (P_high)
0	1	0	Pressure low (P_low)
0	1	1	P_low OR P_high
1	0	0	Data ready
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Tri-state

The device features two fully-programmable interrupt sources (*INT1* and *INT2*) which may be configured to trigger different pressure events. *Figure 10* shows the block diagram of the interrupt generation block and output pressure data.

The device may also be configured to generate, through interrupt pins, a Data Ready signal (*Drdy*) which indicates when a new measured pressure data is available, thus simplifying data synchronization in digital systems.

Figure 10. Interrupt generation block and output pressure data.



INTERRUPT_CFG Interrupt configuration

7	6	5	4	3	2	1	0
RESERVED					LIR	PL_E	PH_E

Address: 23h

Type: R/W

Reset: 00h

Description: Interrupt configuration.

[7:3] RESERVED

[2] LIR: Latch Interrupt request into INT_SOURCE register. Default value: 0.
(0: interrupt request not latched; 1: interrupt request latched)

[1] PL_E: Enable interrupt generation on differential pressure low event. Default value: 0.
(0: disable interrupt request;
1: enable interrupt request on measured differential pressure value lower than preset threshold)

[0] PH_E: Enable interrupt generation on differential pressure high event. Default value: 0
(0: disable interrupt request;
1:enable interrupt request on measured differential pressure value higher than preset threshold)

INT_SOURCE Interrupt source

7	6	5	4	3	2	1	0
0	0	0	0	0	IA	PL	PH

Address: 24h

Type: R

Reset: 00h

Description: INT_SOURCE register is cleared by reading INT_ACK register.

[7:3] 0

[2] IA: Interrupt Active.
(0: no interrupt has been generated; 1: one or more interrupt events have been generated).

[1] PL: Differential pressure Low.
(0: no interrupt has been generated; 1: Low differential pressure event has occurred).

[0] PH: Differential pressure High.
(0: no interrupt has been generated; 1: High differential pressure event has occurred).

THS_P_L Threshold pressure (LSB)

7	6	5	4	3	2	1	0
THS7	THS6	THS5	THS4	THS3	THS2	THS1	THS0

Address: 25h

Type: R/W

Reset: 00h

Description: This register contains the low part of threshold value for pressure interrupt generation. The complete threshold value is given by THS_P_H & THS_P_L and is expressed as unsigned number.

[7:0] THS7 - THS0: Threshold pressure LSB. Default value: 00h.