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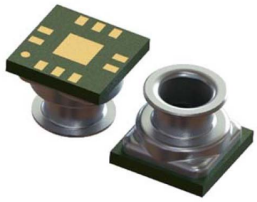
LPS33HW

MEMS pressure sensor: 260-1260 hPa absolute digital output barometer with water-resistant package

Datasheet - production data



CCLGA 10L
3.3 x 3.3 x 2.9 mm

Features

- Pressure sensor with water-resistant package
- 260 to 1260 hPa absolute pressure range
- Current consumption down to 3 µA
- High overpressure capability: 20x full scale
- Embedded temperature compensation
- 24-bit pressure data output
- 16-bit temperature data output
- ODR from 1 Hz to 75 Hz
- SPI and I²C interfaces
- Embedded FIFO
- Interrupt functions: data-ready, FIFO flags, pressure thresholds
- Supply voltage: 1.7 to 3.6 V
- ECOPACK® lead-free compliant

Applications

- Wearable devices
- Altimeters and barometers for portable devices
- GPS applications
- Weather station equipment

Description

The LPS33HW is an ultra-compact piezoresistive pressure sensor which functions as a digital output barometer. The device comprises a sensing element and an IC interface which communicates through I^2C or SPI from the sensing element to the application.

The sensing element, which detects absolute pressure, consists of a suspended membrane manufactured using a dedicated process developed by ST.

The LPS33HW is available in a ceramic LGA package with metal lid. It is guaranteed to operate over a temperature range extending from -40 °C to +85 °C. The package is holed to allow external pressure to reach the sensing element. Gel inside the IC protects the electrical components from water.

Table 1. Device summary

Order codes	Temperature range [°C]	Package	Packing
LPS33HWTR	-40 to +85°C	CCLGA-10L	Tape and reel
LPS33HW			Tray

Contents

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1 Block diagram and pin description

Figure 1. Block diagram

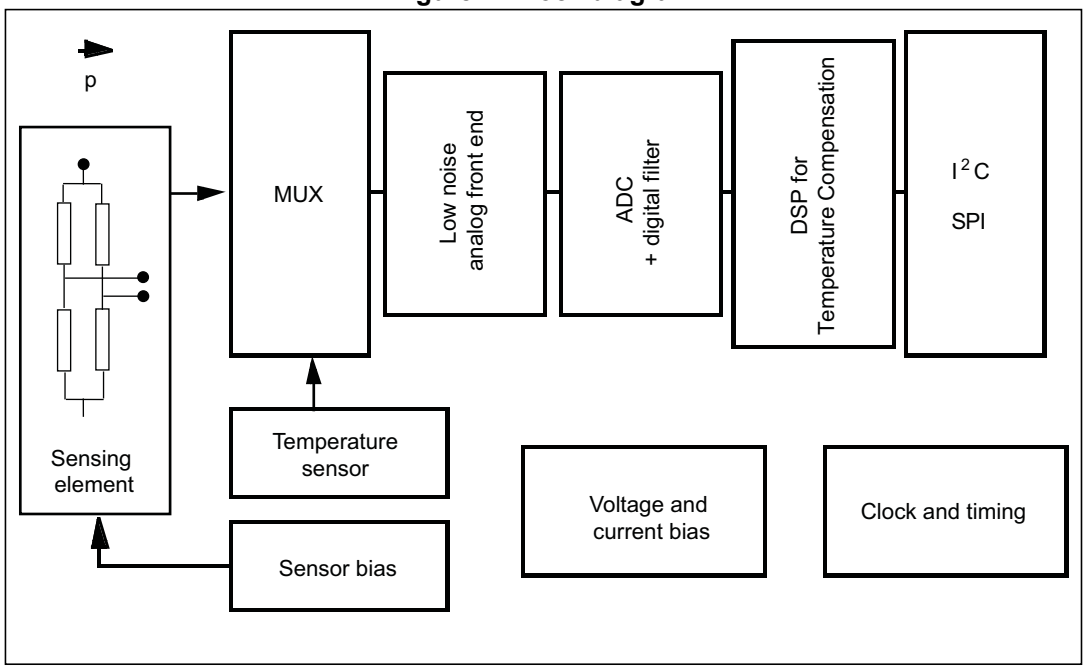


Figure 2. Pin connections (bottom view)

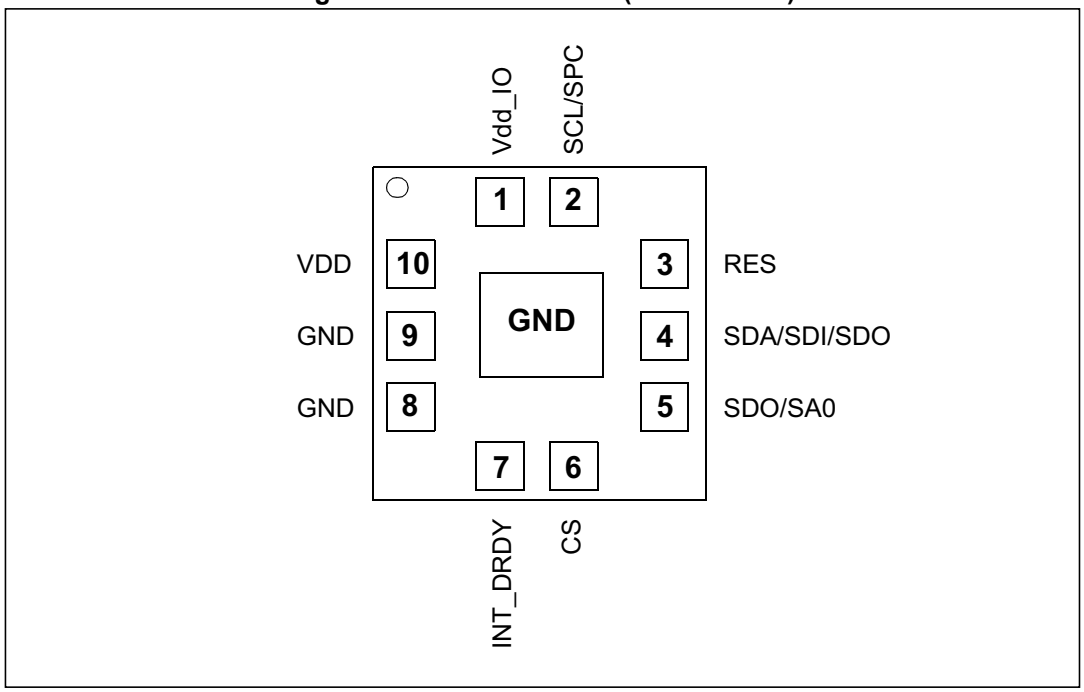


Table 2. Pin description

Pin number	Name	Function
1	Vdd_IO	Power supply for I/O pins
2	SCL SPC	I^2C serial clock (SCL) SPI serial port clock (SPC)
3	Reserved	Connect to GND
4	SDA SDI SDI/SDO	I^2C serial data (SDA) 4-wire SPI serial data input (SDI) 3-wire serial data input/output (SDI/SDO)
5	SDO SA0	4-wire SPI serial data output (SDO) I^2C less significant bit of the device address (SA0)
6	CS	SPI enable I^2C/SPI mode selection (1: SPI idle mode / I^2C communication enabled; 0: SPI communication mode / I^2C disabled)
7	INT_DRDY	Interrupt or data-ready
8	GND	0 V supply
9	GND	0 V supply
10	VDD	Power supply

2 Mechanical and electrical specifications

2.1 Mechanical characteristics

VDD = 1.8 V, T = 25 °C, unless otherwise noted.

Table 3. Pressure and temperature sensor characteristics

Symbol	Parameter	Test condition	Min.	Typ.(1)	Max.	Unit
Pressure sensor characteristics						
PT_{op}	Operating temperature range		-40		+85	°C
PT_{full}	Full accuracy temperature range		0		+65	°C
P_{op}	Operating pressure range		260		1260	hPa
P_{bits}	Pressure output data			24		bits
P_{sens}	Pressure sensitivity			4096		LSB/ hPa
P_{AccRel}	Relative accuracy over pressure(2)	P = 800 - 1100 hPa T = 25 °C		±0.1		hPa
P_{AccT}	Absolute accuracy over temperature	P_{op} T = 0 ~ 65 °C Before OPC(3)		±2.5		hPa
		P_{op} T = 0 ~ 65 °C After OPC(3)		±1		
P_{noise}	RMS pressure noise(4)	Without embedded filtering		0.02		hPa RMS
		With embedded filtering (ODR/20)		0.008		
ODR_{Pres}	Pressure output data rate(5)			1 10 25 50 75		Hz
P_longterm	Pressure accuracy long-term stability			±1		hPa/ year
Temperature sensor characteristics						
T_{op}	Operating temperature range		-40		+85	°C
T_{sens}	Temperature sensitivity			100		LSB/°C
ODR_T	Temperature output data rate(5)			1 10 25 50 75		Hz

1. Typical specifications are not guaranteed.
2. By design.
3. OPC: One-Point Calibration, see registers *RPDS_L (18h)*, *RPDS_H (19h)*.
4. Pressure noise RMS evaluated in a controlled environment, based on the average standard deviation of 32 measurements at highest ODR and LC_EN bit = 0, EN_LPFP = 1, LPFP_CFG = 1 for "with embedded filter (ODR/20)" and LC_EN bit = 0, EN_LPFP = 0, LPFP_CFG = x for "without embedded filter".
5. Output data rate is configured acting on ODR[2:0] in *CTRL_REG1 (10h)*.

2.2 Electrical characteristics

VDD = 1.8 V, T = 25 °C, unless otherwise noted.

Table 4. Electrical characteristics

Symbol	Parameter	Test condition	Min.	Typ.(1)	Max.	Unit
VDD	Supply voltage		1.7		3.6	V
Vdd_IO	IO supply voltage		1.7		Vdd+0.1	V
Idd	Supply current	@ ODR 1 Hz LC_EN bit = 0		15		µA
		@ ODR 1 Hz LC_EN bit = 1		3		
IddPdn	Supply current in power-down mode			1		µA

1. Typical specifications are not guaranteed.

Table 5. DC characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
DC input characteristics						
Vil	Low-level input voltage (Schmitt buffer)	-	-	-	0.2 * Vdd_IO	V
Vih	High-level input voltage (Schmitt buffer)	-	0.8 * Vdd_IO	-	-	V
DC output characteristics						
Vol	Low-level output voltage		-	-	0.2	V
Voh	High-level output voltage		Vdd_IO - 0.2	-	-	V

2.3 Communication interface characteristics

2.3.1 SPI - serial peripheral interface

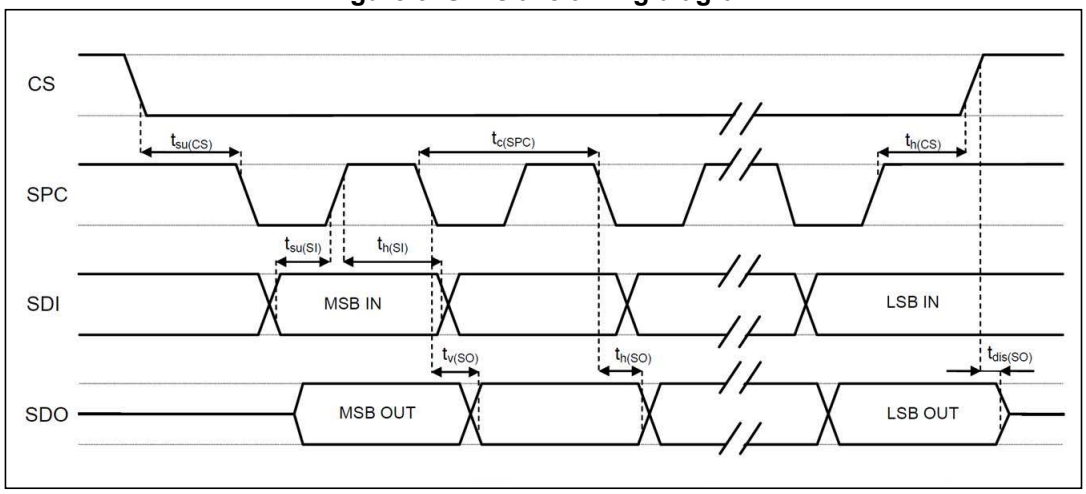
Subject to general operating conditions for Vdd and T_{OP}.

Table 6. SPI slave timing values

Symbol	Parameter	Value(1)		Unit
		Min	Max	
$t_{c(SPC)}$	SPI clock cycle	100		ns
$f_{c(SPC)}$	SPI clock frequency		10	MHz
$t_{su(CS)}$	CS setup time	6		ns
$t_{h(CS)}$	CS hold time	8		
$t_{su(SI)}$	SDI input setup time	5		
$t_{h(SI)}$	SDI input hold time	15		
$t_{v(SO)}$	SDO valid output time		50	
$t_{h(SO)}$	SDO output hold time	9		
$t_{dis(SO)}$	SDO output disable time		50	

1. Values are guaranteed at 10 MHz clock frequency for SPI with both 4 and 3 wires, based on characterization results, not tested in production.

Figure 3. SPI slave timing diagram



Note: Measurement points are done at 0.2·Vdd_IO and 0.8·Vdd_IO, for both ports.

2.3.2 I²C - inter-IC control interface

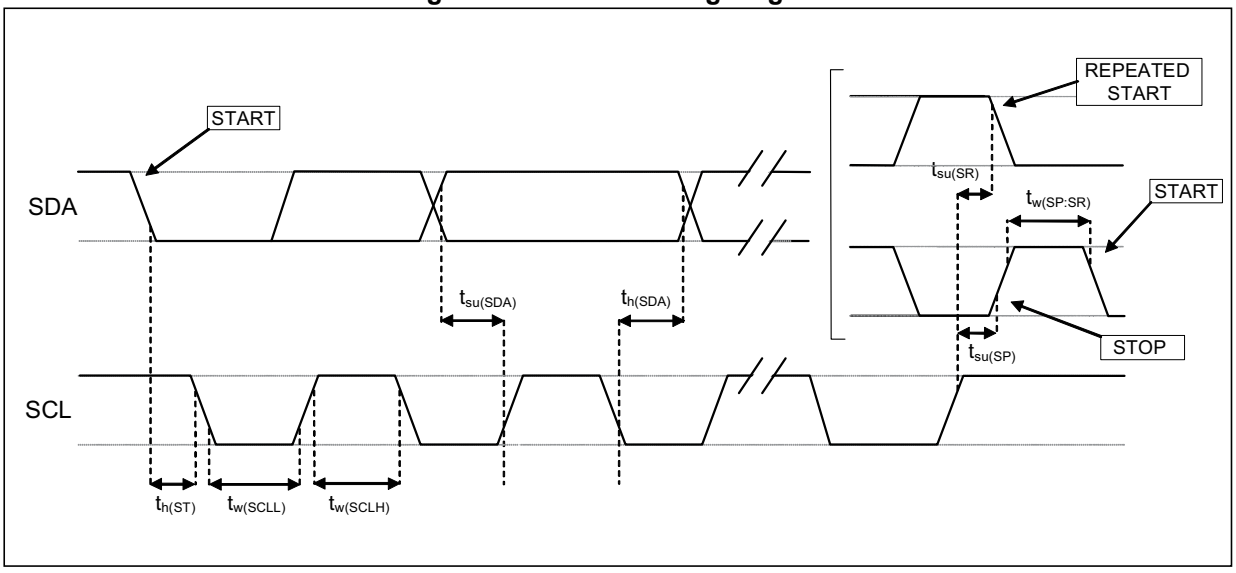
Subject to general operating conditions for Vdd and T_{OP}.

Table 7. I²C slave timing values

Symbol	Parameter (1)	I²C standard mode(1)		I²C fast mode(1)		Unit
		Min	Max	Min	Max	
$f_{(SCL)}$	SCL clock frequency	0	100	0	400	kHz
$t_{w(SCLL)}$	SCL clock low time	4.7		1.3		µs
$t_{w(SCLH)}$	SCL clock high time	4.0		0.6		
$t_{su(SDA)}$	SDA setup time	250		100		ns
$t_{h(SDA)}$	SDA data hold time	0	3.45	0	0.9	µs
$t_{h(ST)}$	START condition hold time	4		0.6		µs
$t_{su(SR)}$	Repeated START condition setup time	4.7		0.6		
$t_{su(SP)}$	STOP condition setup time	4		0.6		
$t_{w(SP:SR)}$	Bus free time between STOP and START condition	4.7		1.3		

1. Data based on standard I²C protocol requirement, not tested in production.

Figure 4. I²C slave timing diagram



Note: Measurement points are done at 0.2·Vdd_IO and 0.8·Vdd_IO, for both ports.

2.4 Absolute maximum ratings

Stress above those listed as “Absolute maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 8. Absolute maximum ratings

Symbol	Ratings	Maximum value	Unit
Vdd	Supply voltage	-0.3 to 4.8	V
Vdd_IO	I/O pins supply voltage	-0.3 to 4.8	V
Vin	Input voltage on any control pin	-0.3 to Vdd_IO +0.3	V
$P_{(air)}$	Overpressure	2	MPa
$P_{(water)}$	Overpressure	1	MPa
T_{STG}	Storage temperature range	-40 to +125	°C
ESD	Electrostatic discharge protection	2 (HBM)	kV

Note: Supply voltage on any pin should never exceed 4.8 V.

This device is sensitive to mechanical shock, improper handling can cause permanent damage to the part.

This device is sensitive to electrostatic discharge (ESD), improper handling can cause permanent damage to the part.

3 Functionality

The LPS33HW is a high-resolution, digital output pressure sensor packaged in a CCLGA package with metal lid. The complete device includes a sensing element based on a piezoresistive Wheatstone bridge approach, and an IC interface which communicates a digital signal from the sensing element to the application.

3.1 Sensing element

An ST proprietary process is used to obtain a silicon membrane for MEMS pressure sensors. When pressure is applied, the membrane deflection induces an imbalance in the Wheatstone bridge piezoresistances whose output signal is converted by the IC interface.

3.2 IC interface

The complete measurement chain is composed of a low-noise amplifier which converts the resistance unbalance of the MEMS sensors (pressure and temperature) into an analog voltage using an analog-to-digital converter.

The pressure and temperature data may be accessed through an I²C/SPI interface thus making the device particularly suitable for direct interfacing with a microcontroller.

The LPS33HW features a data-ready signal which indicates when a new set of measured pressure and temperature data are available, thus simplifying data synchronization in the digital system that uses the device.

3.3 Factory calibration

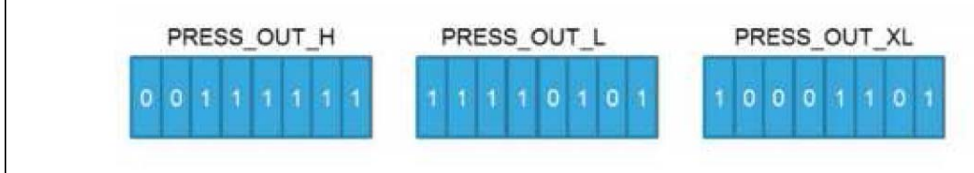
The trimming values are stored inside the device in a non-volatile structure. When the device is turned on, the trimming parameters are downloaded into the registers to be employed during the normal operation which allows the device to be used without requiring any further calibration.

3.4 Interpreting pressure readings

The pressure data are stored 3 registers: *PRESS_OUT_H (2Ah)*, *PRESS_OUT_L (29h)*, and *PRESS_OUT_XL (28h)*. The value is expressed as 2's complement.

To obtain the pressure in hPa, take the two's complement of the complete word and then divide by 4096 LSB/hPa.

Figure 5. Pressure readings



Equation 1

Pressure Value (LSB) = PRESS_OUT_H (2Ah) & PRESS_OUT_L (29h) & PRESS_OUT_XL (28h)
= 3FF58Dh = 4191629 LSB (decimal signed)

Equation 2

$$\text{Pressure (hPa)} = \frac{\text{Pressure Value (LSB)}}{\text{Scaling Factor}} = \frac{4191629\ \text{LSB}}{4096\ \text{LSB/hPa}} = 1023.3\text{hPa}$$

4 FIFO

The LPS33HW embeds 32 slots of 40-bit data FIFO to store the pressure and temperature output values. This allows consistent power saving for the system since the host processor does not need to continuously poll data from the sensor, but it can wake up only when needed and burst the significant data out from the FIFO. This buffer can work according to seven different modes: Bypass mode, FIFO mode, Stream mode, Dynamic-Stream mode, Stream-to-FIFO mode, Bypass-to-Stream and Bypass-to-FIFO mode. The FIFO buffer is enabled when the FIFO_EN bit in *CTRL_REG2 (11h)* is set to '1' and each mode is selected by the FIFO_MODE[2:0] bits in *FIFO_CTRL (14h)*. Programmable FIFO threshold status, FIFO overrun events and the number of unread samples stored are available in the *FIFO_STATUS (26h)*register and can be set to generate dedicated interrupts on the INT_DRDY pad using the *CTRL_REG3 (12h)* register.

FIFO_STATUS (26h)(FTH_FIFO) goes to '1' when the number of unread samples (*FIFO_STATUS (26h)*(FSS5:0)) is greater than or equal to WTM[4:0] in *FIFO_CTRL (14h)*. If *FIFO_CTRL (14h)*(WTM4:0) is equal to 0, *FIFO_STATUS (26h)*(FTH_FIFO) goes to '0'.

FIFO_STATUS (26h)(OVRN) is equal to '1' if a FIFO slot is overwritten.

FIFO_STATUS (26h)(FSS5:0) contains stored data levels of unread samples; when FSS[5:0] is equal to '000000' FIFO is empty, when FSS[5:0] is equal to '100000' FIFO is full and the unread samples are 32.

To guarantee the switching into and out of FIFO mode, discard the first sample acquired.

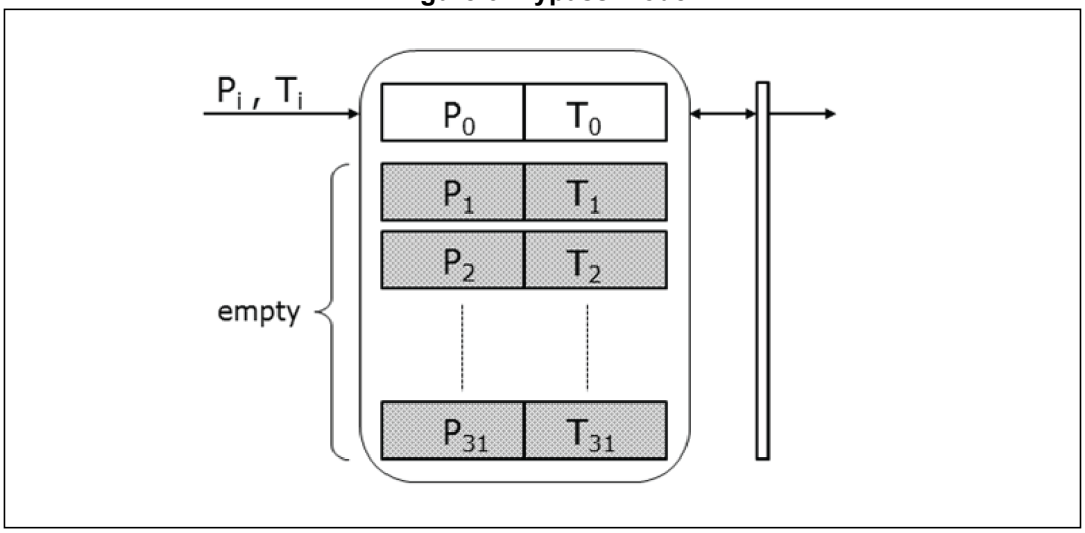
4.1 Bypass mode

In Bypass mode (*FIFO_CTRL (14h)*(FMODE2:0)=000), the FIFO is not operational and it remains empty.

Bypass mode is also used to reset the FIFO when in FIFO mode.

As described in the next figure, for each channel only the first address is used. When new data is available, the older data is overwritten.

Figure 6. Bypass mode



4.2 FIFO mode

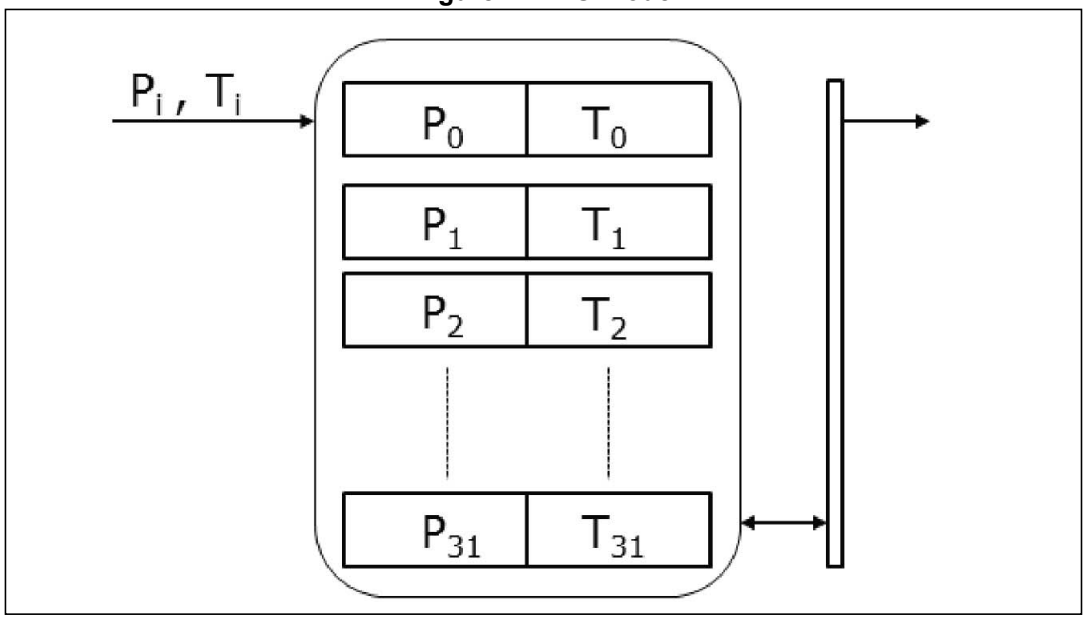
In FIFO mode (*FIFO_CTRL (14h)*(FMODE2:0) = 001) data from the output *PRESS_OUT_H (2Ah)*, *PRESS_OUT_L (29h)*, *PRESS_OUT_XL (28h)* and *TEMP_OUT_H (2Ch)*, *TEMP_OUT_L (2Bh)* are stored in the FIFO until it is overwritten.

To reset FIFO content, Bypass mode the value '000' must be written in *FIFO_CTRL (14h)*(FMODE2:0). After this reset command it is possible to restart FIFO mode writing the value '001' in *FIFO_CTRL (14h)*(FMODE2:0).

FIFO buffer memorizes 32 levels of data but the depth of the FIFO can be resized by setting the *CTRL_REG2 (11h)*(STOP_ON_FTH) bit. If the STOP_ON_FTH bit is set to '1', FIFO depth is limited to *FIFO_CTRL (14h)*(WTM4:0) + 1 data.

A FIFO threshold interrupt can be enabled (F_OVR bit in *CTRL_REG3 (12h)* in order to be raised when the FIFO is filled to the level specified by the WTM4:0 bits of *FIFO_CTRL (14h)*. When a FIFO threshold interrupt occurs, the first data has been overwritten and the FIFO stops collecting data from the input pressure and temperature.

Figure 7. FIFO mode



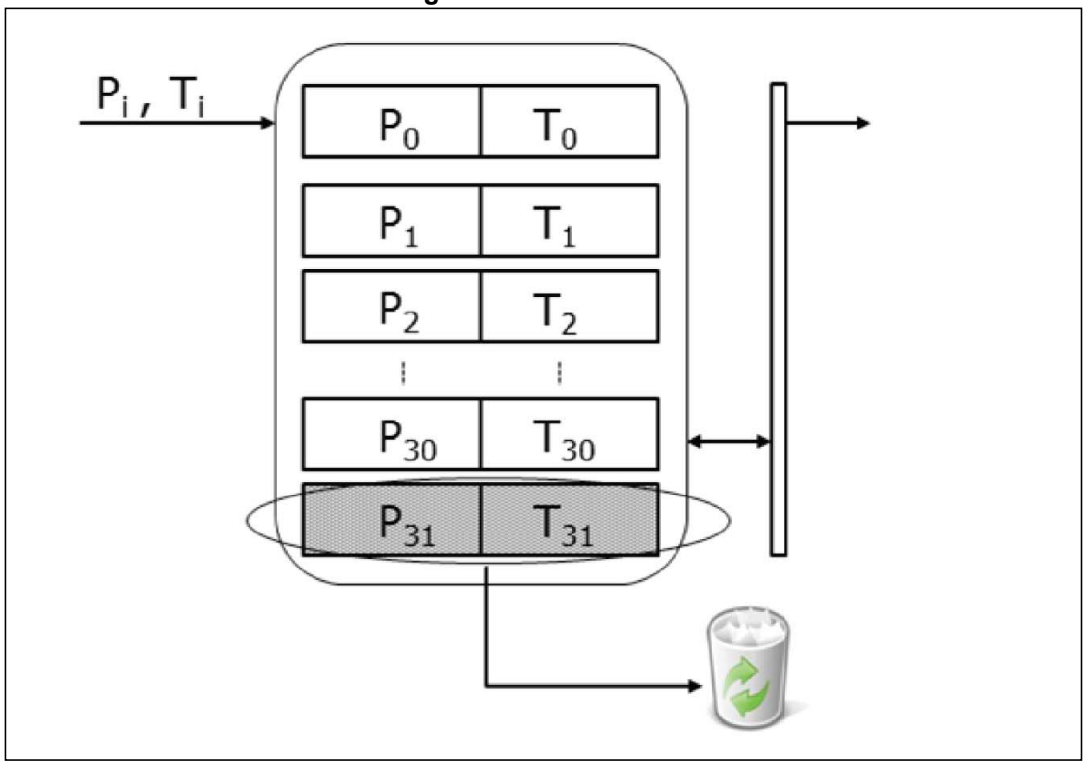
4.3 Stream mode

Stream mode (*FIFO_CTRL (14h)*(FMODE2:0) = 010) provides continuous FIFO update: as new data arrive, the older is discarded.

Once the entire FIFO has been read, the last data read still remains in the FIFO and hence once a new sample is acquired, the *FIFO_STATUS (26h)*(FSS5:0) value rises from 0 to 2.

An overrun interrupt can be enabled, *CTRL_REG3 (12h)*(F_OVR) = '1', in order to inform when the FIFO is full and eventually read its content all at once. If an overrun occurs, the oldest sample in FIFO is overwritten, so if the FIFO was empty, the lost sample has already been read.

Figure 8. Stream mode



In the latter case reading all FIFO content before an overrun interrupt has occurred, the first data read is equal to the last already read in the previous burst, so the number of new data available in FIFO depends on the previous reading.

4.4 Dynamic-Stream mode

In Dynamic-Stream mode (*FIFO_CTRL (14h)*(FMODE2:0) = 110) after emptying the FIFO, the first new sample that arrives becomes the first to be read in a subsequent read burst. In this way the number of new data available in FIFO does not depend on the previous reading.

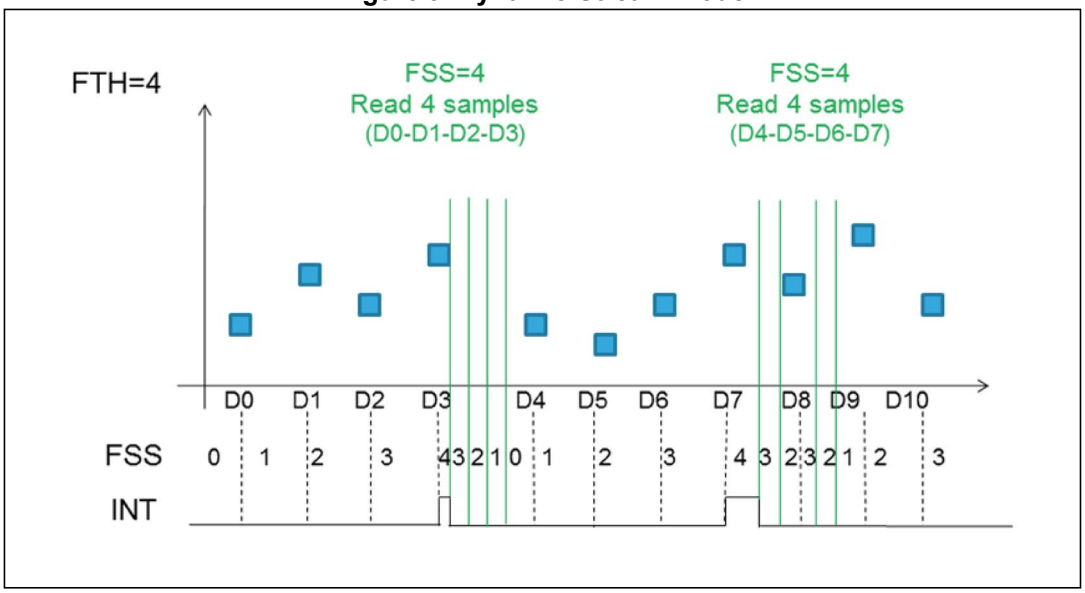
In Dynamic-Stream mode *FIFO_STATUS (26h)*(FSS5:0) is the number of new pressure and temperature samples available in the FIFO buffer.

Stream Mode is intended to be used to read all 32 samples of FIFO within an ODR after receiving an overrun signal.

Dynamic-Stream is intended to be used to read *FIFO_STATUS (26h)*(FSS5:0) samples when it is not possible to guarantee reading data within an ODR.

Also, a FIFO threshold interrupt on the INT_DRDY pad through *CTRL_REG3 (12h)*(F_FTH) can be enabled in order to read data from the FIFO and leave free memory slots for incoming data.

Figure 9. Dynamic-Stream mode



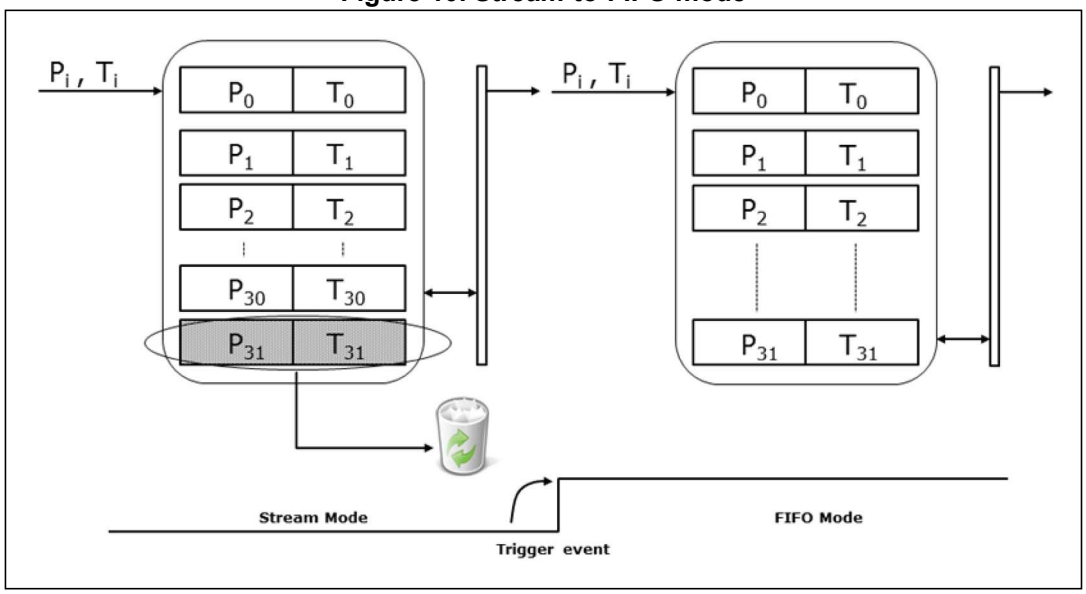
4.5 Stream-to-FIFO mode

In Stream-to-FIFO mode (*FIFO_CTRL (14h)*(FMODE2:0) = 011), FIFO behavior changes according to the *INT_SOURCE (25h)*(IA) bit. When *INT_SOURCE (25h)*(IA) bit is equal to '1', FIFO operates in FIFO mode. When the *INT_SOURCE (25h)*(IA) bit is equal to '0', FIFO operates in Stream mode.

An interrupt generator can be set to the desired configuration through *INTERRUPT_CFG (0Bh)*.

The *INTERRUPT_CFG (0Bh)*(LIR) bit should be set to '1' in order to have latched interrupt.

Figure 10. Stream-to-FIFO mode



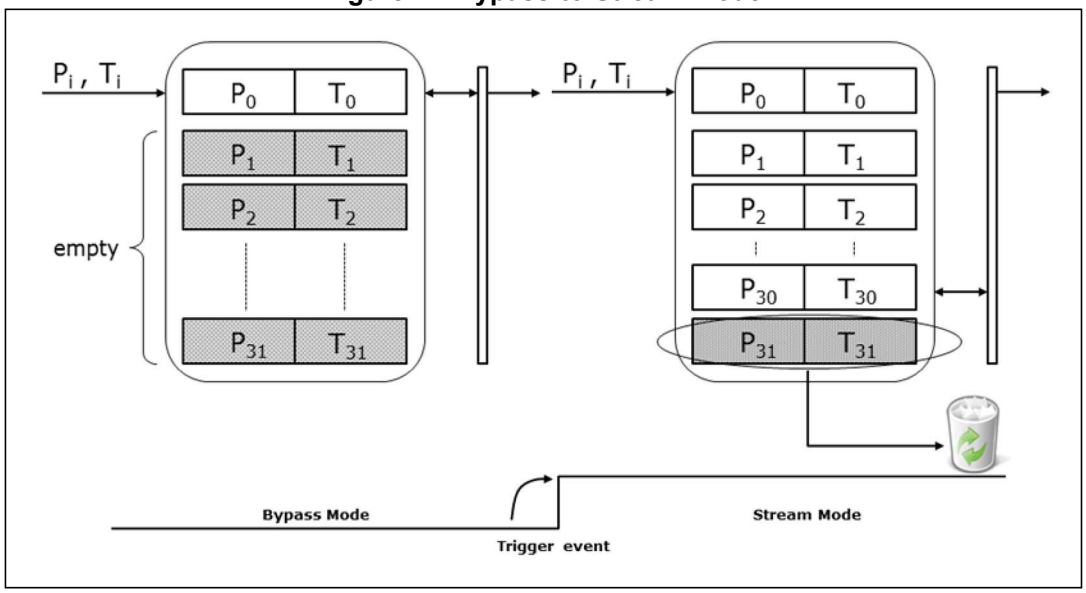
4.6 Bypass-to-Stream mode

In Bypass-to-Stream mode (*FIFO_CTRL (14h)*(FMODE2:0) = '100'), data measurement storage inside FIFO operates in Stream mode when *INT_SOURCE (25h)*(IA) is equal to '1',otherwise FIFO content is reset (Bypass mode).

An interrupt generator can be set to the desired configuration through *INTERRUPT_CFG (0Bh)*.

The *INTERRUPT_CFG (0Bh)*(LIR) bit should be set to '1' in order to have latched interrupt.

Figure 11. Bypass-to-Stream mode



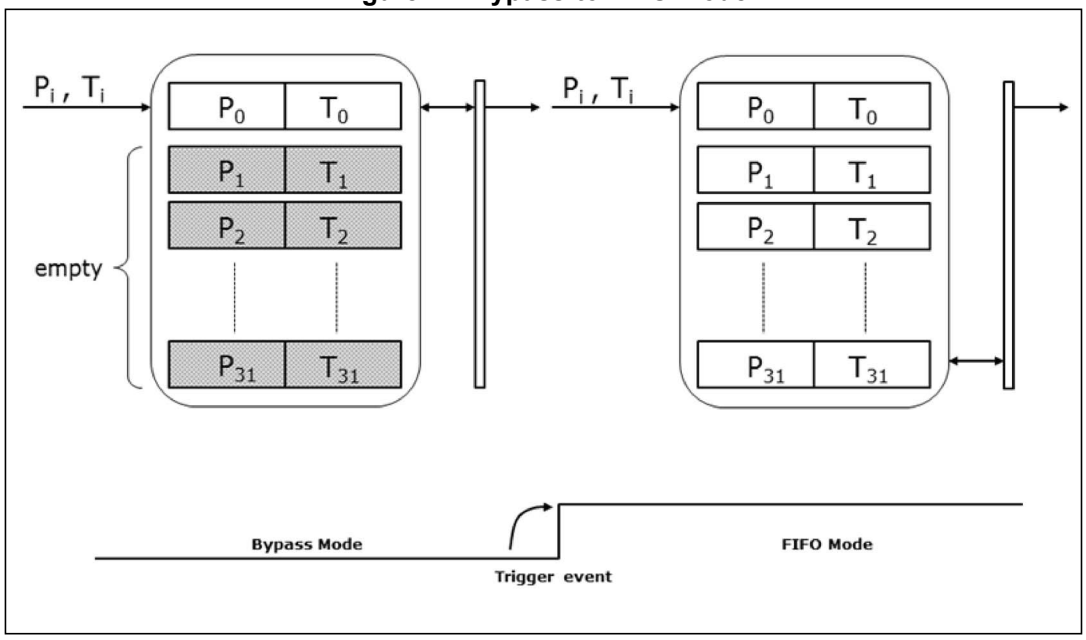
4.7 Bypass-to-FIFO mode

In Bypass-to-FIFO mode (*FIFO_CTRL (14h)*(FMODE2:0) = '111'), data measurement storage inside FIFO operates in FIFO mode when *INT_SOURCE (25h)*(IA) is equal to '1', otherwise FIFO content is reset (Bypass mode).

An interrupt generator can be set to the desired configuration through *INTERRUPT_CFG (0Bh)*.

The *INTERRUPT_CFG (0Bh)*(LIR) bit should be set to '1' in order to have latched interrupt.

Figure 12. Bypass-to-FIFO mode



4.8 Retrieving data from FIFO

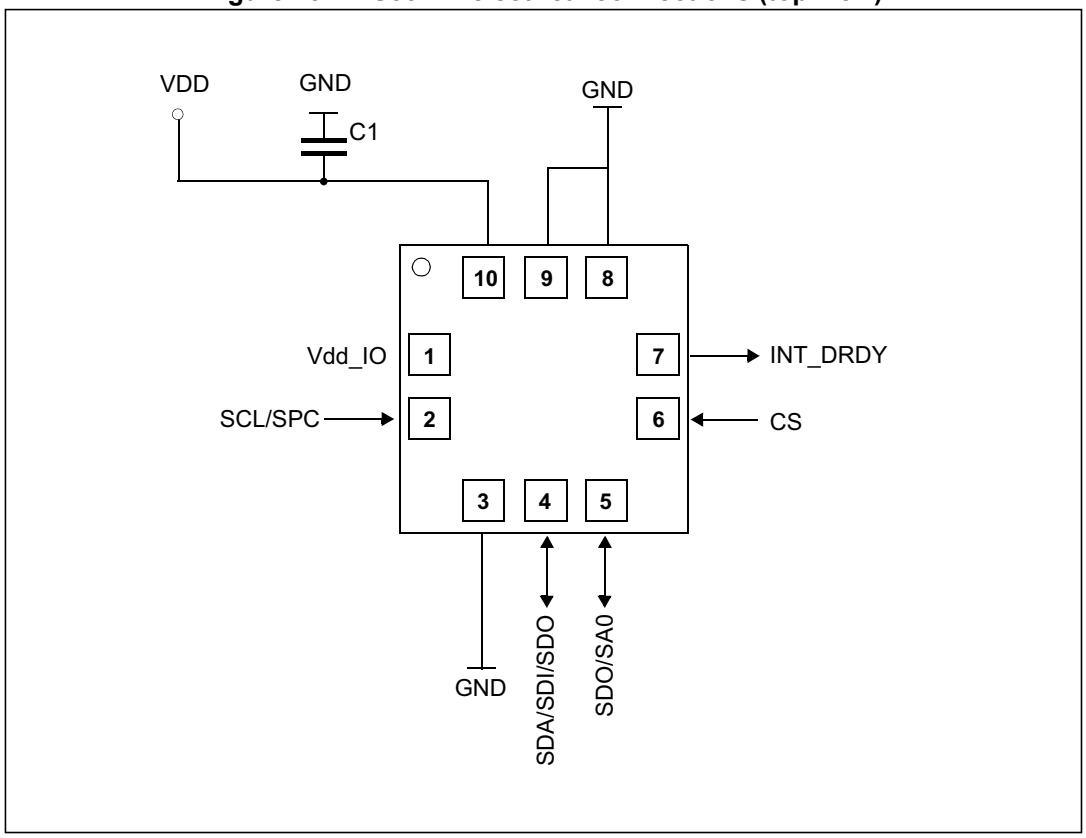
FIFO data is read from *PRESS_OUT_H (2Ah)*, *PRESS_OUT_L (29h)*, *PRESS_OUT_XL (28h)* and *TEMP_OUT_H (2Ch)*, *TEMP_OUT_L (2Bh)*.

Each time data is read from the FIFO, the oldest data are placed in the *PRESS_OUT_H (2Ah)*, *PRESS_OUT_L (29h)*, *PRESS_OUT_XL (28h)*, *TEMP_OUT_H (2Ch)* and *TEMP_OUT_L (2Bh)* registers and both single-read and read-burst operations can be used.

The reading address is automatically updated by the device and it rolls back to 28h when register 2Ch is reached. In order to read all FIFO levels in a multiple byte reading, 160 bytes (5 output registers by 32 levels) must be read.

5 Application hints

Figure 13. LPS33HW electrical connections (top view)



The device power supply must be provided through the VDD line; a power supply decoupling capacitor C1 (100 nF) must be placed as near as possible to the supply pads of the device. Depending on the application, an additional capacitor of 4.7 µF could be placed on the VDD line.

The functionality of the device and the measured data outputs are selectable and accessible through the I²C/SPI interface. When using the I^2C, CS must be tied to Vdd_IO.

All the voltage and ground supplies must be present at the same time to have proper behavior of the IC (refer to *Figure 13*). It is possible to remove VDD while maintaining Vdd_IO without blocking the communication bus, in this condition the measurement chain is powered off.

5.1 Soldering information

The CCLGA package is compliant with the ECOPACK® standard and it is qualified for soldering heat resistance according to JEDEC J-STD-020.

6 Digital interfaces

6.1 IC serial interface

The registers embedded in the LPS33HW may be accessed through both the I²C and SPI serial interfaces. The latter may be SW configured to operate either in 3-wire or 4-wire interface mode.

The serial interfaces are mapped onto the same pads. To select/exploit the I²C interface, the CS line must be tied high (i.e. connected to Vdd_IO).

Table 9. Serial interface pin description

Pin name	Pin description
CS	SPI enable I²C/SPI mode selection (1: SPI idle mode / I²C communication enabled; 0: SPI communication mode / I²C disabled)
SCL/SPC	I²C serial clock (SCL) SPI serial port clock (SPC)
SDA SDI SDI/SDO	I²C serial data (SDA) 4-wire SPI serial data input (SDI) 3-wire serial data input /output (SDI/SDO)
SDO SAO	SPI serial data output (SDO) I²C less significant bit of the device address (SA0)

6.2 I²C serial interface (CS = High)

The LPS33HW I²C is a bus slave. The I²C is employed to write data into registers whose content can also be read back.

The relevant I²C terminology is given in *Table 10.*

Table 10. I²C terminology

Term	Description
Transmitter	The device which sends data to the bus
Receiver	The device which receives data from the bus
Master	The device which initiates a transfer, generates clock signals and terminates a transfer
Slave	The device addressed by the master

There are two signals associated with the I²C bus: the serial clock line (SCL) and the serial data line (SDA). The latter is a bidirectional line used for sending and receiving the data to/from the interface. Both lines have to be connected to Vdd_IO through pull-up resistors.

The I²C interface is compliant with fast mode (400 kHz) I²C standards as well as with the normal mode.

6.2.1 I²C operation

The transaction on the bus is started through a START (ST) signal. A start condition is defined as a HIGH-to-LOW transition on the data line while the SCL line is held HIGH. After this has been transmitted by the master, the bus is considered busy. The next data byte transmitted after the start condition contains the address of the slave in the first 7 bits and the eighth bit tells whether the master is receiving data from the slave or transmitting data to the slave. When an address is sent, each device in the system compares the first seven bits after a start condition with its address. If they match, the device considers itself addressed by the master.

The slave address (SAD) associated to the LPS33HW is 101110xb. The **SDO**/**SA0** pad can be used to modify the less significant bit of the device address. If the SA0 pad is connected to voltage supply, LSb is ‘1’ (address 1011101b), otherwise if the SA0 pad is connected to ground, the LSb value is ‘0’ (address 1011100b). This solution permits to connect and address two different LPS33HW devices to the same I²C lines.

Data transfer with acknowledge is mandatory. The transmitter must release the SDA line during the acknowledge pulse. The receiver must then pull the data line LOW so that it remains stable low during the HIGH period of the acknowledge clock pulse. A receiver which has been addressed is obliged to generate an acknowledge after each byte of data received.

The I²C embedded inside the ASIC behaves like a slave device and the following protocol must be adhered to. After the start condition (ST) a slave address is sent, once a slave acknowledge has been returned (SAK), an 8-bit sub-address will be transmitted (SUB): the 7 LSB represent the actual register address while the MSB has no meaning. The IF_ADD_INC bit in *CTRL_REG2 (11h)* enables sub-address auto increment (IF_ADD_INC is '1' by default), so if IF_ADD_INC = '1' the SUB (sub-address) will be automatically increased to allow multiple data read/write.

The slave address is completed with a Read/Write bit. If the bit is ‘1’ (Read), a repeated START (SR) condition must be issued after the two sub-address bytes; if the bit is ‘0’ (Write) the master will transmit to the slave with direction unchanged. *Table 11* explains how the SAD+read/write bit pattern is composed, listing all the possible configurations.

Table 11. SAD+Read/Write patterns

Command	SAD[6:1]	SAD[0] = SA0	R/W	SAD+R/W
Read	101110	0	1	10111001 (B9h)
Write	101110	0	0	10111000 (B8h)
Read	101110	1	1	10111011 (BBh)
Write	101110	1	0	10111010 (BAh)

Table 12. Transfer when master is writing one byte to slave

Master	ST	SAD + W		SUB		DATA		SP
Slave			SAK		SAK		SAK	