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Platform Manager Development Kit

User's Guide

Introduction

Thank you for choosing the Platform Manager™ Development Kit. This user's guide describes how to start using the Platform Manager Development Kit, an easy-to-use system for evaluating and designing with the Platform Manager mixed-signal device. The kit serves as a development test environment to build designs for power supply management functions such as sequencing, power supply fault logging, trimming, reset generation, high-side MOSFET drive and user logic I/O expansion in an FPGA.

Note: Static electricity can severely shorten the life span of electronic components. Use static-safe handling practices when using this development kit. Store the board in the supplied ESD safe bag. Handle all cables and interconnects in a static-safe environment.
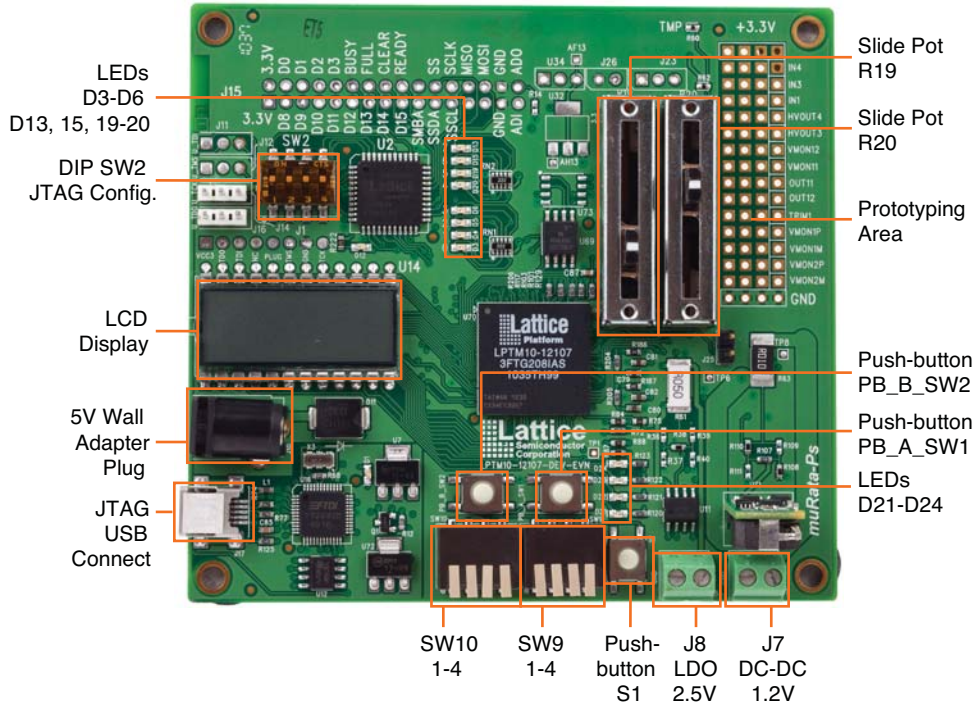
Features

The Platform Manager Development Kit includes:

- Platform Manager Evaluation Board containing the Platform Manager LPTM10-12107 device in a 208-ball ftBGA package
- USB programming support on-board
- 4Mbit SPI Flash memory for logging data and faults
- SPI and I^{2}C interfaces
- 2x16 expansion header for I^{2}C, SPI and general purpose data bus, I/O
- Two 4-bit DIP switches
- Three push-buttons for input control, reset, etc.
- DAC and A/D convertors for trimming power supplies
- LED displays
- LCD display
- Adjustable potentiometers for user faults or demos
- Thermistor circuit for temperature sensing
- LDO to demo sequencing and trim functions
- DC-DC convertor to demo sequencing and trim functions
- Two LDOs for main chip power and VCCIO supplies.
- VMON, voltage monitors for on-board and off-board power supply monitoring
- Off-board screw connectors for user loads and testing
- Prototyping/interface connections
- Pre-loaded Demo – The Platform Manager Development Kit contains a pre-loaded demo design that illustrates many of the key features of the Platform Manager device.
- USB Connector Cable – The Platform Manager Evaluation Board is programmed via the USB cable driven from the user's computer. This USB cable is included in the Platform Manager Development Kit.
- Power Supply – The Platform Manager Evaluation board is powered by an AC adapter (included).
- [Platform Manager Development Kit QuickSTART Guide](#) – Provides information on connecting the Platform Manager Evaluation Board, getting started with the pre-programmed demo, and starting your own design.
- [Platform Manager Development Kit Web Page](#) – The Platform Manager Development Kit Web Page provides access to the latest documentation, demo designs and additional resources.

The contents of this user's guide includes demo operation descriptions, top-level functionality descriptions of various portions of the evaluation board, descriptions of the on-board connectors, switches and a complete set of schematics of the Platform Manager Evaluation Board.

Figure 1. Platform Manager Evaluation Board, Top Side

Use the QuickSTART Guide First

Please use the Platform Manager Development Kit QuickSTART Guide that comes with the Platform Manager Development Kit to get started. The QuickSTART Guide provides a "fast path" for working with the Platform Manager Evaluation Board and the pre-programmed Platform Manager demo. This user's guide augments the QuickSTART guide by providing detailed descriptions of the board demos and schematic descriptions of the Platform Manager Evaluation Board.

Platform Manager Device

The Platform Manager (LPTM10-12107) device is at the heart of the Platform Management Development Kit. This device comes in a 208-ball ftBGA package and integrates both analog functions and digital functions, necessary for advanced board and system level power control. It is a feature-rich device that allows for full power control and reset generation or Platform Management.

Platform Manager is divided into a CPLD section and an FPGA section. The CPLD portion of the Platform Manager is user-configurable logic that is tightly coupled to the power management analog signaling of the Platform Manager. The FPGA section allows for more expansive and sophisticated, LUT-based control of the Platform Manager analog signaling as well as user-defined glue logic. See the Platform Manager Data Sheet for detailed information.

Analog features consist of 12 VMON analog voltage monitors with differential inputs for remote sense. Four high-voltage FET drivers are programmable for both slew rate and voltages up to 12V for driving high-side MOSFETs. For trimming and margin control, the device uses A/D converters and D/A converters for closed loop trim, whereby up to eight power supplies can be trimmed.

On the digital side, there are multiple internal clocks generated from an 8MHz internal oscillator and 16 open-drain outputs. These are controlled by the CPLD section. The FPGA section contains 640 LUTs of FPGA logic and sup-

ports flexible multiple voltage and I/O standard logic pins. The device is programmed with a JTAG interface and runs off a 3.3V rail.

The FPGA section of the Platform Manager is optimized to meet the requirements of board management functions including reset distribution, boundary scan management, fault logging, FPGA load control, and system bus interface. The FPGA section uses look-up tables (LUTs) and distributed memories for flexible and efficient logic implementation. This instant-on capability enables the Platform Manager devices to integrate control functions that are required as soon as power is applied to the board.

Power management functions can be integrated into the CPLD and digital board management functions can be integrated into the FPGA using the LogiBuilder tool provided by PAC-Designer® software. In addition, the FPGA designs can also be implemented in VHDL or Verilog HDL through the ispLEVER® design tool.

The Platform Manager device supports a hardware I²C/SMBus slave interface that can be used to measure voltages through the Analog-to-Digital Converter or is used for trimming and margining using a microcontroller.

There are two JTAG ports integrated into the Platform Manager device: Power JTAG and FPGA JTAG. The Power JTAG interface is used to program the power section of the Platform Manager and the FPGA JTAG is used to configure the FPGA portion of the device. The FPGA configuration memory can be changed in-system without interrupting the operation of the board management section. However, the Power Management section of the platform Manager cannot be changed without interrupting the power management operation.

Figure 2. Device Block Diagram
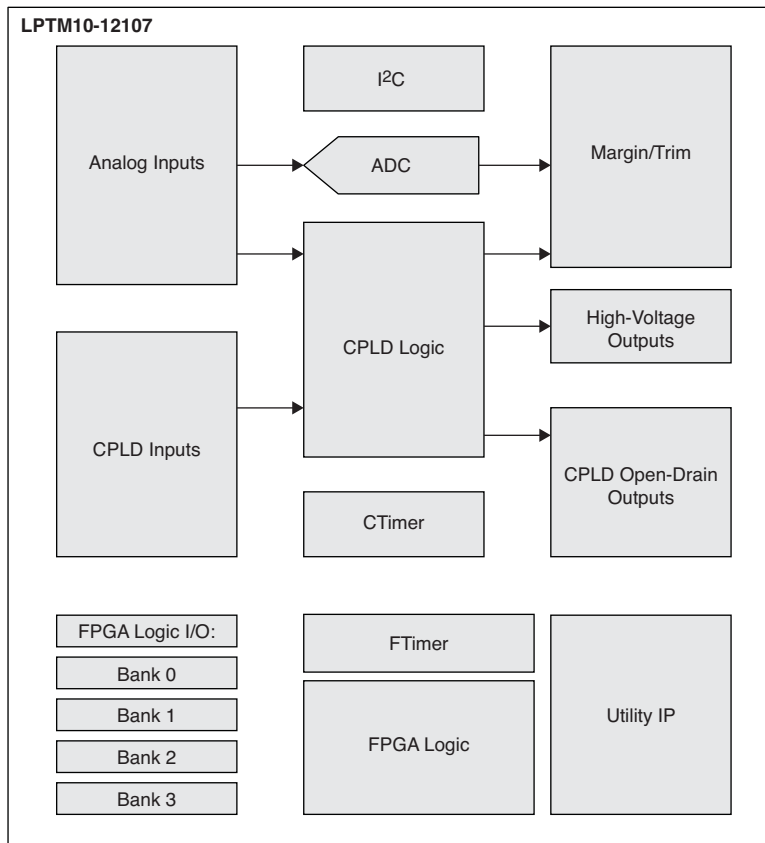
Demonstration Design

The Platform Manager Evaluation Board comes pre-programmed with the Platform Manager Demo to highlight the power control and management abilities of the Platform Manager device. This demo performs the following functions:

- Drives LEDs to represent enable circuits for power supplies

- Reads various VMONs for board power

- Provides two slider pots to fire VMON trip points

- Sequences the LDO and Murata DC-DC power supply

- Receives inputs for switches and push-buttons

- Drives the LCD display panel

Components of this demo include:

- **CPLD LEDs** – There are four LEDs connected to CPLD outputs. LEDs light when open-drain outputs of the CPLD are driven low. These are displayed to represent the board-level power supplies in the example or can be used to show sequencing.

- **FPGA LEDs** – There are eight LEDs connected to FPGA output pins. LEDs light when the FPGA pins are driven low. These are also sequenced to represent power supply enables and display different timing functions.

- **Power Supplies** – The board has two user-programmable power supplies that can be sequenced and trimmed using the Platform Manager and PAC-Designer software. After the LEDs sequence for the three board power supplies, the LDO and DC-DC converter are enabled.

- **Slide Potentiometers** – There are two slide potentiometers available to adjust VMON inputs for monitoring; these are tied to VMON8 and VMON9. The slider pot input to VMON8 and VMON9 has a range of 0V to 3.3V. The inputs can be set to trip on a window comparator within the Platform Manager. The two sliders are used in the demo to start the sequence as well as to cause a fault to occur.

- **LCD Display** – The display is a 3-digit, standard 7-segment display and is driven from 24 FPGA output pins. Segments are ON when each segment decode is driven in opposite polarity to the COM pin. The LCD is toggled at approximately 60Hz using logic in the FPGA. The demo displays a hexadecimal value on the LCD, to change the display, set the DIP switches.

- **Hardware Power Supply Margin Function** – The margining of the LDO and Murata DC-DC converter is done with a signal from the push-buttons. There are two push-buttons adjacent to the DIP switches. Pressing PBA_SW1 and PBB_SW2 drives the margin control to select between closed loop trim and margin settings. Push-buttons are tied high with a pull-up to Bank2. Pressing PBB_SW2/PBA_SW1 drives a low on FPGA inputs. The margining options shown in Table 1 are exercised in Step 5 of the demo.

Table 1. Margining Options

PBAB_SW2, PBA_SW1	Decoded in FPGA	LDO U11 2.5V	DC-DC Module 1.2V
[High, High] 1,1 not pressed	Closed Loop Trim	2.5	1.2V
[High, Low] 1,0	Margin setting 1	2.375	1.14V
[Low, High] 0,1	Margin setting 2	2.625	1.26V
[Low, Low] 0,0	Margin setting 3	2.5V	1.2V

Initial Board Setup

- Set all DIP switches in SW9 and SW10 to the up/off position

- Set all DIP switches in SW2 to the on position

- Set slide pots R19 and R20 in the down position, toward the center of the board

- No jumpers should be installed

Step 1. Test Board Power, LED D1, and All Power Supplies

Step 1 shows the ability of the Platform Manager to monitor and sequence input power rails and on-board supplies. There are five supplies connected to five separate VMON inputs on the Platform Manager Evaluation Board. The first three supplies, 5V, 3.3V, and 2.5V, are power rails that the Platform Manager does not enable; it only monitors them. The second 2.5V supply is an LDO that the Platform Manager enables and then monitors, and the 1.2V supply is a DC-DC converter that the Platform Manager enables and then monitors. There is also control from the Margin/Trim outputs on the Platform Manager to each of these supplies. Table 2 shows how the four LEDs in the display follow the progress of the monitoring, enabling, and sequencing.

- Plug the 5V wall plug supply into the board supply plug.

- The blue LED D1 will be on and will remain lit while the board is powered.

- LEDs D21-D23 cycle through Steps 1-6 as shown in Table 2. Failure to cycle through the steps indicates a power supply error.

Table 2. CPLD LED Pattern 1

Step	D24	D23	D22	D21	Function
1	off	off	off	ON	Wait for 5V supply good
2	off	off	ON	off	Wait for 3.3V supply good
3	off	off	ON	ON	Wait for 2.5V supply good
4	off	ON	off	off	Enable 2.5V LDO, wait for 2.5 good
5	off	ON	off	ON	Enable 1.2V LDO, wait for 1.2 good
6	off	ON	ON	off	Waiting for slide pots R19 and R20 to be raised to top of slide

Step 2. Test Slide Pots R19-R20 and LEDs D3-D6, D13-D14, D19-D20 and D21-D24

Step 2 tests the position of the slide pots, and displays patterns and information on the LEDs and LCD display. The slide pots are connected to two VMON inputs of the Platform Manager and are set to be "good" at about 3V. The demo checks for both pots to be at good levels, then continues to the next step, which is to exercise various digital outputs from the Platform Manager. Platform Manager outputs connect to the LEDs, as shown in the tables below, and also to the LCD. The Closed Loop Trimming function for the LDO and DC-DC converter is also enabled at this point.

- Move both slide pots R19 and R20 to the top (board edge) of their travel. LEDs D21-D24 will cycle on and off as shown in Table 3.

Table 3. CPLD LED Pattern 2

State	D24	D23	D22	D21
1	off	ON	off	ON
2	ON	off	ON	Off
Back to State 1				

- LEDs D3-D6, D13, D15 and D19-D20 will blink on and off in a binary sequence, with D13 the MSB and D3 the LSB. The LCD will display "FF" in the right-most two digits.

- The voltage across the two pins of J8 will measure 2.5V +/- 1%.

- The voltage across the two pins of J7 will measure 1.2V +/- 1%.

Step 3. Test DIP Switches SW9 and SW10

Step 3 continues to exercise the digital inputs and outputs of the Platform Manager. Two of the DIP switches are connected to the digital inputs of the Platform Manager. As these DIP switches are turned on or off, the LCD will display two hexadecimal digits corresponding to the values produced by the four bits of each DIP switch.

- One by one, move DIP switches SW9-SW10 from the off/up position to the on/down position, and then back to the off/up position. The LCD will display corresponding hexadecimal characters representing the hexadecimal value of each DIP switch as it is moved. The value will change for each switch setting, as shown in Table 4. Other values may be created by depressing more than one switch at a time.

Table 4. LCD - Hexadecimal Display

LCD Display	SW10-1	SW10-2	SW10-3	SW10-4	SW9-1	SW9-2	SW9-3	SW9-4
FE	off	off	off	off	off	off	off	ON
Fd	off	off	off	off	off	off	ON	off
Fb	off	off	off	off	off	ON	off	off
F7	off	off	off	off	ON	off	off	off
EF	off	off	off	ON	off	off	off	off
dF	off	off	ON	off	off	off	off	off
bF	off	ON	off	off	off	off	off	off
7F	ON	off	off	off	off	off	off	off

Step 4. Test All Segments of the LCD Display

Similar to Step 3, Step 4 also uses digital inputs. In this step, one of the push-buttons which is connected to a digital input causes the LCD controller to display a looping sequence of numbers from 111-FFF. This sequence repeats on the LCD as long as the push-button is depressed.

- Press and hold PB_B_SW2. The LCD display will show a counting sequence from a blank display, through 111, 222, 333 … FFF, and will repeat. The count may start anywhere in the sequence.

Step 5. Test Two Push-buttons and Trimming/Margining

This step shows the operation of the Closed Loop Trimming, and the ability of the Platform Manager to have different voltage profiles for margining which are selectable on the fly. There are three profiles used for this test. Profile 1 generates the target voltage (e.g., 1.2V) and adjusts the output voltage up by 5%. Profile 2 adjusts the output voltage down by 5%. Pressing either of the push-buttons shown below selects one of the profiles.

- Press and hold push-button PB_A_SW1.
  – The voltage across the 2 pins of J8 will measure approximately 2.625V.
  – The voltage across the 2 pins of J7 will measure approximately 1.26V.

- Release push-button PB_A_SW1.

- Press and hold push-button PB_B_SW2.
  – The voltage across the 2 pins of J8 will measure approximately 2.375V.
  – The voltage across the 2 pins of J7 will measure approximately 1.14V.

- Release push-button PB_B_SW2.

Step 6. Test Push-button S1 for Reset Function

Step 6 illustrates the Platform Manager's ability to sequence through a power-down scenario, and in this case, restart the demo. When push-button S1 is depressed, the DC-DC converter is powered down, followed by the LDO. The sequencer then returns to the beginning of the demo and starts over.

• Move slide pots R19-R20 to the down position (center of the board). Press and release push-button S1. The board will reset and the test will start over.

VID Demo

The Platform Manager Evaluation Board is designed to demonstrate a form of Voltage control by Identification (VID). This demo does not adhere to any specific "standard" VID specification. Rather, it demonstrates a generic type of digital power supply control for the two power supplies on the Platform Manager Evaluation Board. In this demo, the DIP switches are used to set the desired output voltage and to enable or disable the supplies. This demo makes use of the Platform Manager Closed-loop Trim/Fault Logger IP core and a few lines of CPLD and FPGA LogiBuilder code. This design demonstrates the following features:

• Implements closed loop trim on the 2.5V and 1.2V power supplies

• LEDs indicate the status of the LDO and Murata DC-DC power supply enables

• Receives inputs from switches and push-buttons

• A single VID lookup table can be shared between two different power supplies

• Closed-loop Trim/Fault Logger IP configuration

Note: the Fault Logger IP core is not enabled in this demo. For additional information about the Platform Manager IP core, please refer to the [Platform Management Utility Functions IP Core User's Guide](#).

In order to experiment with the VID Demo, the Platform Manager device on the board must be reprogrammed with the pre-compiled design file VID_Demo.jed.

Step 1. Download the VID Demo from the Lattice website.

The VID Demo can be downloaded from the [Platform Manager Development Kit page](#) of the Lattice Semiconductor website.

Step 2. Program the Platform Manager with VID_Demo.jed

Connect the USB cable from the computer to the Platform Manager Evaluation Board.

Warning: If your operating system prompts you to install drivers for new hardware – do not install the default USB drivers or you will have difficulty re-programming the Platform Manager device. Stop and install the Lattice USB drivers found in the ispTools folder on your computer.

Open ispVM™ Version 17.9 or later. Scan the JTAG chain (F2) to find the LPTM10-12107 device. Double-click the row to edit the device information. Browse to the VID_Demo.jed to open the file, set the Operation to **Erase, Program, Verify** and click **OK**. Click the **GO** button to start the re-programming. When the Platform Manager is programmed with the VID demo design LED D21 will be blinking on and off with a period of 500ms.

Step 3. Verify the 2.5V LDO VID Operation

Connect a Digital Volt Meter (DVM) to J8 to monitor the LDO output voltage. The voltage should be near zero with LED D24 off after programming, power-up, or reset by momentarily pressing push button S1. Enter the VID setting from Table 5 (SW[4:1]) on switch SW10 and momentarily press push-button PB_B_SW2 to enable the LDO and set the trim target. Only the following VID codes are valid for the LDO: 0, 10, 11, 12, 13, 14, and 15. The VID code of zero will disable the LDO and turn off LED D24. Any other VID will enable the LDO and turn on LED D24. VID table entries 1 to 9 are below the LDO's trim range and will result in an output near 2.38V. This is because the LDO's trim resistor network is designed to support a range of +/- 5% around the LDO's nominal 2.5V output.

Table 5. Common VID Code Lookup Table

VID	SW1	SW2	SW3	SW4	Voltage	VID Table Code
0	0	0	0	0	0.00	0
1	1	0	0	0	1.14	570
2	0	1	0	0	1.16	580
3	1	1	0	0	1.18	590
4	0	0	1	0	1.19	595
5	1	0	1	0	1.20	600
6	0	1	1	0	1.21	605
7	1	1	1	0	1.22	610
8	0	0	0	1	1.24	620
9	1	0	0	1	1.26	630
10	0	1	0	1	2.40	1200
11	1	1	0	1	2.45	1225
12	0	0	1	1	2.50	1250
13	1	0	1	1	2.55	1275
14	0	1	1	1	2.60	1300
15	1	1	1	1	2.62	1310

Note: 0 = switch in the down position; 1 = switch in the up position.

## Step 4. Verify the 1.2V Murata DC-DC Module VID Operation

Move the DVM to J7 to monitor the Murata DC-DC module output voltage. The measured voltage should be about 0.23V with LED D23 off after programming, power-up, or reset by momentarily pressing push button S1. Enter the VID setting from Table 5 (SW[4:1]) on switch SW9 and momentarily press-push button PB_A_SW1 to enable the DC-DC module and set the trim target. Only VID codes from 0 to 9 are valid for the DC-DC module. The VID code of zero will disable the DC-DC module and turn off LED D23. Any other VID will enable the DC-DC module and turn on LED D23. VID table entries 10 and above exceed the DC-DC module's trim range and will result in an output near 1.27V. This is because the trim resistor network is designed to support a range of +/- 5% around the DC-DC module's nominal 1.2V output. In Table 5, more VID codes are allocated to the DC-DC module to provide finer adjustment of the lower voltage power supply. The VID Table Codes represent the closed loop trim ADC target value and is generated from the IP configuration dialog.

Board Hardware Features

LED Outputs – CPLD

The Platform Manager Evaluation Board has four LEDs tied to the CPLD open-drain outputs. The LEDs are pulled up to 3.3V and are lit when OUT6 through OUT9 are driven to a logic low.
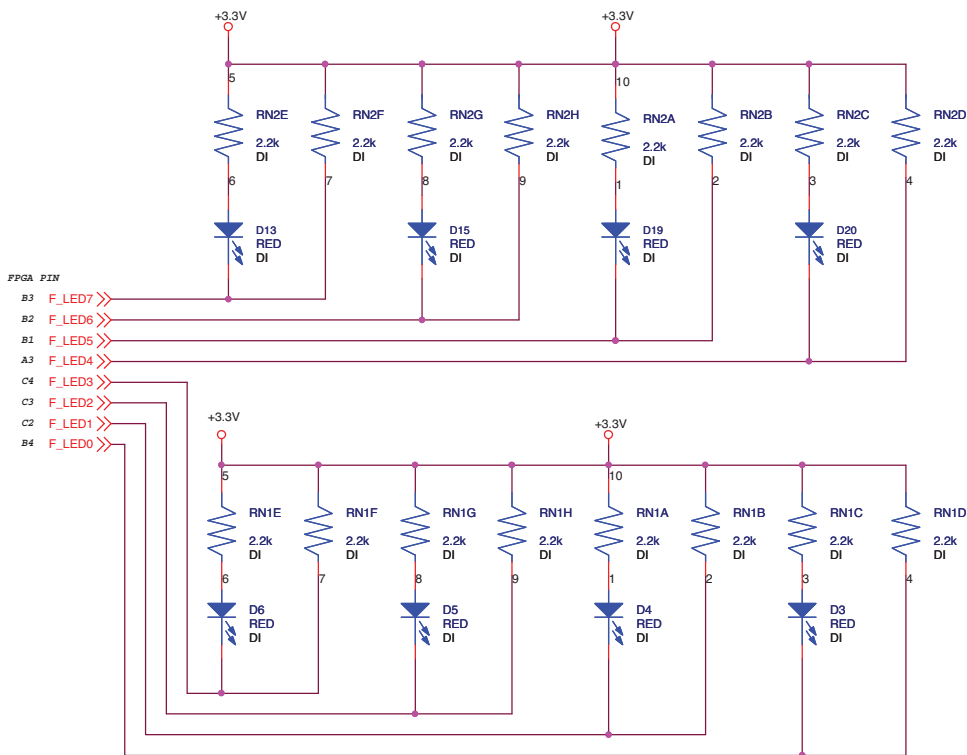
Figure 3. CPLD LEDs
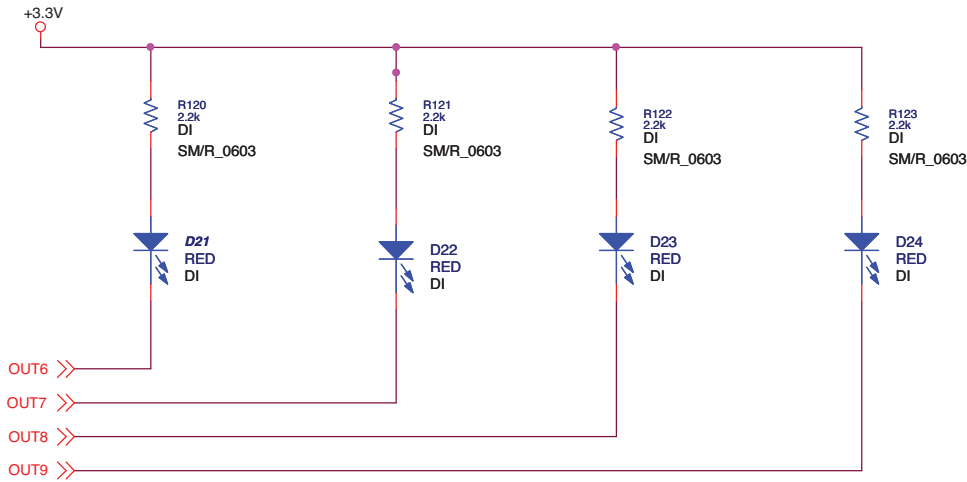
LED Outputs – FPGA

The eight FPGA LEDs are tied to Bank0 of the FPGA pins. They are pulled up to 3.3V and the LEDs are lit when the outputs are driven with a logic low.

Figure 4. FPGA LEDs

Open-Drain CPLD Outputs

There are 16 available outputs for the CPLD. These include four HVOUT pins and 12 3.3V open-drain outputs. The outputs are set up to drive four LEDs for the CPLD, four Fault Logging outputs or general purpose signals to the FPGA, SMBUS Alert and the OUT16_Timer signal. OUT11 and OUT12 are used for enables to the user supplies. OUT16_Timer drives an FPGA clock input for slow clocks and long timers in the FPGA. OUT16 time base is calculated automatically in PAC-Designer and depends on the time delay chosen by the user in the FTimer blocks.

Figure 5. Open-Drain CPLD Outputs
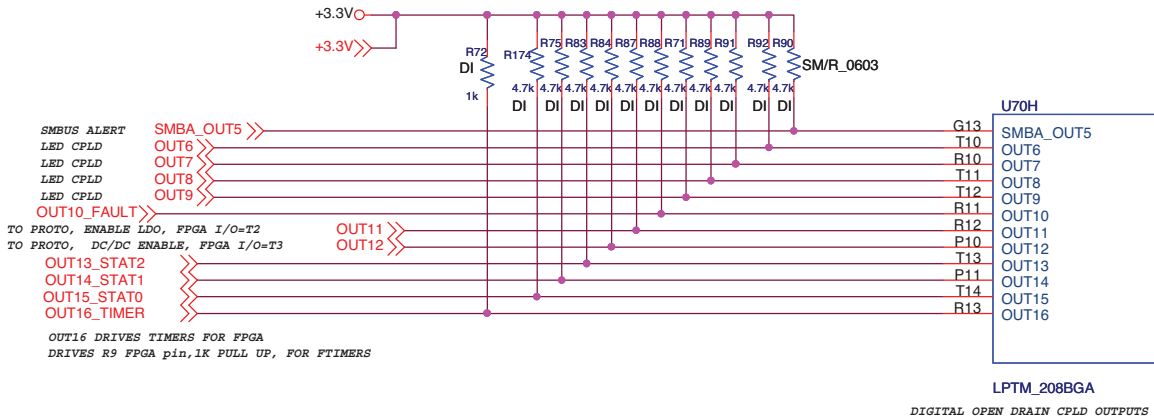
I/O Expansion Header

The Platform Manager Evaluation Board has an unpopulated 32 pin-header for access to I/O signals for the FPGA. These connections are labeled on the board. This allows users to develop custom designs and expand the I/O count for the board

Figure 6. I/O Expansion Header
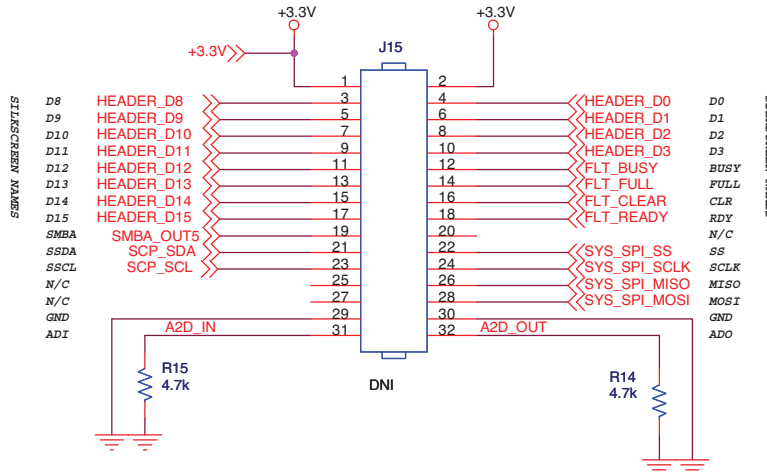
The interface has generic I/Os, SPI control signals, I²C control and fault logging signals. All of these can be set up and programmed by the user for custom I/Os.

LCD Display

The LCD provided is driven by FPGA outputs. The LCD is a set of three 7-segment displays. For more information on LCD usage, see the description of the Platform Manager Demo earlier in this document.

Figure 7. LCD Display
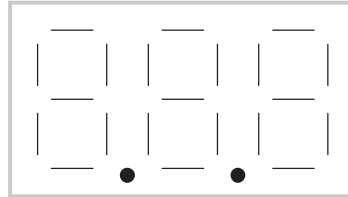
LCD NO BACKLIGHT: DRIVE WITH FPGA OUTPUTS WITH PHASE CONTROL TO LIGHT SEGMENTS

Part# LCD-S301C31TR
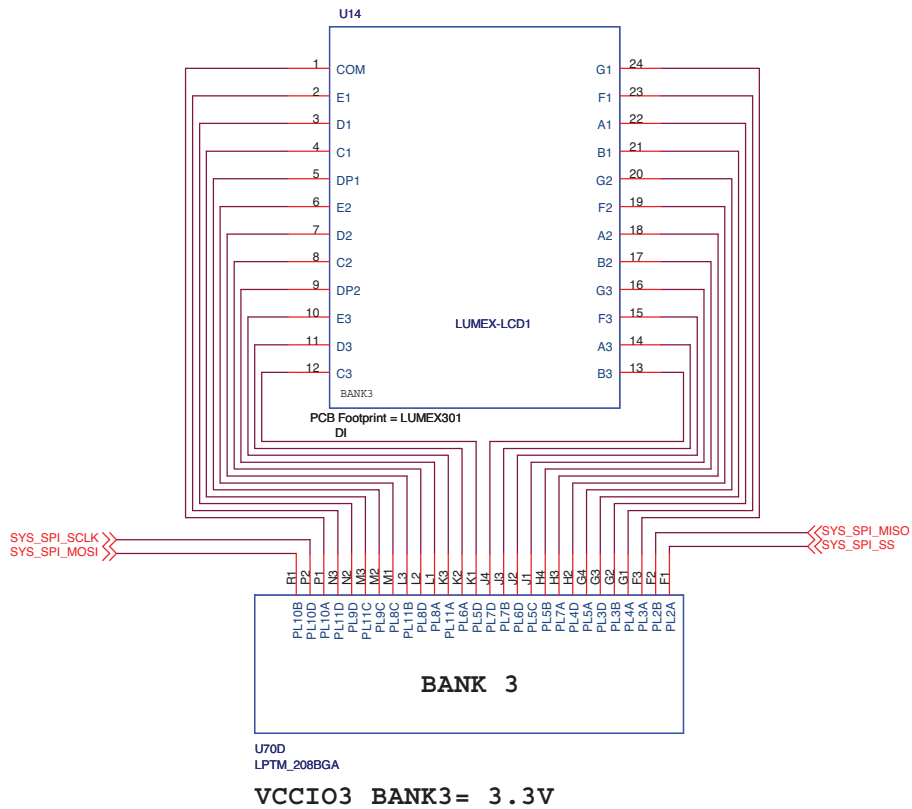
DIP Switches

The Platform Manager Evaluation Board.provides eight DIP switches that are connected to the FPGA portion of the Platform Manager device. In addition, there are four DIP switches for JTAG configuration (SW2).

Figure 8. DIP Switches
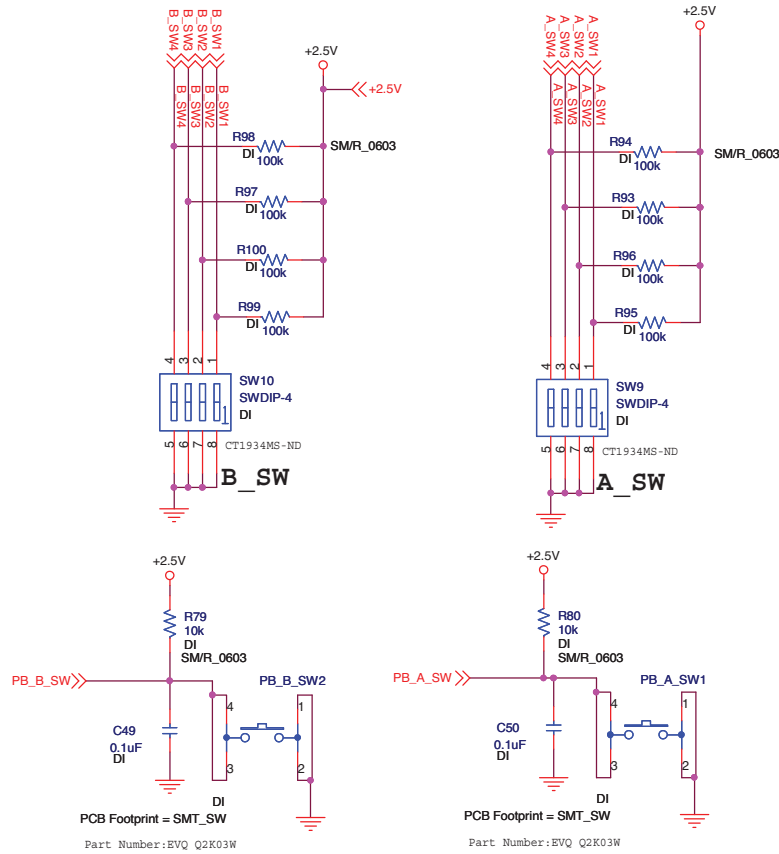
VMON Slide Potentiometers

The two potentiometers are tied to VMON8 and VMON9; these can be used to simulate a fault or to trip a comparator to turn on or off a display or power supply. The voltage on the potentiometer can also be read out from the A/D converter using the I^{2}C port.

Figure 9. VMON Slide Potentiometers
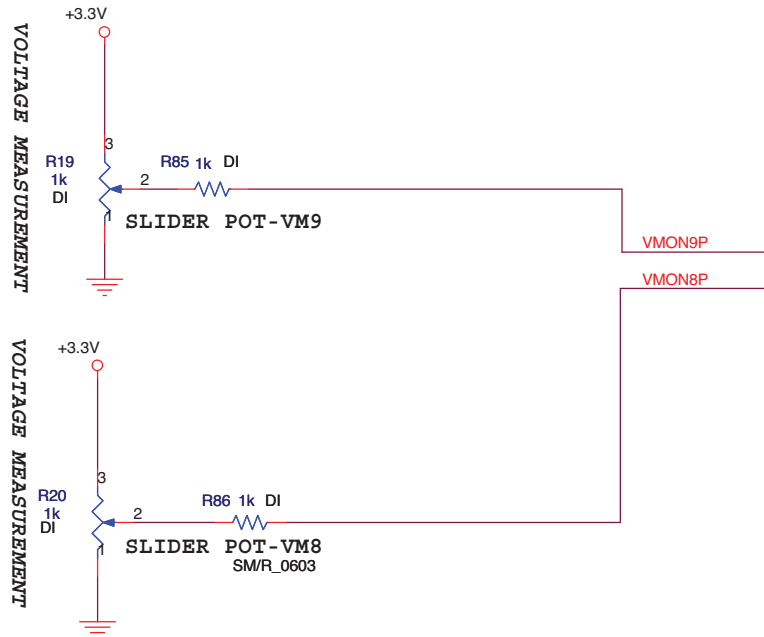
HVOUT MOSFET Ramp Circuits

HVOUTs are used for driving N-channel MOSFETs. HVOUT1 and HVOUT2 are tied to MOSFETs mounted on the evaluation board. Each HVOUT can be set for a different drive current to show voltage ramps at the source of the FET. Note that HVOUT1 can be monitored on VMON1P and HVOUT2 can be monitored on VMON2.

HVOUT3 and HVOUT4 are routed to the prototype area for off-board use.

Figure 10. HVOUT MOSFET Ramp Circuits
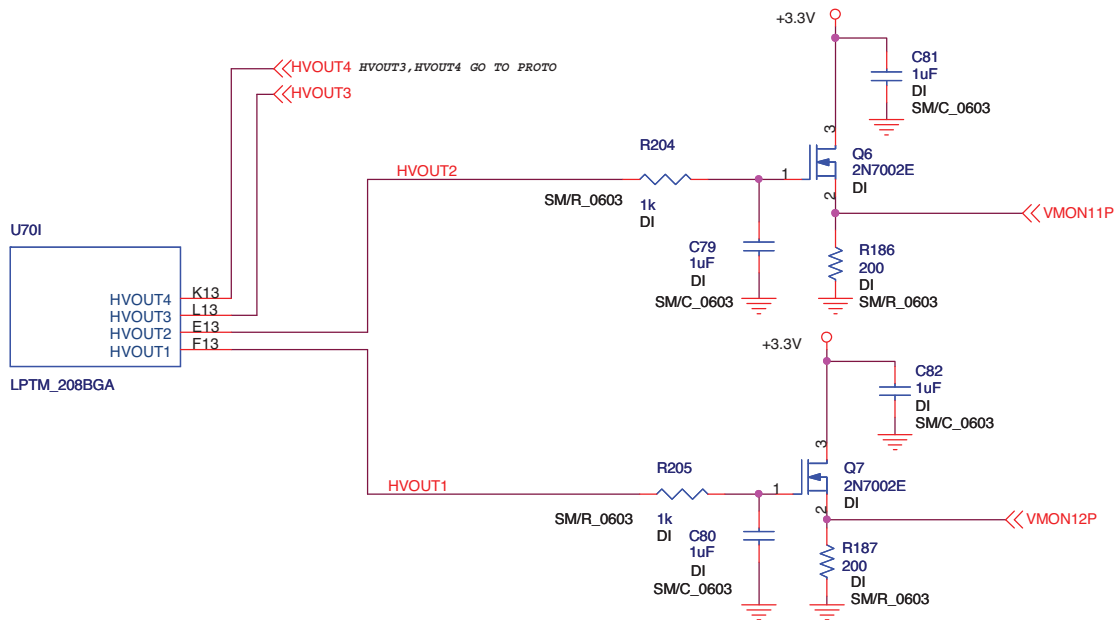
HVOUT1,HVOUT2 drivers do not sequence on board power, they
demonstrate a ramp circuit, controlled by PAC Designer
settings and visible on a scope. FETS are 250mA max!

VMON Voltage Monitor Inputs

There are 12 VMON inputs to the analog section of the device. These are routed to board power supplies, user power supplies, the temperature sensing circuits, slider pots and the prototype area. All VMONs voltages can be read out from the A/D converter using I^2C. The VMONs are described in Table 6.

Table 6. VMON Descriptions

VMON	Description
VMON1	Tied to the prototype area for off-board monitoring or trim applications.
VMON2	Tied to the prototype area for off-board monitoring or trim applications.
VMON3	Monitor for 2.5V power supply used on FPGA Bank1 VCCIO.
VMON4	Monitor for 5V power supply, main wall adapter rail.
VMON5	Voltage monitor for the user DC-DC module supply.
VMON6	Voltage monitor for the user LDO supply.
VMON7	Temperature monitor on the thermistor circuit.
VMON8	Voltage monitor on slide pot R20.
VMON9	Voltage monitor on slide pot R19.
VMON10	Monitor for main 3.3V rail.
VMON11	Voltage monitor for FET ramp circuit and Q6 MOSFET.
VMON12	Voltage monitor for FET ramp circuit and Q7 MOSFET.

Figure 11. Voltage Monitor Inputs
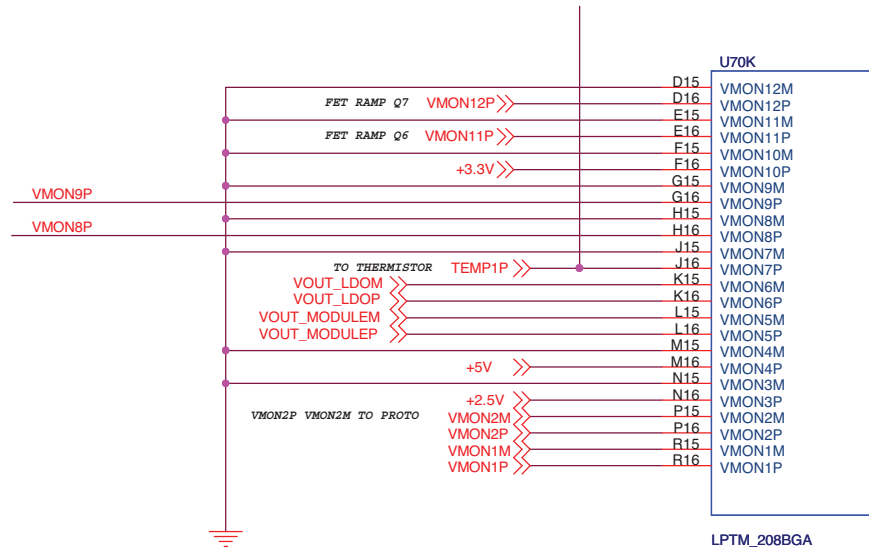
Trim DACs

The Trim DACs are used for margining and trimming power supplies. On the Platform Manager Evaluation Board, the LDO is hooked to TRIM6 and VMON6P/VMON6M. The Murata DC-DC Module is hooked to TRIM5 and VMON5P/VMON5M. These resources provide for closed loop trimming of the supply.

The demo design is set up to trim the LDO to 2.5V and the DC-DC module to 1.2V. Each supply has been biased on the board with resistors for setting the output voltage as well as the resistors required for trimming. If the user would like to select different values, the resistors in the trim network must be changed.

Figure 12. Trim DACs
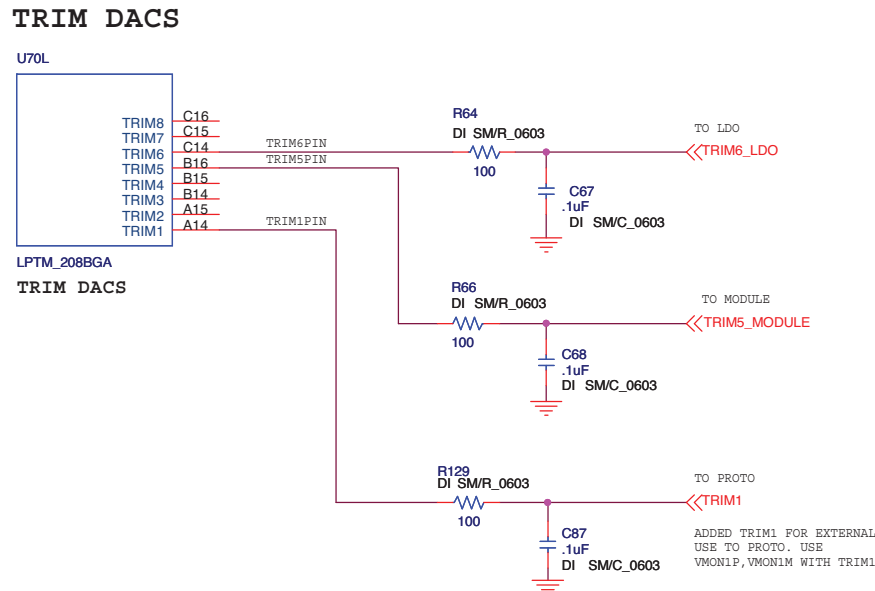
Trimming User Supplies: LDO 2.5V

The trim circuit and LDO user power supply is set up on the board to output 2.5V to the load connectors. Note that in its default configuration, there is a relatively light power load on the evaluation board. Users may add additional

loads to the green screw connectors located at J8. The load should not exceed the maximum ICC of the LDO (1.2A).

Figure 13. LDO 2.5V

Trimming DC-DC Module

The DC-DC Module (Murata OKR DC-DC Module 1.2V) is set to VOUT=1.2V. The trim network is shown connected to TRIM5_Module in Figure 14. If the user needs to program the supply at a different voltage, the resistors R110, R111, R109, R106 will need to be changed and a new DC-DC macro built within PAC-Designer.

Figure 14. DC-DC Module

Temperature Monitoring

The board has a thermistor mounted as a voltage divider circuit that is routed to VMON7. This analog input is a standard VMON. The VMONs are used as a programmable comparator, each has two programmable trip points. By setting the trip points in the software, an over-temp can be used to shut down a power supply or light an LED when a certain temperature is read. The VMON can also be set to a window comparator with a high and low trip point. The VMONs can be read out from the A/D converter using I²C.

Figure 15. Temperature Monitoring

RESET

The evaluation board has one reset push-button. This signal is routed to IN2 of the CPLD. Equations can be written in PAC-Designer for resetting the CPLD sequence. The reset is also routed to the FPGA, where it drives pin F4. Equations must be written to use these pins as a reset function. It is not a full board or chip reset unless the designer sets it up that way.

Figure 16. Reset

On-board SPI Flash Memory

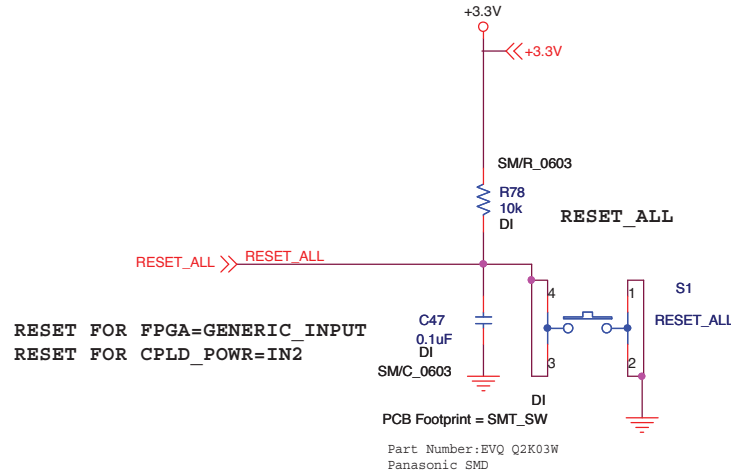The Platform Manager Evaluation Board has a 4MBit SPI Flash memory that is used to record faults in the system. Fault logging is accomplished by monitoring the VMON pins and activating an output pin when a power supply falls outside its programmed range. The VMONs have programmable trip points and support a window compare. If the voltage falls outside the window, a fault is triggered. When a fault is triggered, output pins from the CPLD write to the FPGA and are decoded to represent different fault conditions. Once the fault has occurred, the FPGA finds the next available memory page and writes out the data using SPI. The stored data is non-volatile. The board can be powered down and data read back out of the Flash using design utilities. Lattice provides software tools, reference designs and IP cores that work with the Platform Manager Development Kit or designers can use their own designs.

Figure 17. On-Board SPI Flash Memory
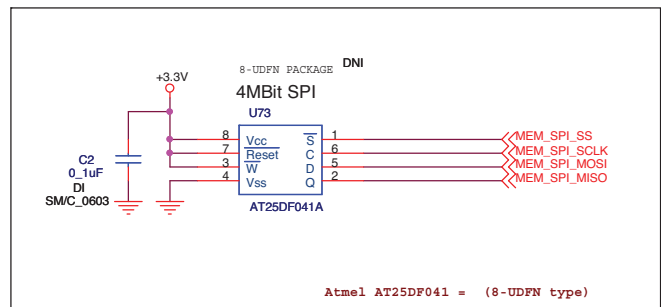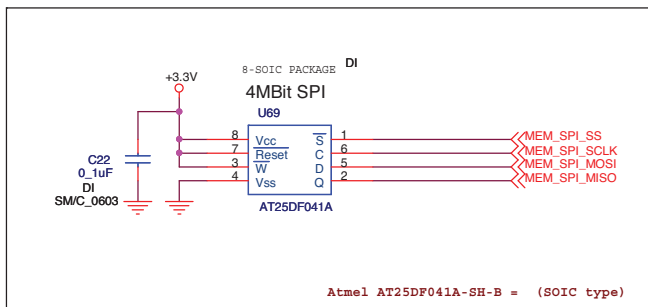
Clock Routing

Table 7. Pin Interconnection for Timers

Package	OUT16 Timer4	Route to	Bank
208-ball ftBGA	OUT16 (R13)	PB9C (R9)	Bank2

To set up additional logic and sequencers in the FPGA in PAC-Designer, the 250kHz CPLDCLK is driven externally and routed to an FPGA pin for a 250kHz clock input. Table 8 shows the connections required for the CPLDCLK, which is externally connected between the dedicated CPLDCLK output pin and an FPGA input pin.

Table 8. Pin Interconnection for CPLDCLK

Package	CPLDCLK	Route to	Bank
208-ball ftBGA	CPLDCLK (C11)	PT6B (D5)	Bank0

Table 9. Pin Interconnection for MCLK

Package	MCLK	Route to	Bank
208-ball ftBGA	MCLK (B11)	PT5B (A2)	Bank0

The 8MHz internal MCLK is also connected externally to the FPGA from the 8MHz MCLK output to an FPGA input. This clock is used for communication and I/O as well as an internal main fabric clock. The Master mode is used to enable the 8MHz internal oscillator.

Figure 18. Clock and Timer Dialog Box
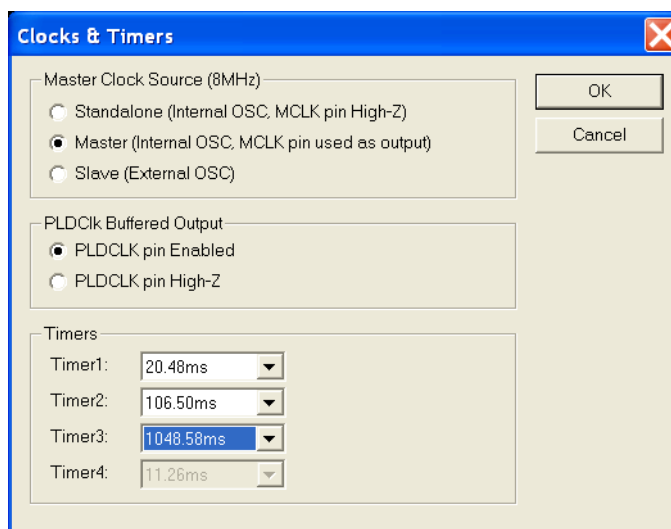
Clock Routing at the Pin

When the design is compiled, PAC-Designer processes the sequencers and synthesizes the logic to be run through fitting and JEDEC generation. These steps are taken care of automatically, once initiated. A report file and a Verilog file are saved in the directory tree structure.

Routing

When using the FPGA clocks and timers, it is important to understand the routing of the pins and the clocks required. In PAC-Designer software, the 8MHz internal clock must be set up for driving to the outside pins and connected externally from pin to pin. The 250kHz PLDCLK is also used externally.

Figure 19. External Connections for Clocks
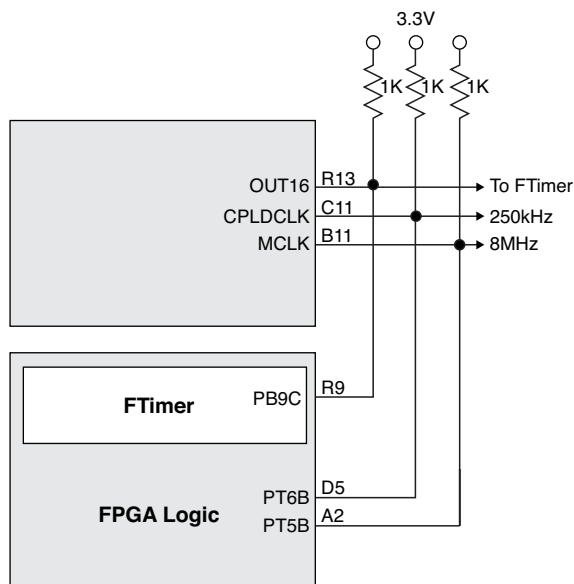
**External Connections for 208-Ball ftBGA
CPLD Logic and CLK Outputs**

Ordering Information

Description	Ordering Part Number	China RoHS Environment-Friendly Use Period (EFUP)
Platform Manager Development Kit	LPTM10-12107-DEV-EVN	

Technical Support Assistance

Hotline: 1-800-LATTICE (North America)
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Internet: www.latticesemi.com

Revision History

Date	Version	Change Summary
October 2010	01.0	Initial release.
October 2010	01.1	Added Appendix C, Configuring the ispMACH 4000 Mux for the Platform Manager Development Kit.
December 2010	01.2	Added VID Demo text section.

Appendix A. Schematic

Figure 20. Mux

FTDI USB to MULTIPLE JTAG Interface Sheet

HEADER 3
J11
DNI

HEADER 3
J12
DNI

HEADER 3
J14
DI

HEADER 3
J16
DI

USB_TDI
4KIO_TDI
4KJ_TDI

USB_TMS
4KIO_TMS
4KJ_TMS

USB_TCK
4KIO_TCK
4KJ_TCK

USB_TDO
4KIO_TDO
4KJ_TDO

+3.3V
R222
330
DI

D12
Red
SM/LED_0603
DI

+3.3V

SW2B
SW_SPST_4
DI

SW2C
SW_SPST_4
DI

SW2D
SW_SPST_4
DI

USB_6MHZ

+3.3V

C64 0.1uF DI SM/C_0603
C65 0.1uF DI SM/C_0603
C69 0.1uF DI SM/C_0603
C71 0.1uF DI SM/C_0603

+3.3V
SM/C_0603

U2
LC4032/4064-T44

VCC VCC VCCO1 VCCO0

BANK0_0 2
BANK0_1 3
BANK0_2 4
BANK0_3 7
BANK0_4 8
BANK0_5 9
BANK0_6 13
BANK0_7 14
BANK0_8 15
BANK0_9 16
BANK0_10 41
BANK0_11 42
BANK0_12 43
BANK0_13 44
GOE0/BANK0_14 40
CLK0/I 39

4KIO_TCK
4KIO_TMS
4KIO_TDI
4KIO_TDO

USB_GPIO_L0
USB_GPIO_L1
USB_GPIO_L2
USB_GPIO_L3

USB_GPIO_H0
USB_GPIO_H1

JTAG_SEL_0
JTAG_SEL_1
JTAG_SEL_2

BANK1_0 18
BANK1_1 19
BANK1_2 20
BANK1_3 21
BANK1_4 22
BANK1_5 24
BANK1_6 25
BANK1_7 26
BANK1_8 29
BANK1_9 30
BANK1_10 31
BANK1_11 35
BANK1_12 36
BANK1_13 37
GOE1/BANK1_14 38
CLK2/I 17

PM_TCK
PM_TMS
PM_TDI
PM_TDO

SYS_SPI_SCLK
SYS_SPI_MOSI
SYS_SPI_SS
SYS_SPI_MISO

FLT_READY
FLT_CLEAR
FLT_FULL
FLT_BUSY

SCP_SCL
SCP_SDA

GND GND GND
TDI TDO TMS TCK

U2
DI

Lattice Number:LC4064V-5TN44C

SW2A
SW_SPST_4
DI

+3.3V   +3.3V
R2 4.7K DI   R1 4.7K DI

0

4KJ_TDI
4KJ_TDO
4KJ_TMS
4KJ_TCK

JTAG_SEL	MODE
0 0 0	JTAG
0 0 1	SPI
0 1 0	I2C
0 1 1	
1 0 0	
1 0 1	
1 1 0	
1 1 1	

J1
1 +3.3V
2 4KIO_TDO
3 4KIO_TDI
4 N/C
5 PLUG
6 4KIO_TMS
7
8 4KIO_TCK

DNI   8 HEADER
Optional JTAG header for straight through 1x8 no USB

Lattice Semiconductor Applications
Email: techsupport@Latticesemi.com
Phone (503) 268-8001 -or- (800) LATTICE

Title: A_MUX
Size B   Project: LPTM10-12107-DEV-EVN
Schematic Rev C
Board Rev C
Date: Aug23 2010
Sheet 1 of 15

Figure 21. Bank0, Bank3

Figure 22. LPTM10-12107-DEC-EVN

RAIL1=LDO

RAIL1=DC/DC MODULE

U11_OUT

VOUT_LDOP

U71_OUT

VOUT_MODULEP

U13
VIN+   VIN-

INA197

TP6
V1_ICC

V+   GND   OUT

DNI

+3.3V

+3.3V

C66
DI   0.1uF
SM/C_0402

U15
VIN+   VIN-

INA197

TP8
V2_ICC

V+   GND   OUT

DNI

+3.3V

+3.3V

C70
DI   0.1uF
SM/C_0402

OP AMPS not populated

Title
CURRENT_SENSE

Size B	Project LPTM10-12107-DEV-EVN		Schematic Rev C
			Board Rev C
Date: Aug 23 2010		Sheet 3 of 15	

Figure 23. Headers Logo

XO-MINI Board Header PIN-OUT

J15

+3.3V

+3.3V

+3.3V

SILKSCREEN NAMES				SILKSCREEN NAMES
D8	HEADER_D8	1	2	HEADER_D0	D0
D9	HEADER_D9	3	4	HEADER_D1	D1
D10	HEADER_D10	5	6	HEADER_D2	D2
D11	HEADER_D11	7	8	HEADER_D3	D3
D12	HEADER_D12	9	10	FLT_BUSY	BUSY
D13	HEADER_D13	11	12	FLT_FULL	FULL
D14	HEADER_D14	13	14	FLT_CLEAR	CLR
D15	HEADER_D15	15	16	FLT_READY	RDY
SMBA	SMBA_OUT5	17	18		N/C
SSDA	SCP_SDA	19	20	SYS_SPI_SS	SS
SSCL	SCP_SCL	21	22	SYS_SPI_SCLK	SCLK
N/C		23	24	SYS_SPI_MISO	MISO
N/C		25	26	SYS_SPI_MOSI	MOSI
GND		27	28		GND
ADI	A2D_IN	29	30	A2D_OUT	ADO
		31	32		

DNI

R15
4.7k

R14
4.7k

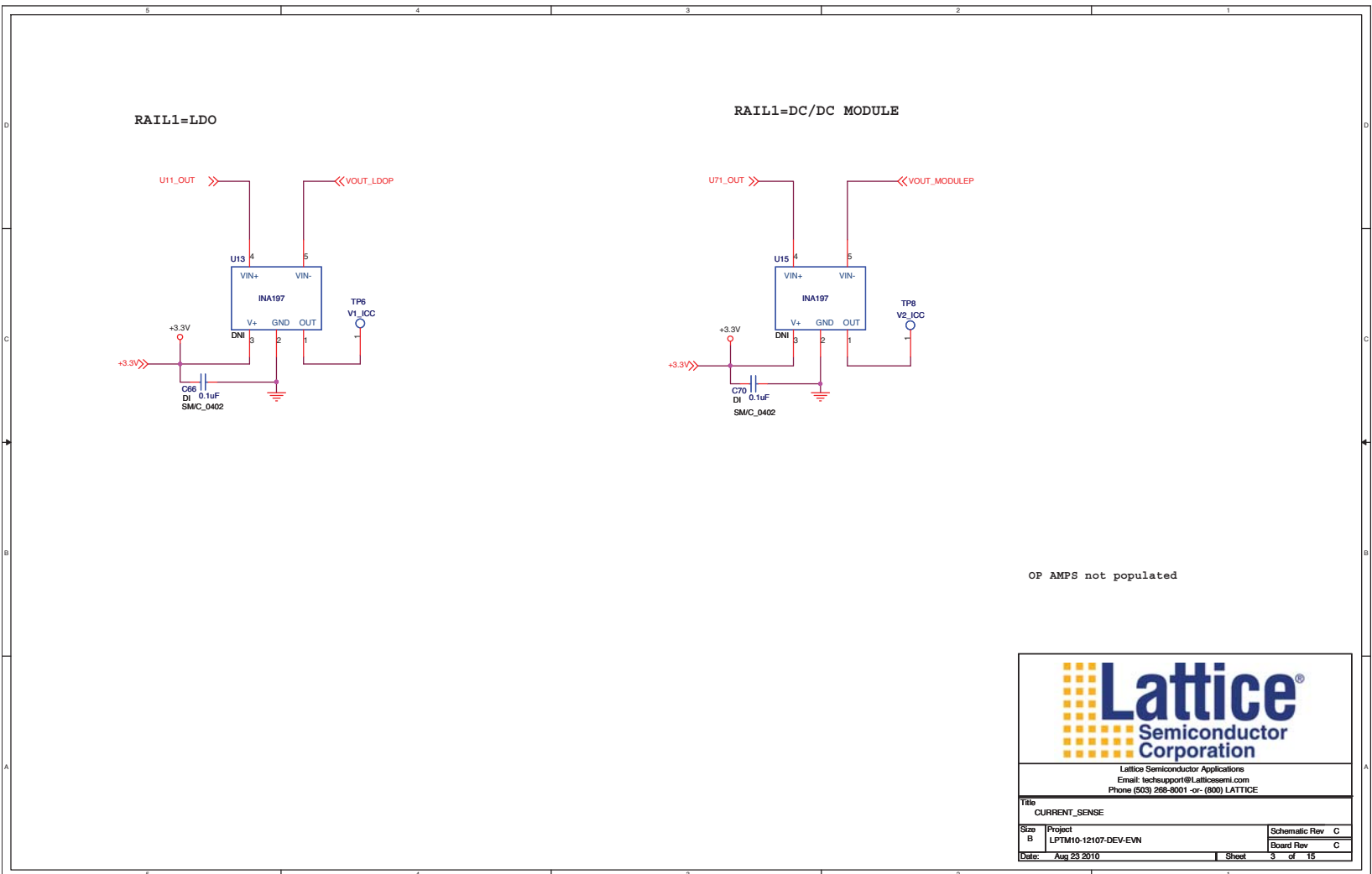| G1	G2	G3	G4
Lattice Logo	WEEE	E-Friendly	CE Mark

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Title
HEADERS_LOGO

Size	Project		Schematic Rev	C
B	LPTM10-12107-DEV-EVN		Board Rev	C

Date: Aug 23 2010 | Sheet 4 of 15