Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

Platform Manager

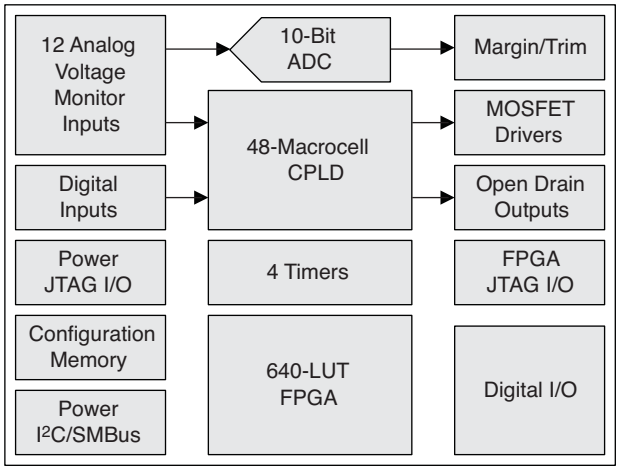
In-System Programmable Power and Digital Board Management

February 2012 Data Sheet DS1036

Features

- **Precision Voltage Monitoring Increases Reliability**
  - 12 independent analog monitor inputs
  - Differential inputs for remote ground sense
  - Two programmable threshold comparators per analog input
  - Hardware window comparison
  - 10-bit ADC for I^2C monitoring
- **High-Voltage FET Drivers Enable Integration**
  - Power supply ramp up/down control
  - Programmable current and voltage output
  - Independently configurable for FET control or digital output
- **Power Supply Margin and Trim Functions**
  - Trim and margin up to eight power supplies
  - Dynamic voltage control through I^2C
  - Independent Digital Closed-Loop Trim function for each output
- **Programmable Timers Increase Control Flexibility**
  - Four independent timers
  - 32 µs to 2 second intervals for timing sequences
- **PLD Resources Integrate Power and Digital Functions**
  - 48-macrocell CPLD
  - 640 LUT4s FPGA
  - Up to 107 digital I/Os
  - Up to 6.1 Kbits distributed RAM
- **Programmable sysIO™ Buffer Supports a Range of Interfaces**
  - LVCMOS 3.3/2.5/1.8/1.5/1.2
  - LVTTL
- **System-Level Support**
  - Single 3.3V supply operation
  - Industrial temperature range: -40°C to +85°C
- **In-System Programmability Reduces Risk**
  - Integrated non-volatile configuration memory
  - JTAG programming interface
- **Package Options**
  - 128-pin TQFP
  - 208-ball ftBGA
  - RoHS compliant and halogen-free

Block Diagram



Description

The Lattice Platform Manager integrates board power management (hot-swap, sequencing, monitoring, reset generation, trimming and margining) and digital board management functions (reset tree, non-volatile error logging, glue logic, board digital signal monitoring and control, system bus interface, etc.) into a single integrated solution.

The Platform Manager device provides 12 independent analog input channels to monitor up to 12 power supply test points. Up to 12 of these input channels can be monitored through differential inputs to support remote ground sensing. Each of the analog input channels is monitored through two independently programmable comparators to support both high/low and in-bounds/out-of-bounds (window-compare) monitor functions. Up to six general purpose 5V tolerant digital inputs are also provided for miscellaneous control functions.

There are 16 open-drain digital outputs that can be used for controlling DC-DC converters, low-drop-out regulators (LDOs) and opto-couplers, as well as for supervisory and general purpose logic interface functions. Four of these outputs (HVOUT1-HVOUT4) may be configured as high-voltage MOSFET drivers. In high-voltage mode these outputs can provide up to 12V for driving the gates of n-channel MOSFETs so that they can be used as high-side power switches controlling the supplies with a programmable ramp rate for both ramp up and ramp down.

The board power management function can be implemented using an internal 48-macrocell CPLD. The status of all of the comparators on the analog input channels as well as the general purpose digital inputs are used as inputs by the CPLD array, and all digital outputs (open-drain as well as HVOUT) may be controlled by the CPLD.

Four independently programmable timers can create delays and time-outs ranging from 32 μs to 2 seconds.

The Platform Manager device incorporates up to eight DACs for generating trimming voltage to control the output voltage of a DC-DC converter. Additionally, each power supply output voltage can be maintained typically within 0.5% tolerance across various load conditions using the Digital Closed Loop Control mode.

The internal 10-bit A/D converter can both be used to monitor the VMON voltage through the I^2C bus as well as for implementing digital closed loop mode for maintaining the output voltage of all power supplies controlled by the monitoring and trimming section of the Platform Manager device.

The FPGA section of the Platform Manager is optimized to meet the requirements of board management functions including reset distribution, boundary scan management, fault logging, FPGA load control, and system bus interface. The FPGA section uses look-up tables (LUTs) and distributed memories for flexible and efficient logic implementation. This instant-on capability enables the Platform Manager devices to integrate control functions that are required as soon as power is applied to the board.

Power management functions can be integrated into the CPLD and digital board management functions can be integrated into the FPGA using the LogiBuilder tool provided by PAC-Designer® software. In addition, the FPGA designs can also be implemented in VHDL or Verilog HDL through the ispLEVER® software design tool.

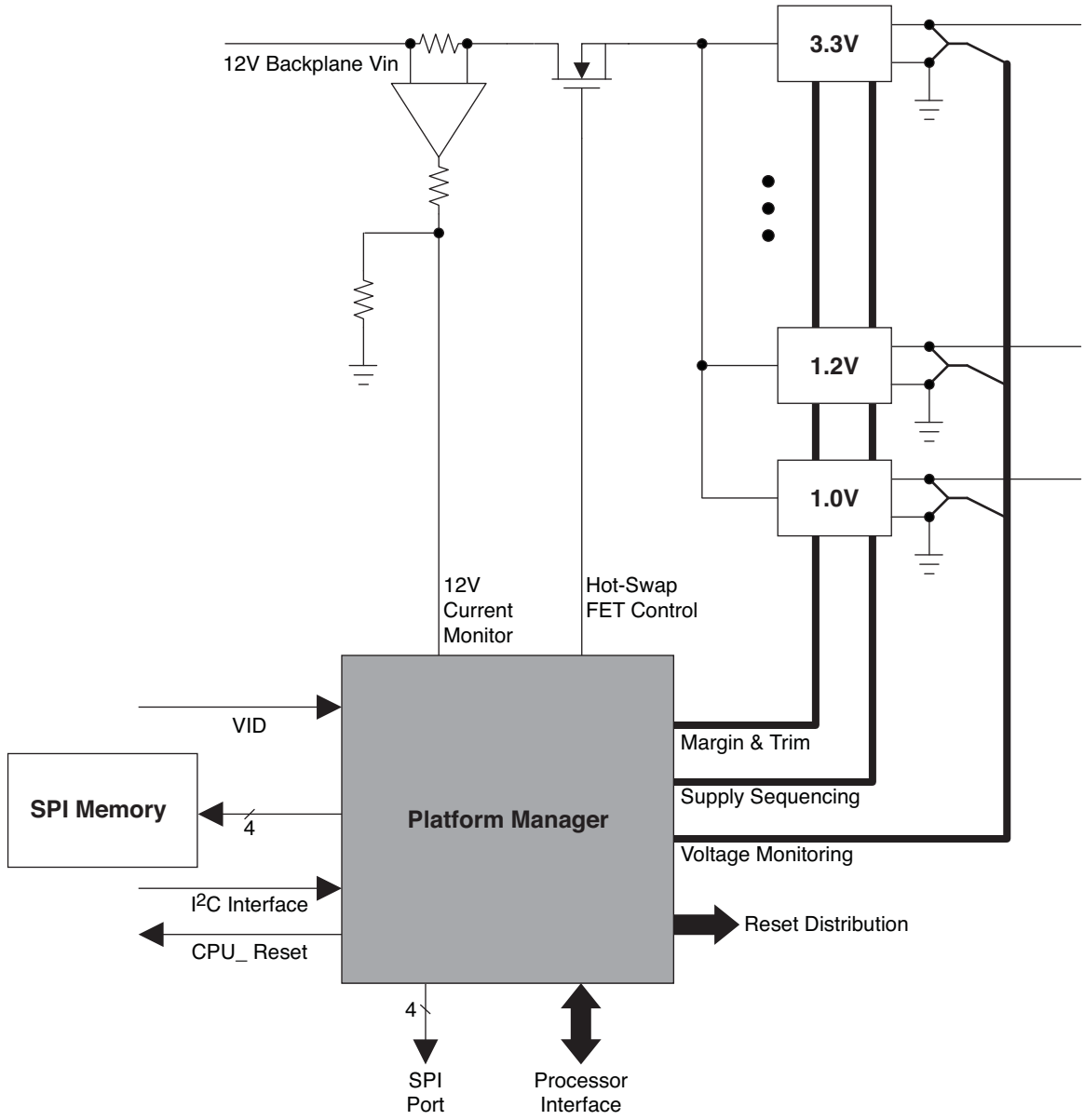
The Platform Manager IC supports a hardware I^2C/SMBus slave interface that can be used to measure voltages through the Analog to Digital Converter or is used for trimming and margining using a microcontroller.

There are two JTAG ports integrated into the Platform Manager device: Power JTAG and FPGA JTAG. The Power JTAG interface is used to program the power section of the Platform Manager and the FPGA JTAG is used to configure the FPGA portion of the device. The FPGA configuration memory can be changed in-system without interrupting the operation of the board management section. However, the Power Management section of the platform Manager cannot be changed without interrupting the power management operation.

Table 1. Platform Manager Family Selection Table

Parameter	LPTM10-1247	LPTM10-12107
Analog Inputs	12	12
Margin and Trim	6	8
Total I/O	47	107
CPLD Macrocells	48	48
FPGA LUTs	640	640
Package	128-pin TQFP	208-ball ftBGA

Figure 1. Typical Platform Manager Application



Note: See reference design, IP documentation and application notes for more information on implementation of individual functions called out above.

Absolute Maximum Ratings[1, 2, 3]

Power Management Core Supply P_{VCCD} . . . . . -0.5 to 4.5V

Power Management Analog Supply P_{VCCA} . . . . . -0.5 to 4.5V

Power Management Digital Input Supply P_{VCCA} (IN[1:4]) P_{VCCINP} . . . . . -0.5 to 6V

Power Management JTAG Logic Supply P_{VCCJ} . . . . . -0.5 to 6V

Power Management Alternate E^2 programming supply APS[4] . . . . . -0.5 to 4V

Power Management Digital Input Voltage (All Digital I/O Pins) V_{IN} . . . . . -0.5 to 6V

VMON Input Voltage . . . . . -0.5 to 6V

VMON Input Voltage Ground Sense . . . . . -0.5 to 6V

Voltage Applied to Power Management Tri-stated Pins (HVOUT[1:4]) . . . . . -0.5 to 13.3V

Voltage Applied to Power Management Tri-stated Pins (OUT[5:16]) . . . . . -0.5 to 6V

Maximum Sink Current on Any Power Management Output . . . . . .23 mA

FPGA Supply Voltage V_{CC} . . . . . -0.5 to 3.75V

FPGA Supply Voltage V_{CCAUX} . . . . . -0.5 to 3.75V

FPGA Output Supply Voltage V_{CCIO} . . . . . -0.5 to 3.75V

FPGA I/O Tri-state Voltage Applied[5] . . . . . -0.5 to 3.75V

FPGA Dedicated Input Voltage Applied[5] . . . . . -0.5 to 4.25V

Device Storage Temperature . . . . . -65 to +150°C

Junction Temperature T_J . . . . . +125°C

1. Stress above those listed under the “Absolute Maximum Ratings” may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.
2. Compliance with the Lattice Thermal Management document is required.
3. All voltages referenced to GND (FPGA section) or GNDA/D (Power sections).
4. The APS pin MUST be left floating when PVCCD and PVCCA are powered.
5. Overshoot and undershoot of -2V to (V_{IHMAX} + 2) volts is permitted for a duration of <20 ns.

Recommended Operating Conditions

Symbol	Parameter	Conditions	Min.	Max.	Units
P_{VCCD}, P_{VCCA}[1]	Core supply voltage at pin		2.8	3.96	V
P_{VCCINP}	Digital input supply for IN[1:4] at pin		2.25	5.5	V
P_{VCCJ}	JTAG logic supply voltage at pin		2.25	3.6	V
APS	Alternate E^2 programming supply at pin	P_{VCCD} and P_{VCCA} powered	No Connect Must Be Left Floating		
		P_{VCCD} and P_{VCCA} not powered	3.0	3.6	V
V_{IN}	Input voltage at digital input pins		-0.3	5.5	V
V_{MON}	Input voltage at V_{MON} pins		-0.3	5.9	V
V_{MONGS}	Input voltage at V_{MONGS} pins		-0.2	0.3	V
V_{OUT}	Open-drain output voltage	OUT[5:16] pins	-0.3	5.5	V
		HVOUT[1:4] pins in open-drain mode	-0.3	13.0	V
V_{CC}[2]	FPGA Core Supply Voltage		3.135	3.465	V
V_{CCAUX}[2]	FPGA Auxiliary Supply Voltage		3.135	3.465	V
V_{CCIO}[3]	FPGA I/O Driver Supply Voltage	V_{CCIO0}, V_{CCIO1}, V_{CCIO3}	1.14	3.465	V
		V_{CCIO2}	2.25	3.6	V
t_{JCOM}	Junction Temperature Commercial Operation	Power applied	0	+85	°C
t_{JIND}	Junction Temperature Industrial Operation	Power applied	-40	+100	°C
$t_{JFLASHCOM}$	Junction Temperature, Flash Programming, Commercial		0	+85	°C
$t_{JFLASHIND}$	Junction Temperature, Flash Programming, Industrial		-40	+100	°C

1. P_{VCCD} and P_{VCCA} must always be tied together.
2. V_{CC} and V_{CCAUX} must always be tied together. Also, like power supplies must be tied together. For example, if V_{CCIO} and V_{CC} are both 3.3V, they must also be the same supply.
3. See recommended voltages by I/O standard in subsequent table.

Digital I/O Hot Socketing Specifications[1, 2, 3]

Symbol	Parameter	Condition	Min.	Typ.	Max	Units
I_{DK}	Input or I/O leakage Current	$0 \le V_{IN} \le V_{IH}$ (MAX)	—	—	+/-1000	µA

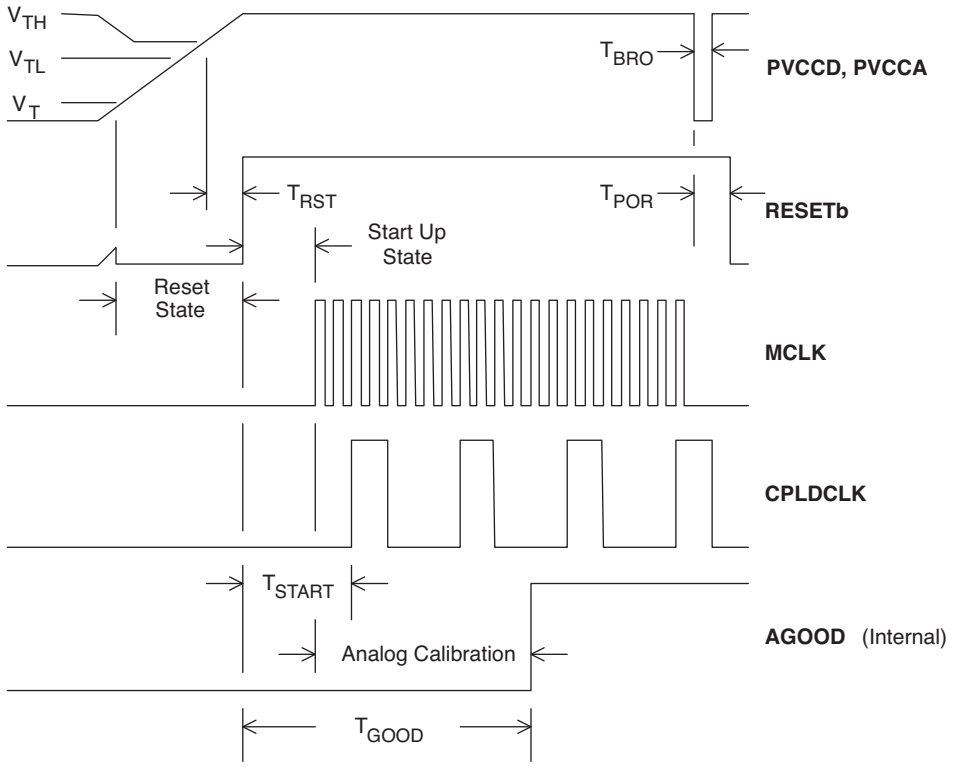
1. Assumes monotonic rise/fall rates for V_{CC}, V_{CCAUX}, and V_{CCIO}.
2. $0 \le V_{CC} \le V_{CC}$ (MAX), $0 \le V_{CCIO} \le V_{CCIO}$ (MAX) and $0 \le V_{CCAUX} \le V_{CCAUX}$ (MAX).
3. I_{DK} is additive to I_{PU}, I_{PD} or I_{BH}.

Power-On Reset – Power Management Section

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
T_{RST}	Delay from V_{TH} to start-up state				100	µs
T_{START}	Delay from RESETb HIGH to CPLDCLK rising edge			5	10	µs
T_{GOOD}	Power-on reset to valid VMON comparator output and AGOOD is true				2.5	ms
T_{BRO}	Minimum duration brown out required to trigger RESETb		1		5	µs
T_{POR}	Delay from brown out to reset state.				13	µs
V_{TL}	Threshold below which RESETb is LOW[1]				2.3	V
V_{TH}	Threshold above which RESETb is HIGH[1]		2.7			V
V_T	Threshold above which RESETb is valid[1]		0.8			V
C_L	Capacitive load on RESETb for master/slave operation				200	pF

1. Corresponds to PVCCA and PVCCD supply voltages.

Figure 2. Power Management Section Power-On Reset



ESD Performance

Pin Group	ESD Stress	Min.	Units
All pins	HBM	1500	V
	CDM	1000	V

DC Electrical Characteristics[1, 2, 3, 4]

Symbol	Parameter	Conditions	Typ.[5]	Max.	Units
P_{ICC}	Power Management section supply current	Normal operation		40	mA
P_{ICCINP}	Power Management section supply current	Normal operation		5	mA
P_{ICCJ}	Power Management section supply current	Normal operation		1	mA
I_{CC}[1]	FPGA Core Power Supply		8.7		mA
I_{CCAUX}	FPGA Auxiliary Power Supply V_{CCAUX} = 3.3V	During initialization (0MHz)	7		mA
I_{CCIO}	FPGA Bank Power Supply[6]	During initialization (0MHz)	2.4		mA

1. For further information on FPGA section supply current, please see details of additional technical documentation at the end of this data sheet.
2. Assumes all FPGA section I/O pins are held at V_{CCIO} or GND.
3. FPGA Frequency = 0 MHz.
4. Typical FPGA user pattern.
5. TJ = 25°C, power supplies at nominal voltage.
6. Per bank, V_{CCIO} = 2.5V. Does not include pull-up/pull-down.

FPGA Supply Current (Sleep Mode)[1, 2]

Symbol	Parameter	Conditions	Typ.[3]	Max.	Units
I_{CC}[1]	FPGA Core Power Supply	Sleep Mode	12	25	µA
I_{CCAUX}	FPGA Auxiliary Power Supply		1	25	µA
I_{CCIO}	Bank Power Supply[4]		2	30	µA

1. Assumes all inputs are configured as LVCMOS and held at the VCCIO or GND.
2. Frequency = 0MHz.
3. T_A = 25°C, power supplies at nominal voltage.
4. Per bank.

DC Electrical Characteristics – FPGA General Purpose I/O

Over Recommended Operating Conditions

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
I_{IL}, I_{IH}[1, 4]	Input or I/O Leakage	$0 \le V_{IN} \le (V_{CCIO} - 0.2V)$	—	—	10	µA
		$(V_{CCIO} - 0.2V) < V_{IN} \le 3.6V$	—	—	40	µA
I_{PU}	I/O Active Pull-up Current	$0 \le V_{IN} \le 0.7\ V_{CCIO}$	-30	—	-150	µA
I_{PD}	I/O Active Pull-down Current	V_{IL} (MAX) $\le V_{IN} \le V_{IH}$ (MAX)	30	—	150	µA
I_{BHLS}	Bus Hold Low sustaining current	$V_{IN} = V_{IL}$ (MAX)	30	—	—	µA
I_{BHHS}	Bus Hold High sustaining current	$V_{IN} = 0.7V_{CCIO}$	-30	—	—	µA
I_{BHLO}	Bus Hold Low Overdrive current	$0 \le V_{IN} \le V_{IH}$ (MAX)	—	—	150	µA
I_{BHHO}	Bus Hold High Overdrive current	$0 \le V_{IN} \le V_{IH}$ (MAX)	—	—	-150	µA
V_{BHT}[3]	Bus Hold trip Points	$0 \le V_{IN} \le V_{IH}$ (MAX)	V_{IL} (MAX)	—	V_{IH} (MIN)	V
C1	I/O Capacitance[2]	V_{CCIO} = 3.3V, 2.5V, 1.8V, 1.5V, 1.2V, V_{CC} = Typ., V_{IO} = 0 to V_{IH} (MAX)	—	8	—	pf
C2	Dedicated Input Capacitance[2]	V_{CCIO} = 3.3V, 2.5V, 1.8V, 1.5V, 1.2V, V_{CC} = Typ., V_{IO} = 0 to V_{IH} (MAX)	—	8	—	pf

1. Input or I/O leakage current is measured with the pin configured as an input or as an I/O with the output driver tri-stated. It is not measured with the output driver active. Bus maintenance circuits are disabled.
2. T_A 25°C, f = 1.0MHz
3. Please refer to V_{IL} and V_{IH} in the sysIO Single-Ended DC Electrical Characteristics table of this document.
4. When V_{IH} is higher than V_{CCIO}, a transient current typically of 30ns in duration or less with a peak current of 6mA can occur on the high-to-low transition.

Programming and Erase Supply Current[1, 2, 3, 4]

Symbol	Parameter	Typ.[5]	Max.	Units
I_{APS}	Power Management $P_{VCCA/D}$ Programming Current		40	mA
I_{CC}	FPGA Core Power Supply	11		mA
I_{CCAUX}	FPGA Auxiliary Power Supply V_{CCAUX} = 3.3V	10		mA
I_{CCIO}	FPGA Bank Power Supply[6]	2		mA

1. For further information on supply current, please see details of additional technical documentation at the end of this data sheet.
2. Assumes all I/O pins are held at V_{CCIO} or GND.
3. Typical user pattern.
4. JTAG programming is at 25 MHz.
5. T_J = 25°C, power supplies at nominal voltage.
6. Per bank. V_{CCIO} = 2.5V. Does not include pull-up/pull-down.

Voltage Monitors

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
R_{IN}	Input resistance		55	65	75	kΩ
C_{IN}	Input capacitance			8		pF
V_{MON} Range	Programmable trip-point range		0.075		5.734	V
V_Z Sense	Near-ground sense threshold		70	75	80	mV
V_{MON} Accuracy	Absolute accuracy of any trip-point[1]			0.2	0.7	%
	Single-ended V_{MON} pins[2, 3]			0.3	0.9	%
HYST	Hysteresis of any trip-point (relative to setting)			1		%
CMR	Common mode rejection			60		dB
t_{PD16}	Propagation delay input to output glitch filter OFF			16		µs
t_{PD64}	Propagation delay input to output glitch filter ON			64		µs

1. Guaranteed by characterization across P_{VCCA} range, operating temperature, process.
2. Single-ended V_{MON} inputs in 128-pin TQFP package only. Single-ended V_{MON} input pins include: 59 (V_{MON1}), 83 (V_{MON9}), 84 (V_{MON10}), 86 (V_{MON11}), 88 (V_{MON12}).
3. No adjacent digital I/O pin switching noise as described in the following table for single-ended V_{MON} trip point error.

Single-Ended Voltage Monitor Trip Point Error[1]

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{MON} Error SE	Single-ended trip point error (with adjacent switching noise)[2]	Pins 85, 87, 89 F_{SWITCH} = 10MHz		2		mV
	Single-ended trip point error (no adjacent switching noise)[2]	Pins 85, 87, 89 F_{SWITCH} = 0Hz; All other digital I/O = 10MHz		1		mV

1. Single-ended V_{MON} inputs in 128-pin TQFP package only. Affected single-ended V_{MON} input pins only include: 83 (V_{MON9}), 84 (V_{MON10}), 86 (V_{MON11}), and 88 (V_{MON12}). Single-ended Vmon input pin 59 (V_{MON1}) is not affected by adjacent switching noise.
2. Defined as TQFP package option adjacent digital I/O pins 85 (PR4B), 87 (PR3D) and 89 (PR2D) configured as outputs switching (F_{SWITCH}) at 10MHz into a 33pF load capacitance.

High Voltage FET Drivers

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{PP}	Gate driver output voltage	12V setting	11.5	12	12.5	V
		10V setting	9.6	10	10.4	
		8V setting	7.7	8	8.3	
		6V setting	5.8	6	6.2	
I_{OUTSRC}	Gate driver source current (HIGH state)	Four settings in software		12.5		µA
				25		
				50		
				100		
$I_{OUTSINK}$	Gate driver sink current (LOW state)	FAST OFF mode	2000	3000		µA
		Controlled ramp settings		100		
				250		
				500		

Margin/Trim DAC Output Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
	Resolution			8 (7+sign)		Bits
FSR	Full scale range			+/-320		mV
LSB	LSB step size			2.5		mV
I_{OUT}	Output source/sink current		-200		200	µA
BPZ	Bipolar zero output voltage (code=80h)	Offset 1		0.6		V
		Offset 2		0.8		
		Offset 3		1.0		
		Offset 4		1.25		
TS	TrimCell output voltage settling time[1]	DAC code changed from 80H to FFH or 80H to 00H			2.5	ms
		Single DAC code change		256		µs
C_LOAD	Maximum load capacitance				50	pF
$T_{UPDATEM}$	Update time through I^2C port[2]	MCLK = 8 MHz		260		µs
TOSE	Total open loop supply voltage error[3]	Full scale DAC corresponds to ±5% supply voltage variation	-1%		+1%	V/V

1. To 1% of set value with 50pf load connected to trim pins.
2. Total time required to update a single TRIMx output value by setting the associated DAC through the I^2C port.
3. This is the total resultant error in the trimmed power supply output voltage referred to any DAC code due to the DAC's INL, DNL, gain, output impedance, offset error and bipolar offset error across the industrial temperature range and the Platform Manager operating P_{VCCA} and P_{VCCD} ranges.

ADC Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
	ADC Resolution			10		Bits
$T_{CONVERT}$	Conversion Time	Time from I^2C Request			200	µs
V_{IN}	Input range Full Scale	Programmable Attenuator = 1	0		2.048	V
		Programmable Attenuator = 3	0		5.9[1]	V
ADC Step Size	LSB	Programmable Attenuator = 1		2		mV
		Programmable Attenuator = 3		6		mV
Eattenuator	Error Due to Attenuator	Programmable Attenuator = 3		+/- 0.1		%

1. Maximum voltage is limited by V_{MONX} pin (theoretical maximum is 6.144V).

ADC Error Budget Across Entire Operating Temperature Range

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
TADC Error	Total Measurement Error at Any Voltage (Differential Analog Inputs)[1]	Measurement Range 600 mV - 2.048V, VMONxGS > -100mV, Attenuator =1	-8	+/-4	8	mV
		Measurement Range 600 mV - 2.048V, VMONxGS > -200mV, Attenuator =1		+/-6		mV
		Measurement Range 0 - 2.048V, VMONxGS > -200mV, Attenuator =1		+/-10		mV
	Total Measurement Error at Any Voltage (Single-Ended Analog Inputs)[2]	Measurement Range 600 mV - 2.048V, Attenuator =1	-8	+/-4	8	mV

1. Total error, guaranteed by characterization, includes INL, DNL, Gain, Offset, and PSR specifications of the ADC.
2. Single-ended V_{MON} inputs in 128-pin TQFP package only. Single-ended Vmon input pins include: 59 (VMON1), 83 (VMON9), 84 (VMON10), 86 (VMON11), 88 (VMON12).

Digital Specifications – Power Management Section Dedicated Inputs

Over Recommended Operating Conditions

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
I_{IL},I_{IH}	Input leakage, no pull-up/pull-down				+/-10	µA
I_{PU}	Input pull-up current (PTMS, PTDI, PTDISEL, PATDI, MCLK)			70		µA
V_{IL}	Voltage input, logic low[1]	PTDI, PTMS, PATDI, PTDISEL, 3.3V supply			0.8	V
		PTDI, PTMS, PATDI, PTDISEL, 2.5V supply			0.7	
		SCL, SDA			30% P_{VCCD}	
		IN[1:4]			30% P_{VCCINP}	
V_{IH}	Voltage input, logic high[1]	PTDI, PTMS, PATDI, PTDISEL, 3.3V supply	2.0			V
		PTDI,P TMS, PATDI, PTDISEL, 2.5V supply	1.7			
		SCL, SDA	70% P_{VCCD}		P_{VCCD}	
		IN[1:4]	70% P_{VCCINP}		P_{VCCINP}	

1. SCL, SDA referenced to P_{VCCD}; IN[1:4] referenced to P_{VCCINP}; PTDO, PTDI, PTMS, PATDI, PTDISEL referenced to P_{VCCJ}.

Digital Specifications – Power Management Section Dedicated Outputs

Over Recommended Operating Conditions

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
$I_{OH-HVOUT}$	Output leakage current	HVOUT[1:4] in open drain mode and pulled up to 12V		35	100	µA
V_{OL}	HVOUT[1:4] (open drain mode),	I_{SINK} = 10mA			0.8	V
	OUT[5:16]	I_{SINK} = 20mA			0.8	
	PTDO, MCLK, CPLDCLK, SDA	I_{SINK} = 4mA			0.4	
V_{OH}	PTDO, MCLK, CPLDCLK	I_{SRC} = 4mA			P_{VCCD} - 0.4	V
$I_{SINKTOTAL}$	All digital outputs				130	mA

sysIO Recommended Operating Conditions

Standard	V_{CCIO} (V)		
	Min.	Typ.	Max.
LVCMOS 3.3	3.135	3.3	3.465
LVCMOS 2.5	2.375	2.5	2.625
LVCMOS 1.8	1.71	1.8	1.89
LVCMOS 1.5	1.425	1.5	1.575
LVCMOS 1.2	1.14	1.2	1.26
LVTTL	3.135	3.3	3.465

sysIO Single-Ended DC Electrical Characteristics

Input/Output Standard	V_{IL}		V_{IH}		V_{OL} Max. (V)	V_{OH} Min. (V)	I_{OL}[1] (mA)	I_{OH}[1] (mA)
	Min. (V)	Max. (V)	Min. (V)	Max. (V)				
LVCMOS 3.3	-0.3	0.8	2.0	3.6	0.4	V_{CCIO} - 0.4	16, 12, 8, 4	-14, -12, -8, -4
					0.2	V_{CCIO} - 0.2	0.1	-0.1
LVTTL	-0.3	0.8	2.0	3.6	0.4	2.4	16	-16
					0.4	V_{CCIO} - 0.4	12, 8, 4	-12, -8, -4
					0.2	V_{CCIO} - 0.2	0.1	-0.1
LVCMOS 2.5	-0.3	0.7	1.7	3.6	0.4	V_{CCIO} - 0.4	16, 12, 8, 4	-14, -12, -8, -4
					0.2	V_{CCIO} - 0.2	0.1	-0.1
LVCMOS 1.8[2]	-0.3	$0.35V_{CCIO}$	$0.65V_{CCIO}$	3.6	0.4	V_{CCIO} - 0.4	16, 12, 8, 4	-14, -12, -8, -4
					0.2	V_{CCIO} - 0.2	0.1	-0.1
LVCMOS 1.5[2]	-0.3	$0.35V_{CCIO}$	$0.65V_{CCIO}$	3.6	0.4	V_{CCIO} - 0.4	8, 4	-8, -4
					0.2	V_{CCIO} - 0.2	0.1	-0.1
LVCMOS 1.2[2]	-0.3	0.42	0.78	3.6	0.4	V_{CCIO} - 0.4	6, 2	-6, -2
					0.2	V_{CCIO} - 0.2	0.1	-0.1

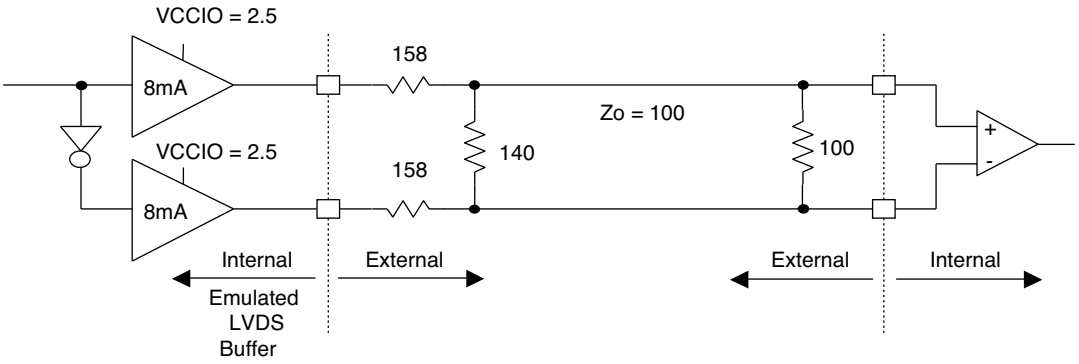
1. The average DC current drawn by I/Os between GND connections, or between the last GND in an I/O bank and the end of an I/O bank, as shown in the logic signal connections table shall not exceed n * 8mA. Where n is the number of I/Os between bank GND connections or between the last GND in a bank and the end of a bank.
2. Lower voltage operation not supported for VCCIO2 bank pins.

sysIO Differential Electrical Characteristics

LVDS Emulation

FPGA section outputs can support LVDS outputs via emulation (LVDS25E), in addition to the LVDS support that is available. The output is emulated using complementary LVCMOS outputs in conjunction with resistors across the driver outputs on all devices. The scheme shown in Figure 3 is one possible solution for LVDS standard implementation. Resistor values in Figure 3 are industry standard values for 1% resistors.

Figure 3. LVDS Using External Resistors (LVDS25E)

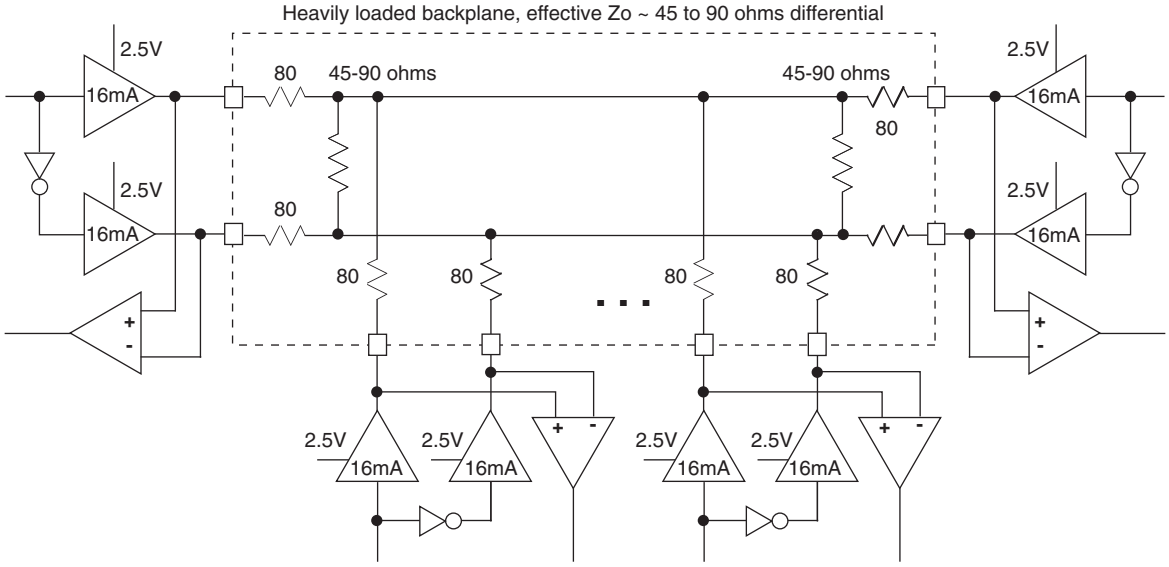


Note: All resistors are ±1%.

BLVDS Emulation

FPGA outputs support the BLVDS standard through emulation. The output is emulated using complementary LVCMOS outputs in conjunction with a parallel external resistor across the driver outputs. BLVDS is intended for use when multi-drop and bi-directional multi-point differential signaling is required. The scheme shown in Figure 4 is one possible solution for bi-directional multi-point differential signals.

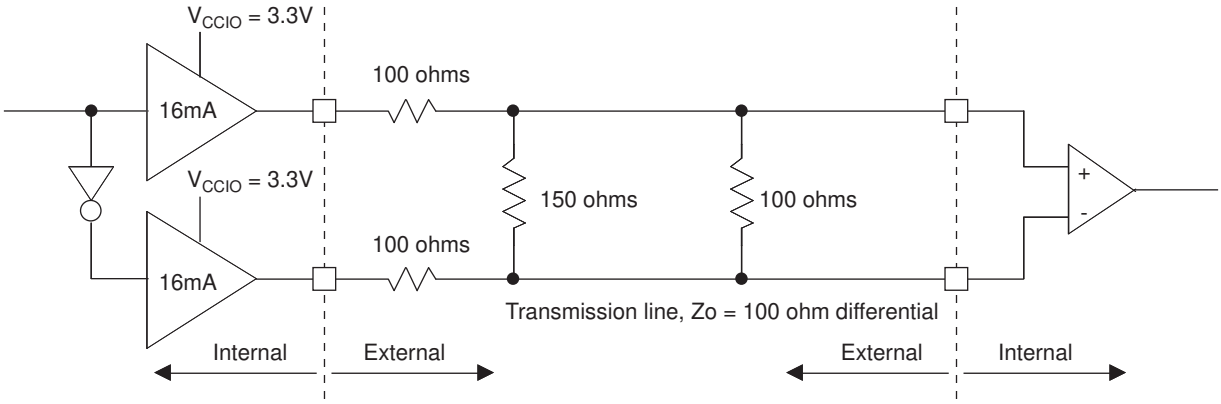
Figure 4. BLVDS Multi-point Output Example



LVPECL Emulation

FPGA outputs support the differential LVPECL standard through emulation. This output standard is emulated using complementary LVCMOS outputs in conjunction with a parallel resistor across the driver outputs on all the devices. The scheme shown in Figure 5 is one possible solution for point-to-point signals.

Figure 5. Differential LVPECL

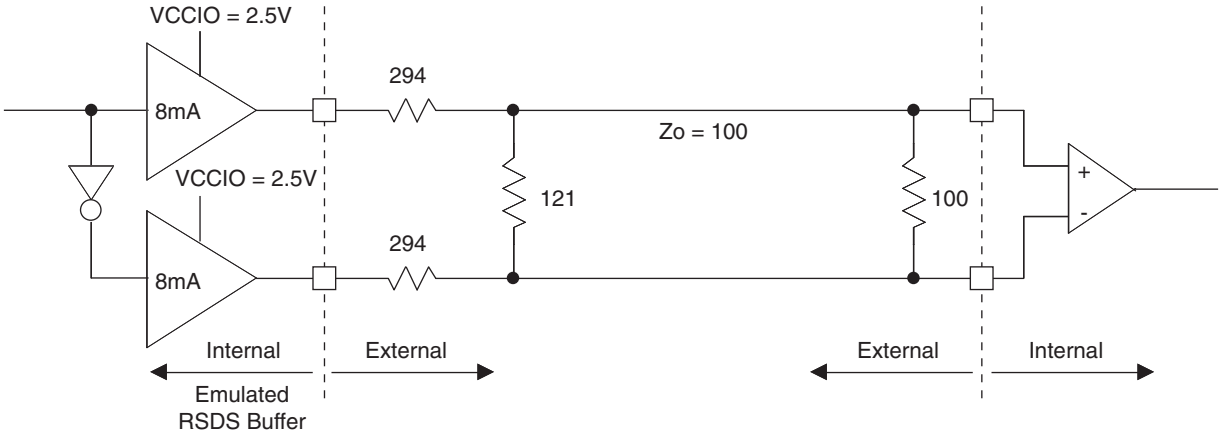


For further information on LVPECL, BLVDS and other differential interfaces please see details of additional technical documentation at the end of the data sheet.

RSDS Emulation

FPGA outputs support the differential RSDS standard. The output standard is emulated using complementary LVCMOS outputs in conjunction with a parallel resistor across the driver outputs on all the devices. The scheme shown in Figure 6 is one possible solution for RSDS standard implementation. Use LVDS25E mode with suggested resistors for RSDS operation. Resistor values in Figure 6 are industry standard values for 1% resistors.

Figure 6. RSDS (Reduced Swing Differential Standard)



Oscillator Transient Characteristics

Over Recommended Operating Conditions

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
f_{CLK}	Power Management internal master clock frequency (MCLK)		7.6	8	8.4	MHz
f_{CLKEXT}	Power Management externally applied master clock (MCLK)		7.2		8.8	MHz
f_{PLDCLK}	CPLDCLK output frequency	f_{CLK} = 8MHz		250		kHz
$f_{FPGACLK}$	FPGA internal master clock frequency		18		26	MHz

Power Management CPLD Timer Transient Characteristics

Over Recommended Operating Conditions

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
Timeout Range	Range of programmable timers (128 steps)	f_{CLK} = 8MHz	0.032		1966	ms
Resolution	Spacing between available adjacent timer intervals				13	%
Accuracy	Timer accuracy	f_{CLK} = 8MHz	-6.67		-12.5	%

Power Management I²C Port Characteristics

Symbol	Definition	100KHz		400KHz		Units
		Min.	Max.	Min.	Max.	
F_{I^2C}	I²C clock/data rate		100[1]		400[1]	KHz
$T_{SU;STA}$	After start	4.7		0.6		us
$T_{HD;STA}$	After start	4		0.6		us
$T_{SU;DAT}$	Data setup	250		100		ns
$T_{SU;STO}$	Stop setup	4		0.6		us
$T_{HD;DAT}$	Data hold; SCL= Vih_min = 2.1V	0.3	3.45	0.3	0.9	us
T_{LOW}	Clock low period	4.7		1.3		us
T_{HIGH}	Clock high period	4		0.6		us
T_F	Fall time; 2.25V to 0.65V		300		300	ns
T_R	Rise time; 0.65V to 2.25V		1000		300	ns
$T_{TIMEOUT}$	Detect clock low timeout	25	35	25	35	ms
T_{POR}	Device must be operational after power-on reset	500		500		ms
T_{BUF}	Bus free time between stop and start condition	4.7		1.3		us

1. If F_{I^2C} is less than 50kHz, then the ADC DONE status bit is not guaranteed to be set after a valid conversion request is completed. In this case, waiting for the $T_{CONVERT}$ minimum time after a convert request is made is the only way to guarantee a valid conversion is ready for readout. When F_{I2C} is greater than 50kHz, ADC conversion complete is ensured by waiting for the DONE status bit.

Timing for Power Management JTAG Operations

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
t_{ISPEN}	Program enable delay time		10	—	—	µs
t_{ISPDIS}	Program disable delay time		30	—	—	µs
t_{HVDIS}	High voltage discharge time, program		30	—	—	µs
t_{HVDIS}	High voltage discharge time, erase		200	—	—	µs
t_{CEN}	Falling edge of PTCK to PTDO active		—	—	15	ns
t_{CDIS}	Falling edge of PTCK to PTDO disable		—	—	15	ns
t_{SU1}	Setup time		5	—	—	ns
t_H	Hold time		10	—	—	ns
t_{CKH}	PTCK clock pulse width, high		20	—	—	ns
t_{CKL}	PTCK clock pulse width, low		20	—	—	ns
f_{MAX}	Maximum PTCK clock frequency		—	—	25	MHz
t_{CO}	Falling edge of PTCK to valid output		—	—	15	ns
t_{PWV}	Verify pulse width		30	—	—	µs
t_{PWP}	Programming pulse width		20	—	—	ms

Figure 7. Erase (User Erase or Erase All) Timing Diagram

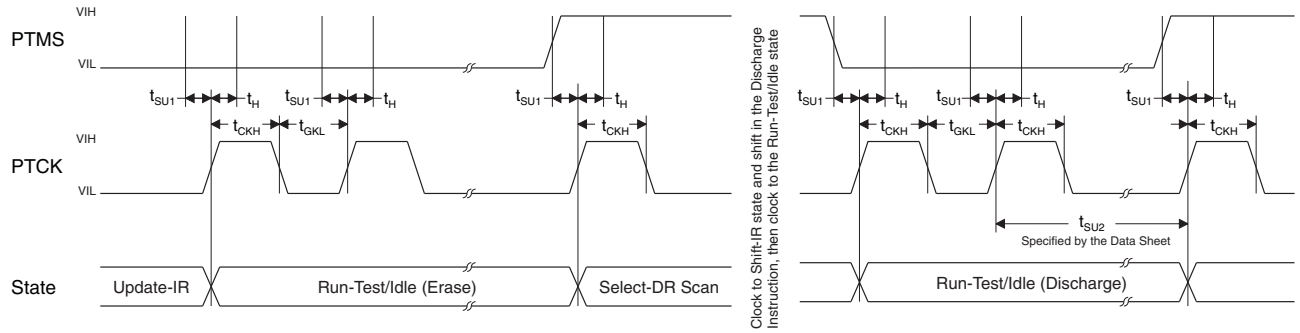


Figure 8. Programming Timing Diagram

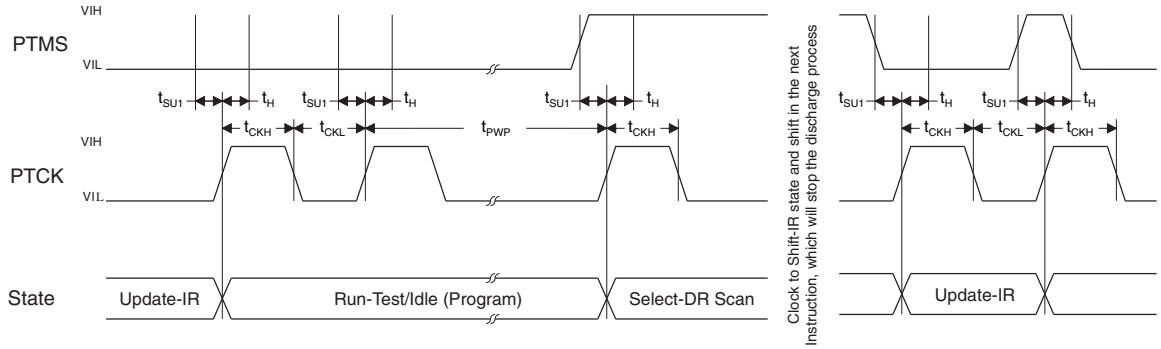


Figure 9. Verify Timing Diagram

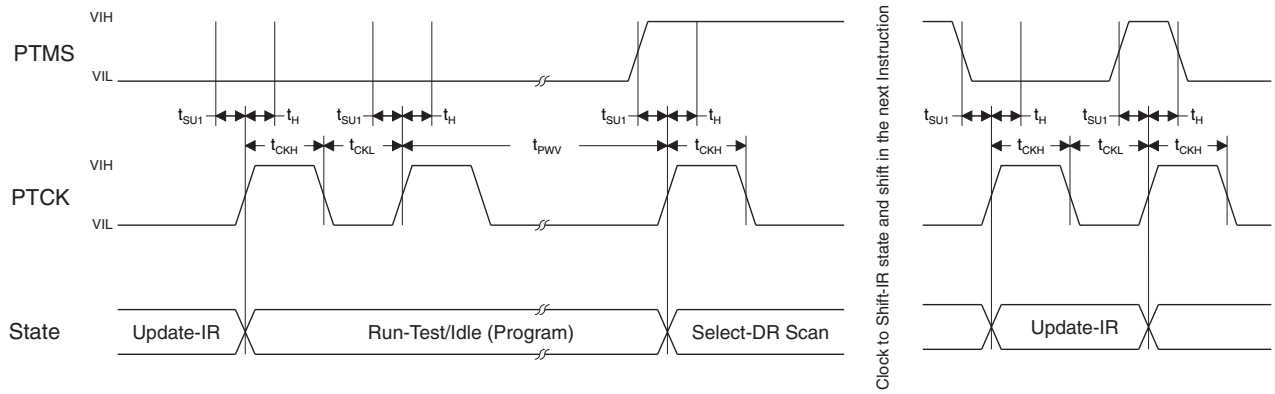
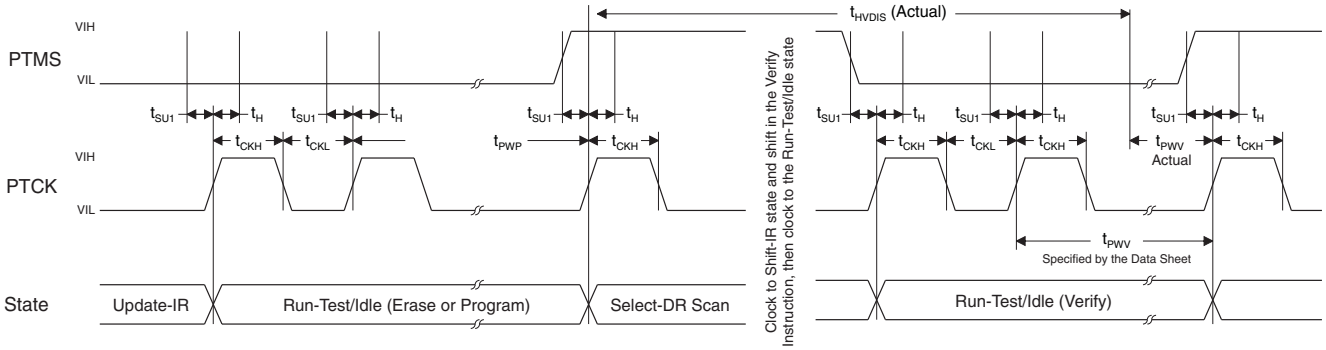


Figure 10. Discharge Timing Diagram



Typical FPGA Building Block Function Performance[1]

Pin-to-Pin Performance (LVCMOS25 12mA Drive)

Function	Timing	Units
Basic Functions		
16-bit decoder	6.7	ns
4:1 MUX	4.5	ns
16:1 MUX	5.1	ns

Register-to-Register Performance

Function	Timing	Units
Basic Functions		
16:1 MUX	487	MHz
16-bit adder	292	MHz
16-bit counter	388	MHz
64-bit counter	200	MHz
Distributed Memory Functions		
16x2 Single Port RAM	434	MHz
64x2 Single Port RAM	320	MHz
128x4 Single Port RAM	261	MHz
32x2 Pseudo-Dual Port RAM	314	MHz
64x4 Pseudo-Dual Port RAM	271	MHz

1. The above timing numbers are generated using the Platform Manager design tool. Exact performance may vary with device and tool version. The tool uses internal parameters that have been characterized but are not tested on every device.

Rev. A 0.19

Derating Logic Timing

Logic Timing provided in the following sections of the data sheet and the Platform Manager design tool are worst case numbers in the operating range. Actual delays may be much faster. The Platform Manager design tool from Lattice can provide FPGA logic timing numbers at a particular temperature and voltage.

FPGA Section External Switching Characteristics[1]

Over Recommended Operating Conditions

Parameter	Description	Min.	Max.	Units
General I/O Pin Parameters (Using Global Clock without PLL)[1]				
t_{PD}	Best Case t_{PD} Through 1 LUT	—	4.9	ns
t_{CO}	Best Case Clock to Output - From PFU	—	5.7	ns
t_{SU}	Clock to Data Setup - To PFU	1.5	—	ns
t_{H}	Clock to Data Hold - To PFU	-0.1	—	ns
f_{MAX_IO}	Clock Frequency of I/O and PFU Register	—	500	MHz
t_{SKEW_PRI}	Global Clock Skew Across Device	—	240	ps

1. General timing numbers based on LVCMOS2.5V, 12 mA.

Rev. A 0.19

FPGA Sleep Mode Timing

Parameter	Description	Min.	Max.	Units
t_{PWRDN}	SLEEPN Low to Power Down	—	400	ns
t_{PWRUP}	SLEEPN High to Power Up	—	600	µs
$t_{WSLEEPN}$	SLEEPN Pulse Width	400	—	ns
t_{WAWAKE}	SLEEPN Pulse Rejection	—	100	ns

FPGA Section Internal Timing Parameters[1]

Over Recommended Operating Conditions

Parameter	Description	Min.	Max.	Units
PFU/PFF Logic Mode Timing				
t_{LUT4_PFU}	LUT4 delay (A to D inputs to F output)	—	0.39	ns
t_{LUT6_PFU}	LUT6 delay (A to D inputs to OFX output)	—	0.62	ns
t_{LSR_PFU}	Set/Reset to output of PFU	—	1.26	ns
t_{SUM_PFU}	Clock to Mux (M0,M1) input setup time	0.15	—	ns
t_{HM_PFU}	Clock to Mux (M0,M1) input hold time	-0.07	—	ns
t_{SUD_PFU}	Clock to D input setup time	0.18	—	ns
t_{HD_PFU}	Clock to D input hold time	-0.04	—	ns
t_{CK2Q_PFU}	Clock to Q delay, D-type register configuration	—	0.56	ns
t_{LE2Q_PFU}	Clock to Q delay latch configuration	—	0.74	ns
t_{LD2Q_PFU}	D to Q throughput delay when latch is enabled	—	0.77	ns
PFU Dual Port Memory Mode Timing				
t_{CORAM_PFU}	Clock to Output	—	0.56	ns
t_{SUDATA_PFU}	Data Setup Time	-0.25	—	ns
t_{HDATA_PFU}	Data Hold Time	0.39	—	ns
t_{SUADDR_PFU}	Address Setup Time	-0.65	—	ns
t_{HADDR_PFU}	Address Hold Time	0.99	—	ns
t_{SUWREN_PFU}	Write/Read Enable Setup Time	-0.30	—	ns
t_{HWREN_PFU}	Write/Read Enable Hold Time	0.47	—	ns
PIO Input/Output Buffer Timing				
t_{IN_PIO}	Input Buffer Delay	—	1.06	ns
t_{OUT_PIO}	Output Buffer Delay	—	1.80	ns

1. Internal parameters are characterized but not tested on every device.

Rev. A 0.19

FPGA Section Timing Adders[1, 2, 3]

Over Recommended Operating Conditions

Buffer Type	Description		Units
Input Adjusters			
LVTTL33	LVTTL	0.01	ns
LVCMOS33	LVCMOS 3.3	0.01	ns
LVCMOS25	LVCMOS 2.5	0.00	ns
LVCMOS18	LVCMOS 1.8	0.10	ns
LVCMOS15	LVCMOS 1.5	0.19	ns
LVCMOS12	LVCMOS 1.2	0.56	ns
Output Adjusters			
LVTTL33_4mA	LVTTL 4mA drive	0.05	ns
LVTTL33_8mA	LVTTL 8mA drive	0.08	ns
LVTTL33_12mA	LVTTL 12mA drive	-0.01	ns
LVTTL33_16mA	LVTTL 16mA drive	0.70	ns
LVCMOS33_4mA	LVCMOS 3.3 4mA drive	0.05	ns
LVCMOS33_8mA	LVCMOS 3.3 8mA drive	0.08	ns
LVCMOS33_12mA	LVCMOS 3.3 12mA drive	-0.01	ns
LVCMOS33_14mA	LVCMOS 3.3 14mA drive	0.70	ns
LVCMOS25_4mA	LVCMOS 2.5 4mA drive	0.07	ns
LVCMOS25_8mA	LVCMOS 2.5 8mA drive	0.13	ns
LVCMOS25_12mA	LVCMOS 2.5 12mA drive	0.00	ns
LVCMOS25_14mA	LVCMOS 2.5 14mA drive	0.47	ns
LVCMOS18_4mA	LVCMOS 1.8 4mA drive	0.15	ns
LVCMOS18_8mA	LVCMOS 1.8 8mA drive	0.06	ns
LVCMOS18_12mA	LVCMOS 1.8 12mA drive	-0.08	ns
LVCMOS18_14mA	LVCMOS 1.8 14mA drive	0.09	ns
LVCMOS15_4mA	LVCMOS 1.5 4mA drive	0.22	ns
LVCMOS15_8mA	LVCMOS 1.5 8mA drive	0.07	ns
LVCMOS12_2mA	LVCMOS 1.2 2mA drive	0.36	ns
LVCMOS12_6mA	LVCMOS 1.2 6mA drive	0.07	ns

1. Timing adders are characterized but not tested on every device.
2. LVCMOS timing is measured with the load specified in Switching Test Conditions table.
3. All other standards tested according to the appropriate specifications.

Rev. A 0.19

Flash Download Time

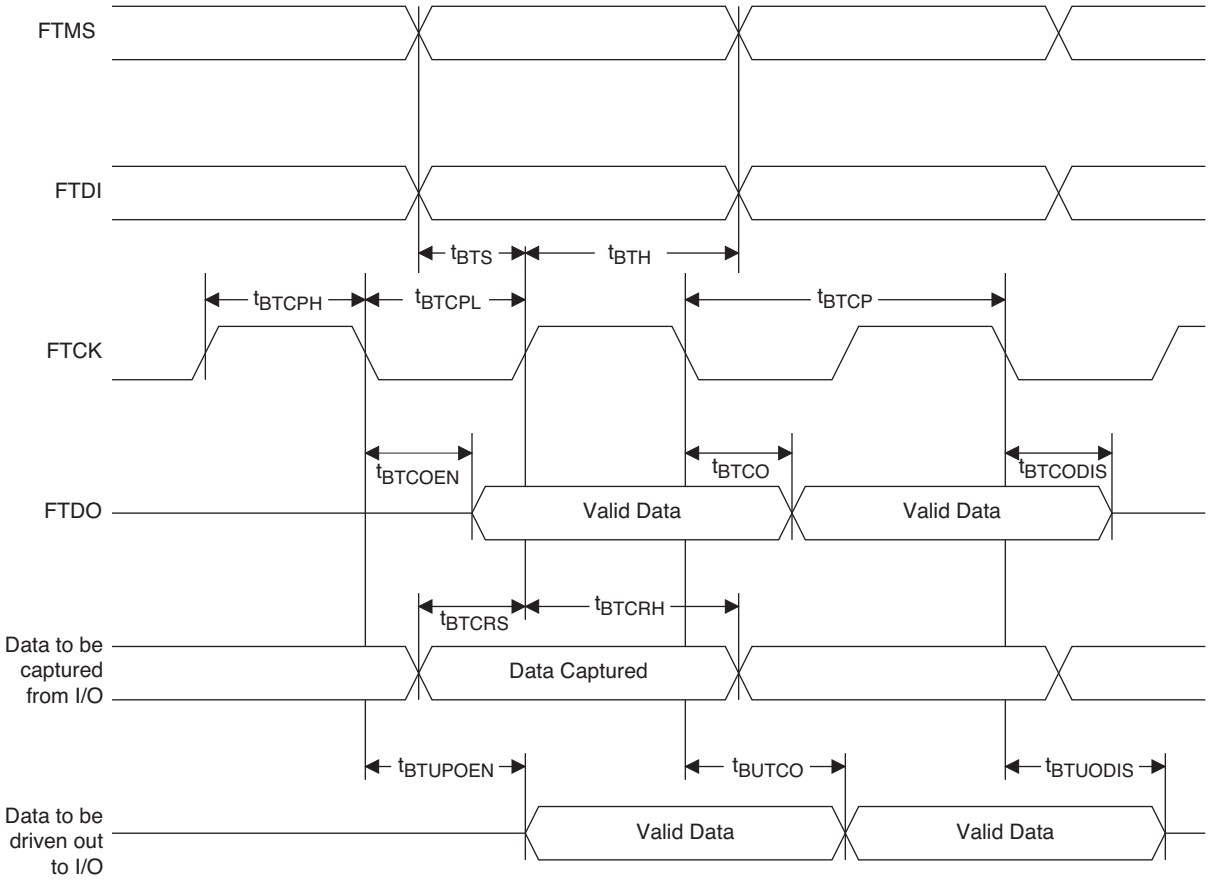
Symbol	Parameter	Min.	Typ.	Max.	Units
$t_{REFRESH}$	V_{CC} or V_{CCAUX} to Device I/O Active	—	—	0.6	ms

FPGA JTAG Port Timing Specifications

Symbol	Parameter	Min.	Max.	Units
f_{MAX}	FTCK [BSCAN] clock frequency	—	25	MHz
t_{BTCP}	FTCK [BSCAN] clock pulse width	40	—	ns
t_{BTCPH}	FTCK [BSCAN] clock pulse width high	20	—	ns
t_{BTCPL}	FTCK [BSCAN] clock pulse width low	20	—	ns
t_{BTS}	FTCK [BSCAN] setup time	8	—	ns
t_{BTH}	FTCK [BSCAN] hold time	10	—	ns
t_{BTRF}	FTCK [BSCAN] rise/fall time	50	—	mV/ns
t_{BTCO}	TAP controller falling edge of clock to output valid	—	10	ns
$t_{BTCODIS}$	TAP controller falling edge of clock to output disabled	—	10	ns
t_{BTCOEN}	TAP controller falling edge of clock to output enabled	—	10	ns
t_{BTCRS}	BSCAN test capture register setup time	8	—	ns
t_{BTCRH}	BSCAN test capture register hold time	25	—	ns
t_{BUTCO}	BSCAN test update register, falling edge of clock to output valid	—	25	ns
$t_{BTUODIS}$	BSCAN test update register, falling edge of clock to output disabled	—	25	ns
$t_{BTUPOEN}$	BSCAN test update register, falling edge of clock to output enabled	—	25	ns

Rev. A 0.19

Figure 11. FPGA JTAG Port Timing Waveforms



FPGA Output Switching Test Conditions

Figure 12 shows the output test load that is used for AC testing. The specific values for resistance, capacitance, voltage, and other test conditions are shown in Table 2.

Figure 12. Output Test Load, LVTTL and LVCMOS Standards

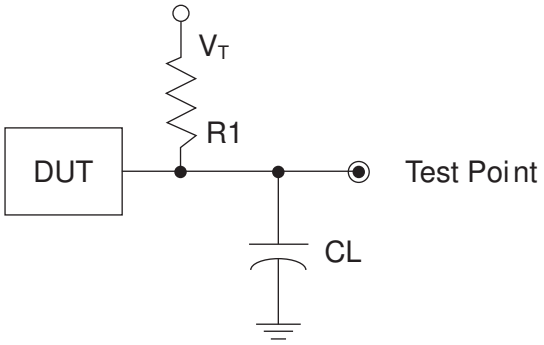


Table 2. Test Fixture Required Components, Non-Terminated Interfaces

Test Condition	R_1	C_L	Timing Ref.	V_T
LVTTL and LVCMOS settings (L -> H, H -> L)	∞	0pF	LVTTL, LVCMOS 3.3 = 1.5V	—
			LVCMOS 2.5 = $V_{CCIO}/2$	—
			LVCMOS 1.8 = $V_{CCIO}/2$	—
			LVCMOS 1.5 = $V_{CCIO}/2$	—
			LVCMOS 1.2 = $V_{CCIO}/2$	—
LVTTL and LVCMOS 3.3 (Z -> H)	188	0pF	1.5	V_{OL}
LVTTL and LVCMOS 3.3 (Z -> L)				V_{OH}
Other LVCMOS (Z -> H)			$V_{CCIO}/2$	V_{OL}
Other LVCMOS (Z -> L)			$V_{CCIO}/2$	V_{OH}
LVTTL + LVCMOS (H -> Z)			V_{OH} - 0.15	V_{OL}
LVTTL + LVCMOS (L -> Z)			V_{OL} - 0.15	V_{OH}

Note: Output test conditions for all other interfaces are determined by the respective standards.