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Platform Manager 2

In-System Programmable
Hardware Management Controller

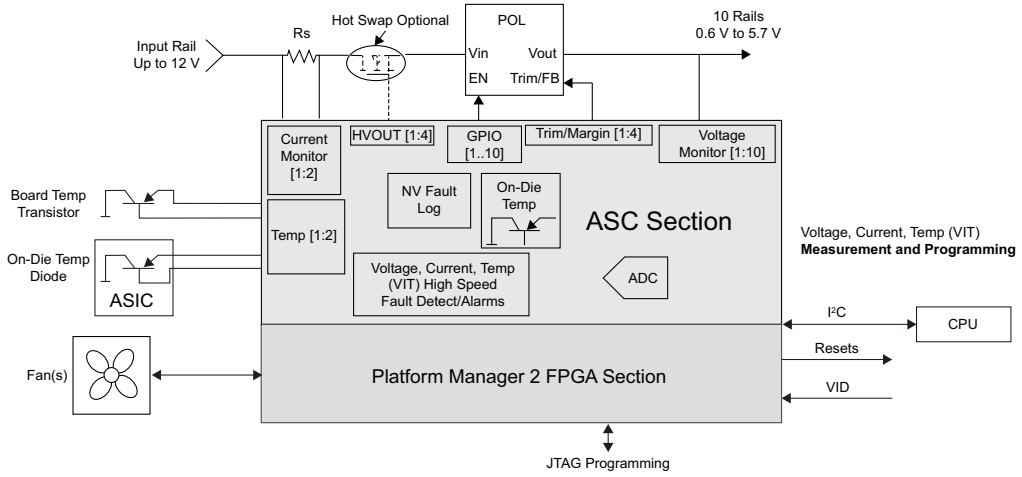
May 2016 **Data Sheet DS1043**

Features

- **Ten Rail Voltage Monitoring and Measurement**
  - UV/OV Fault Detection Accuracy – 0.2% Typ.
  - Fault Detection Speed < 100 µs
  - High Voltage, Single Ended and Differential Sensing
- **Two Channel Wide-Range Current Monitoring and Measurement**
  - High-side current measurement up to 12 V
  - Programmable OC/UC Fault Detect
  - Detects Current faults in <1 µs
- **Three Temperature Monitoring and Measurement Channels**
  - Programmable OT/UT Faults Threshold
  - Two channels of Temperature Monitoring using external diodes
  - On-Chip Temperature Monitor
- **4 High-Side MOSFET Drivers**
  - Programmable Charge Pump
- **Four Precision Trim and Margin Channels**
  - Closed Loop Operation
  - Voltage Scaling and VID Support
- **Ten General Purpose Input/Output**
  - 5 V tolerant I/O
- **Non-Volatile Fault Logging**
- **Programmed through JTAG or I²C**
  - Background Update with Dual-Boot Backup
- **FPGA Resources**
  - 1280 LUT, 98 I/O Version (LPTM21)
- **RAM and Flash Memories**
- **Scalable Hardware Management Architecture**
  - Glueless interface to Hardware Management Expander (L-ASC10)
  - Migrate between LPTM21 and larger density MachXO2 device to extend logic and I/O resources
- **System Level Support**
  - Operating voltage from 4.75 V to 13.2 V or 2.8 V to 3.46 V
  - 12 V DC-DC converter provides 3.3 V supply for ASC Hardware Management Expanders
  - Industrial and commercial temperature ranges
  - 237-ball ftBGA (LPTM21)
  - RoHS compliant and halogen-free
- **Applications**
  - Telecommunication and Networking
  - Industrial, Test and Measurement
  - Medical Systems
  - Servers and Storage Systems
  - High Reliability Systems

Application Diagram

Hardware Management Application Block Diagram



Description

The Lattice Platform Manager 2 device is a fast-reacting, programmable logic based hardware management controller. Platform Manager 2 is an integrated solution combining analog sense and control elements with scalable programmable logic resources. This unique approach allows Platform Manager 2 to integrate Power Management (Power Sequencing, Voltage Monitoring, Trimming and Margining), Thermal Management (Temperature Monitoring, Fan Control, Power Control), and Control Plane functions (System Configuration, I/O Expansion, etc.) as a single device.

Architecturally, the Platform Manager 2 device can be divided into two sections – Analog Sense and Control and FPGA. The Analog Sense and Control (ASC) section provides three types of analog sense channels: voltage (nine standard channels and one high voltage channel), current (one standard voltage and one high voltage) and temperature (two external and one internal).

Each of the analog sense channels is monitored through two independently programmable comparators to support both high/low and in-bounds/out-of-bounds (window-compare) monitor functions. In addition, each of the current sense channels provides a fast fault detect (one µs response time) for detecting short circuit events. The temperature sense channels can be configured to work with different external transistor or diode configurations.

The Analog Sense and Control section also provides ten general purpose 5 V tolerant open-drain digital input/output pins that can be used for controlling DC-DC converters, low-drop-out regulators (LDOs) and opto-couplers, as well as for general purpose logic interface functions. In addition, four high-voltage charge pumped outputs (HVOUT1-HVOUT4) may be configured as high-voltage MOSFET drivers to control high-side MOSFET switches. These HVOUT outputs can also be programmed as static output signals or as switched outputs (to support external charge pump implementation) operating at a dedicated duty cycle and frequency.

The ASC section incorporates four TRIM outputs for controlling the output voltages of DC-DC converters. Each power supply output voltage can be maintained typically within 0.5% tolerance across various load conditions using the Digital Closed Loop Control mode of the trimming block.

The internal 10-bit A/D converter can be used to measure the voltage and current through the I^2C bus. The ADC is also used in the digital closed loop control mode of the trimming block.

The ASC section also provides the capability of logging up to 16 status records into its nonvolatile EEPROM memory. Each record includes voltage, current and temperature monitor signals along with digital input and output levels.

The ASC section includes an output control block (OCB) which allows certain inputs and control signals a direct connection to the digital outputs or HVOUTs, bypassing the ASC-I/F for a faster response. The OCB is used to connect the fast current fault detect signal to an FPGA input directly. It also supports functions such as Hot Swap with a programmable hysteretic controller.

The FPGA section contains non-volatile low cost programmable logic of 1280 Look-Up Tables (LUTs). In addition to the LUT-based logic, the FPGA section features Embedded Block RAM (EBR), Distributed RAM, User Flash Memory (UFM), flexible I/Os, and hardened versions of commonly used functions such as SPI controller, I^2C controller and Timer/counter. The FPGA I/Os offer enhanced features such as drive strength control, slew rate control, buskeeper latches, internal pull-up or pull-down resistors, and open-drain outputs. These features are controllable on a “per-pin” basis.

The power management, thermal management and control plane logic functions are implemented in the FPGA section of Platform Manager 2. The FPGA receives the analog comparator values and inputs from the ASC section and sends output commands to the ASC section through the dedicated ASC-interface (ASC-I/F) high-speed, reliable serial channel. The FPGA hardware management functions are implemented using the Platform Designer tool inside Lattice Diamond software. The Platform Designer tool includes an easy to use sequence and monitor logic

builder tool and a set of pre-engineered components for functions like time-stamped fault logging, voltage by identification (VID), and fan control.

The Platform Manager 2 is designed to enable seamless scaling of the number of voltage, current and temperature sense channels in the system by adding external Analog Sense and Control (ASC) Hardware Management Expanders. The algorithm implemented within the FPGA can access and control these external ASCs through the dedicated ASC-I/F. Larger systems with up to eight ASC devices can be created by using a MachXO2 FPGA in place of the Platform Manager 2 device. The companion devices are connected in a scalable, star topology to Platform Manager 2 or MachXO2.

The Platform Manager 2 has an I^2C interface which is used by the FPGA section for ASC interface configuration. The I^2C interface also provides the mechanism for parameter measurement or I/O control or status. For example, voltage trim targets can be set over the I^2C bus and measured voltage, current, or temperature values can be read over the I^2C bus.

The Platform Manager 2 device can be programmed in-system through JTAG or I^2C interfaces. The configuration is stored in on-chip non-volatile memory. Upon power-on, the FPGA section configuration is transferred to the on-chip SRAM and the device operates from SRAM. It is possible to update the non-volatile memory content in the background without interrupting the system operation.

Block Diagram

Figure 1. Platform Manager 2 Block Diagram

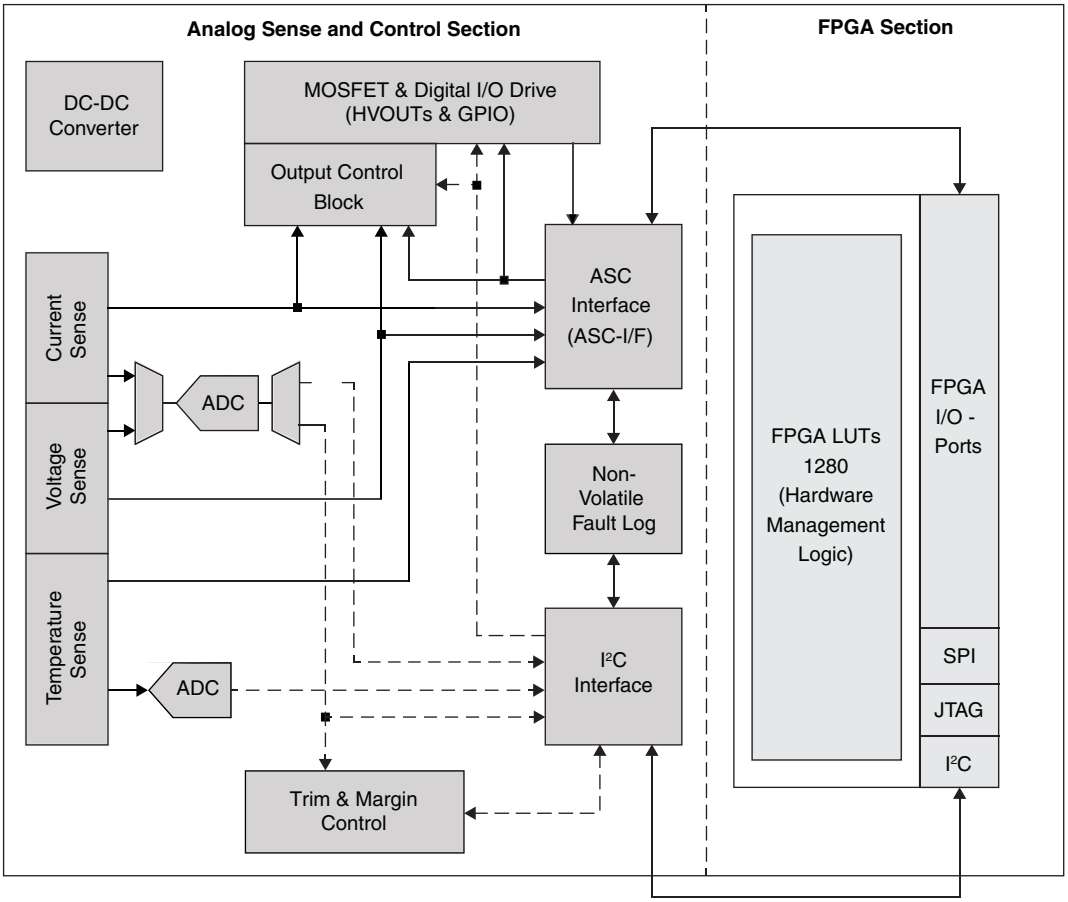


Table 1. Platform Manager 2 Device Features

	LPTM21
Analog Sense and Control Section	
Voltage Monitor Inputs	10
Current Monitor Inputs	2
Temperature Monitor Inputs	2
Trim Outputs	4
High Voltage Outputs	4
GPIO pins (5V tolerant)	10
FPGA section	
LUTs	1280
Distributed RAM (Kbits)	10
EBR SRAM (Kbits)	64
Number of EBR SRAM Blocks (9 Kbits/block)	7
UFM (Kbits)	64
Hardened Functions I^2C SPI Timer/Counter	 2 1 1
Package	**Digital I/Os**[1]
237 - ftBGA	95

1. Digital I/O count does not include SDA_M, SCL_M or JTAGENB pins.

DC and Switching Characteristics

Absolute Maximum Ratings[1, 2, 3]

Symbol	Parameter	Conditions	Min	Max.	Units
Supply Voltages					
V_{CCA}	ASC Supply		–0.5	3.75	V
V_{CC}	FPGA Core Supply Voltage[4]		–0.5	3.75	V
V_{CCIO}	FPGA Output Supply Voltage[4]		–0.5	3.75	V
V_{VDC}	Power Supply Input to DC-DC Converter		–0.5	13.3	V
Monitor and I/O Pin Voltages					
V_{IN_VMON}	VMON input voltage		–0.5	6	V
V_{IN_VMONGS}	VMON input voltage ground sense		–0.5	6	V
V_{IN_HIMONP}	High voltage IMON input voltage		–0.5	13.3	V
$V_{IN\_HIMONN\_HVMON}$	High voltage IMON return / VMON input voltage		–0.5	13.3	V
V_{DIFF_HIMON}	High voltage IMON differential voltage		–2.0	2.0	V
V_{IN_IMONP}	Low voltage IMON1 input voltage		–0.5	6.0	V
V_{IN_IMONN}	Low voltage IMON1 return voltage		–0.5	6.0	V
V_{DIFF_IMON}	Low voltage IMON1 differential voltage		–2.0	2.0	V
V_{IN_TMONP}	TMON input voltage		–0.5	V_{CCA}	V
V_{IN_TMONN}	TMON return voltage		–0.5	V_{CCA}	V
V_{IN_GPIO}	Digital input voltage (ASC Section)		–0.5	6	V
V_{OUT}	Open-drain output voltage (ASC Section)	HVOUT [1:4]	–0.5	13.3	V
		GPIO[1:10]	–0.5	6	V
V_{TRIM}	TRIM output voltage		–0.5	V_{CCA}	V
V_{TRI_FPGA}	FPGA PIO Tri-State Voltage Applied[5, 4]		–0.5	3.75	V
V_{IN_FPGA}	FPGA PIO Dedicated Input Voltage Applied[4]		–0.5	3.75	V
Other					
$I_{SINKMAX}$	Maximum Sink Current on any ASC Section output			23	mA
T_S	Device Storage Temperature (Ambient)		–55	+125	°C
T_J	Junction Temperature		–40	+125	°C

1. Stress above those listed under the “Absolute Maximum Ratings” may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.
2. Compliance with the Lattice Thermal Management document is required.
3. All voltages referenced to GND.
4. Overshoot and Undershoot of –2 V to (VIHMAX +2) volts is permitted for a duration of < 20 ns.
5. The dual function I2C pins SCL_M and SDA_M are limited to –0.25 to 3.75 V or to –0.3 V with a duration of < 20 ns.

Recommended Operating Conditions[1]

Symbol	Parameter	Conditions	Min	Max.	Units
Supply Voltages					
V_{CCA}	ASC Supply		2.8	3.465	V
V_{CC}	FPGA Core Supply Voltage		2.8	3.465	V
V_{CCIO}[2, 3]	FPGA Output Supply Voltage		1.14	3.465	V
V_{VDC}	VDC Supply[5]		4.75	13.2	V
Monitor and I/O Pin Voltages					
V_{IN_VMON}	V_{MON} input voltage		–0.3	5.9	V
V_{IN_VMONGS}	V_{MON} input voltage ground sense		–0.2	0.3	V
V_{IN_HIMONP}	High voltage IMON input voltage[4]		4.5	13.2	V
$V_{IN\_HIMONN\_HVMON}$	High voltage IMON return /VMON voltage[4]		4.5	13.2	V
V_{DIFF_HIMON}	High voltage IMON differential voltage		0	500	mV
V_{IN_IMONP}	Low voltage IMON1 input voltage	Low Side Sense Disabled	0.6	5.9	V
		Low Side Sense Enabled	–0.3	1.0	V
V_{IN_IMONN}	Low voltage IMON1 return voltage	Low Side Sense Disabled	0.6	5.9	V
		Low Side Sense Enabled	–0.3	1.0	V
V_{DIFF_IMON}	Low voltage IMON1 differential voltage		0	500	mV
V_{IN_GPIO}	Digital input voltage (ASC Section)		–0.3	5.5	V
V_{OUT}	Open-drain output voltage (ASC Section)	HVOUT [1:4]	–0.3	13.2	V
		GPIO[1:10]	–0.3	5.5	V
Other					
T_{JCOM}	Junction Temperature (Commercial)		0	+85	°C
T_{JIND}	Junction Temperature (Industrial)		–40	+100	°C

1. Like power supplies must be tied together. For example, if V_{CCIO} and V_{CC} are both the same voltage, they must also be the same supply. VCCA, VCC, VCCIO0 and VCCIO1 should all be tied together. See the System Connections section for more details.
2. See recommended voltage by I/O standard in subsequent table.
3. V_{CCIO} pins of unused I/O banks should be connected to the V_{CC} power supply on boards.
4. HIMON circuits are operational down to 3V. Accuracy is guaranteed within Recommended Operating Conditions
5. VDC supply voltage only required when on-chip DC-DC converter controller is used to generate VCCA/VCC. VDC should be left open when VCCA/VCC are supplied directly.

Power Supply Ramp Rates[1]

Symbol	Parameter	Min.	Typ.	Max.	Units
t_{RAMP}	Power supply ramp rates for all V_{CC} and V_{CCIO} power supplies.	0.01	—	100	V/ms

1. Assumes monotonic ramp rates.

DC/DC Converter[1,2]

Symbol	Parameter	Conditions	Min	Typ.	Max.	Units
V_{VDC}	Input Supply		4.75		13.2	V
F_{DC}	PWM Frequency			215		kHz
V_{VDC_OUT}	Regulated Supply Voltage		3.1	3.3	3.45	V
V_{VDC_DRVoh}	HDRV	Isrc=4mA	3.17			V
V_{VDC_DRVol}	HDRV	Isrc=4mA			0.34	V

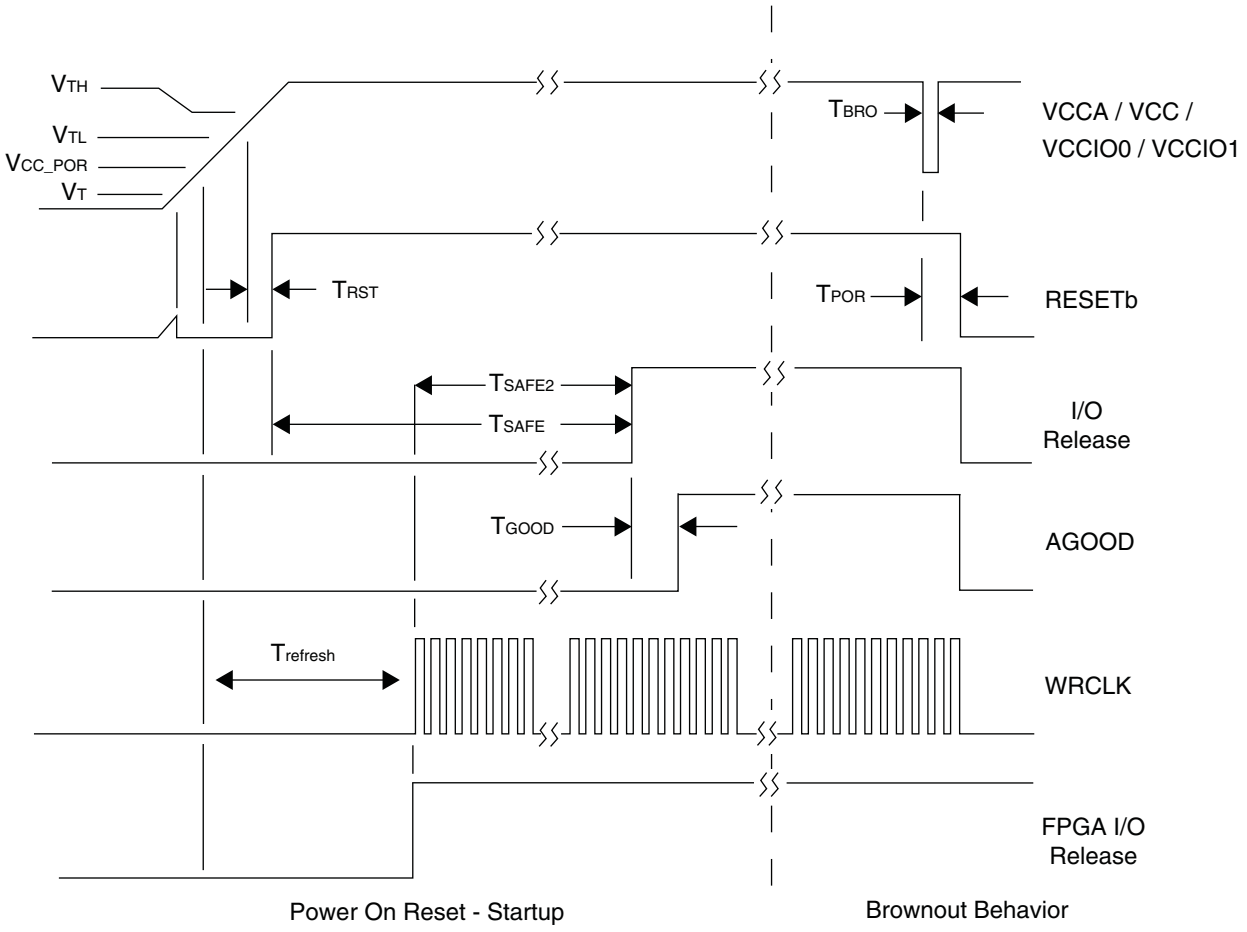
1. DC-DC converter performance is dependent on external component selection. See the For Further Information section for more details.
2. Valid for load currents up to 250 mA.

Power-On-Reset and Flash Download Time

Symbol	Parameter	Conditions	Min	Typ.	Max.	Units
Analog Sense and Control Section						
T_{RST}	Delay from V_{TH} to start-up state				100	us
T_{SAFE}	Delay from RESETb release to ASC Safe State Exit and I/O Release[2, 3]			1.8		ms
T_{SAFE2}	Delay from WRCLK start to ASC Safe State Exit and I/O Release[2, 3, 4]		56			us
T_{GOOD}	Delay from I/O release to A_{GOOD} asserted high in FPGA section[5]			16		us
T_{BRO}	Minimum duration brown out required to trigger RESETb		1		5	us
T_{POR}	Delay from Brown out to reset state				13	us
V_{TL}	Threshold below which RESETb is LOW				2.3	V
V_{TH}	Threshold above which RESETb is Hi-Z		2.7			V
V_T	Threshold above which RESETb is valid		0.8			V
C_L	Capacitive load on RESETb				200	pF
FPGA Section						
$V_{CC\_PORUPEXT}$[1]	Power-On-Reset ramp up trip point (external VCC power supply)		1.5		2.1	V
$V_{PORUPIO}$[1]	Power-On_Reset ramp up trip point (VCCIO0 power supply)		0.9		1.06	V
$T_{refresh}$[6]	Flash Download Time (Power-On-Reset to Device I/O active)	LPTM21		1.9		ms

1. These POR trip points are provided for guidance only. Device operation is only characterized for power supply voltages specified under recommended operating conditions.
2. Both T_{SAFE} and T_{SAFE2} must complete before I/O are released from Safe State.
3. During the calibration period before T_{SAFE} and T_{SAFE2}, the ASC may ignore RESETb being driven low. After T_{SAFE} and T_{SAFE2}, the ASC can be reset by another device by driving RESETb low.
4. Safe State is released at ASC after a fixed number (64) of WRCLK cycles (typ.8 MHz frequency) and three ASC-I/F data packets are properly detected.
5. AGOOD asserted in the FPGA on the next ASC-I/F packet after I/O exits Safe State as ASC.
6. FPGA flash download time has a direct influence on WRCLK start time. See Figure 2.

Figure 2. Platform Manager 2 Power-On Reset



DC Electrical Characteristics

Symbol	Parameter	Device	Min	Typ.[5]	Max.	Units
I_{CCA}	Supply Current (Analog Section)			25	35	mA
$I_{CC-HVOUT}$	Supply Current Adder per HVOUT, V_{HVOUT} = 12 V, Isrc = 100 uA				2	mA
I_{CC}[1, 2, 3, 4]	Static Core Supply Current (FPGA Section)	LPTM21		3.49		mA
I_{CCIO}[1, 2, 3, 4, 6]	Static Bank Power Supply, V_{CCIO} = 2.5 V			500		µA

1. For further information on FPGA section supply current, please see details of additional technical documentation at the end of this data sheet.
2. Assumes blank pattern with the following characteristics: all outputs are tri-stated, all inputs are configured as LVCMOS and held at V_{CCIO} or GND, on-chip oscillator is off, on-chip PLL is off.
3. Frequency = 0 MHz.
4. To determine the FPGA peak start-up current data, use the Power Calculator tool.
5. Tj = 25C, power supplies at nominal voltage.
6. Does not include pull-up/pull-down.

Programming and Erase Supply Current

Symbol	Parameter	Device	Min	Typ.[5]	Max.	Units
I_{CCA}	Supply Current (Analog Section)				40	mA
I_{CC}[1, 2, 3, 4]	Core Supply Current (FPGA Section)	LPTM21		18.8		mA
I_{CCIO}[1, 2, 3, 4, 6]	Bank Power Supply, V_{CCIO} = 2.5 V			500		µA

1. For further information on FPGA section supply current, please see details of additional technical documentation at the end of this data sheet.
2. Assumes all FPGA section inputs are held at V_{CCIO} or GND and all outputs are tri-stated.
3. Typical user pattern.
4. JTAG programming is at 25 MHz.
5. Tj = 25C, power supplies at nominal voltage.
6. Per bank, does not include pull-up/pull-down.

FPGA Configuration Memory Programming / Erase Specifications

Symbol	Parameter	Min.	Max.[1]	Units
$N_{PROGCYC}$	Flash Programming cycles per $t_{RETENTION}$	—	10,000	Cycles
	Flash functional programming cycles	—	100,000	
$t_{RETENTION}$	Data retention at 100 °C junction temperature	10	—	Years
	Data retention at 85 °C junction temperature	20	—	

1. Maximum Flash memory reads are limited to 7.5E13 cycles over the lifetime of the product.

FPGA I/O Hot Socketing Specifications[1, 2, 3]

Symbol	Parameter	Condition	Max.	Units
I_{DK}	Input or I/O leakage Current	0 < V_{IN} < V_{IH} (MAX)	+/–1000	µA

1. Insensitive to sequence of V_{CC} and V_{CCIO}. However, assumes monotonic rise/fall rates for V_{CC} and V_{CCIO}.
2. 0 < V_{CC} < V_{CC} (MAX), 0 < V_{CCIO} < V_{CCIO} (MAX).
3. I_{DK} is additive to I_{PU}, I_{PD} or I_{BH}.

ESD Performance

Please refer to the Platform Manager 2 Product Family Qualification Summary for complete qualification data, including ESD performance.

Digital Specifications

Symbol	Parameter	Conditions	Min	Typ.	Max.	Units
Analog Sense and Control Section						
I_{IL},I_{IH}	Input leakage, no pull-up, pull-down[7]				+/ 10	µA
I_{PD}	Active Pull-Down Current[7]	GPIO[1:10] configured as Inputs, Internal Pull-Down enabled		200		µA
$I_{PD-ASCIF}$	Input Leakage (WDAT and WRCLK)[8]	Internal Pull-Down		175		µA
$I_{OH-HVOUT}$	Output Leakage Current	HVOUT[1:4] in open drain mode and pulled up to 12 V		35	100	µA
$I_{PU-RESETb}$	Input Pull-Up Current (RESETb)			–50		µA
V_{IL}	Voltage input, logic low	GPIO[1:10]			0.8	V
		SCL_S/SDA_S			30% V_{CCA}	
V_{IH}	Voltage input, logic high	GPIO[1:10]	2.0			V
		SCL_S/SDA_S	70% V_{CCA}			
V_{OL}	HVOUT[1:4] (open drain mode)	I_{SINK} = 10 mA			0.8	V
	GPIO[1:10]	I_{SINK} = 20 mA			0.8	
$I_{SINKTOTAL}$[6]	All digital outputs				130	mA
FPGA Section – Programmable I/O						
I_{IL},I_{IH}[1,4]	Input or I/O Leakage	Clamp OFF and $V_{CCIO} < V_{IN} < V_{IH}$ (MAX)			+175	µA
		Clamp OFF and $V_{IN} = V_{CCIO}$	–10		10	µA
		Clamp OFF and V_{CCIO} –0.97V < V_{IN} < V_{CCIO}	–175			µA
		Clamp OFF and 0V < V_{IN} < V_{CCIO} –0.97 V			10	µA
		Clamp OFF and V_{IN} = GND			10	µA
		Clamp ON and 0V < V_{IN} < V_{CCIO}			10	µA
I_{PU}	I/O Active Pull-up Current	0< V_{IN} < 0.7 V_{CCIO}	–30		–309	µA
I_{PD}	I/O Active Pull-down Current	V_{IL} (MAX) < V_{IN} < V_{CCIO}	30		305	µA
I_{BHLS}	Bus Hold Low Sustaining Current	V_{IN} = V_{IL} (MAX)	30			µA
I_{BHHS}	Bus Hold High Sustaining Current	V_{IN} = 0.7 V_{CCIO}	–30			µA
I_{BHLO}	Bus Hold Low Overdrive Current	0 ≤ V_{IN} ≤ V_{CCIO}			305	µA
I_{BHHO}	Bus Hold High Overdrive Current	0 ≤ V_{IN} ≤ V_{CCIO}			–309	µA
V_{BHT}[3]	Bus Hold Trip Points		V_{IL} (MAX)		V_{IH} (MIN)	V
C1	I/O Capacitance[2]	V_{CCIO} = 3.3 V, 2.5 V, 1.8 V, 1.5 V, 1.2 V V_{CC} = Typ. V_{IO} = 0 to VIH (MAX)	3	5	9	pF
C2	Dedicated Input Capacitive	V_{CCIO} = 3.3 V, 2.5 V, 1.8 V, 1.5 V, 1.2 V, V_{CC} = Typ. V_{IO} = 0 to VIH (MAX)	3	5.5	7	pF

Digital Specifications (Cont.)

Symbol	Parameter	Conditions	Min	Typ.	Max.	Units
V_{HYST}	Hysteresis for Schmitt Trigger Inputs[5]	V_{CCIO} = 3.3 V, Hysteresis = Large		450		mV
		V_{CCIO} = 2.5 V, Hysteresis = Large		250		mV
		V_{CCIO} = 1.8 V, Hysteresis = Large		125		mV
		V_{CCIO} = 1.5 V, Hysteresis = Large		100		mV
		V_{CCIO} = 3.3 V, Hysteresis = Small		250		mV
		V_{CCIO} = 2.5 V, Hysteresis = Small		150		mV
		V_{CCIO} = 1.8 V, Hysteresis = Small		60		mV
		V_{CCIO} = 1.5 V, Hysteresis = Small		40		mV

1. Input or I/O leakage current is measured with the pin configured as an input or as an I/O with the output driver tri-stated. It is not measured with the output driver active. Bus maintenance circuits are disabled.
2. T_A 25 °C, f = 1.0 MHz.
3. Please refer to VIL and VIH in the sysIO Single-Ended DC Electrical Characteristics table of this document.
4. When VIH is higher than VCCIO, a transient current typically of 30ns in duration or less with a peak current of 6mA can occur on the high-to-low transition. For true LVDS output pins in LPTM21, VIH must be less than or equal to VCCIO.
5. With bus keeper circuit turned on. For more details, refer to TN1202, MachXO2 sysIO Usage Guide.
6. Sum of maximum current sink from all digital outputs combined. Reliable operation is not guaranteed if this value is exceeded.
7. During safe-state, all GPIO default to output, see the Safe State section for more details. GPIO[1:6] and GPIO[10] default to active low output. This will result in a leakage current dependent on the input voltage which can exceed the specified input leakage
8. WRCLK and WDAT pins may see transients above 1 mA in hot socket conditions. DC levels will remain below 1 mA.

Voltage Monitors[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Units
R_{VMON_in}	Input Resistance		55	65	75	kΩ
C_{VMON_in}	Input Capacitance			8		pF
V_{MON} Range	Programmable trip-point Range		0.075		5.734	Volts
V_{MON} Accuracy	Absolute accuracy of any trip-point – Differential VMON pins	VMON voltage > 0.650 V		0.2	0.7	%
	Single-ended VMON pins	VMON voltage > 0.650 V		0.3	0.9	%
V_{MON} HYST	Hysteresis of any trip-point (relative to setting)			1		%
V_{MON} CMR	Differential VMON Common mode rejection ratio			60		dB
V_Z Sense	Low Voltage Sense Trip Point Error – Differential VMON1-4	Trip Point = 0.075 V	–5		+5	mV
		Trip Point = 0.150 V	–5		+5	mV
		Trip Point = 0.300 V	–10		+10	mV
		Trip Point = 0.545 V	–15		+15	mV
	Low Voltage Sense Trip Point Error – Single-Ended VMON5-9	Trip Point = 0.080 V	–10		+10	mV
		Trip Point = 0.155 V	–15		+15	mV
		Trip Point = 0.310 V	–25		+25	mV
		Trip Point = 0.565 V	–55		+55	mV
High Voltage Monitor						
HV_{MON} Range	High Voltage VMON programmable trip-point range		0.3		13.2	Volts
HV_{MON} Accuracy	HVMON Absolute accuracy of any trip-point	HVMON voltage > 1.8 V		0.4	1.0	%
V_Z Sense	Low Voltage Sense Trip Point Error - HVMON pin	Trip Point = 0.220 V	–20		+20	mV
		Trip Point = 0.425 V	–35		+35	mV
		Trip Point = 0.810 V	–75		+75	mV
		Trip Point = 1.280 V	–130		+130	mV

1. VMON accuracy may degrade based on SSO conditions of FPGA section, especially bank 1. See the System Connections section for more details.

Current Monitors

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$I_{IMONPleak}$	IMON1P input leakage	Low Side Sense Disabled Fast Trip Point V_{sns} = 500 mV	–2		250	µA
		Low Side Sense Enabled Fast Trip Point V_{sns} = 500 mV	–2		40	µA
$I_{IMONNleak}$	IMON1N input leakage	Low Side Sense Disabled Fast Trip Point V_{sns} = 500 mV	–2		2	µA
		Low Side Sense Enabled Fast Trip Point V_{sns} = 500 mV	–200		2	µA
$I_{HIMONPleak}$	HIMONP input leakage	Fast Trip Point V_{sns} = 500 mV			550	µA
$I_{HIMONNleak}$	HIMONN_HVMON input leakage				350	µA
$I_{MONA/B}$ Accuracy[2]	HIMON, IMON1A/B Comparator Trip Point accuracy	Gain = 100x		8		%
		Gain = 50x		5		%
		Gain = 25x		3		%
		Gain = 10x		2		%
$I_{MONA/B}$ Gain	Programmable Gain Setting	Four settings in software		10		V/V
				25		V/V
				50		V/V
				100		V/V
I_{MONF} Accuracy[2]	Fast comparator trip-point accuracy	V_{sns}[1] = 50 mV, 100 mV, or 150 mV		8		%
		V_{sns} = 200 mV, 250 mV, or 300 mV		5		%
		V_{sns} = 400 mV or 500 mV		3		%
t_{IMONF}	Fast comparator response time				1	µs

1. V_{sns} is the differential voltage between IMON1P and IMON1N (or HIMONP and HIMONN).
2. IMON accuracy may degrade based on SSO conditions of FPGA section, especially bank 1. See the System Connections section for more details.

ADC Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
	Resolution			10		Bits
$t_{CONVERT}$	Conversion Time from I^2C Request				200	µs
Voltage Monitors						
$V_{VMON-IN}$	Input Range Full scale	Programmable Attenuator = 1	0		2.048	V
		Programmable Attenuator = 3	0		5.91	
LSB	ADC Step Size	Programmable Attenuator = 1		2		mV
		Programmable Attenuator = 3		6		
$E_{VMON-attenuator}$	Error due to attenuator	Programmable Attenuator = 3		+/– 0.1		%
High Voltage Monitor						
$V_{HVMON-IN}$	Input Range Full scale	Programmable Attenuator = 4	0		8.192	V
		Programmable Attenuator = 8	0		13.21	
LSB	ADC Step Size	Programmable Attenuator = 4		8		mV
		Programmable Attenuator = 8		16		
$E_{HVMON-attenuator}$	Error due to attenuator	Programmable Attenuator = 4		+/–0.2		%
		Programmable Attenuator = 8		+/–0.4		%
Current Monitors						
$t_{IMON-sample}$	Sample period of HVIMON and IMON1 conversions for averaged value	4 Settings via I^2C command		1		ms
				2		
				4		
				8		
$V_{IMON-IN}$	Input Range Full scale[1]	Programmable Gain 10x	0		200	mV
		Programmable Gain 25x	0		80	
		Programmable Gain 50x	0		40	
		Programmable Gain 100x	0		20	
LSB	ADC Step Size	Programmable Gain 10x		0.2		mV
		Programmable Gain 25x		0.08		
		Programmable Gain 50x		0.04		
		Programmable Gain 100x		0.02		

1. Differential voltage applied across HIMONP/IMON1P and HIMONN/IMO1N before programmable gain amplification.

ADC Error Budget Over Entire Operating Temperature Range

Symbol	Parameter	Conditions	Min	Typ	Max	Units
TADC Error	Total ADC Measurement Error at Any Voltage (Differential Analog Inputs)[1, 3]	Measurement Range 600mV - 2.048 V, VMONxGS > -100 mV, Attenuator =1	–8	+/– 4	8	mV
		Measurement Range 600mV - 2.048 V, VMONxGS > –200 mV, Attenuator =1		+/– 6		mV
		Measurement Range 0 - 2.048 V, VMONxGS > –200 mV, Attenuator =1		+/– 10		mV
	Total Measurement Error at Any Voltage (Single-Ended Analog Inputs including IMON)[1, 2, 3]	Measurement Range 600 mV - 2.048 V, Attenuator =1	–8	+/– 4	8	mV

1. Total error, guaranteed by characterization, includes INL, DNL, Gain, Offset, and PSR specs of the ADC.
2. Programmable gain error on IMON not included.
3. ADC accuracy may degrade based on SSO conditions of FPGA section, especially bank 1. See the System Connections section for more details

Temperature Monitors

Symbol	Parameter	Conditions	Min	Typ	Max	Units
T_{MON_REMOTE} Accuracy[1, 7]	Temp Error – Remote Sensor	Ta = –40 to +85 ºC Td = –64 to 127 ºC		1		ºC
T_{MON_INT} Accuracy[7]	Internal Sensor – Relative to ambient[6]	Ta=–40 to +85 ºC		1		ºC
Resolution				0.25		ºC
T_{MON} Range	Programmable threshold range		–64		155	ºC
T_{MON} Offset	Temperature offset	Programmable in software	–63.75		63.75	ºC
T_{MON} Hysteresis	Hysteresis of trip points	Programmable in software	0		63	ºC
t_{TMON_settle}[2]	Temperature measurement settling time[3]	Measurement Averaging Coefficient = 1		15		ms
		Measurement Averaging Coefficient = 8		120		ms
		Measurement Averaging Coefficient = 16		240		ms
T_n	Ideality Factor ***n***	Programmable in software	0.9		2	
T_{limit}	Temperature measurement limit[4]				160	ºC
C_{TMON}	Maximum Capacitance between T_{MONP} and T_{MONN} pins				200	pF
$R_{TMONSeries}$	Equivalent external resistance to sensor[5]				200	ohms

1. Accuracy number is valid for the use of a grounded collector PNP configuration, programmed with proper ideality factor, and 16x measurement filter enabled. Any other device or configuration can have additional errors, including beta, series resistance and ideality factor accuracy. See Temperature Monitor Inputs section for more details.
2. Settling time based on one TMON enabled. For multiple TMONs, settling time can be multiplied by the number of enabled TMON channels.
3. Settling time is defined as the time is takes a step change to settle to within 1% of the measured value.
4. All values above T_{limit} read as 0x3FF over I^2C. There is no cold temperature limiting reading, although performance is not specified below –64 ºC.
5. This is the maximum series resistance which the TMON circuit can compensate out. Equivalent series resistance includes all board trace wiring (TMONP and TMONN) as well as parasitic base and emitter resistances. Re=1/gm should not be included as part of series resistance.
6. Internal sensor is subject to self-heating, dependent on PCB design and device configuration. Self-heating not included in published accuracy.
7. TMON accuracy may degrade based on SSO conditions of FPGA section, especially bank 1. See the System Connections section for more details

High Voltage FET Drivers

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{PP}	Gate driver output voltage	Four settings in software		12		Volts
				10		
				8		
				6		
I_{OUTSRC}	Gate driver source current (HIGH state)	Four settings in software		12.5		µA
				25		
				50		
				100		
$I_{OUTSINK}$	Gate driver sink current (LOW state)	Four settings in software		100		µA
				250		
				500		
				3000		
Frequency	Switched Mode Frequency	Two settings in software		15.625		kHz
				31.25		
Duty Cycle	Switched Mode Programmable Duty Cycle Range	Programmable in software	6.25		93.75	%
	Duty Cycle step size			6.25		%

Margin/Trim DAC Output Characteristics

Symbol	Parameter	Conditions	Min	Typ.	Max.	Units
	Resolution			8 (7 + sign)		Bits
FSR	Full scale range			+/– 320		mV
LSB	LSB step size			2.5		mV
I_{OUT}	Output source/sink current		–200		200	µA
I_{TRIM_Hi-Z}	Tri-state mode leakage			0.1		µA
BPZ	Bipolar zero output voltage (code=80h)	Four settings in software		0.6		V
				0.8		
				1.0		
				1.25		
t_S	TrimCell output voltage settling time[1]	DAC code changed from 80H to FFH or 80H to 00H			2.5	ms
		Single DAC code change		260		µs
C_LOAD	Maximum load capacitance				50	pF
TOSE	Total open loop supply voltage error[2]	Full scale DAC corresponds to +/– 5% supply voltage variation	–1%		+1%	V/V

1. To 1% of set value with 50 pF load connected to trim pins.
2. Total resultant error in the trimmed power supply output voltage referred to any DAC code due to DAC's INL, DNL, gain, output impedance, offset error and bipolar offset error across the temperature, V_{CCA} ranges of the device.

Fault Log / User Tag EEPROM

Symbol	Parameter	Conditions	Min	Typ.	Max.	Units
Records	Number of available fault log records in EEPROM			16		Records
$t_{faultTrigger}$	Minimum active time of trigger signal to start fault recording		64			µs
$t_{faultRecord}$	Time to copy fault record to EEPROM				5	ms

Analog Sense and Control Oscillator

Symbol	Parameter	Conditions	Min	Typ.	Max.	Units
CLK_{ASC}	Internal ASC0 Clock		7.6	8	8.4	MHz
CLK_{ext}	Externally Applied Clock		7.6	8	8.4	MHz

FPGA sysIO Recommended Operating Conditions

Standard	V_{CCIO} (V)			V_{REF} (V)		
	Min.	Typ.	Max.	Min.	Typ.	Max.
LVCMOS 3.3	3.135	3.3	3.465	—	—	—
LVCMOS 2.5	2.375	2.5	2.625	—	—	—
LVCMOS 1.8	1.71	1.8	1.89	—	—	—
LVCMOS 1.5	1.425	1.5	1.575	—	—	—
LVCMOS 1.2	1.14	1.2	1.26	—	—	—
LVTTL	3.135	3.3	3.465	—	—	—
PCI[3]	3.135	3.3	3.465	—	—	—
SSTL25	2.375	2.5	2.625	1.15	1.25	1.35
SSTL18	1.71	1.8	1.89	0.833	0.9	0.969
HSTL18	1.71	1.8	1.89	0.816	0.9	1.08
LVDS25[1, 2]	2.375	2.5	2.625	—	—	—
LVDS33[1, 2]	3.135	3.3	3.465	—	—	—
LVPECL[1]	3.135	3.3	3.465	—	—	—
BLVDS[1]	2.375	2.5	2.625	—	—	—
RSDS[1]	2.375	2.5	2.625	—	—	—
SSTL18D	1.71	1.8	1.89	—	—	—
SSTL25D	2.375	2.5	2.625	—	—	—
HSTL18D	1.71	1.8	1.89	—	—	—

1. Inputs on-chip. Outputs are implemented with the addition of external resistors.
2. LPTM21 has dedicated LVDS buffers.
3. Input on the bottom bank of the LPTM21 only.

FPGA sysIO Single-Ended DC Electrical Characteristics[1, 2]

Input/Output Standard	V_{IL}		V_{IH}		V_{OL} Max. (V)	V_{OH} Min. (V)	I_{OL} Max.[4] (mA)	I_{OH} Max.[4] (mA)
	Min. (V)[3]	Max. (V)	Min. (V)	Max. (V)				
LVCMOS 3.3 LVTTL	–0.3	0.8	2.0	3.6	0.4	V_{CCIO} - 0.4	4	–4
							8	–8
							12	–12
							16	–16
							24	–24
					0.2	V_{CCIO} - 0.2	0.1	–0.1
LVCMOS 2.5	-0.3	0.7	1.7	3.6	0.4	V_{CCIO} - 0.4	4	–4
							8	–8
							12	–12
							16	–16
					0.2	V_{CCIO} - 0.2	0.1	–0.1
LVCMOS 1.8	–0.3	$0.35V_{CCIO}$	$0.65V_{CCIO}$	3.6	0.4	V_{CCIO} - 0.4	4	–4
							8	–8
							12	–12
					0.2	V_{CCIO} - 0.2	0.1	–0.1
LVCMOS 1.5	–0.3	$0.35V_{CCIO}$	$0.65V_{CCIO}$	3.6	0.4	V_{CCIO} - 0.4	4	–4
							8	–8
					0.2	V_{CCIO} - 0.2	0.1	–0.1
LVCMOS 1.2	–0.3	$0.35V_{CCIO}$	$0.65V_{CCIO}$	3.6	0.4	V_{CCIO} - 0.4	4	–2
							8	–6
					0.2	V_{CCIO} - 0.2	0.1	–0.1
PCI	–0.3	$0.3V_{CCIO}$	$0.5V_{CCIO}$	3.6	$0.1V_{CCIO}$	$0.9V_{CCIO}$	1.5	–0.5
SSTL25 Class I	–0.3	V_{REF} - 0.18	V_{REF} + 0.18	3.6	0.54	V_{CCIO} - 0.62	8	8
SSTL25 Class II	–0.3	V_{REF} - 0.18	V_{REF} +0.18	3.6	NA	NA	NA	NA
SSTL18 Class I	–0.3	V_{REF} - 0.125	V_{REF} +0.125	3.6	0.40	V_{CCIO} - 0.40	8	8
SSTL18 Class II	–0.3	V_{REF} - 0.125	V_{REF} +0.125	3.6	NA	NA	NA	NA
HSTL18 Class I	–0.3	V_{REF} - 0.1	V_{REF} +0.1	3.6	0.40	V_{CCIO} - 0.40	8	8
HSTL18 Class II	–0.3	V_{REF} - 0.1	V_{REF} +0.1	3.6	NA	NA	NA	NA

1. Platform Manager 2 devices allow LVCMOS inputs to be placed in I/O banks where V_{CCIO} is different from what is specified in the applicable JEDEC specification. This is referred to as a ratioed input buffer. In a majority of cases this operation follows or exceeds the applicable JEDEC specification. The cases where Platform Manager 2 devices do not meet the relevant JEDEC specification are documented in the table below.
2. Platform Manager 2 devices allow for LVCMOS referenced I/Os which follow applicable JEDEC specifications. For more details about mixed mode operation please refer to please refer to TN1202, MachXO2 sysIO Usage Guide.
3. The I^2C pins SCL_M and SDA_M are limited to a V_{IL} min of –0.25V or to –0.3V with a duration of <10ns.
4. The average DC current drawn by I/Os between GND connections, or between the last GND in an I/O bank and the end of an I/O bank, as shown in the logic signal connections table shall not exceed n * 8mA. Where n is the number of I/Os between bank GND connections or between the last GND in a bank and the end of a bank.

Input Standard	V_{CCIO} (V)	V_{IL} Max. (V)
LVCMOS 33	1.5	0.685
LVCMOS 25	1.5	0.687
LVCMOS 18	1.5	0.655

FPGA sysIO Differential Electrical Characteristics

The LVDS differential output buffers are available on the top side of the LPTM21 device.

LVDS

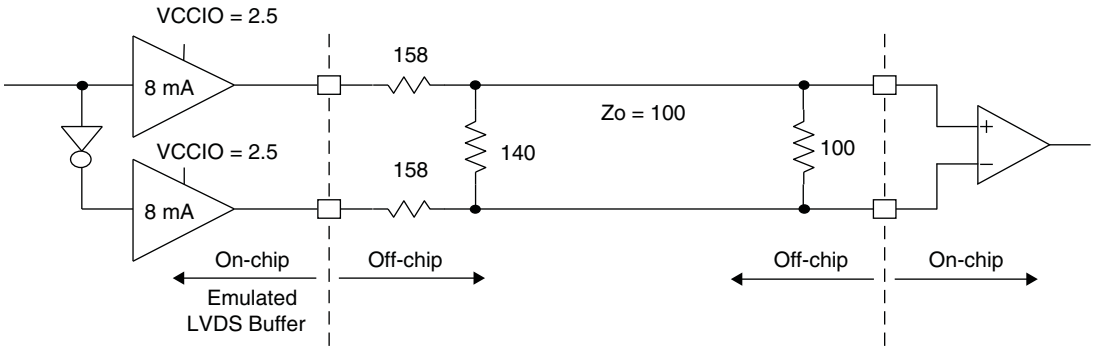
Over Recommended Operating Conditions

Parameter Symbol	Parameter Description	Test Conditions	Min.	Typ.	Max.	Units
V_{INP}, V_{INM}	Input Voltage	V_{CCIO} = 3.3	0	—	2.605	V
		V_{CCIO} = 2.5	0	—	2.05	V
V_{THD}	Differential Input Threshold		±100	—		mV
V_{CM}	Input Common Mode Voltage	V_{CCIO} = 3.3V	0.05	—	2.6	V
		V_{CCIO} = 2.5V	0.05	—	2.0	V
I_{IN}	Input current	Power on	—	—	±10	µA
V_{OH}	Output high voltage for V_{OP} or V_{OM}	R_T = 100 Ohm	—	1.375	—	V
V_{OL}	Output low voltage for V_{OP} or V_{OM}	R_T = 100 Ohm	0.90	1.025	—	V
V_{OD}	Output voltage differential	(V_{OP} - V_{OM}), R_T = 100 Ohm	250	350	450	mV
ΔV_{OD}	Change in V_{OD} between high and low		—	—	50	mV
V_{OS}	Output voltage offset	(V_{OP} - V_{OM})/2, R_T = 100 Ohm	1.125	1.20	1.395	V
ΔV_{OS}	Change in V_{OS} between H and L		—	—	50	mV
I_{OSD}	Output short circuit current	V_{OD} = 0V driver outputs shorted	—	—	24	mA

LVDS Emulation

FPGA section outputs can support LVDS outputs via emulation (LVDS25E). The output is emulated using complementary LVCMOS outputs in conjunction with resistors across the driver outputs on all devices. The scheme shown in Figure 3 is one possible solution for LVDS standard implementation. Resistor values in Figure 3 are industry standard values for 1% resistors.

Figure 3. LVDS Using External Resistors (LVDS25E)



Note: All resistors are ±1%.

Table 2. LVDS25E DC Conditions

Over Recommended Operating Conditions

Parameter	Description	Typ.	Units
Z_{OUT}	Output impedance	20	Ohms
R_S	Driver series resistor	158	Ohms
R_P	Driver parallel resistor	140	Ohms
R_T	Receiver termination	100	Ohms
V_{OH}	Output high voltage	1.43	V
V_{OL}	Output low voltage	1.07	V
V_{OD}	Output differential voltage	0.35	V
V_{CM}	Output common mode voltage	1.25	V
Z_{BACK}	Back impedance	100.5	Ohms
I_{DC}	DC output current	6.03	mA

BLVDS

FPGA section outputs support the BLVDS standard through emulation. The output is emulated using complementary LVCMOS outputs in conjunction with resistors across the driver outputs. The input standard is supported by the LVDS differential input buffer. BLVDS is intended for use when multi-drop and bi-directional multi-point differential signaling is required. The scheme shown in Figure 4 is one possible solution for bi-directional multi-point differential signals.

Figure 4. BLVDS Multi-point Output Example

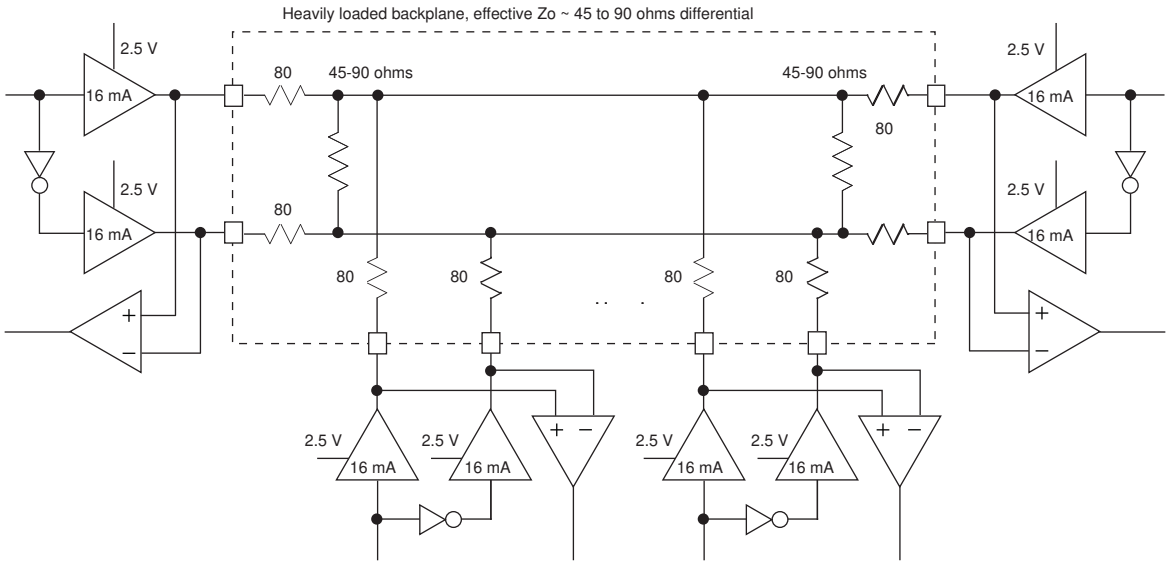


Table 3. BLVDS DC Conditions[1]

Over Recommended Operating Conditions

Symbol	Description	Nominal		Units
		Zo = 45	Zo = 90	
Z_{OUT}	Output impedance	10	10	Ohms
R_S	Driver series resistance	80	80	Ohms
R_{TLEFT}	Left end termination	45	90	Ohms
R_{TRIGHT}	Right end termination	45	90	Ohms
V_{OH}	Output high voltage	1.376	1.480	V
V_{OL}	Output low voltage	1.124	1.020	V
V_{OD}	Output differential voltage	0.253	0.459	V
V_{CM}	Output common mode voltage	1.250	1.250	V
I_{DC}	DC output current	11.236	10.204	mA

1. For input buffer, see LVDS table.

LVPECL

FPGA section outputs support the differential LVPECL standard through emulation. This output standard is emulated using complementary LVCMOS outputs in conjunction with resistors across the driver outputs on all the devices. The LVPECL input standard is supported by the LVDS differential input buffer. The scheme shown in Figure 5 is one possible solution for point-to-point signals.

Figure 5. Differential LVPECL

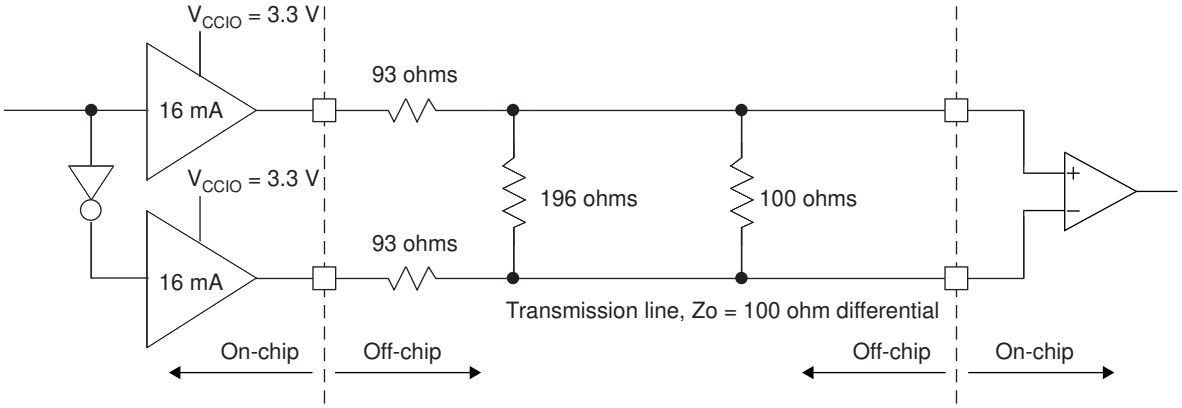


Table 4. LVPECL DC Conditions[1]

Over Recommended Operating Conditions

Symbol	Description	Nominal	Units
Z_{OUT}	Output impedance	10	Ohms
R_S	Driver series resistor	93	Ohms
R_P	Driver parallel resistor	196	Ohms
R_T	Receiver termination	100	Ohms
V_{OH}	Output high voltage	2.05	V
V_{OL}	Output low voltage	1.25	V
V_{OD}	Output differential voltage	0.80	V
V_{CM}	Output common mode voltage	1.65	V
Z_{BACK}	Back impedance	100.5	Ohms
I_{DC}	DC output current	12.11	mA

1. For input buffer, see LVDS table.

For further information on LVPECL, BLVDS and other differential interfaces please see details of additional technical documentation at the end of the data sheet.

RSDS

FPGA section outputs support the differential RSDS standard. The output standard is emulated using complementary LVCMOS outputs in conjunction with resistors across the driver outputs on all the devices. The RSDS input standard is supported by the LVDS differential input buffer. The scheme shown in Figure 6 is one possible solution for RSDS standard implementation. Use LVDS25E mode with suggested resistors for RSDS operation. Resistor values in Figure 6 are industry standard values for 1% resistors.

Figure 6. RSDS (Reduced Swing Differential Standard)

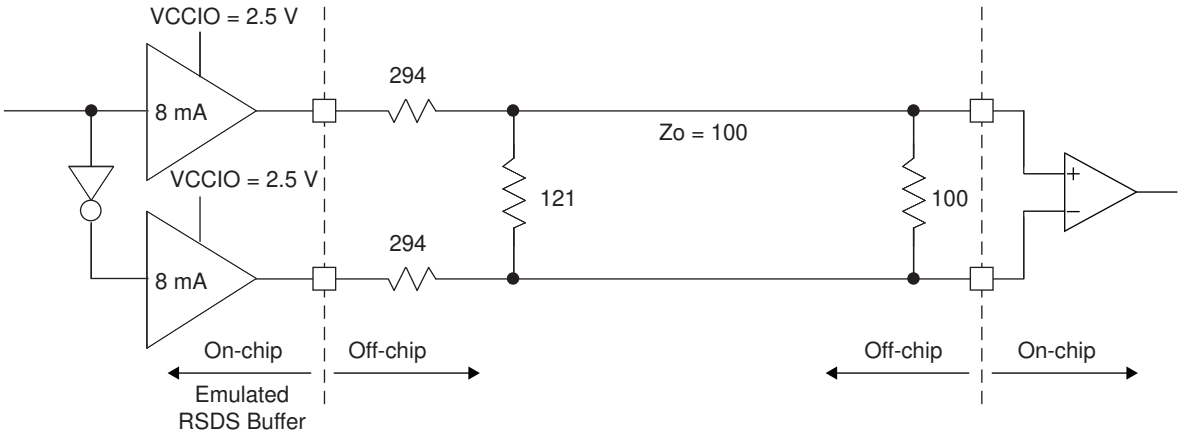


Table 5. RSDS DC Conditions

Parameter	Description	Typical	Units
Z_{OUT}	Output impedance	20	Ohms
R_S	Driver series resistor	294	Ohms
R_P	Driver parallel resistor	121	Ohms
R_T	Receiver termination	100	Ohms
V_{OH}	Output high voltage	1.35	V
V_{OL}	Output low voltage	1.15	V
V_{OD}	Output differential voltage	0.20	V
V_{CM}	Output common mode voltage	1.25	V
Z_{BACK}	Back impedance	101.5	Ohms
I_{DC}	DC output current	3.66	mA

Typical Building Block Function Performance[1]

Pin-to-Pin Performance (LVCMOS25 12 mA Drive)

Function	Timing	Units
Basic Functions		
16-bit decoder	8.9	ns
4:1 MUX	7.5	ns
16:1 MUX	8.3	ns

Register-to-Register Performance

Function	Timing	Units
Basic Functions		
16:1 MUX	412	MHz
16-bit adder	297	MHz
16-bit counter	324	MHz
64-bit counter	161	MHz
Embedded Memory Functions		
1024x9 True-Dual Port RAM (Write Through or Normal, EBR output registers)	183	MHz
Distributed Memory Functions		
16x4 Pseudo-Dual Port RAM (one PFU)	500	MHz

1. The above timing numbers are generated using the Diamond design tool. Exact performance may vary with device and tool version. The tool uses internal parameters that have been characterized but are not tested on every device.

FPGA External Switching Characteristics[1, 2, 3]

Over Recommended Operating Conditions

Symbol	Parameter	Device	Min	Max.	Units
Primary Clocks					
f_{MAX_PR}[4]	Frequency for Primary Clock Tree	LPTM21		388	MHz
t_{W_PRI}	Clock Pulse Width for Primary Clock	LPTM21	0.5		ns
t_{SKEW_PRI}	Primary Clock Skew Within a Device	LPTM21		868	ps
Pin-LUT-Pin Propagation Delay					
t_{PD}	Best case propagation delay through one LUT-4	LPTM21		6.72	ns
General I/O Pin Parameters					
t_{CO}	Clock to Output – PIO Output Register	LPTM21		7.44	ns
t_{SU}	Clock to Data Setup – PIO Input Register	LPTM21	–0.17		ns
t_{H}	Clock to Data Hold – PIO Input Register	LPTM21	1.88		ns
t_{SU_DEL}	Clock to Data Setup – PIO Input Register with Data Input Delay	LPTM21	1.63		ns
t_{H_DEL}	Clock to Data Hold – PIO Input Register with Input Data Delay	LPTM21	–0.24		ns
f_{MAX_IO}	Clock Frequency of I/O and PFU Register	LPTM21		388	MHz

1. Exact performance may vary with device and design implementation.
2. General I/O timing numbers based on LVCMOS 2.5, 8 mA, 0pf load.
3. The t_{SU_DEL} and t_{H_DEL} values use the SCLK_ZERHOLD default step size. Each step is 105 ps.
4. This number for general purpose usage. Duty cycle tolerance is +/–10%.

sysCLOCK PLL Timing

Over Recommended Operating Condition

Parameter	Descriptions	Conditions	Min.	Max.	Units
f_{IN}	Input Clock Frequency (CLKI, CLKFB)		7	400	MHz
f_{OUT}	Output Clock Frequency (CLKOP, CLKOS, CLKOS2)		1.5625	400	MHz
f_{OUT2}	Output Frequency (CLKOS3 cascaded from CLKOS2)		0.0122	400	MHz
f_{VCO}	PLL VCO Frequency		200	800	MHz
f_{PFD}	Phase Detector Input Frequency		7	400	MHz
AC Characteristics					
t_{DT}	Output Clock Duty Cycle	Without duty trim selected[3]	45	55	%
t_{DT_TRIM}[7]	Edge Duty Trim Accuracy		–75	75	%
t_{PH}[4]	Output Phase Accuracy		–6	6	%

sysCLOCK PLL Timing (Cont.)

Over Recommended Operating Condition

Parameter	Descriptions	Conditions	Min.	Max.	Units
t_{OPJIT}[1, 8]	Output Clock Period Jitter	f_{OUT} > 100MHz	—	150	ps p-p
		f_{OUT} < 100MHz	—	0.007	UIPP
	Output Clock Cycle-to-cycle Jitter	f_{OUT} > 100MHz	—	180	ps p-p
		f_{OUT} < 100MHz	—	0.009	UIPP
	Output Clock Phase Jitter	f_{PFD} > 100MHz	—	160	ps p-p
		f_{PFD} < 100MHz	—	0.011	UIPP
	Output Clock Period Jitter (Fractional-N)	f_{OUT} > 100MHz	—	230	ps p-p
		f_{OUT} < 100MHz	—	0.12	UIPP
	Output Clock Cycle-to-cycle Jitter (Fractional-N)	f_{OUT} > 100MHz	—	230	ps p-p
		f_{OUT} < 100MHz	—	0.12	UIPP
t_{SPO}	Static Phase Offset	Divider ratio = integer	–120	120	ps
t_W	Output Clock Pulse Width	At 90% or 10%[3]	0.9	—	ns
t_{LOCK}[2, 5]	PLL Lock-in Time		—	15	ms
t_{UNLOCK}	PLL Unlock Time		—	50	ns
t_{IPJIT}[6]	Input Clock Period Jitter	$f_{PFD} \geq$ 20 MHz	—	1,000	ps p-p
		f_{PFD} < 20 MHz	—	0.02	UIPP
t_{HI}	Input Clock High Time	90% to 90%	0.5	—	ns
t_{LO}	Input Clock Low Time	10% to 10%	0.5	—	ns
t_{STABLE}[5]	STANDBY High to PLL Stable		—	15	ms
t_{RST}	RST/RESETM Pulse Width		1	—	ns
t_{RSTREC}	RST Recovery Time		1	—	ns
t_{RST_DIV}	RESETC/D Pulse Width		10	—	ns
t_{RSTREC_DIV}	RESETC/D Recovery Time		1	—	ns
$t_{ROTATE-SETUP}$	PHASESTEP Setup Time		10	—	ns
t_{ROTATE_WD}	PHASESTEP Pulse Width		4	—	VCO Cycles

1. Period jitter sample is taken over 10,000 samples of the primary PLL output with a clean reference clock. Cycle-to-cycle jitter is taken over 1000 cycles. Phase jitter is taken over 2000 cycles. All values per JESD65B.
2. Output clock is valid after t_{LOCK} for PLL reset and dynamic delay adjustment.
3. Using LVDS output buffers.
4. CLKOS as compared to CLKOP output for one phase step at the maximum VCO frequency. See TN1199, MachXO2 sysCLOCK PLL Design and Usage Guide for more details.
5. At minimum $f_{PFD.}$ As the f_{PFD} increases the time will decrease to approximately 60% the value listed.
6. Maximum allowed jitter on an input clock. PLL unlock may occur if the input jitter exceeds this specification. Jitter on the input clock may be transferred to the output clocks, resulting in jitter measurements outside the output specifications listed in this table.
7. Edge Duty Trim Accuracy is a percentage of the setting value. Settings available are 70 ps, 140 ps, and 280 ps in addition to the default value of none.
8. Jitter values measured with the internal oscillator operating. The jitter values will increase with loading of the PLD fabric and in the presence of SSO noise.