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PREPARED BY : DATE	SHARP	SPEC No. LD-24311A
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	DISPLAY DEVICE BUSINESS GROUP SHARP CORPORATION	PAGE : 31pages
	SPECIFICATION	APPLICABLE GROUP DISPLAY DEVICE BUSINESS GROUP

REVISION :

DEVICE SPECIFICATION FOR

TFT-LCD Module

MODEL No.

LQ043T1DG28

These parts have corresponded with the RoHS directive.

☐ CUSTOMER'S APPROVAL

BY _____

BY J.Kawanishi

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SHARP CORPORATION

RECORDS OF REVISION

LQ043T1DG28

SPEC No.	DATE	REVISED No	PAGE	SUMMARY	NOTE
LD-24311A	2012/4/23	A		–	

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1. Applicable Scope

This specification is applicable to TFT-LCD Module “LQ043T1DG28”.

2. General Description

This module is a color active matrix LCD module incorporating amorphous silicon TFT (Thin Film Transistor). It is composed of a color TFT-LCD panel, driver IC , Input FPC, a back light unit and touch panel. Graphics and texts can be displayed on a 480 x 272 x RGB dots panel with about 262k colors by supplying 18bit data signals (6bit x RGB), four timing signals, 3wires 24bit serial interface signals, logic (Typ. +3.3V), analog (Typ. +3.3V) supply voltages for TFT-LCD panel driving and supply voltage for back light.

3. Mechanical (Physical) Specifications

Item	Specifications	Unit
Screen size	10.9 (4.3” type) diagonal	cm
Active area	95.04 (H) × 53.856 (V)	mm
Pixel format	480 (H) x 272 (V)	pixel
	1Pixel =R+G+B dots	-
Pixel pitch	0.198 (H) x 0.198 (V)	mm
Pixel configuration	R,G,B horizontal stripes	-
Display mode	Normally white	-
Unit outline dimensions	105.5 (W) x 67.2 (H) x 4.2 (D)	mm
Mass	About 51	g
Surface hardness	2H	-
Surface treatment	Anti glare	-

※The above-mentioned table indicates module sizes without some projections and FPC.
For detailed measurements and tolerances, please refer to 18. Outline Dimensions.

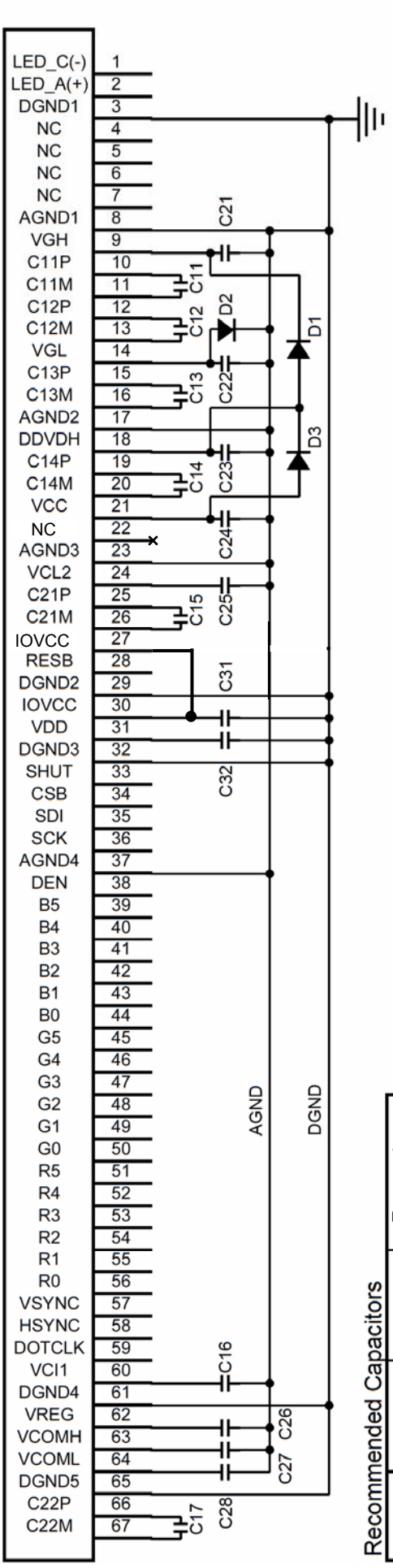
4. Input Terminal Names and Functions

Recommendation CN：[HIROSE] FH26G-67S-0.3SHBW(05) or [KYOCERA ELCO] 00 6281 067 2X2 829 +

Pin No	Symbol	I/O	Description	Remarks
1	LED_C (-)	-	Power supply for LED (Cathode)	
2	LED_A(+)	-	Power supply for LED (Anode)	
3	DGND1	-	Digital Ground	
4	X1(R)	O	Touch Panel Right Electrode	
5	Y2(B)	O	Touch Panel Bottom Electrode	
6	X2(L)	O	Touch Panel Left Electrode	
7	Y1(T)	O	Touch Panel Top Electrode	
8	AGND1	-	Analog Ground	
9	VGH	-	Connect a Stabilizing capacitor to GND	Note 4-1
10	C11P	-	Connect a Booster capacitor to C11M	Note 4-1
11	C11M	-	Connect a Booster capacitor to C11P	Note 4-1
12	C12P	-	Connect a Booster capacitor to C12M	Note 4-1
13	C12M	-	Connect a Booster capacitor to C12P	Note 4-1
14	VGL	-	Connect a Stabilizing capacitor to GND	Note 4-1
15	C13P	-	Connect a Booster capacitor to C13M	Note 4-1
16	C13M	-	Connect a Booster capacitor to C13P	Note 4-1
17	AGND2	-	Analog Ground	
18	DDVDH	-	Connect a Stabilizing capacitor to GND	Note 4-1
19	C14P	-	Connect a Booster capacitor to C14M	Note 4-1
20	C14M	-	Connect a Booster capacitor to C14P	Note 4-1
21	VCC	-	Booster input voltage pin	
22	NC	-	No connection	
23	AGND3	-	Analog Ground	
24	VCL2	-	Connect a Stabilizing capacitor to GND	Note 4-1
25	C21P	-	Connect a Booster capacitor to C21M	Note 4-1
26	C21M	-	Connect a Booster capacitor to C21P	Note 4-1
27	IOVCC	-	Voltage input pin for logic I/O	Note 4-1
28	RESB	I	System reset	
29	DGND2	-	Digital Ground	
30	IOVCC	-	Voltage input pin for logic I/O	
31	VDD	-	Connect a Stabilizing capacitor to GND	Note 4-1
32	DGND3	-	Digital Ground	
33	SHUT	I	Sleep mode control	
34	CSB	I	Chip select pin of serial interface	
35	SDI	I	Data input pin in serial mode	
36	SCK	I	Clock input pin in serial mode	
37	AGND4	-	Analog Ground	Note 4-1
38	DEN	I	Display enable signal	
39	B5	I	BLUE data signal(MSB)	
40	B4	I	BLUE data signal	
41	B3	I	BLUE data signal	

Pin No.	Symbol	I/O	Description	Remarks
42	B2	I	BLUE data signal	
43	B1	I	BLUE data signal	
44	B0	I	BLUE data signal(LSB)	
45	G5	I	GREEN data signal(MSB)	
46	G4	I	GREEN data signal	
47	G3	I	GREEN data signal	
48	G2	I	GREEN data signal	
49	G1	I	GREEN data signal	
50	G0	I	GREEN data signal(LSB)	
51	R5	I	RED data signal(MSB)	
52	R4	I	RED data signal	
53	R3	I	RED data signal	
54	R2	I	RED data signal	
55	R1	I	RED data signal	
56	R0	I	RED data signal(LSB)	
57	VSYNC	I	Frame synchronization signal	
58	HSYNC	I	Line synchronization signal	
59	DOTCLK	I	Dot-clock signal	
60	VCI1	-	Connect a Stabilizing capacitor to GND	Note 4-1
61	DGND4	-	Digital Ground	
62	VREG	-	Connect a Stabilizing capacitor to GND	Note 4-1
63	VCOMH	-	Connect a Stabilizing capacitor to GND	Note 4-1
64	VCOML	-	Connect a Stabilizing capacitor to GND	Note 4-1
65	DGND5	-	Digital Ground	
66	C22P	-	Connect a Booster capacitor to C22M	Note 4-1
67	C22M	-	Connect a Booster capacitor to C22P	Note 4-1

[Note 4-1] Recommended Capacitors and Diodes



Recommended Capacitors

Ref No.	Capacitance	Rated Voltage	Temperature Characteristic
C11	1 µF	6.3 V	B(JIS) or X5R(EIA)
C12	1 µF	6.3 V	B(JIS) or X5R(EIA)
C13	1 µF	6.3 V	B(JIS) or X5R(EIA)
C14	1 µF	6.3 V	B(JIS) or X5R(EIA)
C15	1 µF	10 V	B(JIS) or X5R(EIA)
C16	2.2 µF	6.3 V	B(JIS) or X5R(EIA)
C17	1 µF	10 V	B(JIS) or X5R(EIA)
C21	2.2 µF	25 V	B(JIS) or X5R(EIA)
C22	2.2 µF	25 V	B(JIS) or X5R(EIA)
C23	4.7 µF	10 V	B(JIS) or X5R(EIA)
C24	2.2 µF	6.3 V	B(JIS) or X5R(EIA)
C25	4.7 µF	6.3 V	B(JIS) or X5R(EIA)
C26	4.7 µF	10 V	B(JIS) or X5R(EIA)
C27	4.7 µF	10 V	B(JIS) or X5R(EIA)
C28	4.7 µF	6.3 V	B(JIS) or X5R(EIA)
C31	2.2 µF	6.3 V	B(JIS) or X5R(EIA)
C32	2.2 µF	6.3 V	B(JIS) or X5R(EIA)
D1	Schottky diode	VF＜0.38V/5mA@25°C, VR≧25V	
D2	Schottky diode	VF＜0.38V/5mA@25°C, VR≧25V	
D3	Schottky diode	VF＜0.38V/5mA@25°C, VR≧25V	

[Note]
C11P/M, C12P/M, C13P/M, C14P/M, C21P/M, C22P/M are high voltage switching lines on FPC.
Surround/shield by AGND to avoid noise coupling to other pins.
Also aware the PCB design to avoid other components to be affected by noise on those dcdc pins.

5. Absolute Maximum Ratings

Item	Symbol	Conditions	Rated value	Unit	Remarks
Input voltage	VI	Ta = 25°C	-0.3 ~ IOVCC+0.3	V	Note 5-1
Logic I/O power supply voltage	IOVCC	Ta = 25°C	-0.3 ~ +4.0	V	
Analog power supply voltage	VCC	Ta = 25°C	AGND-0.3 ~ +4.6	V	
Temperature for storage	Tstg	-	-30~ +85	°C	Note 5-2
Temperature for operation	Topr	-	-10 ~ +70	°C	Note 5-2, 5-3
LED input electric current	I_{LED}	Ta = 25°C	35	mA	Note 5-4
LED electricity consumption	P_{LED}	Ta = 25°C	123	mW	Note 5-4

[Note 5-1] RESB, SHUT, CSB, SDI, SCK, DEN, B5~B0, G5~G0, R5~R0, VSYNC, HSYNC, DOTCLK

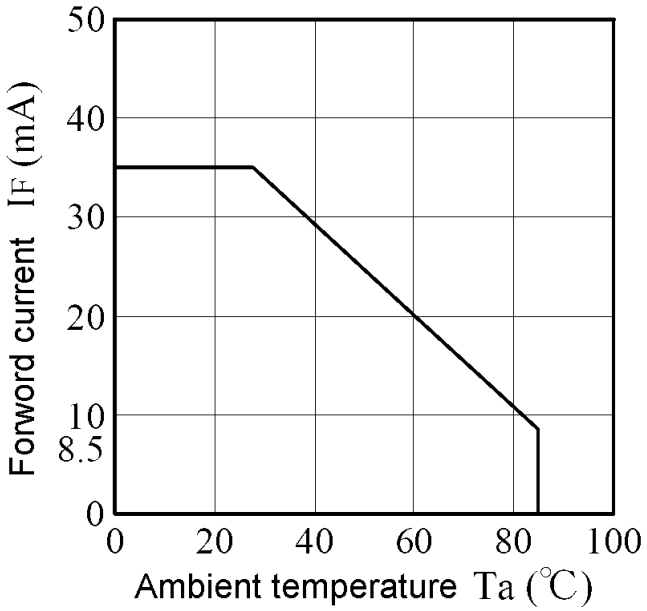
[Note 5-2] Humidity: 95%RH Max. (Ta≦40°C)

Maximum bulb temperature under 39°C (Ta>40°C) See to it that no dew will be condensed.

[Note 5-3] The high temperature is the panel surface temperature regulations.

[Note 5-4] Power consumption of one LED (Ta = 25°C).

Ambient temperature and the maximum input are fulfilling the following operating conditions.



6. Electrical Characteristics

6-1. TFT LCD Panel Driving

Ta = 25°C

Item		Symbol	Min.	Typ.	Max.	Unit	Remarks
Logic I/O power supply	DC voltage	IOVCC	+3.0	+3.3	+3.6	V	
	DC current	I_{IOVCC}	-	0.1	0.2	mA	Note 6-1
Analog power supply	DC voltage	VCC	+3.2	+3.3	+3.4	V	Note 6-1 Note 6-6
	DC current	I_{VCC}	-	16	24	mA	Note 6-3
Permissive input Ripple voltage		$V_{RFIOVCC}$	-	-	100	mVp-p	Note 6-4
		V_{RFVCC}	-	-	100	mVp-p	Note 6-4
Logic Input Voltage	High	V_{IH}	0.8xIOVCC	-	IOVCC	V	Note 6-5
	Low	V_{IL}	0	-	0.2xIOVCC	V	Note 6-5
Logic input Current		I_{IH} / I_{IL}	-1	-	1	μA	Note 6-5

[Note 6-1] IOVCC = +3.3V, VCC = +3.3V, f_{VSYNC} = 60Hz

Current situation for I_{IOVCC}: Black & White checker flag pattern

[Note 6-2] Refer to Recommended Capacitors and Register setting.

[Note 6-3] IOVCC = +3.3V, VCC = +3.3V, f_{VSYNC} = 60Hz

Current situation for I_{VCC}: All black pattern

[Note 6-4] IOVCC = +3.3V, VCC = +3.3V

[Note 6-5] RESB, SHUT, CSB, SDI, SCK, DEN, B5~B0, G5~G0, R5~R0, VSYNC, HSYNC, DOTCLK

[Note 6-6] When it is out of the above recommended operating voltage, for example, in case of

+3.0V≦VCC＜+3.3V, +3.4V＜VCC≦+3.6V, the module does not break.

But the deterioration of display quality, flicker etc., may be occurred.

6-2. Register Setting

IOVCC and VCC ON (※hold RESB = “L”, hold SHUT = “H”)

↓

Wait min. 1ms

↓

Hard Reset (RESB “L” → “H”)

↓

Wait max.100us

↓

Display Data Start (DOTCLK, HSYNC, VSYNC)

↓

Register Setting (※)

Reg.#	Register	Data (Gamma2.2)	Remark
R00 h	Panel Driving Control	0013 h	Note 6-7
R01 h	Power Control 1	9A09 h	
R02 h	Power Control 2	9A11 h	
R03 h	Power Control 3	1100 h	
R04 h	Power Control 4	1100 h	
R05 h	Power Control 5	0232 h	
R06 h	Horizontal Back Porch Control	000E h	Note 6-8
R07 h	Vertical Back Porch Control	0004 h	Note 6-9
R09 h	Interface Control	0001 h	
R0A h	Power Control 6	1A61 h	
R0B h	Power Control 7	FF9B h	
R0C h	Power Control 8	00B0 h	
R0D h	Power Control 9	CA53 h	
R0E h	Power Control 10	CA53 h	
R10 h	Gamma Set 1	0616 h	
R11 h	Gamma Set 2	7916 h	
R12 h	Gamma Set 3	0805 h	
R13 h	Gamma Set 4	0217 h	
R14 h	Gamma Set 5	3121 h	
R15 h	Gamma Set 6	1707 h	
R16 h	Gamma Set 7	750F h	
R17 h	Gamma Set 8	1B0D h	
R18 h	Gamma Set 9	0106 h	
R19 h	Gamma Set 10	1112 h	

↓

Wait min. 5ms

↓

Sleep mode →Normal mode conversion (SHUT “H” → “L”)

↓

Wait min.10 frame

↓

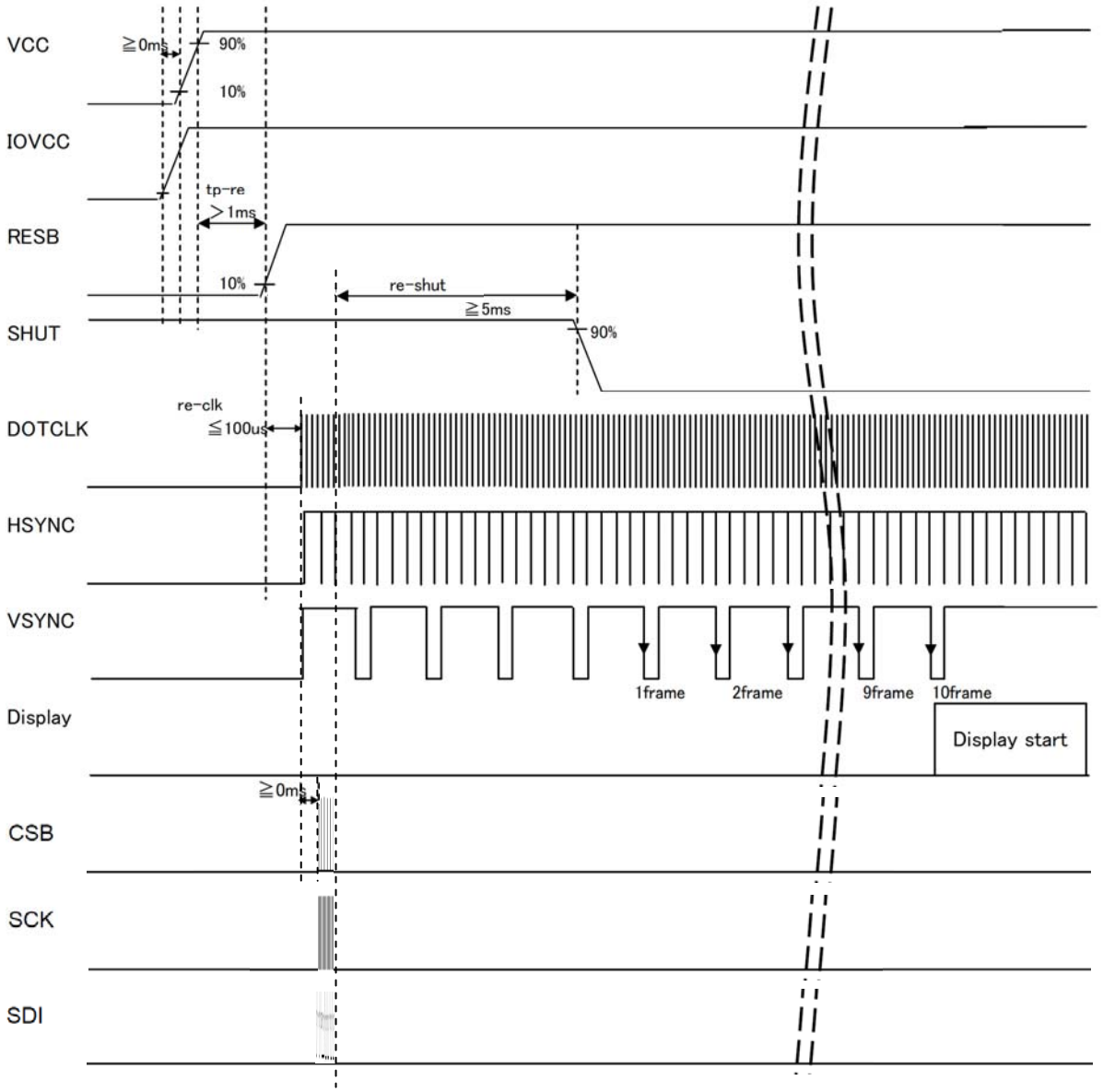
Back light ON

↓

Display ON

※If a setting other than the Register setting is captured temporarily due to disturbances such as electrostatic discharge, the normal display is restored by transmitting the recommended setting again.

(At this time, it is not necessary to turn on the power again or perform initializing with RESB.)



Characteristics	symbol	Min	Typ	Max	Units
VCC on to rising edge of RESB	tp-re	1	-	-	ms
Register set to Falling edge of SHUT	re-shut	5	-	-	ms
RESB on to rising edge of DOTCLK	re-clk	-	-	100	usec
Falling edge of SHUT to display start	tshut-on	-	-	10	frame
-- 1 line: 512 clk -- 1 frame: 278 line -- PIXCLK = 8.5MHz		-	167	-	msec

※Display starts at 10th falling edge of VSYNC after the falling edge of SHUT.

[Note 6-7]

Panel Driving Control (R00h)

R/W	DC	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	RL	0	0	0	0	TB	0	0	0	0	1	0	0	1	1
POR		0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	1

TB: Selects the output shift direction of the gate driver.

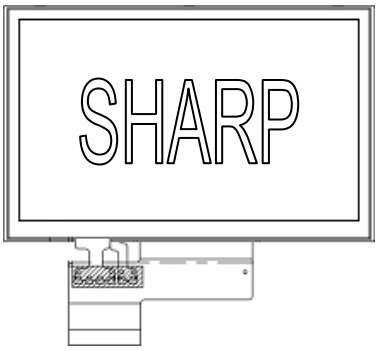
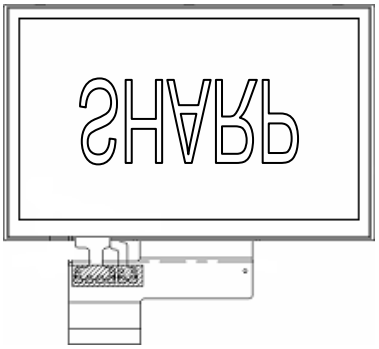
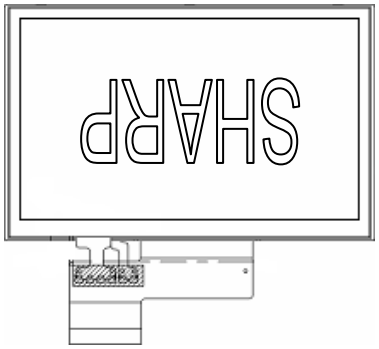
When TB = “0”, Top shifts to Bottom.

When TB = “1”, Bottom shifts to Top.

RL: Selects the output shift direction of the source driver.

When RL =”0”, Left shifts to Right.

When RL =“1”, Right shifts to Left.

	RL = “0”	RL = “1”
TB = “0”		
TB = “1”		

[Note 6-8]

Horizontal Back Porch Control (R06h)

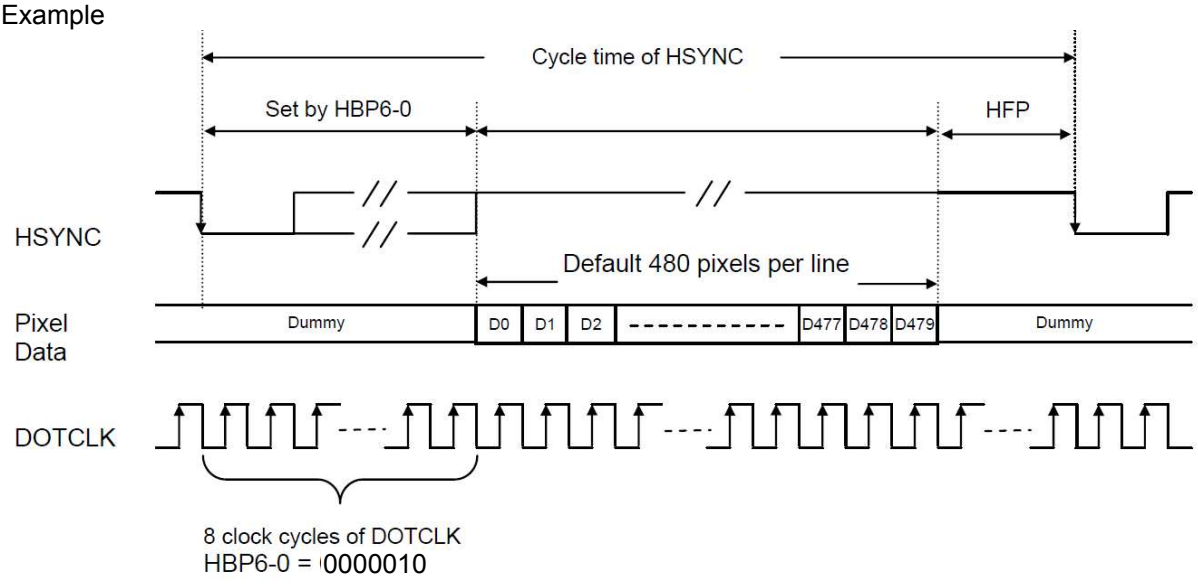
R/W	DC	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	0	HBP6	HBP5	HBP4	HBP3	HBP2	HBP1	HBP0
POR		0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0

Number of DOTCLK for HSYNC active low period must be smaller than that of HBP.

HBP6-0: Set the delay period from falling edge of HSYNC signal to first valid data.

HBP6	HBP5	HBP4	HBP3	HBP2	HBP1	HBP0	No. of clock cycle of DOTCLK
0	0	0	0	1	0	0	2
0	0	0	0	1	0	1	3
0	0	0	0	1	1	0	4
0	0	0	0	1	1	1	5
0	0	0	0	0	0	0	6
0	0	0	0	0	0	1	7
0	0	0	0	0	1	0	8
0	0	0	0	0	1	1	9
0	0	0	1	1	0	0	10
				:			: Step = 1 :
1	1	1	0	0	1	1	121
1	1	1	1	1	0	0	122
1	1	1	1	1	0	1	123
1	1	1	1	1	1	0	124
1	1	1	1	1	1	1	125
1	1	1	1	0	0	0	126
1	1	1	1	0	0	1	127
1	1	1	1	0	1	0	128
1	1	1	1	0	1	1	129

Example



[Note 6-9]

Vertical Back Porch Control (R07h)

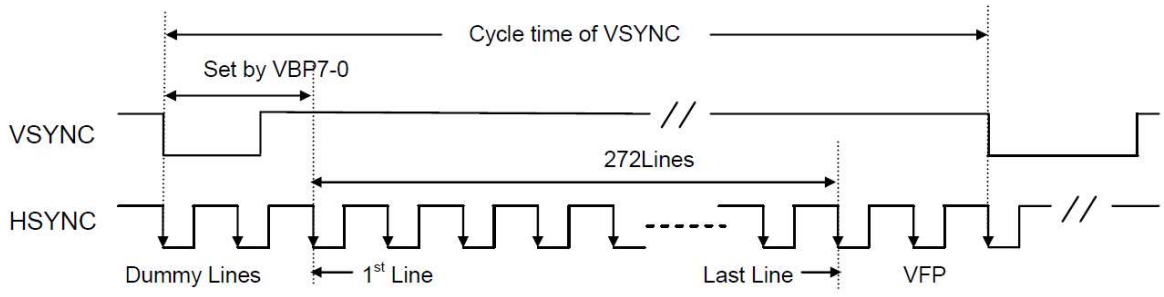
R/W	DC	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	VBP7	VBP6	VBP5	VBP4	VBP3	VBP2	VBP1	VBP0
POR		0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

VBP7-0: Set the delay period from falling edge of VSYNC to first valid line.

The line data within this delay period will be treated as dummy line.

VBP7	VBP6	VBP5	VBP4	VBP3	VBP2	VBP1	VBP0	No. of clock cycle of HSYNC
0	0	0	0	0	0	0	0	Setting inhibited
0	0	0	0	0	0	0	1	1
0	0	0	0	0	0	1	0	2
0	0	0	0	0	0	1	1	3
0	0	0	0	0	1	0	0	4
			:					: Step = 1 :
1	1	1	0	0	0	0	0	224
1	1	1	0	0	0	0	1	225
1	1	1	1	*	*	*	*	Reserved

Example; VBP = 2 line



6-3. Power Down Sequence

Back light OFF

↓

Normal mode →Sleep mode conversion (SHUT “L” → “H”)

↓

Wait min.10 frame time

↓

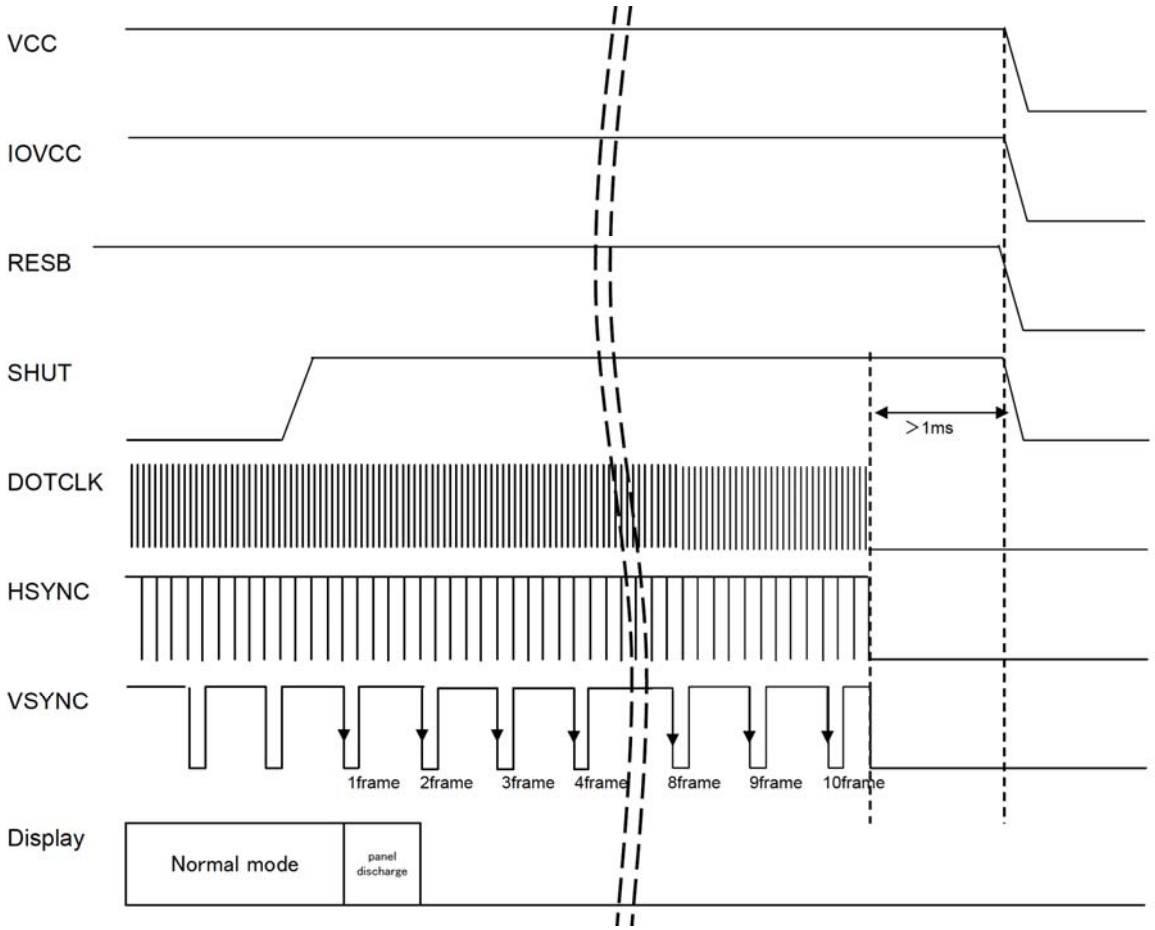
Display Data Stop (VSYNC, HSYNC, DOTCLK)

↓

Wait min.1ms

↓

VCC,IOVCC OFF



Characteristics	symbol	Min	Typ	Max	Units
Rising edge of SHUT to input-signal off	Tshut-dotclk Off	10	-	-	frame
-- 1 line: 512 clk -- 1 frame: 278 line -- PIXCLK = 8.5MHz		167	-	-	msec
Input-signal-off to IOVCC off	toff-vdd	1	-	-	ms

Note1) DOTCLK/HSYNC/VSYNC must be maintained at least 10 frames after the rising edge of SHUT.

Note2) Display become off at the 2nd falling edge of VSYNC after the rising edge of SHUT.

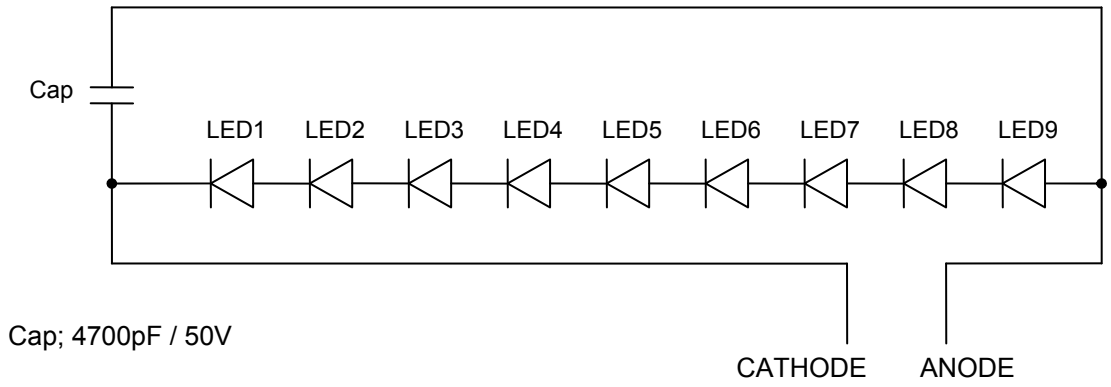
6-4. Back light driving

The back light system has 9 pieces LED

[LED] NSSW006T (Nichia)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remark
Rated Voltage	V_{BL}	-	28.8	31.5	V	
Rated Current	I_L	-	20	-	mA	Ta=25°C
Power consumption	W_L	-	576	-	mW	

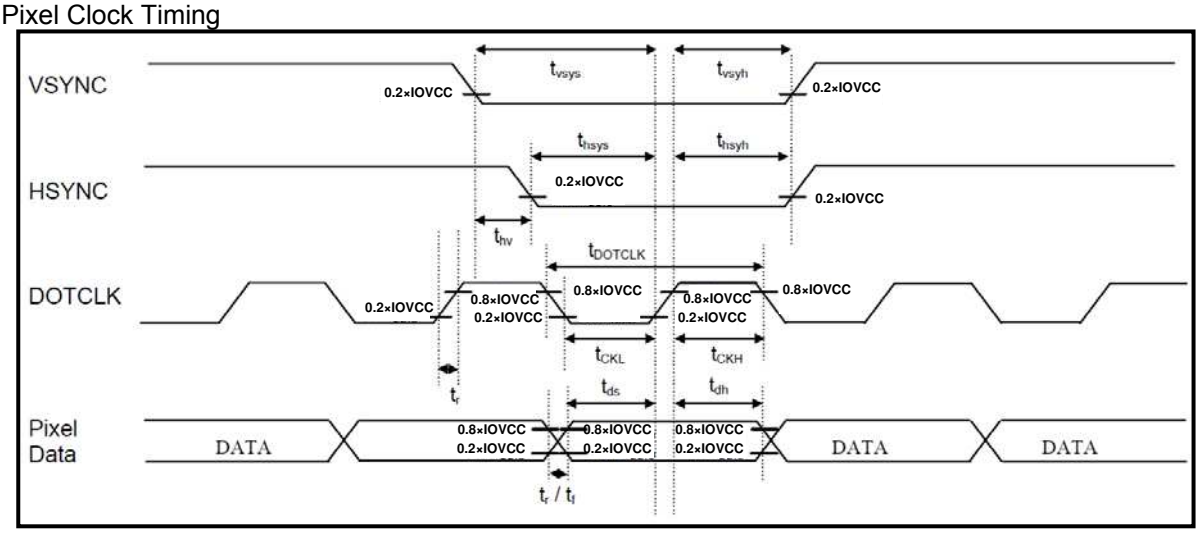
[LED-FPC circuit]



Cap; 4700pF / 50V

7. Timing characteristics of input signals

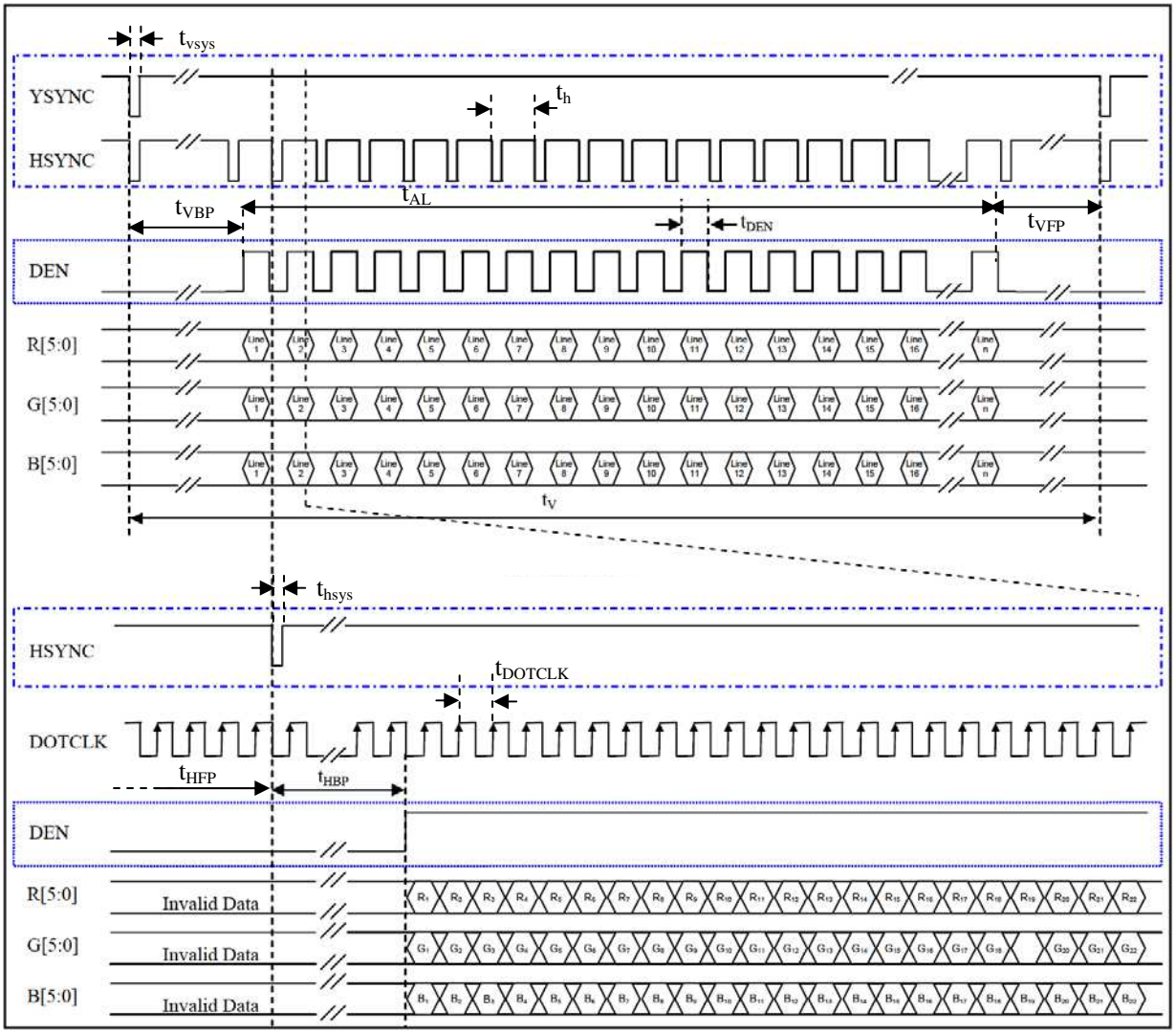
7-1. Pixel Clock Timing



IOVCC=2.7V~3.6V

Characteristics	Symbol	Min	Typ	Max	Units
DOTCLK Frequency	f_{DOTCLK}	-	8.54	12	MHz
DOTCLK Period	t_{DOTCLK}	83	-	-	nsec
DOTCLK Low Period	t_{CKL}	41	-	-	nsec
DOTCLK High Period	t_{CKH}	41	-	-	nsec
Vertical Sync Setup Time	t_{vsys}	20	-	-	nsec
Vertical Sync Hold Time	t_{vsyh}	20	-	-	nsec
Horizontal Sync Setup Time	t_{hsys}	20	-	-	nsec
Horizontal Sync Hold Time	t_{hsyh}	20	-	-	nsec
Phase difference of Sync signal falling edge	t_{hv}	0	-	t_H -2	t_{DOTCLK}
Data Setup Time	t_{ds}	20	-	-	nsec
Data Hold Time	t_{dh}	20	-	-	nsec
Rise / Fall Time	t_r / t_f	-	-	10	nsec

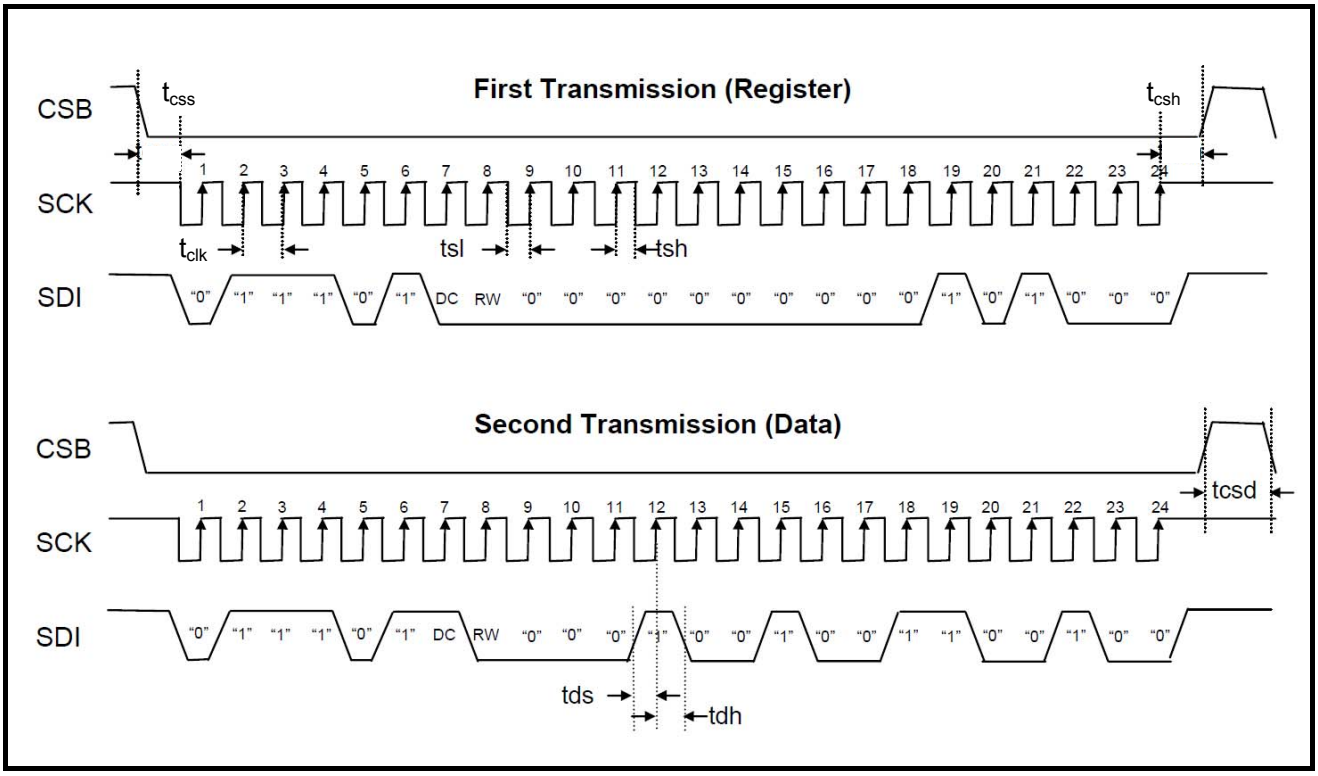
7-2. 18-bit RGB Interface Timing Diagram & Transaction Example



Characteristics		Symbol	DEN Mode ※			Units
			Min	Typ	Max	
Serial Clock Frequency		$1/t_{DOTCLK}$	—	8.54	12.0	MHz
Horizontal	One Line Period	t_H	505	512	—	t_{DOTCLK}
	Active Data Period	$t_{data,}$ t_{DEN}	480	480	480	t_{DOTCLK}
	Horizontal Back Porch	t_{HBP}	2	16	—	t_{DOTCLK}
	Horizontal Front Porch	t_{HFP}	2	16	—	t_{DOTCLK}
	Horizontal sync Period	t_{hsys}	2	—	t_H -2	t_{DOTCLK}
Vertical	One Field Period	t_V	275	278	—	t_H
	Active Line Period	t_{AL}	272	272	272	t_H
	Vertical Back Porch	t_{VBP}	2	4	—	t_H
	Vertical Front Porch	t_{VFP}	1	2	—	t_H
	Vertical sync Period	t_{vsys}	1	2	T_V-2	t_H
	Frequency※	1/tv	50	60	-	t_H

※If frequency is low, the display grade, flicker and others may become deterioration. Keep frequency over 50Hz(1/Tv). Although this module is operated in DEN mode to decide a horizontal first position, the inputs of not only DEN but Hsync and Vsync are also required.

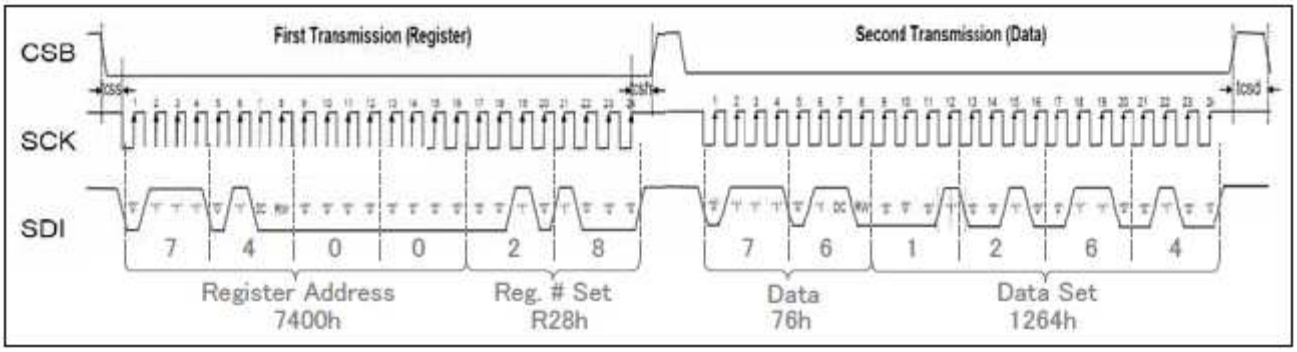
7-3. SPI Interface Timing Diagram & Transaction Example (3-wires 24 bit)



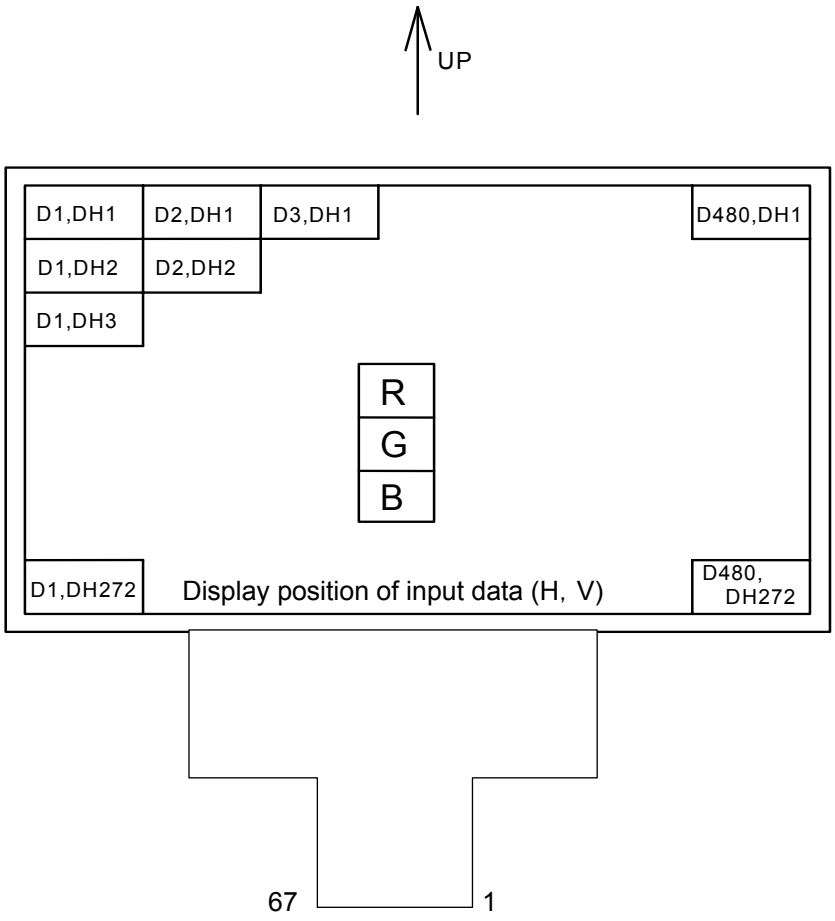
IOVCC=2.7V～3.6V

Characteristics	symbol	Min	Typ	Max	Units
Serial Clock Frequency	fclk	-	-	20	MHz
Serial Clock Cycle Time	tclk	50	-	-	nsec
Clock Low Width	tsl	25	-	-	nsec
Clock High Width	tsh	25	-	-	nsec
Chip Select Setup Time	tcss	10	-	-	nsec
Chip Select Hold Time	tcsh	10	-	-	nsec
Chip Select High Delay Time	tcsd	25	-	-	nsec
Data Setup Time	tds	10	-	-	nsec
Data Hold Time	tdh	10	-	-	nsec

Register write example　　example）write 「1264h」to Register＃「R28h」



7-4. Input Data Signals and Display Position on the screen



8. Input Signals, Basic Colors and Gray Scale of Each Color

	Colors & Gray Scale	Gray Scale	Date signal																	
			R0	R1	R2	R3	R4	R5	G0	G1	G2	G3	G4	G5	B0	B1	B2	B3	B4	B5
			LSB					MSB	LSB					MSB	LSB					MSB
Basic Color	Black	–	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue	–	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1
	Green	–	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
	Cyan	–	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
	Red	–	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	Magenta	–	1	1	1	1	1	1	0	0	0	0	0	0	1	1	1	1	1	1
	Yellow	–	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0
	White	–	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Gray Scale of Red	Black	GS0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	⇧	GS1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Darker	GS2	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	⇧	↓				↓						↓						↓		
	⇩	↓				↓						↓						↓		
	Brighter	GS61	1	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	⇩	GS62	0	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	Red	GS63	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
Gray Scale of Green	Black	GS0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	⇧	GS1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
	Darker	GS2	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
	⇧	↓				↓						↓						↓		
	⇩	↓				↓						↓						↓		
	Brighter	GS61	0	0	0	0	0	0	1	0	1	1	1	1	0	0	0	0	0	0
	⇩	GS62	0	0	0	0	0	0	0	1	1	1	1	1	0	0	0	0	0	0
	Green	GS63	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
Gray Scale of Blue	Black	GS0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	⇧	GS1	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0
	Darker	GS2	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
	⇧	↓				↓						↓						↓		
	⇩	↓				↓						↓						↓		
	Brighter	GS61	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	1	1
	⇩	GS62	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1
	Blue	GS63	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1

0: Low level voltage, 1: High level voltage

Each basic color can be displayed in 64 gray scales from 6 bit data signals.

According to the combination of 18 bit data signals, the 262k color display can be achieved on the screen.

9. Optical Characteristics

Module characteristics

Ta = 25°C, IOVCC = +3.3V, VCC = +3.3V

Parameter		Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Viewing angle range (With Wide View)	Horizontal	θ 3	CR≧10	-	80	-	deg.	[Note 9-1] [Note 9-4]
		θ 9		-	80	-	deg.	
	Vertical	θ 12		-	55	-	deg.	
		θ 6		-	80	-	deg.	
Contrast ratio		CR	Optimum viewing angle	250	500	-	-	[Note 9-2] [Note 9-4]
Response Time	Rise	Tr	θ=0°	-	22	40	ms	[Note 9-3]
	Decay	Td		-	8	20	ms	[Note 9-4]
Chromaticity of White		x		0.26	0.31	0.36	-	[Note 9-4]
		y		0.29	0.34	0.39	-	
Luminance of white		X_L		240	300	-	cd/m²	I_{LED}=20mA [Note 9-4]
The life of LED (Reference)			I_{LED}=20mA	(10,000)			hour	[Note 9-5]

* The optical characteristics measurements are operated under a stable luminescence (I_{LED} = 20mA) and a dark condition. (Refer to Fig.9-1 and Fig.9-2)

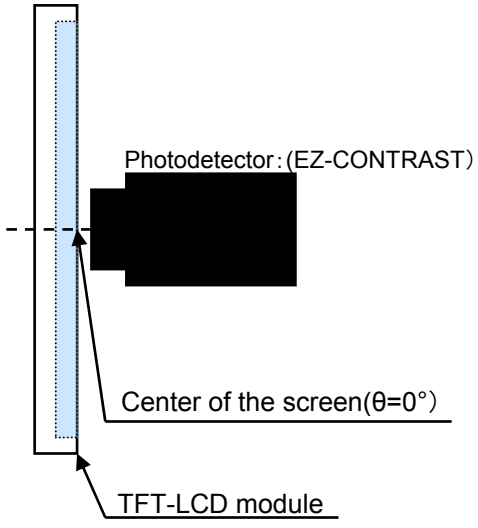


Fig.9-1 Viewing angle range measurement method

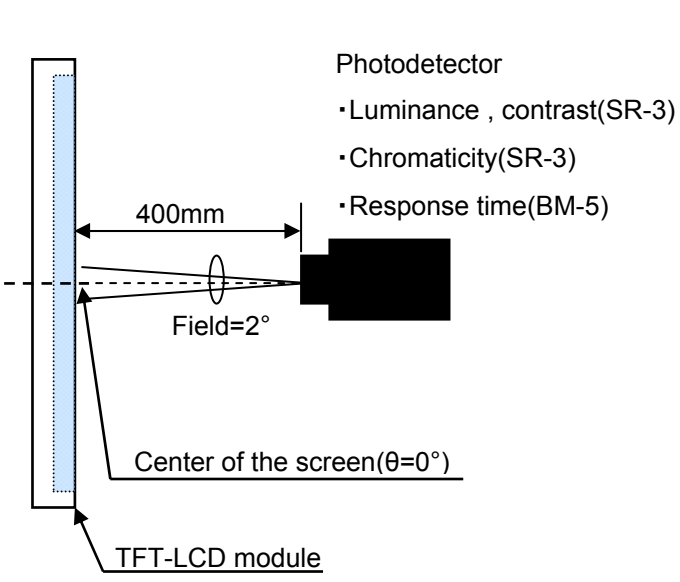
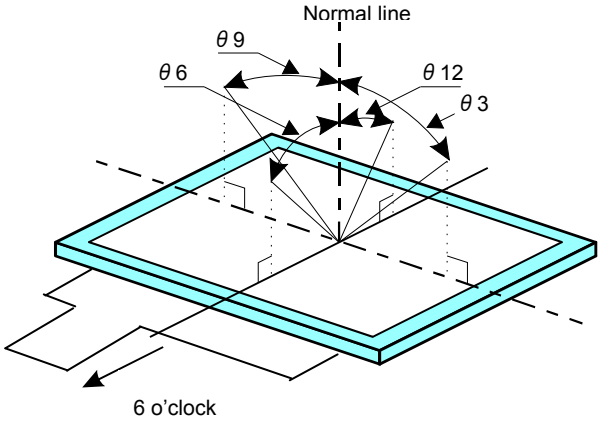


Fig.9-2 Luminance / Contrast/Chromaticity / Response time measurement method

[Note 9-1] Definitions of viewing angle range



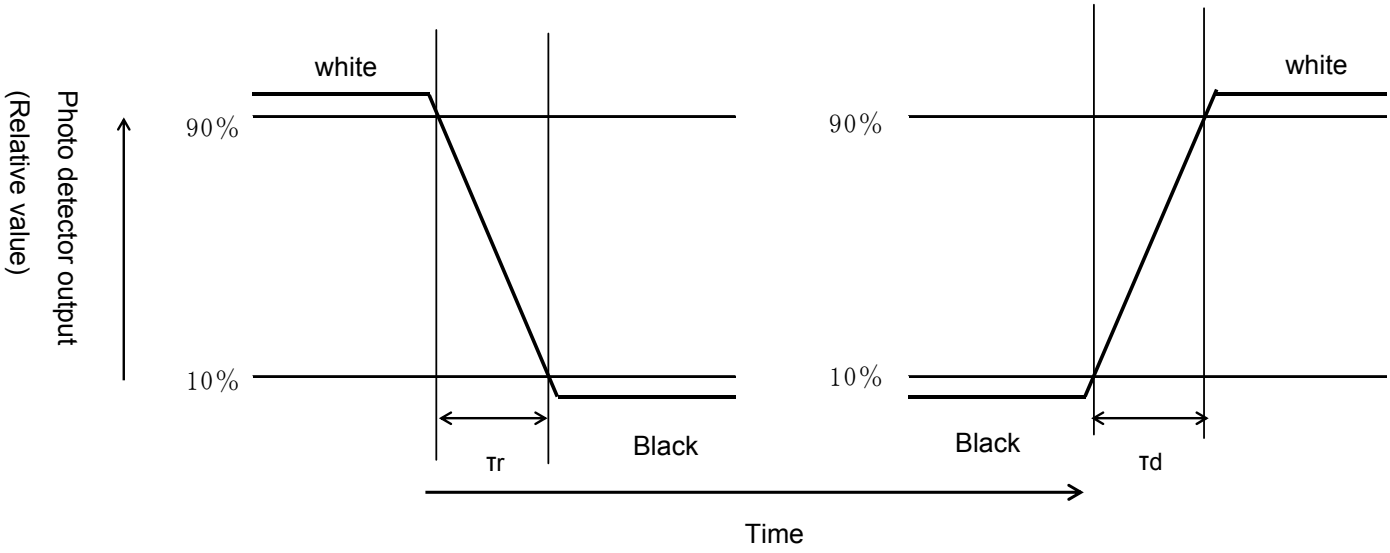
[Note 9-2] Definition of contrast ratio

The contrast ratio is defined as the following

$$\text{Contrast ratio (CR)} = \frac{\text{Luminance (brightness) with all pixels white}}{\text{Luminance (brightness) with all pixels black}}$$

[Note 9-3] Definition of response time

The response time is defined as the following figure and shall be measured by switching the input signal for "black" and "white"



[Note 9-4] This shall be measured at center of the screen.

[Note 9-5] The life of LED (Reference)

Luminosity will become 50% on more for an initial value in about 10,000H which condition is Ta=25℃ and I_{LED}=20mA.

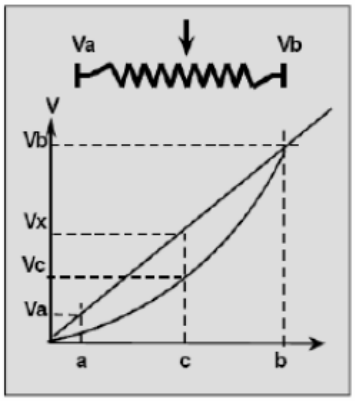
10. Touch panel characteristics

Parameter	Min.	Typ.	Max.	Unit	Remark
Input voltage	-	5.0	7.0	V	
Resistor between terminals(XL-XR)	200	750	1600	Ω	
Resistor between terminals(YU-YD)	100	270	900	Ω	
Line linearity(X direction)	-	-	1.5	%	Note 10-3
Line linearity(Y direction)	-	-	1.5	%	
Insuration resistance	20	-	-	MΩ	at DC25V
Minimum power to push Ⅰ	-	-	80	g	Note 10-1
Minimum power to push Ⅱ	-	-	50	g	Note 10-2

[Note 10-1] It is applied inside (2～12mm) from Active area with use of 0.8mm stylus pen.

[Note 10-2] It is applied inside 12mm from Active area with use of 0.8mm stylus pen.

[Note 10-3] Linearity is defined as accuracy of position when a touch panel is pushed. That is, it is defined as a deviation to the detection voltage over the ideal voltage as follows.



Va : Starting point voltage
Vb : Ending point voltage
a : Starting point
b : Ending point
c ; Measuring point
Vc : Measured voltage of c
Vx : Expecting voltage of c

Linearity = (Vx-Vc)/(Vb-Va) x 100

11. Handling of modules

11-1. Inserting the FPC into its connector and pulling it out.

1) Be sure to turn off the power supply and the signals when inserting or disconnecting the cable.
2) Please insert for too much stress not to join FPC in the case of insertion of FPC.

11-2. Handling of FPC

1) The bending radius of the FPC on flexible part should be more than R0.6mm, and it should be bent evenly.
2) Do not dangle the LCD module by holding the FPC, or do not give any stress to it.
3) Do not add stress to the terminal area of FPC and LCD panel.
4) Do not bend FPC to the display direction when handling and mounting.

11-3. Mounting of the module

1) The module should be held on to the plain surface. Do not give any warping or twisting stress to the module. Refer to 18.Outline Dimensions about the handling area in surface and gasket area in back. When LCD surface is pushed by the power over 300gf/cm^2, with use of handling area, the pooling may occur at a different place from the pushed place. Because there is a grade difference in the pooling, check and judge after mounting.

2) Please consider that GND can ground a modular metal portion etc. so that static electricity is not charged to the module.

3) Design guidance for touch panel (T/P)

a) Example of housing design

(1) If a consumer will put a palm on housing in normal usage, care should be taken as follows.

(2) Keep the gap, for example 0.3 to 0.7mm, between bezel edge and T/P surface.

The reason is to avoid the bezel edge from contacting T/P surface that may cause a “short” with bottom layer. (See Fig.1)

(3) Inserting a cushion material is recommended.

(4) The cushion material should be limited just on the busbar insulation paste area.

If it is over the transparent insulation paste area, a ”short” may be occurred.

(5) There is one part where a resistance film is left in the T/P part of the end of the pole.

Design to keep insulation from the perimeter to prevent from mis-operation and so on.

b) Mounting on display and housing bezel

(1) In all cases, the T/P should be supported from the backside of the Plastic.

(2) Do not to use an adhesive-tape to bond it on the front of T/P and hang it to the housing bezel.

(3) Never expand the T/P top layer (PET-film) like a balloon by internal air pressure.

The life of the T/P will be extremely short.

(4) The dimensions of top layer and PET are changing with environmental temperature and humidity.

Avoid a stress from housing bezel to top layer, because it may cause “waving”

(5) The input to the T/P sometimes distorts touch panel itself.

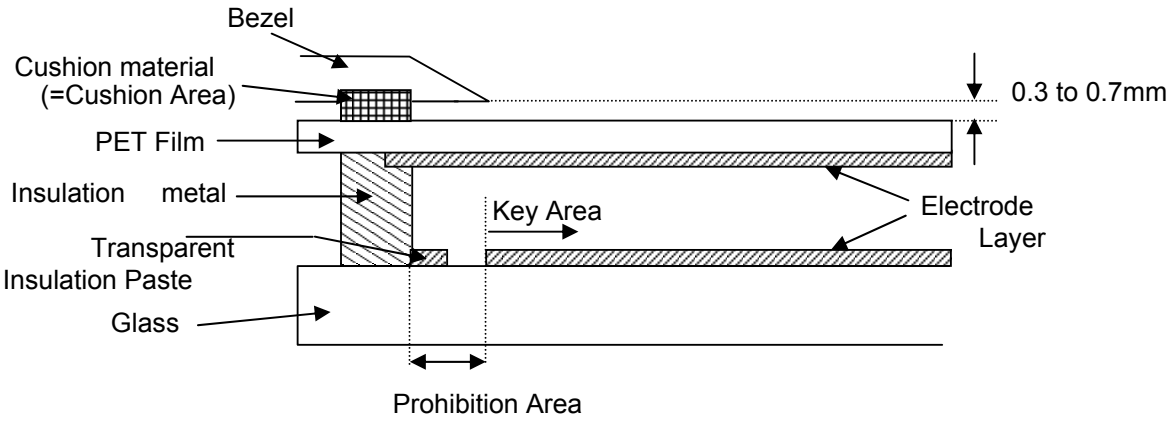


Fig.1