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	MOBILE LIQUID CRYSTAL DISPLAY GROUP SHARP CORPORATION **SPECIFICATION**	MOBILE LIQUID CRYSTAL DISPLAY DIVISION II

DEVICE SPECIFICATION FOR

Control IC of TFT-LCD

Type No. LQ0DZC2291

CUSTOMER'S APPROVAL

DATE

BY

PRESENTED

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RECORDS OF REVISION

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Note: In this ASIC Specification, binary notation, decimal notation and hexadecimal notation are described according to the rules below.

Binary notation: Double quotation marks are used, e.g., “111000” or “1001”. Otherwise, ‘b’ is appended, e.g., 111000b.

Hexadecimal notation: ‘0x’ is used, e.g., 0x3F or 0x2D. Otherwise, ‘H’ is appended, e.g., 20H or 1000H.

Decimal notation: Unless binary notation and hexadecimal notation are used, decimal notation is used.

– CONTENTS –

1. Overview and Features of Product

1.1. Product Overview

This product is a timing controller for liquid crystal module to display four kinds of resolutions, i.e., WVGA (800RGB[H] × 480[V], WQVGA (400RGB[H] × 240[V]), WEGA1 (480RGB[H] × 272[V]) and WEGA2 (480RGB[H] × 240[V]). Moreover, RGB independent gamma can be controlled by adding external EEPROM. This controller has an auto-loading function. After resetting, the controller reads the register set values/independent gamma parameters from the external EEPROM and works according to the set values.

1.2. Main Features

a) Timing controller (for WVGA, WQVGA, WEGA1 and WEGA2) contained
b) ROMOFF setting (It can be specified whether external EEPROM should be disabled or enabled.)
c) HSY/VSY input monitoring function. (“Free Run” is shown when HSY/VSY has not yet been input and when an error has been occurred in input.)
d) Free Run Display (Blue background screen 1H = 1200 clk or more/1V = 700 Lines or more）
e) Horizontal/vertical reverse display available.
f) Independent gamma setting (supported only for ROMOFF = 0)
g) External D/A Converter 8ch control output supported (only for ROMOFF = 0)
h) External A/D Converter 2ch control output supported (only for ROMOFF = 0)
i) Internal register control with I2C (only for ROMOFF = 0)

1.3. Block diagram

Figure 1-1 shows a simplified block diagram of LQ0DZC2291.

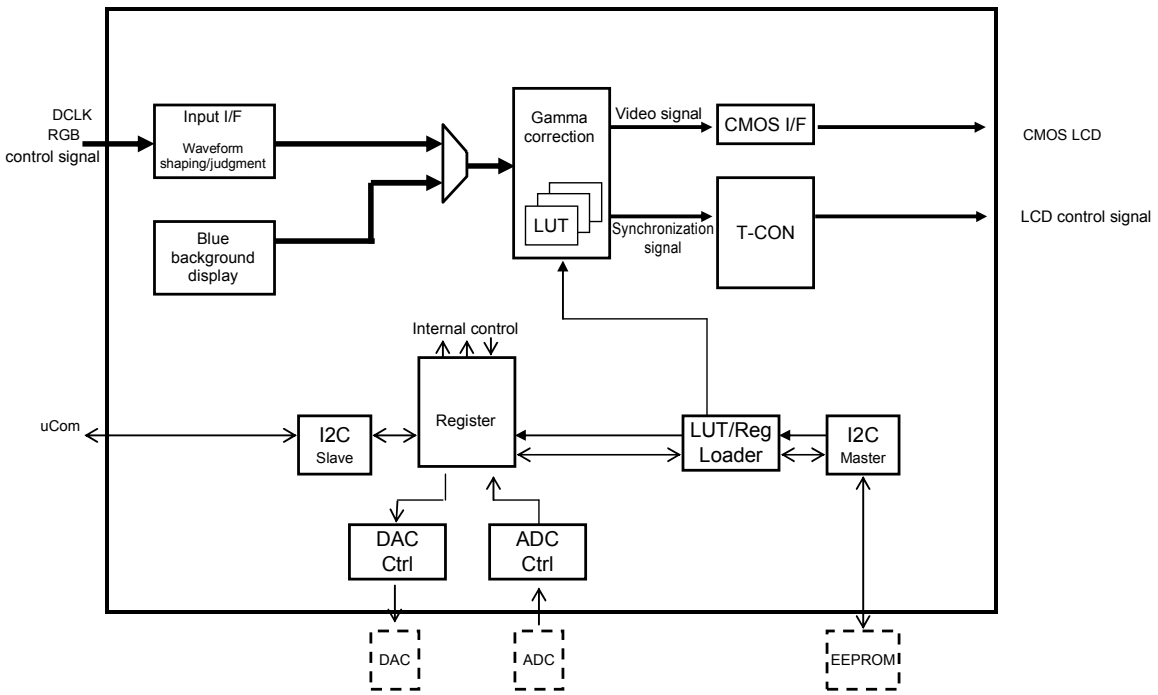


Figure 1-1: Simplified Block Diagram of LQ0DZC2291

Overview of block diagram is described below.

(1) Input I/F

Receives 18-bit parallel data input externally and passes it to the image processing block stated below. Waveform shaping (Hsy/Vsy phase difference absorption), pulse noise elimination (pulse of 2 clk or less) from control signal and synchronization signal input judgment are performed here.

(2) Blue background display

A block to generate the blue background display when Input I/F of (1) has judged that there is no synchronization signal input.

(3) Gamma correction

The gamma correction function allows to process input video data per RGB data and adjust the gamma curve per R, G and B. (This is available only for ROMOFF = '0'.)

(4) T-CON

A block of timing controller to drive a panel of four kinds of resolutions, i.e., WVGA, WQVGA, WEGA1 and /WEGA2.

(5) LUT/Reg_Loader

A block to read a data from the external EEPROM, which is connected to have an initial value of an ASIC's internal register and internal LUT, and to update the data for the register and LUT.

(6) DAC Ctrl

External D/C converter can be connected and controlled to set up the liquid crystal display gradation and specify the COM signal. In this block, a control signal to DAC is generated to control DAC.

(7) ADC Ctrl

External A/D converter can be connected and controlled. This block receives a signal from ADC and stores a data in the internal register of ASIC. Thermistor and photo sensor can be connected and monitored, by way of example.

2. Pin Description

2.1. Pin Layout

Table 2-1 describes all the pins.

Table 2-1: Pin Description

PIN No.	I/O Attribute	Pin Name	Drive Power	Description of Function	Operation when it is not be used
1	–	VDD			
2	I	IG0		Green data input pin (LSB)	
3	I	IG1		Green data input pin	
4	I	IG2		Green data input pin	
5	I	IG3		Green data input pin	
6	I	IG4		Green data input pin	
7	I	IG5		Green data input pin (MSB)	
8	I	IB0		Blue data input pin (LSB)	
9	I	IB1		Blue data input pin	
10	I	IB2		Blue data input pin	
11	I	IB3		Blue data input pin	
12	I	IB4		Blue data input pin	
13	I	IB5		Blue data input pin (MSB)	
14	Id	ROMOFF		Setting whether external EEPROM should be disabled or enabled	
15	Iu	VRVC		Vertical scan reversal	
16	Iu	HRVC		Horizontal scan reversal	
17	Id	SMC		ASIC test pin	OPEN/GND
18	Id	GMDSEL		Gate start pulse output setting	
19	O	SOUT		ASIC test pin	OPEN
20	I	TMC		ASIC test pin	OPEN/GND
21	Id	AMC		ASIC test pin	OPEN/GND
22	Iu	VSY		Vertical synchronization signal input pin	
23	Id	HENAB		Horizontal data enable input pin	
24	Iu	HSY		Horizontal synchronization signal input pin	
25	–	VDD			
26	–	GND			
27	I	DCLK		Clock input pin	
28	–	GND			
29	Isu	FRESET		ASIC reset pin	
30	–	VDD			
31	Id	S_SEL		Source driver setting pin	
32	Id	G_SEL		Gate driver setting pin	
33	Id	DSEL1		Resolution setting pin 1	
34	Id	DSEL2		Resolution setting pin 2	
35	Id	TEST1		ASIC test pin	GND
36	–	GND			
37	Iou	SERDIO	3mA	Serial data I/O pin	OPEN
38	Iu	SERCK		Serial clock input pin	OPEN/VDD
39	O	ADCCK	3mA	ADC clock output pin	OPEN
40	O	ADCCS	3mA	ADC chip select output pin	OPEN
41	O	ADCDI	3mA	ADC control data output pin	OPEN
42	–	ADCDO		ADC data input pin	OPEN/VDD
43	O	DACDI	3mA	DAC data output pin	OPEN
44	O	DACLD	3mA	DAC load output pin	OPEN
45	IOu	DACCK	3mA	DAC clock output pin	OPEN
46	–	GND			
47	O	ROMCK	3mA	EEPROM clock output pin	OPEN
48	O	ROMWC	3mA	EEPROM write protect output pin	OPEN
49	IOu	ROMDIO	3mA	EEPROM data I/O pin	OPEN
50	–	GND			

PIN No.	I/O Attribute	Pin Name	Drive Power	Description of Function	Operation when it is not be used
51	–	VDD			
52	O	OR0	6mA	Red data output pin (LSB)	
53	O	OR1	6mA	Red data output pin	
54	O	OR2	6mA	Red data output pin	
55	O	OR3	6mA	Red data output pin	
56	O	OR4	6mA	Red data output pin	
57	O	OR5	6mA	Red data output pin (MSB)	
58	–	GND			
59	O	OG0	6mA	Green data output pin (LSB)	
60	O	OG1	6mA	Green data output pin	
61	O	OG2	6mA	Green data output pin	
62	O	OG3	6mA	Green data output pin	
63	O	OG4	6mA	Green data output pin	
64	O	OG5	6mA	Green data output pin (MSB)	
65	–	VDD			
66	O	OB0	6mA	Blue data output pin (LSB)	
67	O	OB1	6mA	Blue data output pin	
68	O	OB2	6mA	Blue data output pin	
69	O	OB3	6mA	Blue data output pin	
70	O	OB4	6mA	Blue data output pin	
71	O	OB5	6mA	Blue data output pin (MSB)	
72	–	GND			
73	IO	STHR	6mA	* [1]Start pulse I/O signal	
74	IO	STHL	6mA	* [1]Start pulse I/O signal	
75	–	VDD			
76	–	GND			
77	O	CLK	12mA	Source driver sampling clock	
78	–	GND			
79	O	STB	6mA	Source driver latch pulse output	
80	O	REV	6mA	Source driver polarity reversal control output	
81	O	FS / REVC	6mA	* Offset cancel / COM polarity reversal signal output	
82	O	LBR	3mA	Source driver horizontal reversal control output	
83	IO	GSPOI / MODE2	3mA	* Gate start pulse / Gate mode setting pin	
84	O	R/L	3mA	Gate driver vertical reversal control output	
85	IO	GSPIO / SPS	3mA	* Gate start pulse	
86	O	GOE / MODE1	3mA	* Gate driver control output	
87	O	GCK / CLS	3mA	* Gate driver shift clock	
88	I	TEB		ASIC test pin	VDD
89	Id	TEST2		ASIC test pin	GND
90	O	ALLON	3mA	Full gate output ON setting output	OPEN
91	O	DCON	3mA	Power supply circuit control output	
92	O	G_SLP	3mA	Gate slope control pin	OPEN
93	–	VDD			
94	I	IR0		Red data input pin (LSB)	
95	I	IR1		Red data input pin	
96	I	IR2		Red data input pin	
97	I	IR3		Red data input pin	
98	I	IR4		Red data input pin	
99	I	IR5		Red data input pin (MSB)	
100	–	GND			

I: Input pin O: Output pin IO: I/O pin d: Pull-down for input pin u: Pull-up for input pin su: Schmitt input pin

* [1] Table 12-3 on page 22.

*[2] Refer to Table 2-2 on page 10.

2.2. Pin Settings

Table 2-2 describes the pin settings.

Table 2-2: Pin Settings

<table>
<tr><th>Pin name</th><th>Function</th></tr>
<tr><td>S_SEL (*)</td><td>Source setting pin
For how to set this pin, ask the person in charge of Sharp Corporation.</td></tr>
<tr><td>G_SEL (*)</td><td>Gate setting pin
For how to set this pin, ask the person in charge of Sharp Corporation.</td></tr>
<tr><td>VRVC</td><td>Gate driver scan direction setting
Refer to Chapter 11 “Horizontal/Vertical Reverse Display”.</td></tr>
<tr><td>HRVC</td><td>Source driver scan direction setting
Refer to Chapter 11 “Horizontal/Vertical Reverse Display”.</td></tr>
<tr><td>GMDSEL</td><td>Gate start pulse output setting
Lo: Normal mode
Hi: Interlacing two-pulse mode</td></tr>
<tr><td>D_SEL1 (*)
D_SEL2 (*)</td><td>Input resolution switch setting pin
<table>
<tr><th>Resolution</th><th>D_SEL1</th><th>D_SEL2</th></tr>
<tr><td>WVGA</td><td>0</td><td>0</td></tr>
<tr><td>WQVGA</td><td>1</td><td>0</td></tr>
<tr><td>WEGA1</td><td>0</td><td>1</td></tr>
<tr><td>WEGA2</td><td>1</td><td>1</td></tr>
</table></td></tr>
<tr><td>ROMOFF (*)</td><td>EEPROM setting pin
Lo: EEPEOM is enabled.
Hi: EEPEOM is disabled.

If ROMOFF is set to ‘1’, this ASIC is used as a timing controller. Therefore, register control, DAC control, etc. cannot be performed.</td></tr>
<tr><td>FRESET</td><td>Reset pin (Lo-Active)
* Time constant shall be 10 ms or less. Refer Figure 2-1.</td></tr>
</table>

Do not change any setting of pins marked with *, after the ASIC power supply turns ON.

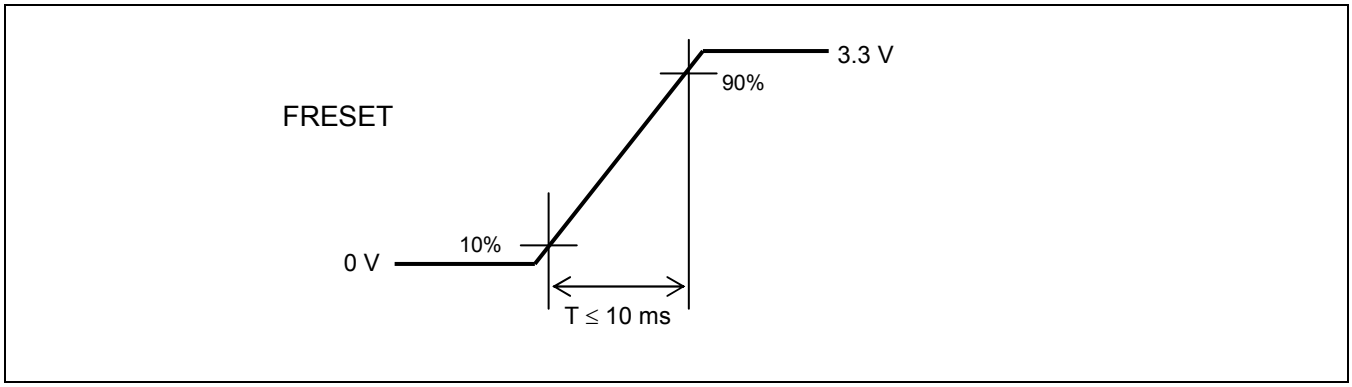


Figure 2-1 FREST Time Constant

3. Absolute Maximum Ratings

Table 3-1: Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply voltage	V_{DD}	-0.5 to +4.6	V
Input voltage	V_I	-0.5 to +4.6	V
Output voltage	V_O	-0.5 to +4.6	V
Operating temperature	T_A	-40 to +85	℃
Storage temperature	T_{stg}	-65 to +150	℃

4. Electrical Specification

4.1. Recommended Operating Range

Table 4-1: Recommended Operating Range

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Supply voltage*[1]	V_{DD}		2.7	3.15	3.6	V
Ambient temperature	T_A		-40		85	℃
Input voltage, high*[1]	V_{IH}		2.00		V_{DD}	V
Input voltage, low*[1]	V_{IL}		0		0.8	V
Positive trigger voltage	V_P	Schmitt Buffer	1.4		2.4	V
Negative trigger voltage	V_N		0.8		1.6	V
Hysteresis voltage	V_H		0.3		1.5	V
Input rise time	t_{ri}		0		200	ns
Input fall time	t_{fi}		0		200	ns
Input rise time	t_{ri}	Schmitt Buffer	0		10	ms
Input fall time	t_{fi}		0		10	ms

* The following Supply voltage conditions operate.

Condition1

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	V_{DD}	3.0		3.6	V
Input voltage, high	V_{IH}	$0.7V_{DD}$		V_{DD}	V
Input voltage, low	V_{IL}	0		$0.3V_{DD}$	V

Condition2

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	V_{DD}	2.7		3.0	V
Input voltage, high	V_{IH}	$0.75V_{DD}$		V_{DD}	V
Input voltage, low	V_{IL}	0		$0.25V_{DD}$	V

4.2. DC Electrical Specification

Table 4-2: DC Electrical Specification

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Static current consumption	I_{DDS}	V_I=V_{DD} or GND			300	μA
Off-state output current	I_{OZ}	V_0=V_{DD} or GND			±10	μA
Output short-circuit current	I_{OS}	V_0=GND			-250	mA
Input leakage current	I_I	V_I=V_{DD} or GND			±1.0	μA
	I_I	V_I=GND (pull-up 50kΩ)	-28	-83	-190	μA
	I_I	V_I=V_{DD} (pull-down 50kΩ)	28	83	190	μA
Pull-up resistor (50kΩ)	R_{PU}	V_I=GND	18.9	39.8	107.1	kΩ
Pull-down resistor (50kΩ)	R_{PD}	V_I=V_{DD}	18.9	39.8	107.1	kΩ
Output current,low	I_{OL}	V_{OL}=0.4V (I_{OL}=3mA type)	3.0			mA
		V_{OL}=0.4V (I_{OL}=6mA type)	6.0			mA
		V_{OL}=0.4V (I_{OL}=12mA type)	12.0			mA
Output current,high	I_{OH}	V_{OH}=2.4V (I_{OL}=3mA type)	-3.0			mA
		V_{OH}=2.4V (I_{OL}=6mA type)	-6.0			mA
		V_{OH}=2.4V (I_{OL}=12mA type)	-12.0			mA

4.3. AC Electrical Specification

Table 4-3: AC Electrical Specification

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Output rise time	t_r	Output buffer C_L=15pF	2		10	ps
Output fall time	t_r	Output buffer C_L=15pF	2		10	ps

5. Register Map

Table 5-1 shows the register map list of LQ0DZC2291.

Table 5-1: Register Map List

	address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Initial value
★	00h	da_0ch[7:0]								0000_0000b
★	01h	da_1ch[7:0]								0000_0000b
★	02h	da_2ch[7:0]								0000_0000b
★	03h	da_3ch[7:0]								0000_0000b
★	04h	da_4ch[7:0]								0000_0000b
★	05h	da_5ch[7:0]								1111_1111b
★	06h	da_6ch[7:0]								0111_1000b
★	07h	da_7ch[7:0]								0000_0000b
★	08h	henab[7:0]								1100_0010b
★	09h	-		venab[7:0]						0010_0011b
★	0Ah	-					rsel	vrvc	hrvc	0000_0000b
★	0Bh		stb_hl[6:0]							0100_0101b
★	0Ch	gck_hl[7:0]								1010_1010b
★	0Dh	-	slp_ctrl[6:0]							0100_0011b
★	0Eh	gamma_enb	-							0000_0000b
★	0Fh	test								0000_0000b
★	10h	test								0000_0000b
○	20h	rom_adrs[7:0]								
○	21h	rom_data[7:0]								
○	22h	-						r_read	r_write	
○	23h	test								
○	24h	test								
○	25h	test								
△	30h	-							allon	
△	31h	-							als	
◇	32h	ready	-					jinput	jenable	
△	33h	test								
◇	34h	adc_data1								
◇	35h	adc_data2								

★: Register for auto-loading

als register value 0: Inaccessible.

als register value 1: Write/Read can be done from a host.

○: Register not for auto-loading

als register value 0: Inaccessible

als register value 1: Write/Read can be done from a host.

△: Register not for auto-loading

Regardless of the als register value, Write/Read can be done.

◇: Read-Only register

Regardless of the als register value, Read only can be done.

6. Conditions for Input Signal

6.1. Conditions for Image Signal Input

Table 6-1 to Table 6-4 and Figure 6-1 to Figure 6-4 show the input range specifications for the WVGA, WQVGA, WEGA1 and WEGA2 modes. Also, Table 6-5 shows the horizontal/vertical display data capture position list in the WVGA, WQVGA, WEGA1 and WEGA2 display modes.

Table 6-1: WVGA Input Timing Specifications

WVGA [D_SEL1=0, D_SEL2=0]

ITEM		Symbol	Min.	Typ.	Max.	UNIT	Remark
DCLK	Frequency	tCLK	26.62	33.26	34.60	MHz	Frequency:1/(tV/tH(clk))
	Hi Time	tWCH	5	-	-	ns	
	Low Width	tWCL	5	-	-	ns	
Data[I* 0-5]	Setup time	tDS	5	-	-	ns	
	Hold time	tDH	5	-	-	ns	
Hsy	Cycle	tH(t)	31.45	31.75	38.46	µs	
		tH(clk)	1024	1056	1088	ck	
	Pulse Width	tHPW	5	-	tH-5	ck	
Vsy	Cycle	tV	520	525	635	line	
	Pulse Width	tVPW	2	-	TV-2	line	
frame rate		fV	50	60	60	Hz	
Horizontal display period		tHA	-	800	-	ck	
Hsy_DCLK phase defference		tHC	A-8	A	A+8	ns	A=tWCH(1/2(DCLK))
Hsy_Vsy phase defference		tVH	-10	0	10	ck	
Vertical fromt porch		tVFP	5	-	-	line	
Vertical back porch		tVBP	-	35	-	line	In case ROMOFF='1'
			10	28	35	line	In case ROMOFF='0'
Vertical display porch		tVA	-	480	-	line	
Enable signal[HENAB]	Setup time	tES	5	-	-	ns	
	Hold time	tEH	5	-	-	ns	
	Pulse Width	tEP	-	800	-	ck	
Horizontal front porch		tHFP	2	-	-		
Horizontal display starting position		tHBP	-	194	-		*1
		tHBP	20	-	222	ck	*2

*1: This spec is appied for HENAB Lo mode and W/O EEPROM mode

*2: This spec is applied for HENAB active mode or W/EEPROM mode

Table 6-2: WQVGA Input Timing Specifications

WQVGA [D_SEL1=1, D_SEL2=0]

ITEM		Symbol	Min.	Typ.	Max.	UNIT	Remark
DCLK	Frequency	tCLK	6.96	7.99	9.19	MHz	Frequency:1/(tV/tH(clk))
	Hi Time	tWCH	5	-	-	ns	
	Low Width	tWCL	5	-	-	ns	
Data[I* 0-5]	Setup time	tDS	5	-	-	ns	
	Hold time	tDH	5	-	-	ns	
Hsy	Cycle	tH(t)	61.3	63.6	70.5	µs	
		tH(clk)	491	508	563	ck	
	Pulse Width	tHPW	5	-	TH-5	ck	
Vsy	Cycle	tV	258	262	284	line	
	Pulse Width	tVPW	2	-	TV-2	line	
frame rate		fV	50	60	60	Hz	
Horizontal display period		tHA	-	400	-	ck	
Hsy_DCLK phase defference		tHC	A-8	A	A+8	ns	A=tWCH(1/2(DCLK))
Hsy_Vsy phase defference		tVH	-10	0	10	ck	
Vertical fromt porch		tVFP	5	-	-	line	
Vertical back porch		tVBP	-	20	-	line	In case ROMOFF='1'
			9	-	20	line	In case ROMOFF='0'
Vertical display porch		tVA	-	240	-	line	
Enable signal[HENAB]	Setup time	tES	5	-	-	ns	
	Hold time	tEH	5	-	-	ns	
	Pulse Width	tEP	-	400	-	ck	
Horizontal front porch		tHFP	2	-	-		
Horizontal display starting position		tHBP	-	87	-		*1
		tHBP	20	-	126	ck	*2

*1: This spec is appied for HENAB Lo mode and W/O EEPROM mode

*2: This spec is applied for HENAB active mode or W/EEPROM mode

Table 6-3: WEGA1 Input Timing Specifications

WEGA1 [D_SEL1=0, D_SEL2=1]

ITEM		Symbol	Min.	Typ.	Max.	UNIT	Remark
DCLK	Frequency	tCLK	8.58	9.70	10.99	MHz	Frequency:1/(tV/tH(clk))
	Hi Time	tWCH	5	-	-	ns	
	Low Width	tWCL	5	-	-	ns	
Data[I* 0-5]	Setup time	tDS	5	-	-	ns	
	Hold time	tDH	5	-	-	ns	
Hsy	Cycle	tH(t)	58.8	64.1	66.5	µs	
		tH(clk)	571	622	646	ck	
	Pulse Width	tHPW	5	-	tH-5	ck	
Vsy	Cycle	tV	283	312	344	line	
	Pulse Width	tVPW	2	-	TV-2	line	
frame rate		fV	50	50	60	Hz	
Horizontal display period		tHA	-	480	-	ck	
Hsy_DCLK phase defference		tHC	A-8	A	A+8	ns	A=tWCH(1/2(DCLK))
Hsy_Vsy phase defference		tVH	-10	0	10	ck	
Vertical fromt porch		tVFP	2	-	-	line	
Vertical back porch		tVBP	-	31	-	line	In case ROMOFF='1'
			9	-	41	line	In case ROMOFF='0'
Vertical display porch		tVA	-	272	-	line	
Enable signal[HENAB]	Setup time	tES	5	-	-	ns	
	Hold time	tEH	5	-	-	ns	
	Pulse Width	tEP	-	480	-	ck	
Horizontal front porch		tHFP	2	-	-		
Horizontal display starting position		tHBP	-	116	-		*1
		tHBP	20	-	164	ck	*2

*1: This spec is appied for HENAB Lo mode and W/O EEPROM mode

*2: This spec is applied for HENAB active mode or W/EEPROM mode

Table 6-4: WEGA2 Input Timing Specifications

WEGA2 [D_SEL1=1, D_SEL2=1]

ITEM		Symbol	Min.	Typ.	Max.	UNIT	Remark
DCLK	Frequency	tCLK	8.35	9.59	11.17	MHz	Frequency:1/(tV/tH(clk))
	Hi Time	tWCH	5	-	-	ns	
	Low Width	tWCL	5	-	-	ns	
Data[I* 0-5]	Setup time	tDS	5	-	-	ns	
	Hold time	tDH	5	-	-	ns	
Hsy	Cycle	tH(t)	61.3	63.6	70.5	µs	
		tH(clk)	589	610	685	ck	
	Pulse Width	tHPW	5	-	TH-5	ck	
Vsy	Cycle	tV	258	262	284	line	
	Pulse Width	tVPW	2	-	TV-2	line	
frame rate		fV	50	60	60	Hz	
Horizontal display period		tHA	-	480	-	ck	
Hsy_DCLK phase defference		tHC	A-8	A	A+8	ns	A=tWCH(1/2(DCLK))
Hsy_Vsy phase defference		tVH	-10	0	10	ck	
Vertical fromt porch		tVFP	2	-	-	line	
Vertical back porch		tVBP	-	20	-	line	In case ROMOFF='1'
			9	-	20	line	In case ROMOFF='0'
Vertical display porch		tVA	-	240	-	line	
Enable signal[HENAB]	Setup time	tES	5	-	-	ns	
	Hold time	tEH	5	-	-	ns	
	Pulse Width	tEP	-	480	-	ck	
Horizontal front porch		tHFP	2	-	-		
Horizontal display starting position		tHBP	-	104	-		*1
		tHBP	20	-	152	ck	*2

*1: This spec is appied for HENAB Lo mode and W/O EEPROM mode

*2: This spec is applied for HENAB active mode or W/EEPROM mode

6.2. Horizontal timing 1 HENAB = Active input

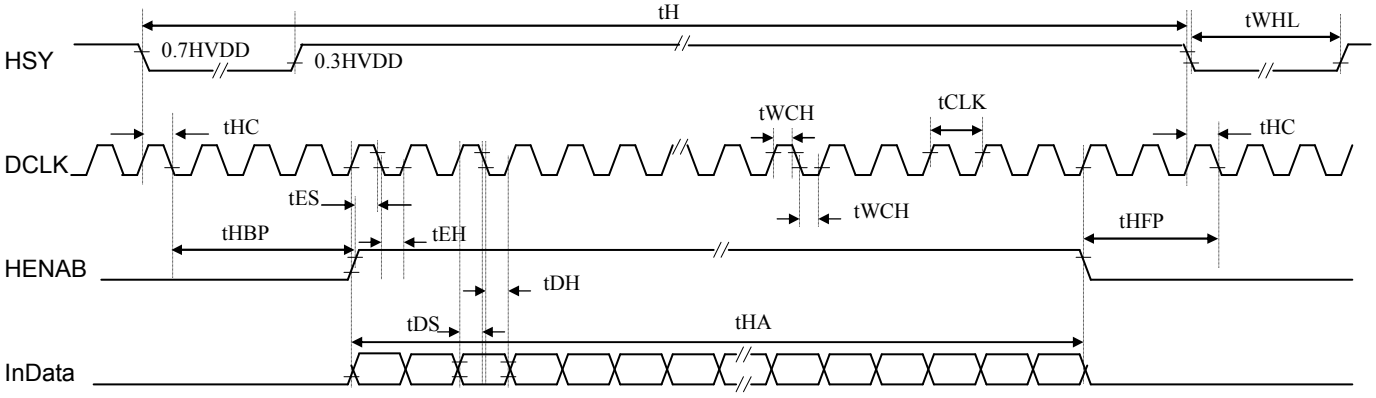


Figure 6-1: WVGA/WQVGA/WEGA1/WEGA2 Input Data Format (HENAB active/horizontal timing)

“InData” above shows the image signal bus of IR0-5, IG0-5 and IB0-5 collectively. This applies to any “InData” after this.

6.3. Horizontal timing 2 HENAB = Fixed to Lo

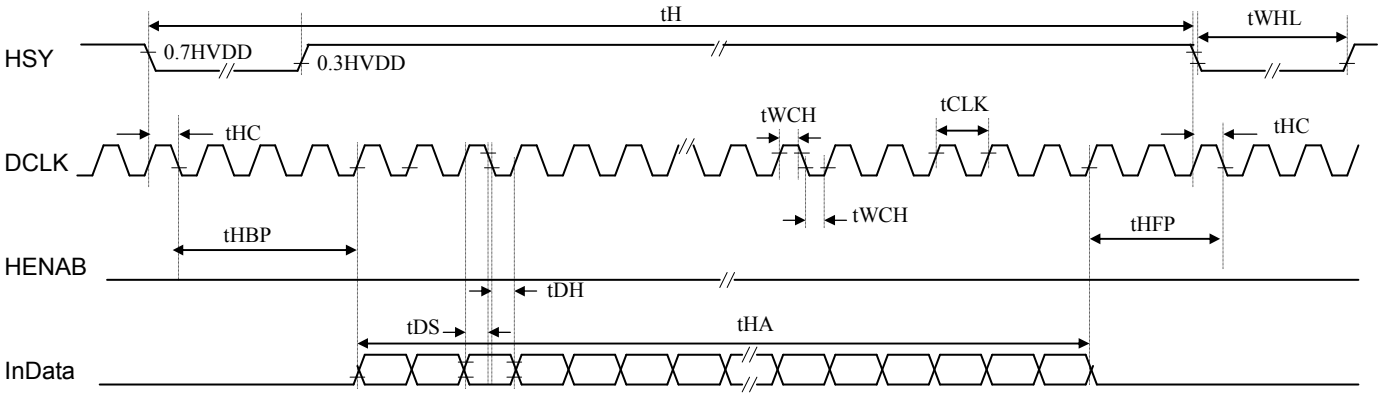


Figure 6-2: WVGA/WQVGA/WEGA1/WEGA2 Input Data Format (HENAB_Lo fixed/horizontal timing)

6.4. Vertical timing 1 HENAB = Active input

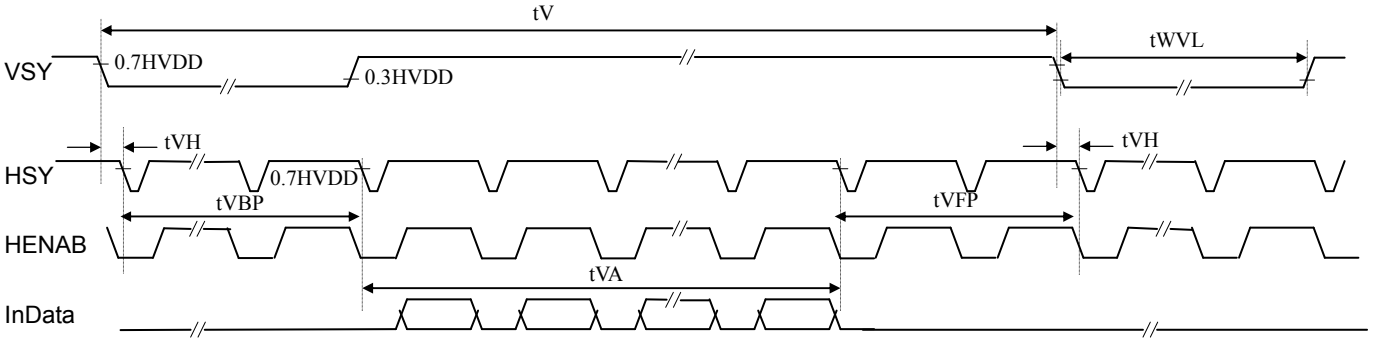


Figure 6-3: WVGA/WQVGA/WEGA1/WEGA2 Input Data Format (HENAB active/vertical timing)

6.5. Vertical timing 2 HENAB = Fixed to Lo

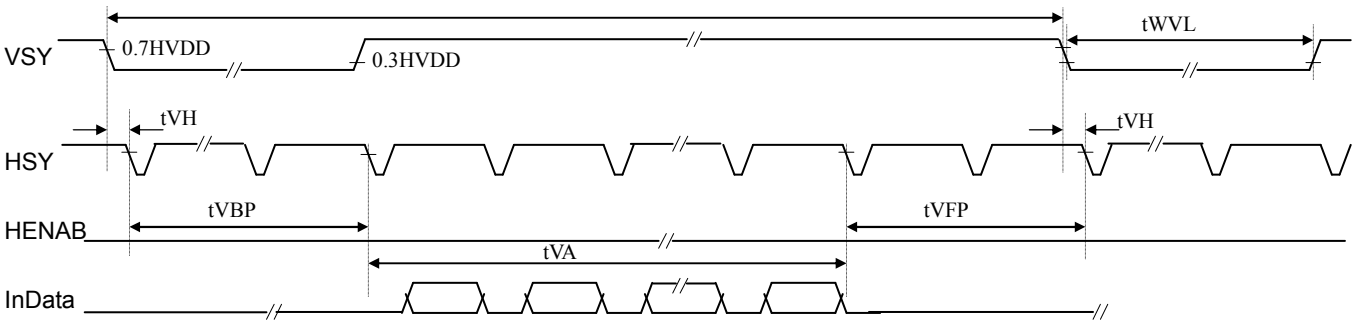


Figure 6-4: WVGA/WQVGA/WEGA1/WEGA2 Input Data Format (HENAB_Lo fixed/vertical timing)

6.6. Horizontal/Vertical Data Capture Position

Table 6-5: Horizontal/Vertical Data Capture Position in WVGA/WQVGA/WEGA1/WEGA2 Display Mode

HENAB input type	ROMOFF setting	tHBP	tVBP
Fixed to Lo	0	A	B
	1	Each condition for input signal tHBP	Each condition for input signal tVBP
Active input	0	DENAB ↑	B
	1	DENAB ↑	Each condition for input signal tVBP

A: Decided according to a henab register set value.

B: Decided according to a venab register set value.

7. Serial Input Conditions (I2C)

7.1. Protocol

Figure 7-1 shows the protocol for I2C used for LQ0DZC2291.

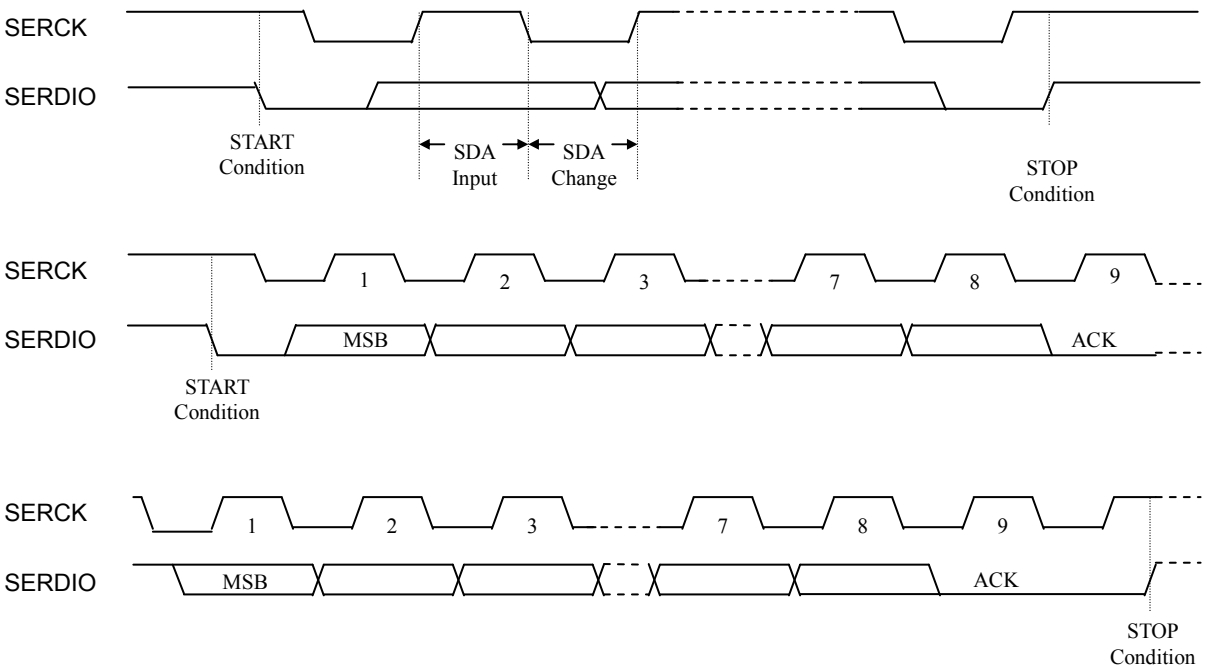


Figure 7-1: I2C Protocol

7.2. Serial Interface AC Characteristics

Figure 7-2 and Table 5-1 show the specifications for AC characteristics of I2C serial I/F.

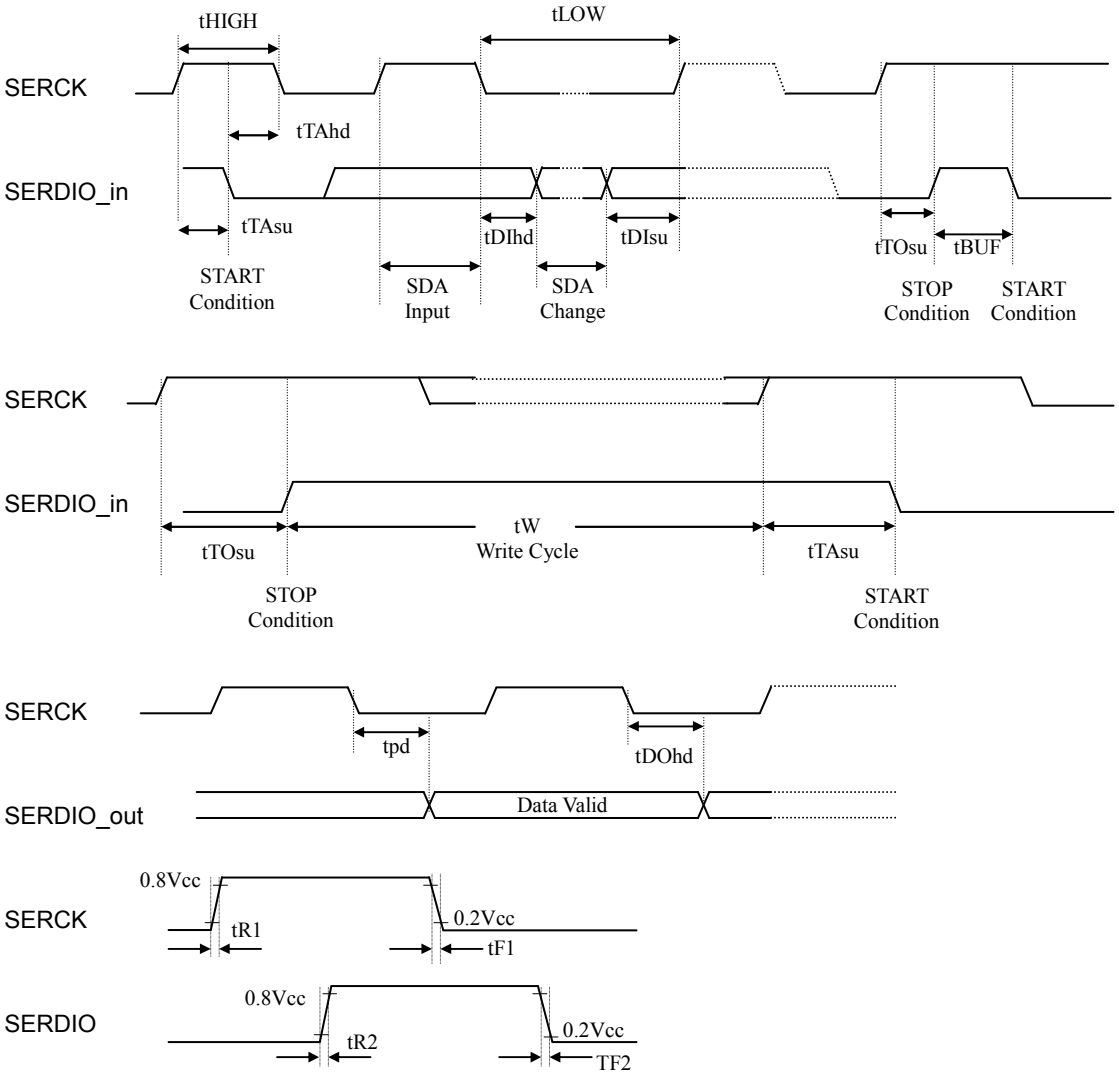


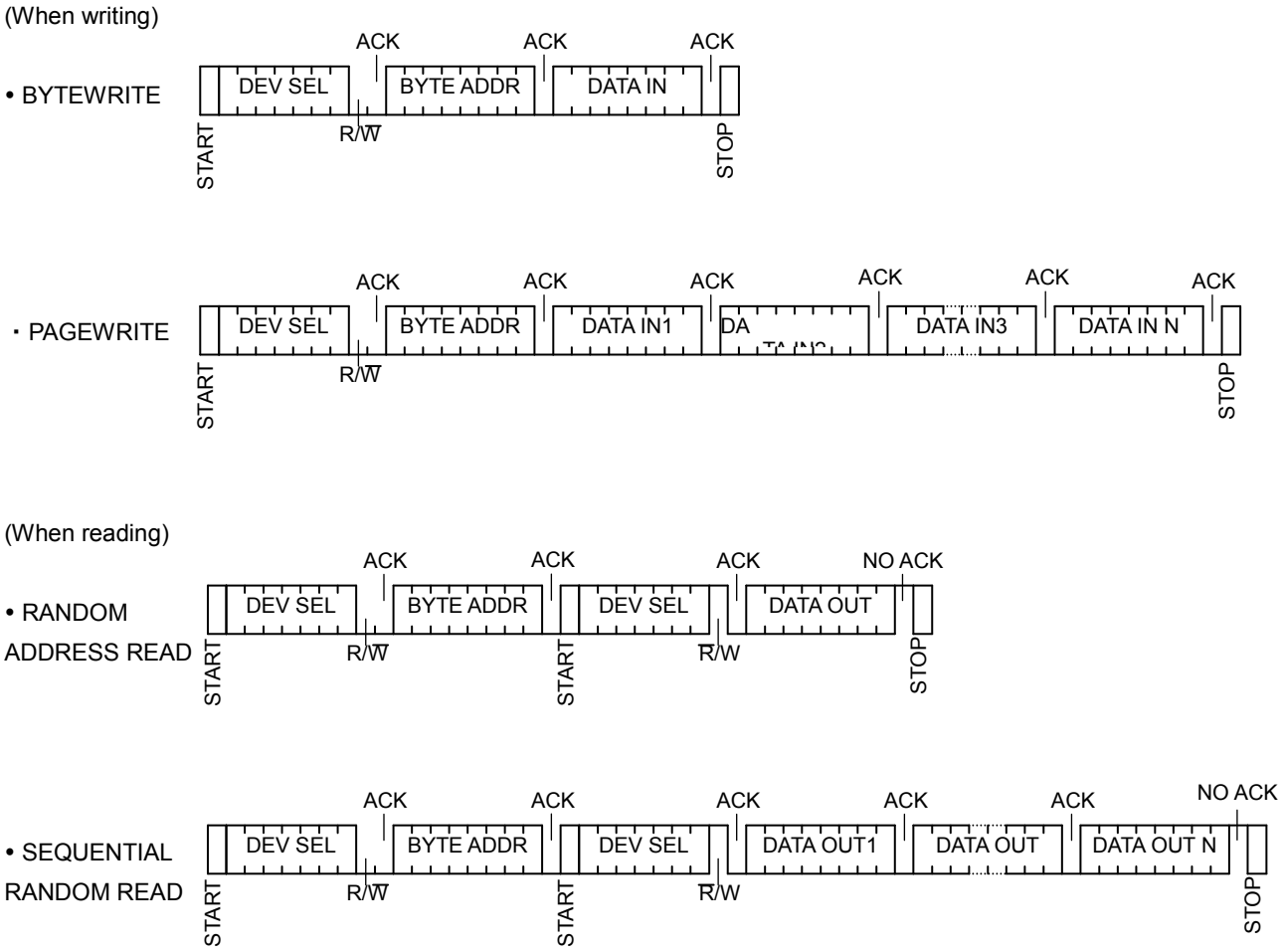
Figure 7-2: AC Specifications for Serial I/F

Table 7-1: AC Specifications for Serial I/F

Item	Symbol	Min.	Max.	Unit
Clock frequency	fSCK		400	kHz
Data clock “Hi” time	tHIGH	600		ns
Data clock “Lo” time	tLOW	1200		ns
Clock rise time	tR1		40	ns
Clock fall time	tF1		40	ns
Data rise time	tR2		40	ns
Data fall time	tF2		40	ns
Input data setup time	tDIsu	100		ns
Input data hold time	tDIhd	0		ns
Output data hold time	tDOhd	200		ns
Output data delay time	tpd	200	900	ns
Start condition setup time	tTAsu	600		ns
Start condition hold time	tTAhd	600		ns
Stop condition setup time	tTOsu	600		ns
Bus release time before transfer start	tBUF	1300		ns
Writing time	tW		10	ms

7.3. Instruction to Write/Read to/from ASIC

Figure 7-3 shows how to Write/Read to/from ASIC with I2C of LQ0DZC2291.



* DEV_SEL of this ASIC is “1000111”.

Figure 7-3: How to Write/Read with I2C

8. Description of Function and Supported Register

8.1. Outline of Loading

This ASIC can transfer the initial values of ASIC's internal register and the parameters for gamma correction, which are stored in EEPROM, to ASIC, when external EEPROM is connected and the ROMOFF pin is set to "0". Transfer EEPROM data from EEPROM into ASIC's internal register and LUT is referred to as "loading" in this document. There are two types of loading in this ASIC, as described below.

(1) Initial loading

This refers to transferring a data in EEPROM as ASIC's initial value into the internal register and LUT after canceling ASIC reset (FREST). This allows to fix an initial operation of ASIC.

(2) Auto-loading

For address 0x31[0]:als = '0', this ASIC transfers a data in EEPROM into ASIC's internal register and LUT once a 64V period.

For the ASIC's internal register, all the registers are not always loaded from EEPROM. Refer to the register map of Table 5-1 and Table 8-1 below and check whether the register should be loaded or not.

Table 8-1: Enabling/Disabling Loading and Access from Host

	ALS="0"	ALS="1"
Register to be loaded (Marked with ★ in the register map)	Access prohibited	Write/Read can be done
Register not to be loaded (Marked with ○ in the register map)	Access prohibited	Write/Read can be done
Register not to be loaded (Marked with △ in the register map)	Write/Read can be done	Write/Read can be done
Read-Only register (Marked with ◇ in the register map)	Read can be done	Read can be done

8.2. Description of Register Regarding Loading

Table 8-2 shows the registers regarding loading.

Table 8-2: Registers Regarding Loading

address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Initial value
31h	-							als	xxxx_xxx0b

als=0 Auto-loading enabled: Any access from I2C to a register area to be loaded is prohibited.
als=1 Auto-loading disabled: Register access functions completely.

32h	ready						jinput	jenable	

ready Hi: Initial EEPROM loading completed.
Lo: Initial EEPROM loading in process.

jinput Hi: When HSY/VSY has not yet been input
Lo: At a normal input operation

jenable Hi: When Henable has been input
Lo: when Henable has not yet been input

9. Power ON Sequence

Figure 9-1 below shows the power ON sequence.

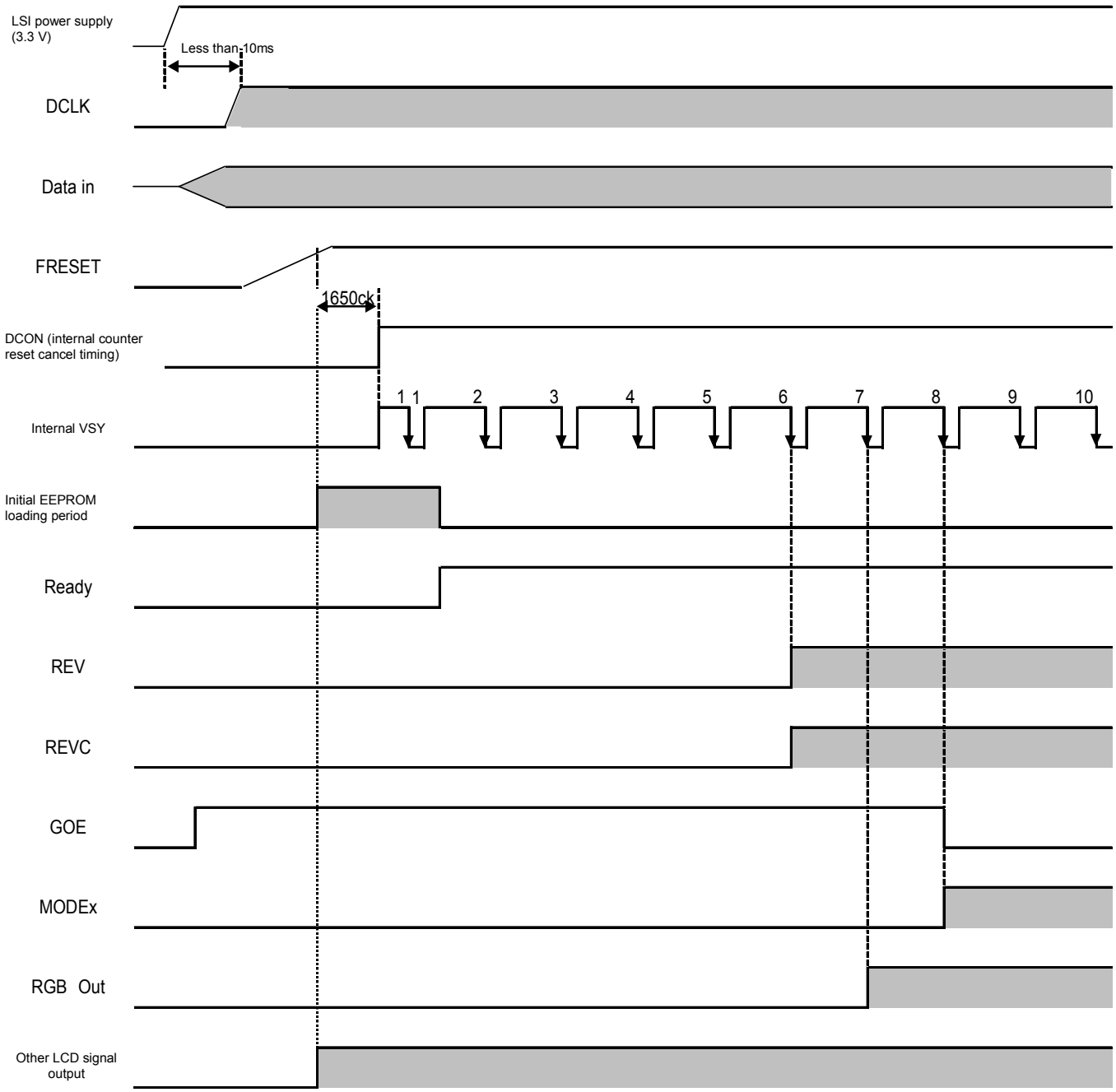


Figure 9-1: Power ON Sequence

Procedure:

(1) When ASIC has turned on, change the reset pin (FRESET) of this ASIC from “Lo” to “Hi” and cancel the reset.

(2) When the reset has been cancelled, ASIC loads the initial values of internal register and LUT from EEPROM (for a maximum period of approximately 2 V).

* In this period, access with I2C from an external CPU to a register to be loaded is prohibited. When making access, check that the ready register is “1” (i.e., initial loading has been completed).

(3) Power ON sequence starts with VsyActive immediately after DCON has become “Hi”.

(4) REV reversal starts according to the Vsy(6) timing. (Polarity reversal starts.)

(5) Data output starts according to the Vsy(7) timing.

(6) The liquid crystal display enters a normal operation state at Vsy(8).

10. I/O Format

Table 10-1 below describes the registers regarding I/O of timing controller (T-CON).

Table 10-1: Registers for I/O format

	address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Initial value
★	08h	henab[7:0]								0010_0011b
★	09h	-	venab[5:0]							0010_0011b

henab: Horizontal display start position specified when the HENABLE signal is fixed to Lo.
venab: Vertical display start position specified.
* Available only when ROMOFF = '0' is set.

★	0Ah	-						rsel	vrvc	hrvc	0000_0000b

rsel, vrvc ,hrvc: Scan direction change setting
* Refer to "Chapter 12: Horizontal/Vertical Reverse Display".

★	0Bh	-	stb_hl[6:0]							0100_0101b

stb_l: Adjustment of STB in Hi period. Pulse width of STB is adjusted and charge share time is adjusted.
* Refer to the set values listed in Table 10-2.

★	0Ch	gck_hl[7:0]								1010_1010b

gck_hl: Adjustment of CLS in Hi period.
* Refer to the set values listed in Table 10-2.

★	0Dh	-	slp_ctrl[6:0]							0100_0011b

slp_ctrl: Adjustment of G_SLP in Lo period.
* Refer to the set values listed in Table 10-2.

★: Auto-loading register

For the initial setting of stb_hl / gck_hl / slp_ctrl when ROMOFF = '0' has been specified, refer to Table 10-2.

Table 10-2: Setting for stb_hl / gckhl / slp_ctrl

	stb_hl	gck_hl	slp_ctrl
WVGA	69	70	67
WQVGA	16	40	16
WEGA1	20	49	19
WEGA2	20	49	19

Perform the gate driver pulse output setting through the GMDSEL pin. Refer to Table 10-3.

Table 10-3: Gate Start Pulse Output Setting

GMDSEL Pin	Gate start pulse output setting
0	Normal mode
1	Interlacing two-pulse mode

11. FreeRun Display

11.1. Overview of FreeRun Display

This ASIC shows the blue background stored internally when a synchronization signal (Hsy/Vsy) input externally has been disappeared.

11.2. Conditions for Transition to FreeRun

This ASIC counts Hsy/Vsy input externally. If the conditions below are met, this ASIC shows the blue background judging that there is no external input or an input error has occurred.

A value of clk of 1H ≥ 1200 clk
A value of clk of 1H ≤ tHA

The number of lines of 1V ≥ 700 lines
The number of lines of 1V ≤ tVA

11.3. Conditions for Recovery from FreeRun

The ASIC counts Hsy/Vsy input externally in the FreeRun state. When the conditions below have been met and the same count value is obtained twice continuously, the ASIC shows the external input signal display judging that there is an external input.

(tHA < a value of clk of 1H < 1200 clk) & the same count value obtained twice continuously
(tVA < the number of lines of 1V < 700 line) & the same count value obtained twice continuously

12. Horizontal/Vertical Reverse Display

This ASIC can reverse the display horizontally/vertically. The source/gate driver scan direction is set through an input pin, i.e., the HRCV pin/VRVC pin, or a register. The settings are described below.

Table 12-1: Horizontal/Vertical Reverse Display Settings

With or without ROM	ROMOFF='0'		ROMOFF='1'
EEPROM setting 0x0a rsel value	rsel='0'	rsel='1'	
Gate/source scan direction setting	15 pin VRVC/ 16 pin HRVC	0x0a vrvc/hrvc register value	15pin VRVC/ 16pin HRVC

Table 10-2: Register Regarding Horizontal/Vertical Reverse Display

	address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Initial value
★	0Ah	-					rsel	vrvc	hrvc	0000_0000b

rsel	For 0' setting, the vertical/horizontal reverse display is set by the input pins VRVC and HRVC. For 1' setting, the vertical/horizontal reverse display is set by the register values vrvc and hrvc.
vrvc	If the rsel register value is '1', the vertical reverse display is set.
hrvc	If the rsel register value is '1', the horizontal reverse display is set.

The HRVC pin/hrvc register setting and the I/O of LBR/STHR/STHL are shown below.

Table 12-3: I/O Related to Horizontal Reverse Display

HRVC pin/ hrvc register	LBR	STHR	STHL
0	0	Input	Output
1	1	Output	Input

※Please confirm the I/O relation described in specifications of LCD, and connect it with LQ0DZC2291.

The VRVC pin/vrvc register setting and the I/O of RL/GSPOI_MODE2/GSPIO_SPS are shown below.

Table 12-4: I/O Related to Vertical Reverse Display

	G_SEL='0'			G_SEL='1'		
VRVC/ vrvc register	R/L	GSPOI_ MODE2	GSPIO_ SPS	R/L	GSPOI_ MODE2	GSPIO_ SPS
0	0	Output (GSPOI)	Input (GSPIO)	1	Output (MODE2)	Output (SPS)
1	1	Input (GSPOI)	Output (GSPIO)	0	Output (MODE2)	Output (SPS)

13. RGB Independent Gamma Correction

13.1. Overview of RGB Independent Gamma Correction

By mapping an input 6-bit data to a 8-bit signal based on the parameter stored in EEPROM, the 6-bit data is converted into 8-bit data in ASIC. This allows to control the gamma characteristics of input data per R, G and B independently. This ASIC is for 6-bit liquid crystal panel. So, the data is converted into 8-bit data in a pseudo way by the FRC technology and is displayed on the 6-bit panel. For turning ON/OFF the independent gamma conversion, refer to the register Map. (This is available only for ROMOFF = '0'.)

13.2. Description of Register Regarding RGB Independent Gamma Correction

Table 13-1 shows the register regarding RGB independent gamma correction.

Table 13-1: Register Regarding RGB Independent Gamma Correction

	address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Initial value
★	0Eh	gamma_en	-							0***_****b

gamma_en: Setting to turn ON/OFF RGB independent gamma
gamma_en='0': Independent gamma correction is disabled. (The gamma correction is omitted.)
gamma_en='1': Independent gamma correction is enabled.

13.3. Flow of Use of Independent Gamma Function

As described above, the independent gamma parameters are loaded from EEPROM. Those independent gamma parameters are stored in the 192 addresses from 0x40 to 0xFF in EEPROM. Therefore, to use the independent gamma function, (1) write the set values corresponding to input gradations in advance and (2) store the data of 0x80 in the address 0x0E (gamma_enb) where is an auto-loading area in EEPROM.