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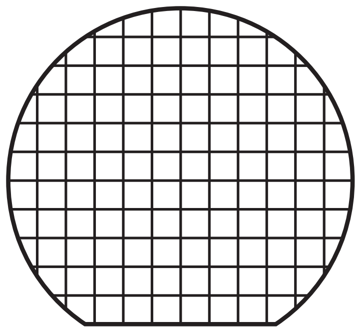
LRI2K

2048-bit EEPROM tag IC at 13.56 MHz, with 64-bit UID and kill code, ISO 15693 and ISO 18000-3 Mode 1 compliant

Features

- ISO 15693 standard fully compliant
- ISO 18000-3 Mode 1 standard fully compliant
- 13.56 MHz ±7 kHz carrier frequency
- To tag: 10% or 100% ASK modulation using 1/4 (26 Kbit/s) or 1/256 (1.6 Kbit/s) pulse position coding
- From tag: load modulation using Manchester coding with 423 kHz and 484 kHz subcarriers in low (6.6 Kbit/s) or high (26 Kbit/s) data rate mode. Supports the 53 Kbit/s data rate with Fast commands
- Internal tuning capacitor (21 pF, 23.5 pF, 28.5 pF, 97 pF)
- 1 000 000 Erase/Write cycles (minimum)
- 40 year data retention (minimum)
- 2048 bits EEPROM with Block Lock feature
- 64-bit unique identifier (UID)
- Electrical article surveillance capable (software controlled)
- Kill function
- Read & Write (Block of 32 bits)
- 5 ms programming time
- Packages
  - ECOPACK® (RoHS compliant)

UFDFPN8 (MB)
2 × 3 mm² (MLP)



Wafer

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1 Description

The LRI2K is a contactless memory powered by the received carrier electromagnetic wave. It is a 2048-bit electrically erasable programmable memory (EEPROM). The memory is organized as 64 blocks of 32 bits. The LRI2K is accessed via the 13.56 MHz carrier electromagnetic wave on which incoming data are demodulated from the received signal amplitude modulation (ASK: amplitude shift keying). The received ASK wave is 10% or 100% modulated with a data rate of 1.6 Kbit/s using the 1/256 pulse coding mode or a data rate of 26 Kbit/s using the 1/4 pulse coding mode.

Outgoing data are generated by the LRI2K load variation using Manchester coding with one or two subcarrier frequencies at 423 kHz and 484 kHz. Data are transferred from the LRI2K at 6.6 Kbit/s in low data rate mode and 26 Kbit/s fast data rate mode. The LRI2K supports 53 Kbit/s in high data rate mode with one subcarrier frequency at 423 kHz.

The LRI2K follows the ISO 15693 recommendation for radio-frequency power and signal interface.

Figure 1. Pad connections

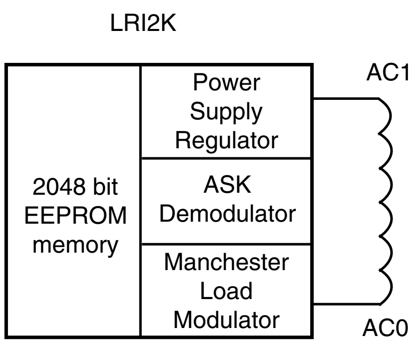
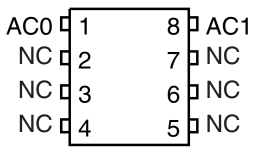


Table 1. Signal names

Signal name	Function
AC1	Antenna coil
AC0	Antenna coil

Figure 2. UFDFPN8 (MLP) connections



1. NC means not connected internally.

1.1 Memory mapping

The LRI2K is divided into 64 blocks of 32 bits. Each block can be individually write-protected using the Lock command.

Table 2. LRI2K memory map

Add	0 7	8 15	16 23	24 31
0	User area			
1	User area			
2	User area			
3	User area			
4	User area			
5	User area			
6	User area			
7	User area			
8	User area			
	User area			
	User area			
	User area			
60	User area			
61	User area			
62	User area			
63	User area			
	UID 0	UID 1	UID 2	UID 3
	UID 4	UID 5	UID 6	UID 7
	AFI	DSFID		
	Kill code			

The User area consists of blocks that are always accessible in read mode. Write operations are possible if the addressed block is not protected. During a write operation, the 32 bits of the block are replaced by the new 32-bit value.

The LRI2K also has a 64-bit block that is used to store the 64-bit unique identifier (UID). The UID is compliant to the ISO 15963 description, and its value is used during the anticollision sequence (Inventory). This block is not accessible by the user and its value is written by ST on the production line.

The LRI2K also includes an AFI register in which the application family identifier is stored, and a DSFID register in which the data storage family identifier used in the anticollision algorithm is stored. The LRI2K has an additional 32-bit block in which the kill code is stored.

1.2 Commands

The LRI2K supports the following commands:

- ***Inventory***, used to perform the anticollision sequence.
- ***Stay Quiet***, used to put the LRI2K in quiet mode, where it does not respond to any inventory command.
- ***Select***, used to select the LRI2K. After this command, the LRI2K processes all Read/Write commands with Select_flag set.
- ***Reset To Ready***, used to put the LRI2K in the ready state.
- ***Read Block***, used to output the 32 bits of the selected block and its locking status.
- ***Write Block***, used to write the 32-bit value in the selected block, provided that it is not locked.
- ***Lock Block***, used to lock the selected block. After this command, the block cannot be modified.
- ***Read Multiple Blocks***, used to read the selected blocks and send back their value.
- ***Write AFI***, used to write the 8-bit value in the AFI register.
- ***Lock AFI***, used to lock the AFI register.
- ***Write DSFID***, used to write the 8-bit value in the DSFID register.
- ***Lock DSFID***, used to lock the DSFID register.
- ***Get System Info***, used to provide the system information value
- ***Get Multiple Block Security Status***, used to send the security status of the selected block.
- ***Initiate***, used to trigger the tag response to the Inventory Initiated sequence.
- ***Inventory Initiated***, used to perform the anticollision sequence triggered by the Initiate command.
- ***Kill***, used to definitively deactivate the tag.
- ***Write Kill***, used to write the 32-bit Kill code value
- ***Lock Kill***, used to lock the Kill Code register.
- ***Fast Initiate***, used to trigger the tag response to the Inventory Initiated sequence.
- ***Fast Inventory Initiated***, used to perform the anticollision sequence triggered by the Initiate command.
- ***Fast Read Block***, used to output the 32 bits of the selected block and its locking status.
- ***Fast Read Multiple Blocks***, used to read the selected blocks and send back their value.

1.3 Initial dialogue for vicinity cards

The dialog between the vicinity coupling device (VCD) and the vicinity integrated circuit card or VICC (LRI2K) takes place as follows:

- activation of the LRI2K by the RF operating field of the VCD
- transmission of a command by the VCD
- transmission of a response by the LRI2K

These operations use the RF power transfer and communication signal interface described below (see *Power transfer*, *Frequency* and *Operating field*). This technique is called RTF (reader talk first).

1.3.1 Power transfer

Power is transferred to the LRI2K by radio frequency at 13.56 MHz via coupling antennas in the LRI2K and the VCD. The RF operating field of the VCD is transformed on the LRI2K antenna as an AC voltage which is rectified, filtered and internally regulated. The amplitude modulation (ASK) on this received signal is demodulated by the ASK demodulator.

1.3.2 Frequency

The ISO 15693 standard defines the carrier frequency (f_c) of the operating field as 13.56 MHz ±7 kHz.

1.3.3 Operating field

The LRI2K operates continuously between H_{min} and H_{max}.

- The minimum operating field is H_{min} and has a value of 150 mA/m rms.
- The maximum operating field is H_{max} and has a value of 5 A/m rms.

A VCD must generate a field of at least H_{min} and not exceeding H_{max} in the operating volume.

2 Communication signal from VCD to LRI2K

Communications between the VCD and the LRI2K take place using the modulation principle of ASK (amplitude shift keying). Two modulation indexes are used, 10% and 100%. The LRI2K decodes both. The VCD determines which index is used.

The modulation index is defined as [a – b]/[a + b] where a is the peak signal amplitude and b the minimum signal amplitude of the carrier frequency.

Depending on the choice made by the VCD, a "pause" will be created as described in *Figure 3* and *Figure 4*.

The LRI2K is operational for any degree of modulation index between 10% and 30%.

Figure 3. 100% modulation waveform

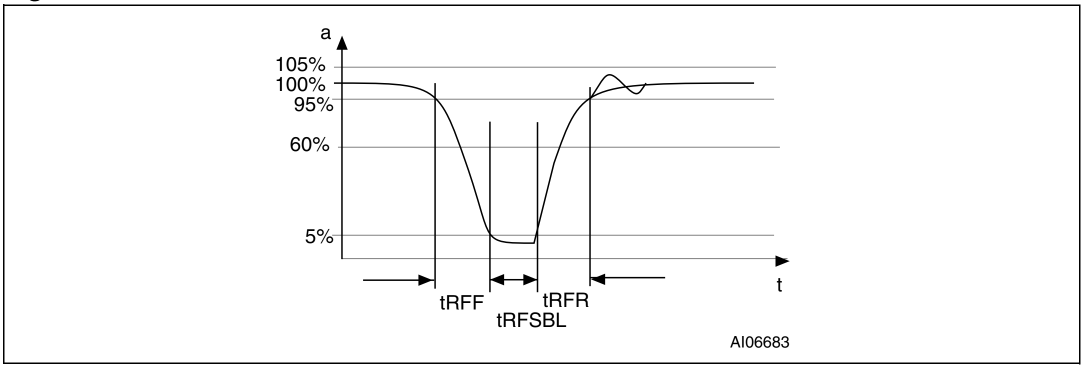
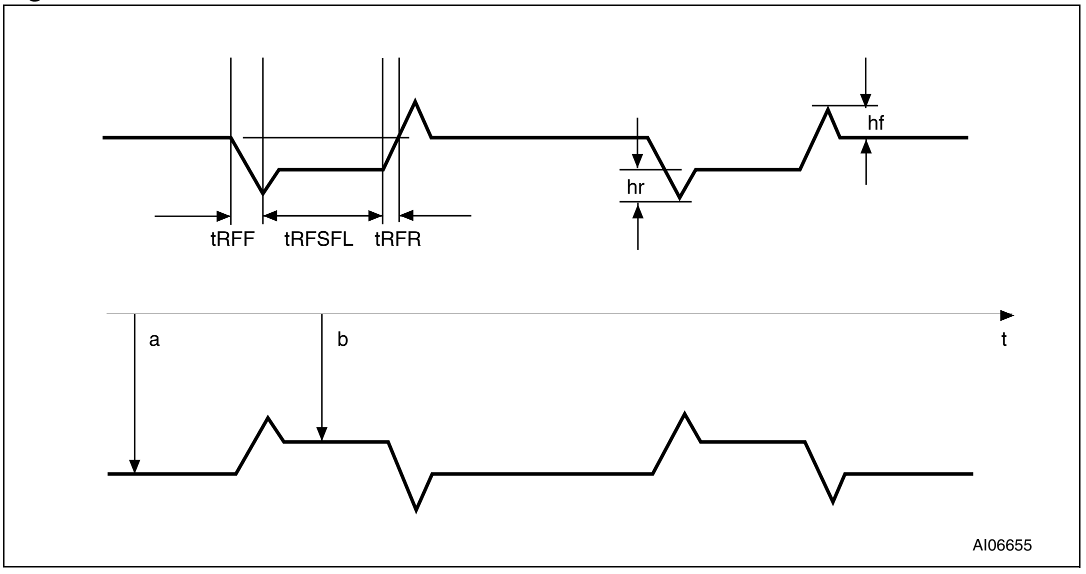


Table 3. 10% modulation parameters

Symbol	Parameter definition	Value
hr	0.1 x (a – b)	max
hf	0.1 x (a – b)	max

Figure 4. 10% modulation waveform



3 Data rate and data coding

The data coding implemented in the LRI2K uses pulse position modulation. Both data coding modes that are described in the ISO 15693 are supported by the LRI2K. The selection is made by the VCD and indicated to the LRI2K within the start of frame (SOF).

3.1 Data coding mode: 1 out of 256

The value of one single byte is represented by the position of one pause. The position of the pause on 1 of 256 successive time periods of 18.88 µs ($256/f_C$), determines the value of the byte. In this case the transmission of one byte takes 4.833 ms and the resulting data rate is 1.65 Kbits/s ($f_C/8192$).

Figure 5 illustrates this pulse position modulation technique. In this Figure, data E1h (225 decimal) is sent by the VCD to the LRI2K.

The pause occurs during the second half of the position of the time period that determines the value, as shown in *Figure 6*.

A pause during the first period transmits the data value 00h. A pause during the last period transmits the data value FFh (255 decimal).

Figure 5. 1 out of 256 coding mode

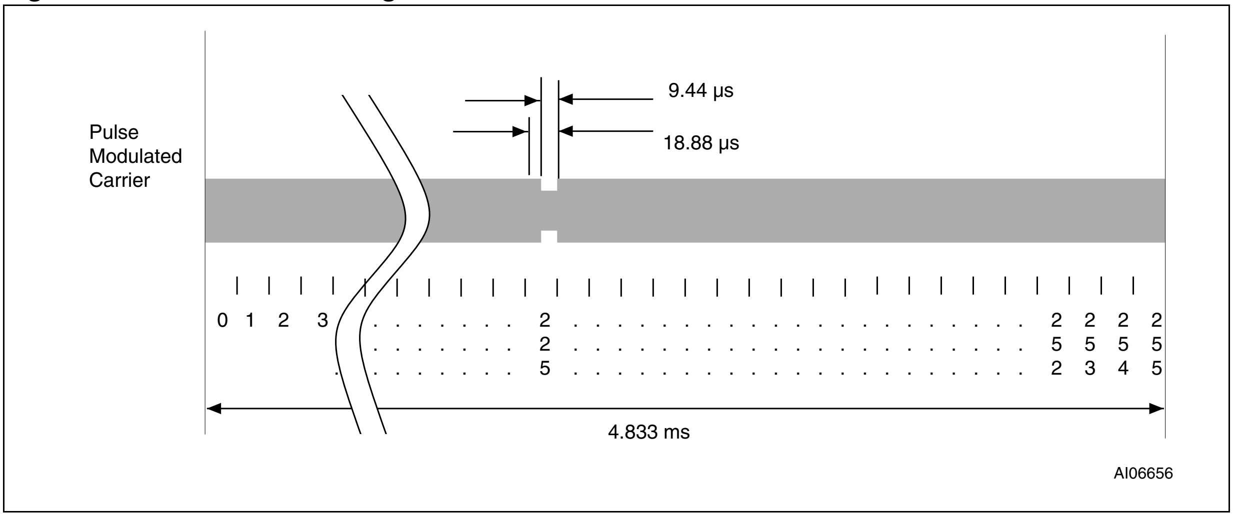
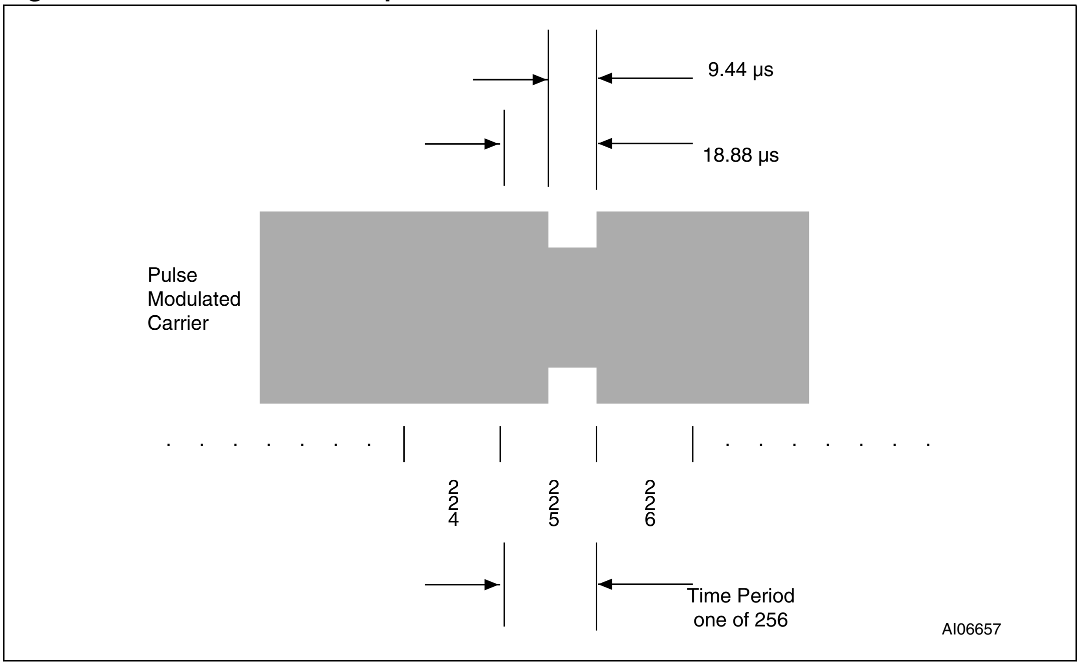


Figure 6. Detail of one time period



3.2 Data coding mode: 1 out of 4

The value of 2 bits is represented by the position of one pause. The position of the pause on 1 of 4 successive time periods of 18.88 µs (256/f_C) determines the value of the 2 bits. Four successive pairs of bits form a byte, where the least significant pair of bits is transmitted first.

In this case the transmission of one byte takes 302.08 µs and the resulting data rate is 26.48 Kbit/s (f_C/512). *Figure 7* illustrates the 1 out of 4 pulse position technique and coding. *Figure 8* shows the transmission of E1h (225d - 1110 0001b) by the VCD.

Figure 7. 1 out of 4 coding mode

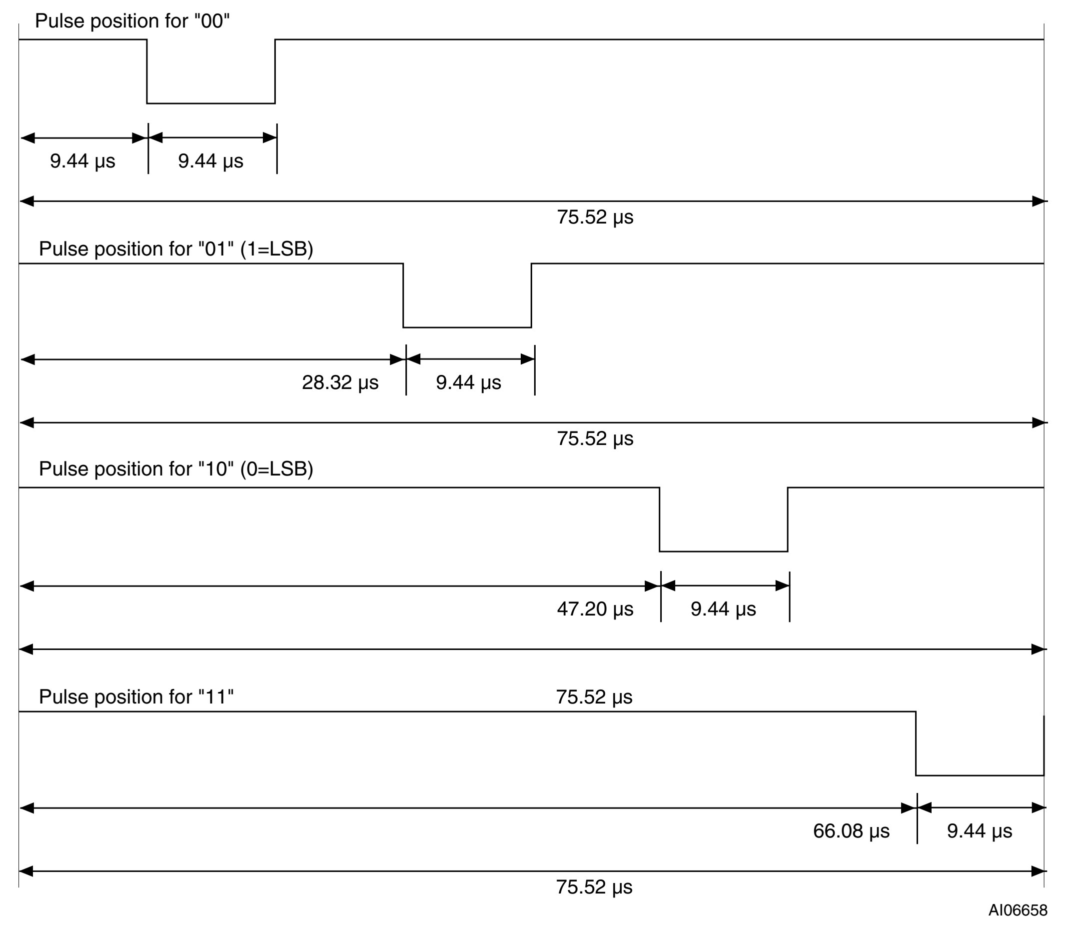
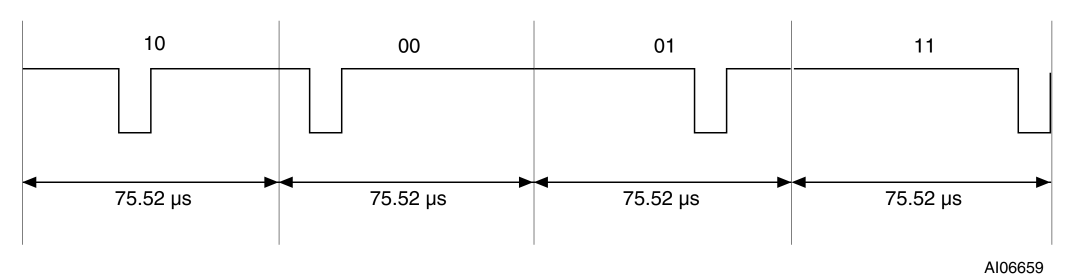


Figure 8. 1 out of 4 coding example



3.3 VCD to LRI2K frames

Frames are delimited by a start of frame (SOF) and an end of frame (EOF). They are implemented using code violation. Unused options are reserved for future use.

The LRI2K is ready to receive a new command frame from the VCD 311.5 µs (t_2) after sending a response frame to the VCD.

The LRI2K takes a Power-On time of 0.1 ms after being activated by the powering field. After this delay, the LRI2K is ready to receive a command frame from the VCD.

3.4 Start of frame (SOF)

The SOF defines the data coding mode the VCD is to use for the following command frame.

The SOF sequence described in *Figure 9* selects the 1 out of 256 data coding mode.

The SOF sequence described in *Figure 10* selects the 1 out of 4 data coding mode.

The EOF sequence for either coding mode is described in *Figure 11*.

Figure 9. SOF to select 1 out of 256 data coding mode

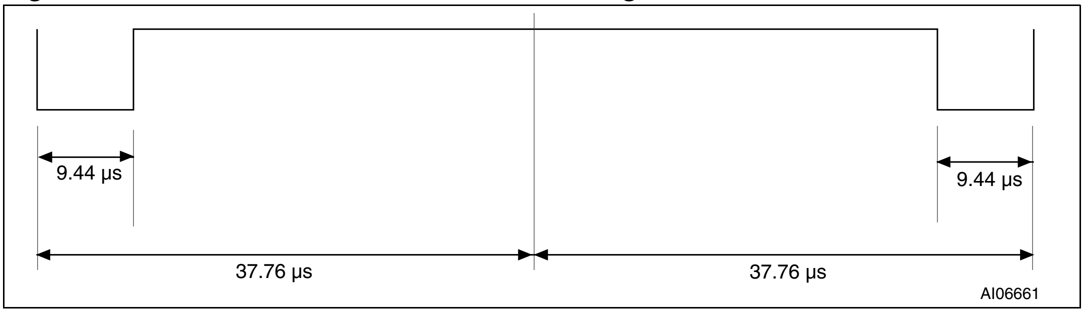


Figure 10. SOF to select 1 out of 4 data coding mode

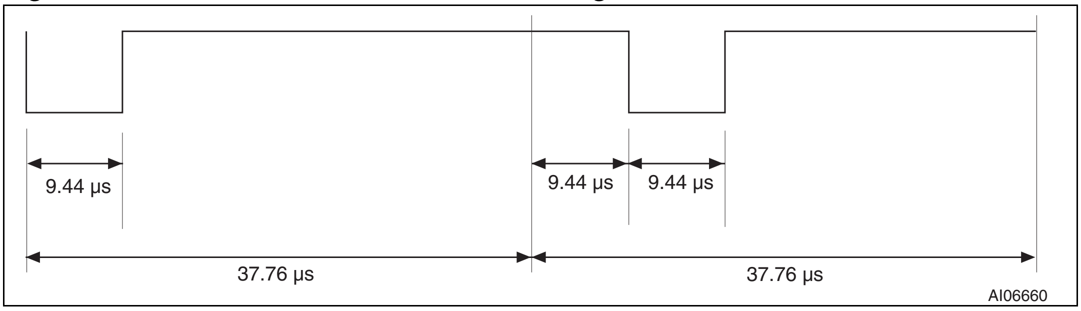
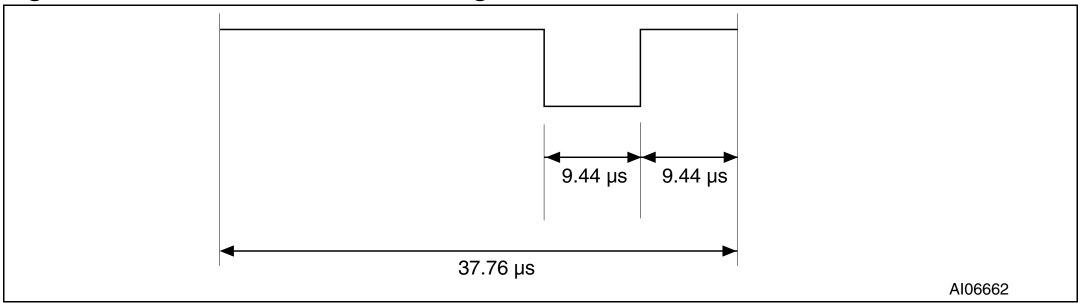


Figure 11. EOF for either data coding mode



4 Communications signal from LRI2K to VCD

The LRI2K has several modes defined for some parameters, owing to which it can operate in different noise environments and meet different application requirements.

4.1 Load modulation

The LRI2K is capable of communication with the VCD via an inductive coupling area whereby the carrier is loaded to generate a subcarrier with frequency f_S. The subcarrier is generated by switching a load in the LRI2K.

The load-modulated amplitude received on the VCD antenna shall be at least 10 mV when measured as described in the test methods defined in International Standard ISO 10373-7.

4.2 Subcarrier

The LRI2K supports the one-subcarrier and two-subcarrier response formats. These formats are selected by the VCD using the first bit in the protocol header. When one subcarrier is used, the frequency f_{S1} of the subcarrier load modulation is 423.75 kHz (f_C/32). When two subcarriers are used, frequency f_{S1} is 423.75 kHz (f_C/32), and frequency f_{S2} is 484.28 kHz (f_C/28). When using the two-subcarrier mode, the LRI2K generates a continuous phase relationship between f_{S1} and f_{S2}.

4.3 Data rates

The LRI2K can respond using the low or the high data rate format. The selection of the data rate is made by the VCD using the second bit in the protocol header. It also supports the x2 mode available on all the Fast commands. *Table 4* shows the different data rates produced by the LRI2K using the different response format combinations.

Table 4. Response data rate

Data rate		One subcarrier	Two subcarriers
Low	Standard commands	6.62 Kbits/s (f_c/2048)	6.67 Kbits/s (f_c/2032)
	Fast commands	13.24 Kbits/s (f_c/1024)	not applicable
High	Standard commands	26.48 Kbits/s (f_c/512)	26.69 Kbits/s (f_c/508)
	Fast commands	52.97 Kbits/s (f_c/256)	not applicable

5 Bit representation and coding

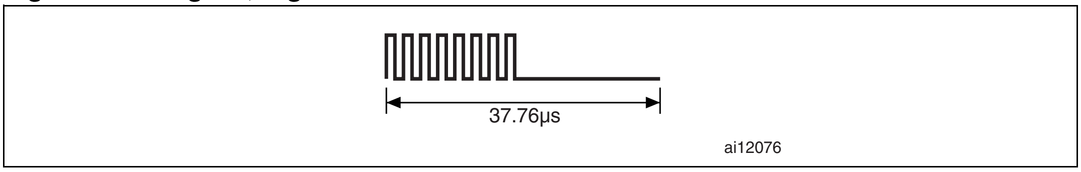
Data bits are encoded using Manchester coding, according to the following schemes. For the low data rate, the same subcarrier frequency or frequencies is/are used, in this case the number of pulses is multiplied by 4 and all times are increased by this factor. For the Fast commands using one subcarrier, all pulse numbers and times are divided by 2.

5.1 Bit coding using one subcarrier

5.1.1 High data rate

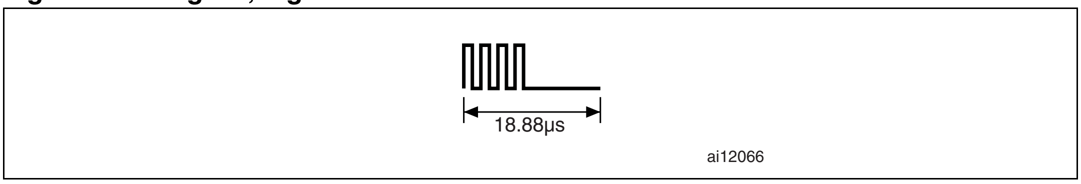
A logic 0 starts with 8 pulses at 423.75 kHz (f_C/32) followed by an unmodulated time of 18.88 µs as shown in *Figure 12*.

Figure 12. Logic 0, high data rate



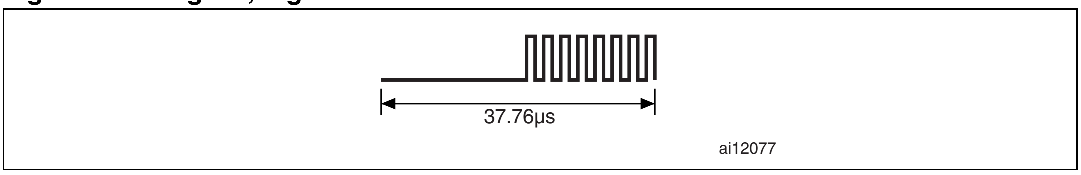
For the Fast commands, a logic 0 starts with 4 pulses at 423.75 kHz (f_C/32) followed by an unmodulated time of 9.44 µs as shown in *Figure 13*.

Figure 13. Logic 0, high data rate x2



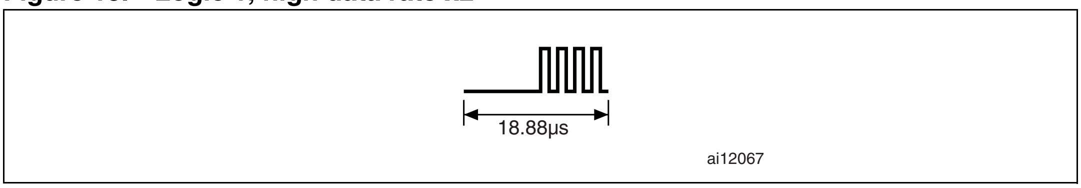
A logic 1 starts with an unmodulated time of 18.88 µs followed by 8 pulses at 423.75 kHz (f_C/32) as shown in *Figure 14*.

Figure 14. Logic 1, high data rate



For the Fast commands, a logic 1 starts with an unmodulated time of 9.44 µs followed by 4 pulses at 423.75 kHz (f_C/32) as shown in *Figure 15*.

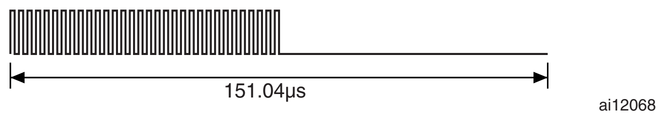
Figure 15. Logic 1, high data rate x2



5.1.2 Low data rate

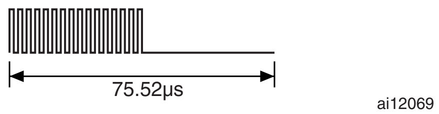
A logic 0 starts with 32 pulses at 423.75 kHz (f_C/32) followed by an unmodulated time of 75.52 µs as shown in *Figure 16*.

Figure 16. Logic 0, low data rate



For the fast commands, a logic 0 starts with 16 pulses of 423,75 kHz (f_C/32) followed by an unmodulated time of 37,76 µs as shown in *Figure 17*.

Figure 17. Logic 0, low data rate x2

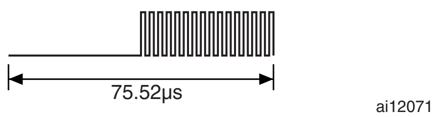


A logic 1 starts with an unmodulated time of 75,52 µs followed by 32 pulses of 423,75 kHz (f_C/32) as shown in *Figure 18*.

Figure 18. Logic 1, low data rate

For the Fast commands, a logic 1 starts with an unmodulated time of 37.76 µs followed by 16 pulses at 423.75 kHz (f_C/32) as shown in *Figure 19*.

Figure 19. Logic 1, low data rate x2

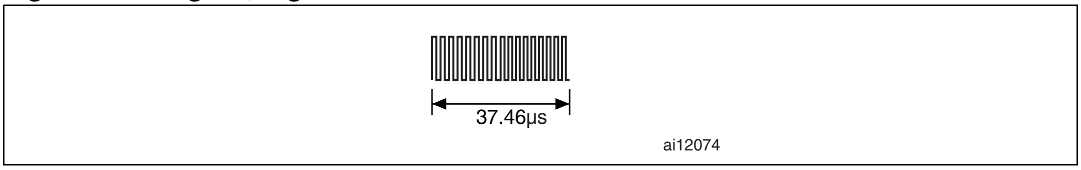


5.2 Bit coding using two subcarriers

5.2.1 High data rate

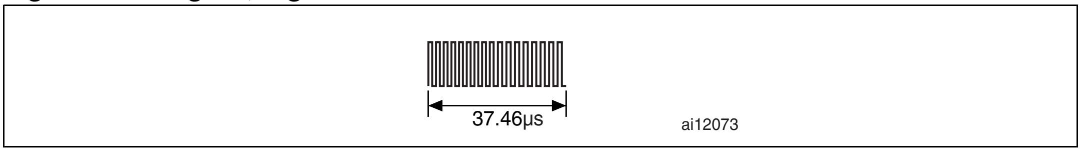
A logic 0 starts with 8 pulses at 423.75 kHz (f_C/32) followed by 9 pulses at 484.28 kHz (f_C/28) as shown in *Figure 20*. For the Fast commands, the x2 mode is not available.

Figure 20. Logic 0, high data rate



A logic 1 starts with 9 pulses at 484.28 kHz (f_C/28) followed by 8 pulses at 423.75 kHz (f_C/32) as shown in *Figure 21*. For the Fast commands, the x2 mode is not available.

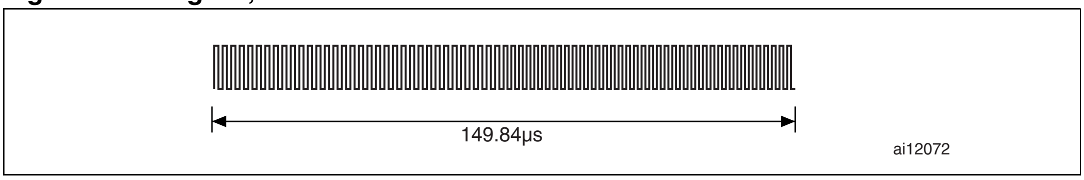
Figure 21. Logic 1, high data rate



5.2.2 Low data rate

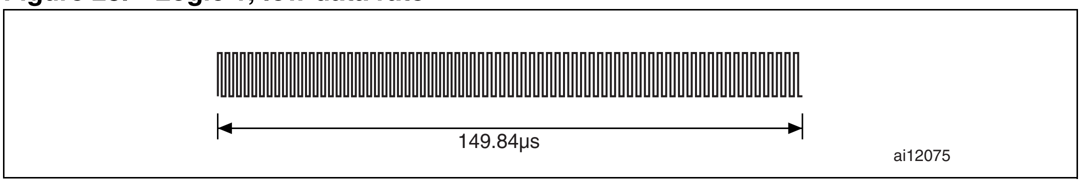
A logic 0 starts with 32 pulses at 423.75 kHz (f_C/32) followed by 36 pulses at 484.28 kHz (f_C/28) as shown in *Figure 22*. For the Fast commands, the x2 mode is not available.

Figure 22. Logic 0, low data rate



A logic 1 starts with 36 pulses at 484.28kHz (f_C/28) followed by 32 pulses at 423.75kHz (f_C/32) as shown in *Figure 23*. For the fast commands, the x2 mode is not available.

Figure 23. Logic 1, low data rate



6 LRI2K to VCD frames

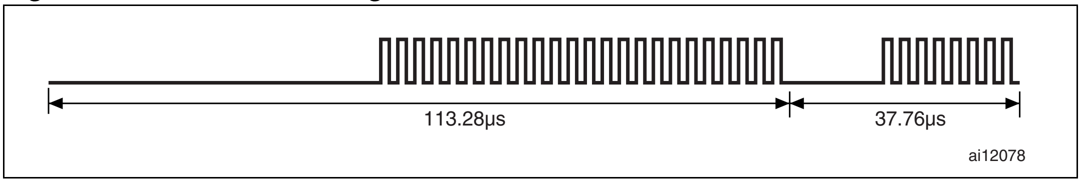
Frames are delimited by an SOF and an EOF. They are implemented using code violation. Unused options are reserved for future use. For the low data rate, the same subcarrier frequency or frequencies is/are used. In this case the number of pulses is multiplied by 4. For the Fast commands using one subcarrier, all pulse numbers and times are divided by 2.

6.1 SOF when using one subcarrier

6.1.1 High data rate

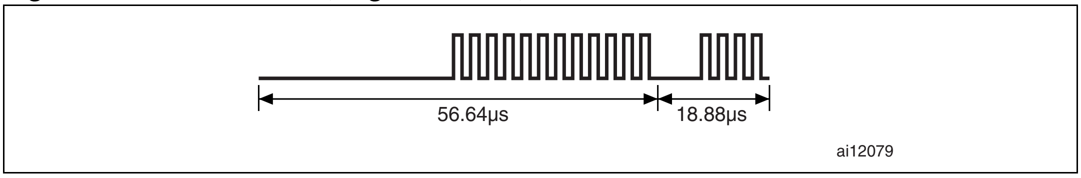
The SOF includes an unmodulated time of 56.64 µs followed by 24 pulses at 423.75 kHz (f_C/32), and a logic 1 that consists of an unmodulated time of 18.88 µs followed by 8 pulses at 423.75 kHz. The SOF is shown in *Figure 24*.

Figure 24. Start of frame, high data rate, one subcarrier



For the Fast commands, the SOF comprises an unmodulated time of 28.32 µs, followed by 12 pulses at 423.75 kHz (f_C/32), and a logic 1 that consists of an unmodulated time of 9.44 µs followed by 4 pulses at 423.75 kHz as shown in *Figure 25*.

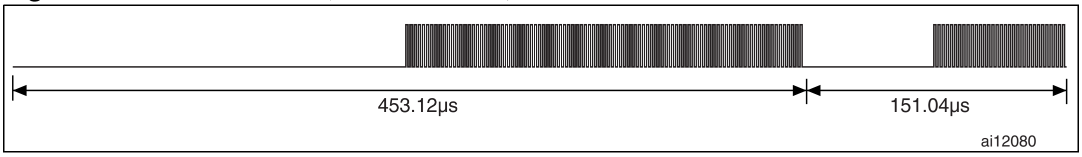
Figure 25. Start of frame, high data rate, one subcarrier x2



6.1.2 Low data rate

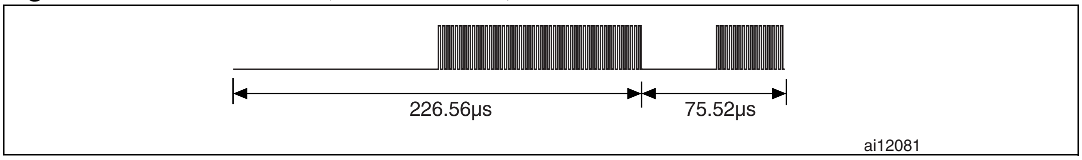
SOF comprises an unmodulated time of 226.56 µs, followed by 96 pulses at 423.75 kHz (f_C/32), and a logic 1 that consists of an unmodulated time of 75.52 µs followed by 32 pulses at 423.75 kHz as shown in *Figure 26*.

Figure 26. Start of frame, low data rate, one subcarrier



For the Fast commands, the SOF comprises an unmodulated time of 113.28 µs followed by 48 pulses at 423.75 kHz (f_C/32), and a logic 1 that includes an unmodulated time of 37.76 µs followed by 16 pulses at 423.75 kHz as shown in *Figure 27*.

Figure 27. Start of frame, low data rate, one subcarrier x2



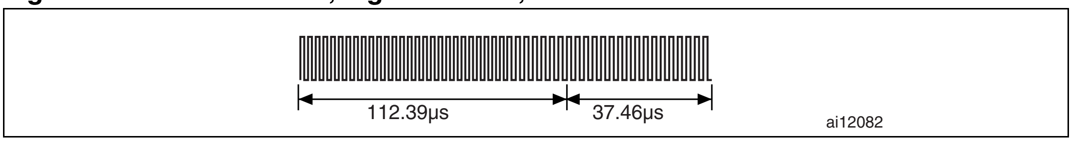
6.2 SOF when using two subcarriers

6.2.1 High data rate

The SOF comprises 27 pulses at 484.28 kHz (f_C/28), followed by 24 pulses at 423.75 kHz (f_C/32), and a logic 1 that includes 9 pulses at 484.28 kHz followed by 8 pulses at 423.75 kHz as shown in *Figure 28*.

For the Fast commands, the x2 mode is not available.

Figure 28. Start of frame, high data rate, two subcarriers

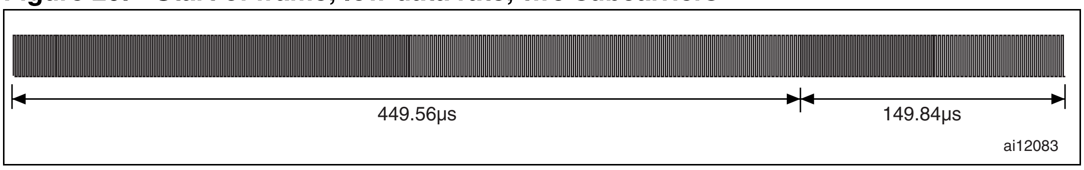


6.2.2 Low data rate

The SOF comprises 108 pulses at 484.28 kHz (f_C/28) followed by 96 pulses at 423.75 kHz (f_C/32), and a logic 1 that includes 36 pulses at 484.28 kHz followed by 32 pulses at 423.75 kHz as shown in *Figure 29*.

For the Fast commands, the x2 mode is not available.

Figure 29. Start of frame, low data rate, two subcarriers

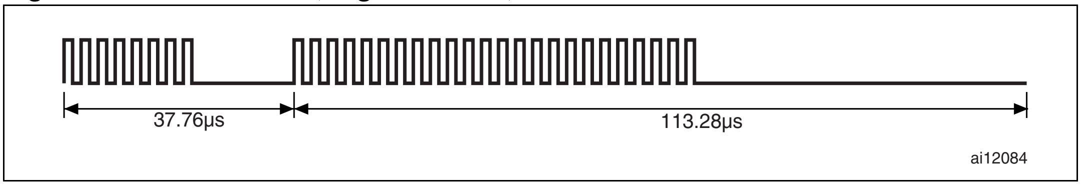


6.3 EOF when using one subcarrier

6.3.1 High data rate

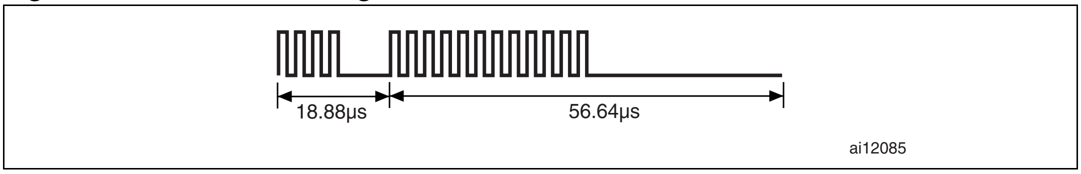
The EOF comprises a logic 0 that includes 8 pulses at 423.75 kHz and an unmodulated time of 18.88 µs, followed by 24 pulses at 423.75 kHz (f_C/32) and by an unmodulated time of 56.64 µs as shown in *Figure 30*.

Figure 30. End of frame, high data rate, one subcarrier



For the Fast commands, the EOF comprises a logic 0 that includes 4 pulses at 423.75 kHz and an unmodulated time of 9.44 µs, followed by 12 pulses at 423.75 kHz (f_C/32) and an unmodulated time of 28.32 µs as shown in *Figure 31*.

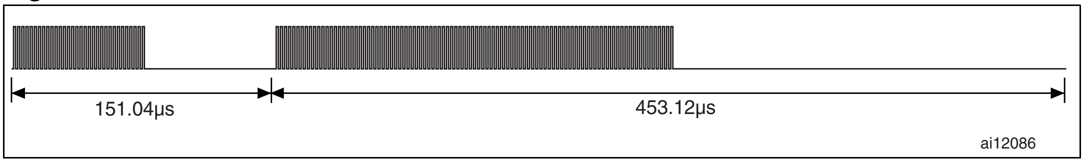
Figure 31. End of frame, high data rate, one subcarrier x2



6.3.2 Low data rate

The EOF comprises a logic 0 that includes 32 pulses at 423.75 kHz and an unmodulated time of 75.52 µs, followed by 96 pulses at 423.75 kHz (f_C/32) and an unmodulated time of 226.56 µs as shown in *Figure 32*.

Figure 32. End of frame, low data rate, one subcarrier



For the Fast commands, the EOF comprises a logic 0 that includes 16 pulses at 423.75 kHz and an unmodulated time of 37.76 µs, followed by 48 pulses at 423.75 kHz (f_C/32) and an unmodulated time of 113.28 µs as shown in *Figure 33*.

Figure 33. End of frame, low data rate, one subcarrier x2