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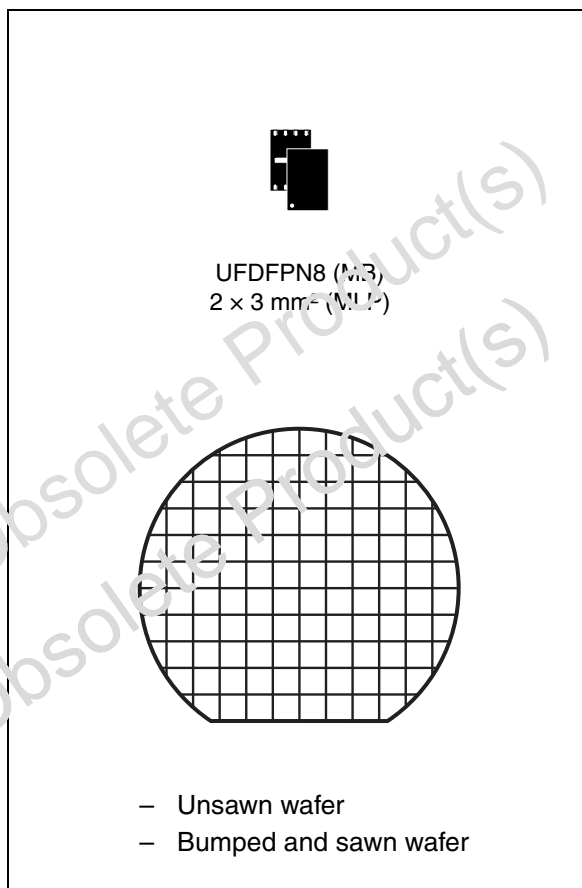


LRI64

Memory tag IC at 13.56 MHz, with 64-bit unique ID and WORM user area, ISO 15693 and ISO 18000-3 Mode 1 compliant

Features

- ISO 15693 compliant
- ISO 18000-3 Mode 1 compliant
- 13.56 MHz \pm 7 kHz carrier frequency
- Supported data transfer to the LRI64:
10% ASK modulation using "1-out-of-4" pulse position coding (26 Kbit/s)
- Supported data transfer from the LRI64:
Load modulation using Manchester coding with 423 kHz single subcarrier in fast data rate (26 Kbit/s)
- Internal tuning capacitor (21 pF, 28.5 pF, 97 pF)
- 7 \times 8 bits WORM user area
- 64-bit unique identifier (UID)
- Read Block and Write Block commands (3-bit blocks)
- 7 ms programming time (typical)
- More than 40-year data retention
- Electrical article surveillance (EAS) capable (software controlled)
- Packages
 - ECOMPACK® (RoHS compliant)



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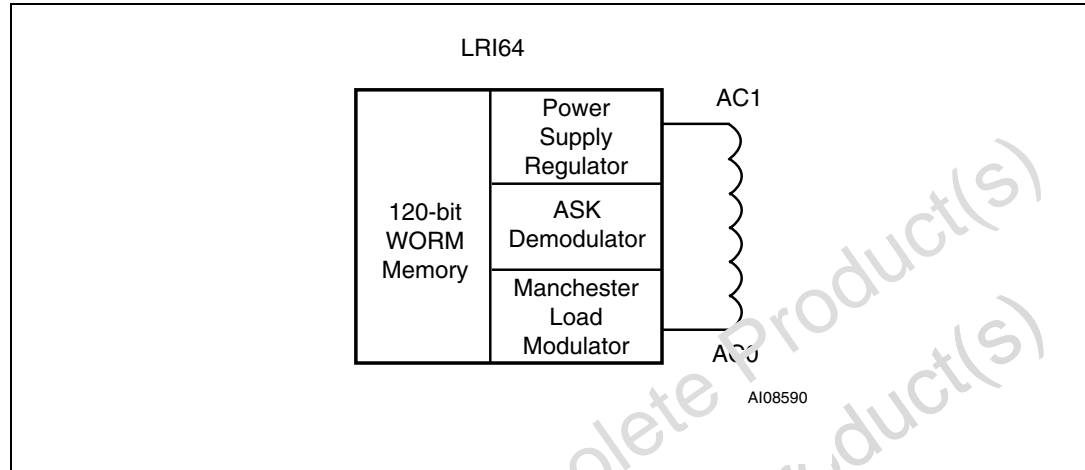
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1 Description

The LRI64 is a contactless memory, powered by an externally transmitted radio wave. It contains a 120-bit non-volatile memory. The memory is organized as 15 blocks of 8 bits, of which 7 blocks are accessible as write-once read-many (WORM) memory.

Figure 1. Logic diagram



The LRI64 is accessed using a 13.56 MHz carrier wave. Incoming data are demodulated from the received amplitude shift keying (ASK) signal, 10% modulated. The data are transferred from the reader to the LRI64 at 26 Kbit/s, using the “1-out-of-4” pulse encoding mode.

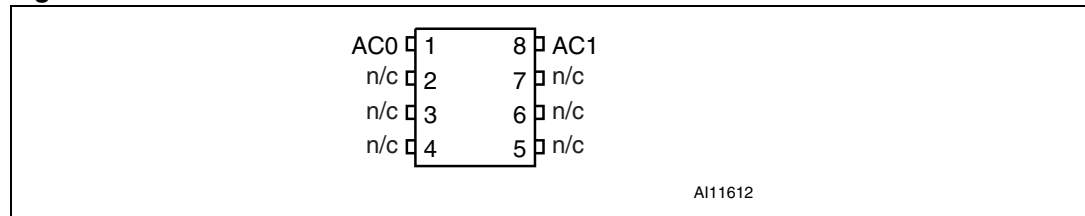
Outgoing data are sent by the LRI64, generated by load variation on the carrier wave, using Manchester coding with a single subcarrier frequency of 423 kHz. The data are transferred from the LRI64 to the reader at 26 Kbit/s, in the high data rate mode.

The LRI64 supports the high data rate communication protocols of ISO 15693 and ISO 18000-3 Mode 1 recommendations. All other data rates and modulations are not supported by the LRI64.

Table 1. Signal names

Signal name	Description
AC1	Antenna coil
AC0	Antenna coil

Figure 2. UDFPN8 connections

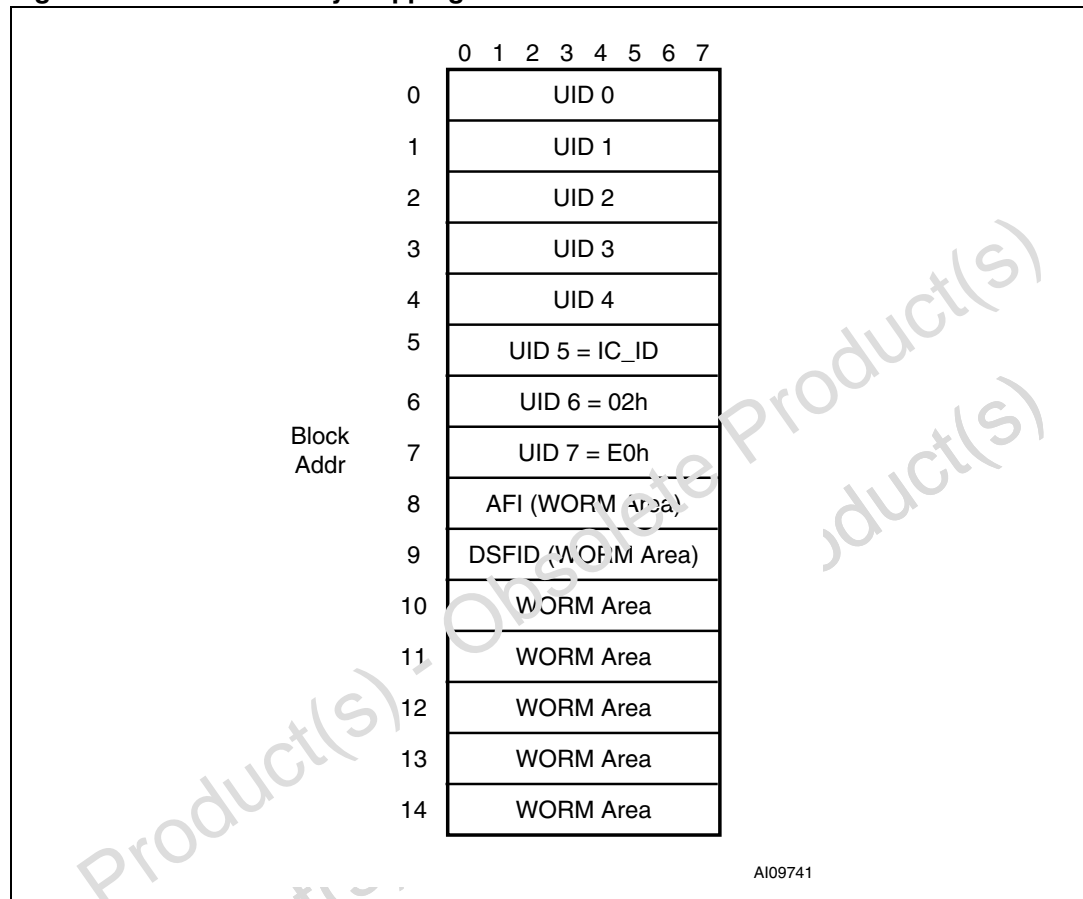


1. n/c means not connected internally.

1.1 Memory mapping

The LRI64 is organized as 15 blocks of 8 bits as shown in [Figure 3](#). Each block is automatically write-protected after the first valid write access.

Figure 3. LRI64 memory mapping



The LRI64 uses the first 8 blocks (blocks 0 to 7) to store the 64-bit unique identifier (UID). The UID is used during the anticollision sequence (Inventory). It is written, by ST, at time of manufacture, but part of it can be customer-accessible and customer-writable, on special request.

The LRI64 has an AFI register, in which to store the application family identifier value, which is also used during the anticollision sequence.

The LRI64 has a DSFID register, in which to store the data storage format identifier value, which is used for the LRI64 Inventory answer.

The five following blocks (blocks 10 to 14) are write-once read-many (WORM) memory. It is possible to write to each of them once. After the first valid write access, the block is automatically locked, and only read commands are possible.

2 Signal description

AC1, AC0

The pads for the antenna coil. AC1 and AC0 must be directly bonded to the antenna.

3 Commands

The LRI64 supports the following commands:

3.1 Inventory

Used to perform the anticollision sequence. The LRI64 answers to the inventory command when all of the 64 bits of the UID have been correctly written.

3.2 Stay Quiet

Used to put the LRI64 in Quiet mode. In this mode, the LRI64 only responds to commands in Addressed mode.

3.3 Read Block

Used to output the 8 bits of the selected block.

3.4 Write Block

Used to write a new 8-bit value in the selected block, provided that the block is not locked. This command can be issued only once to each block.

3.5 Get_System_Info

Used to allow the application system to identify the product. It gives the LRI64 memory size, and IC reference (IC_ID).

3.6 Initial Dialogue for Vicinity Cards

The dialogue between the vicinity coupling device (VCD) and the LRI64 is conducted according to a technique called reader talk first (RTF). This involves the following sequence of operations:

1. activation of the LRI64 by the RF operating field of the VCD
2. transmission of a command by the VCD
3. transmission of a response by the LRI64

4 Power transfer

Power transfer to the LRI64 is accomplished by inductive coupling of the 13.56 MHz radio signal between the antennas of the LRI64 and VCD. The RF field transmitted by the VCD induces an AC voltage on the LRI64 antenna, which is then rectified, smoothed and voltage-regulated. Any amplitude modulation present on the signal is demodulated by the amplitude shift keying (ASK) demodulator.

4.1 Frequency

ISO 15693 and ISO 18000-3 Mode 1 standards define the carrier frequency (f_C) of the operating field to be 13.56 MHz \pm 7kHz.

4.2 Operating field

The LRI64 operates continuously between H_{min} and H_{max} .

- The minimum operating field is H_{min} and has a value of 100mA/m (rms).
- The maximum operating field is H_{max} and has a value of 5A/m (rms).

A VCD generates a field of at least H_{min} and not exceeding H_{max} in the operating volume.

5 Communication signal from VCD to LRI64

Communications between the VCD and the LRI64 involves a type of amplitude modulation called amplitude shift keying (ASK).

The LRI64 only supports the 10% modulation mode specified in ISO 15693 and ISO 18000-3 Mode 1 standards. Any request that the VCD might send using the 100% modulation mode, is ignored, and the LRI64 remains in its current state. However, the LRI64 is, in fact, operational for any degree of modulation index from between 10% and 30%.

The modulation index is defined as $(a-b)/(a+b)$ where a and b are the peak and minimum signal amplitude, respectively, of the carrier frequency, as shown in [Figure 4](#).

Table 2. 10% modulation parameters

Parameter	Min	Max
hr	–	0.1 x (a-b)
hf	–	0.1 x (a-b)

Figure 4. 10% modulation waveform

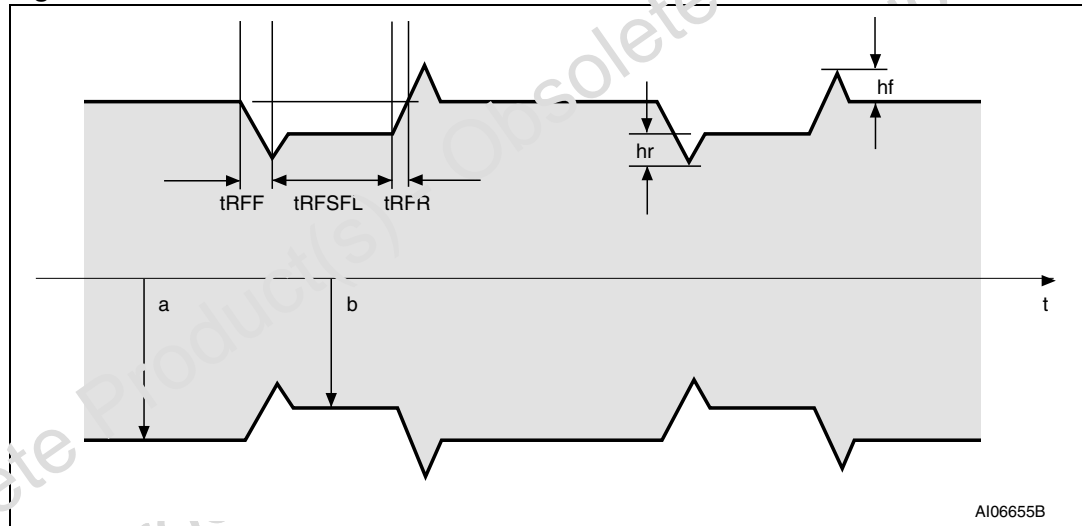
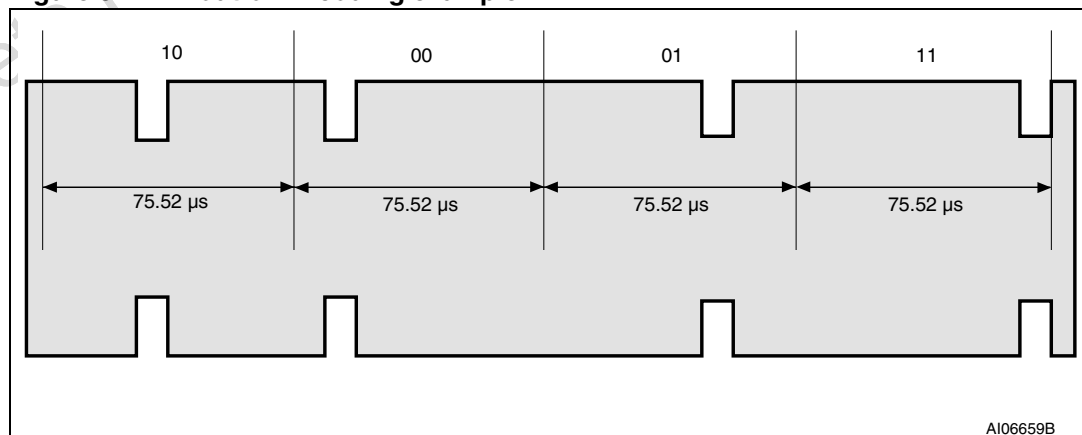


Figure 5. “1-out-of-4” coding example



6 Data rate and data coding

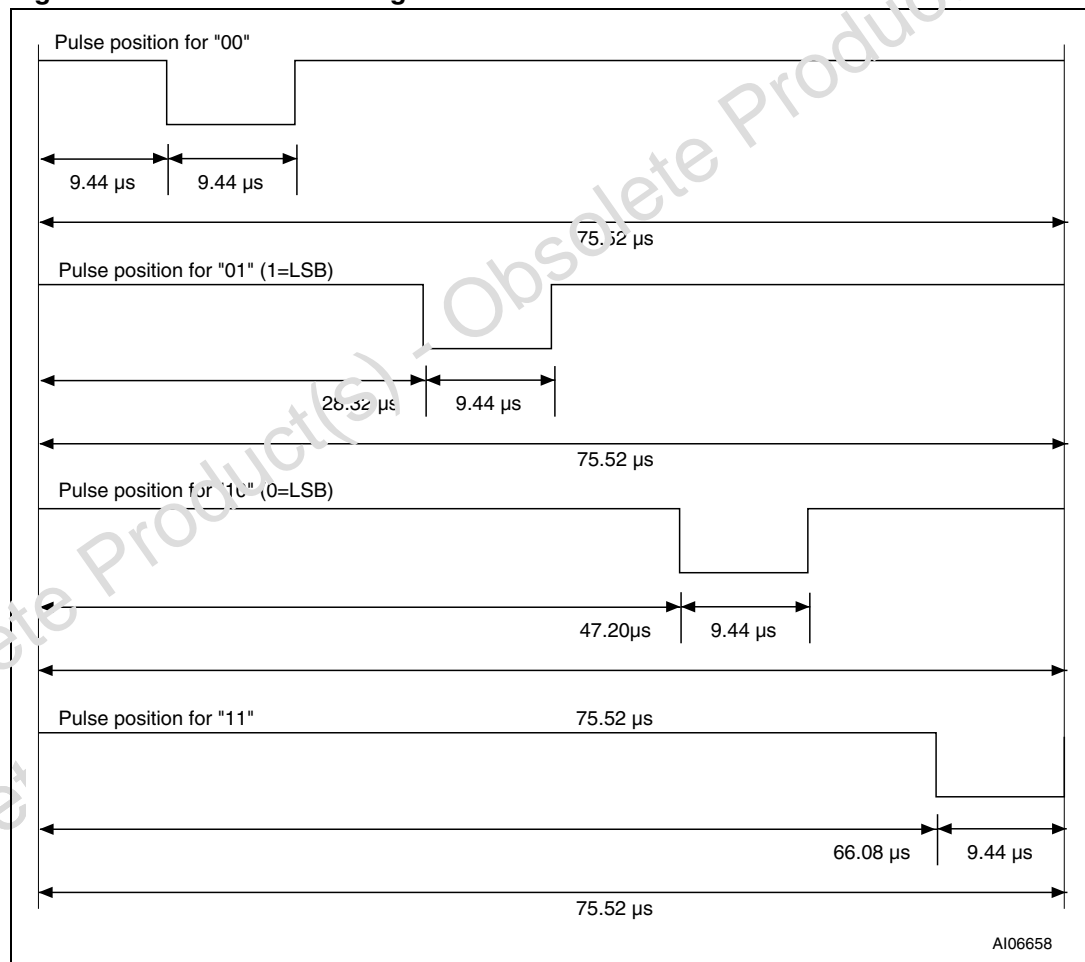
The data coding method involves pulse position modulation. The LRI64 supports the “1-out-of-4” pulse coding mode. Any request that the VCD might send in the “1-out-of-256” pulse coded mode, is ignored, and the LRI64 remains in its current state.

Two bit values are encoded at a time, by the positioning of a pause of the carrier frequency in one of four possible $18.88 \mu\text{s}$ ($256/f_C$) time slots, as shown in [Figure 6](#).

Four successive pairs of bits form a byte. The transmission of one byte takes $302.08 \mu\text{s}$ and, consequently, the data rate is 26.48 Kbit/s ($f_C/512$).

The encoding for the least significant pair of bits is transmitted first. For example [Figure 5](#) shows the transmission of E1h (225d, 1110 0001b) by the VCD.

Figure 6. “1-out-of-4” coding mode



7 VCD to LRI64 frames

Request frames are delimited by a start of frame (SOF) and an end of frame (EOF) and are implemented using a code violation mechanism. Unused options are reserved for future use.

The LRI64 is ready to receive a new command frame from the VCD after a delay of t_2 (see [Table 14](#)) after having sent a response frame to the VCD.

The LRI64 generates a power-on delay of t_{POR} (see [Table 14](#)) after being activated by the powering field. After this delay, the LRI64 is ready to receive a command frame from the VCD.

In ISO 15693 and ISO 18000-3 Mode 1 standards, the SOF is used to define the data coding mode that the VCD is going to use in the following command frame.

The SOF that is shown in [Figure 7](#) selects the “1-out-of-4” data coding mode. (The LRI64 does not support the SOF for the “1-out-of-256” data coding mode.)

The corresponding EOF sequence is shown in [Figure 8](#).

Figure 7. Request SOF, using the “1-out-of-4” data coding mode

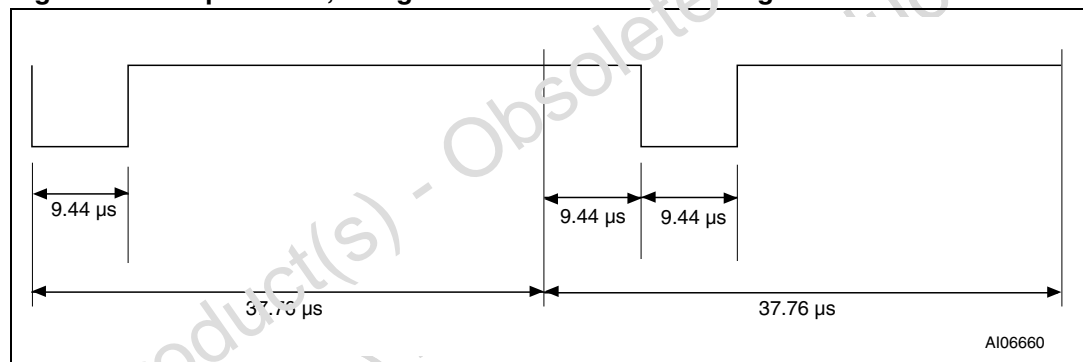
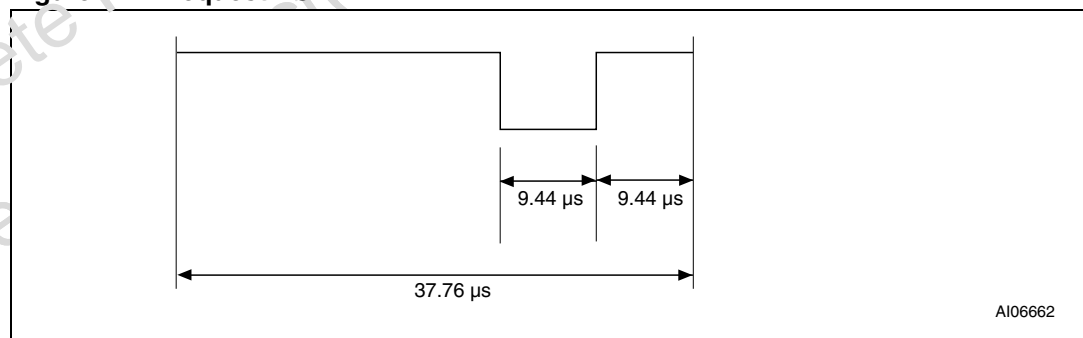


Figure 8. Request EOF



8 Communications signal from LRI64 to VCD

ISO 15693 and ISO 18000-3 Mode 1 standards define several modes, for some parameters, to cater for use in different application requirements and noise environments. The LRI64 does not support all of these modes, but supports the single subcarrier mode at the fast data rate.

8.1 Load modulation

The LRI64 is capable of communication to the VCD via the inductive coupling between the two antennas. The carrier is loaded, with a subcarrier with frequency f_S , generated by switching a load in the LRI64.

The amplitude of the variation to the signal, as received on the VCD antenna, is at least 10 mV, when measured as described in the test methods defined in International Standard ISO 10373-7.

8.2 Subcarrier

The LRI64 supports the one subcarrier modulation response format. This format is selected by the VCD using the first bit in the protocol header.

The frequency, f_S , of the subcarrier load modulation is 423.75 kHz ($=f_C/32$).

8.3 Data rate

The LRI64 response uses the high data rate format (26.48 Kbit/s). The selection of the data rate is made by the VCD using the second bit in the protocol header.

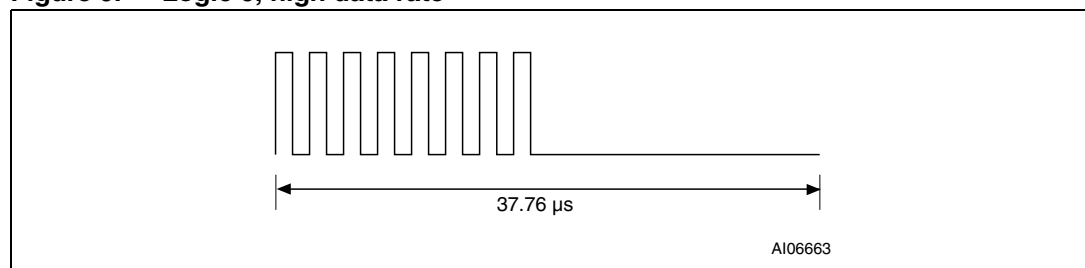
8.4 Bit representation and coding using one subcarrier, at the high data rate

Data bits are encoded using Manchester coding, as described in [Figure 9](#) and [Figure 10](#).

8.4.1 Logic 0

A logic 0 starts with 8 pulses of 423.75 kHz ($f_C/32$) followed by an unmodulated period of 18.88 μ s as shown in [Figure 9](#).

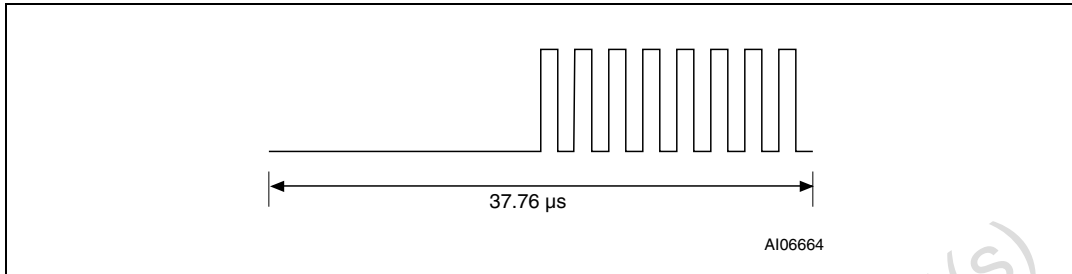
Figure 9. Logic 0, high data rate



8.4.2 Logic 1

A logic 1 starts with an unmodulated period of 18.88 μs followed by 8 pulses of 423.75 kHz ($f_c/32$) as shown in [Figure 10](#).

Figure 10. Logic 1, high data rate



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9 LRI64 to VCD frames

Response frames are delimited by a start of frame (SOF) and an end of frame (EOF) and are implemented using a code violation mechanism. The LRI64 supports these in the one subcarrier mode, at the fast data rate, only.

The VCD is ready to receive a response frame from the LRI64 before $320.9\mu\text{s}$ (t_1) after having sent a command frame.

9.1 LRI64 SOF

SOF comprises three parts: (see [Figure 11](#))

- an unmodulated period of $56.64\mu\text{s}$,
- 24 pulses of 423.75 kHz ($f_c/32$),
- a logic 1 which starts with an unmodulated period of $18.88\mu\text{s}$ followed by 8 pulses of 423.75 kHz .

9.2 LRI64 EOF

EOF comprises three parts: (see [Figure 12](#))

- a logic 0 which starts with 8 pulses of 423.75 kHz followed by an unmodulated period of $18.88\mu\text{s}$.
- 24 pulses of 423.75 kHz ($f_c/32$),
- an unmodulated time of $56.64\mu\text{s}$.

Figure 11. Response SOF, using high data rate and one subcarrier

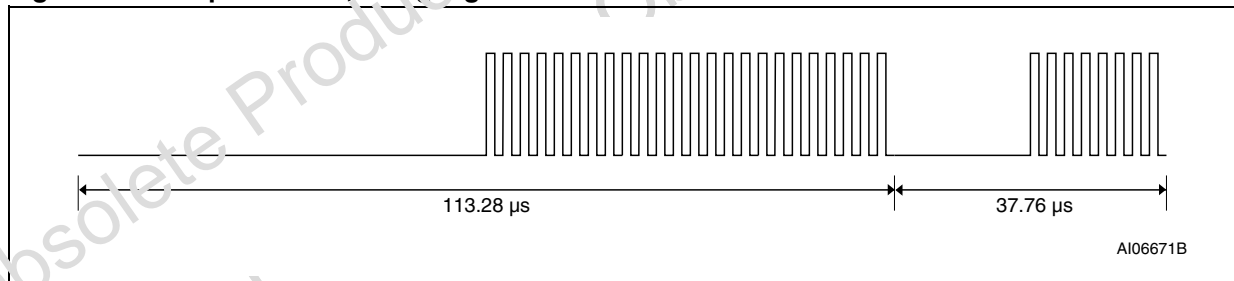
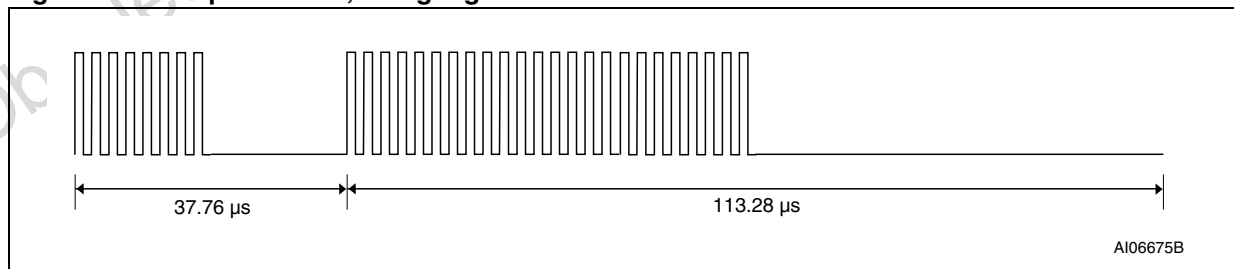


Figure 12. Response EOF, using high data rate and one subcarrier



10 Special fields

10.1 Unique identifier (UID)

Members of the LRI64 family are uniquely identified by a 64-bit unique identifier (UID). This is used for addressing each LRI64 device uniquely and individually, during the anticollision loop and for one-to-one exchange between a VCD and an LRI64.

The UID complies with ISO/IEC 15963 and ISO/IEC 7816-6. It is a read-only code, and comprises (as summarized in *Figure 13*):

- 8-bit prefix, the most significant bits, set at E0h
- 8-bit IC manufacturer code (ISO/IEC 7816-6/AM1), set at 02h (for STMicroelectronics)
- 48-bit unique serial number

Figure 13. UID format

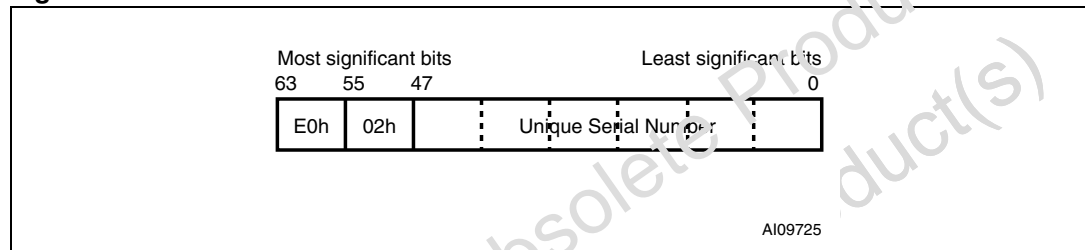
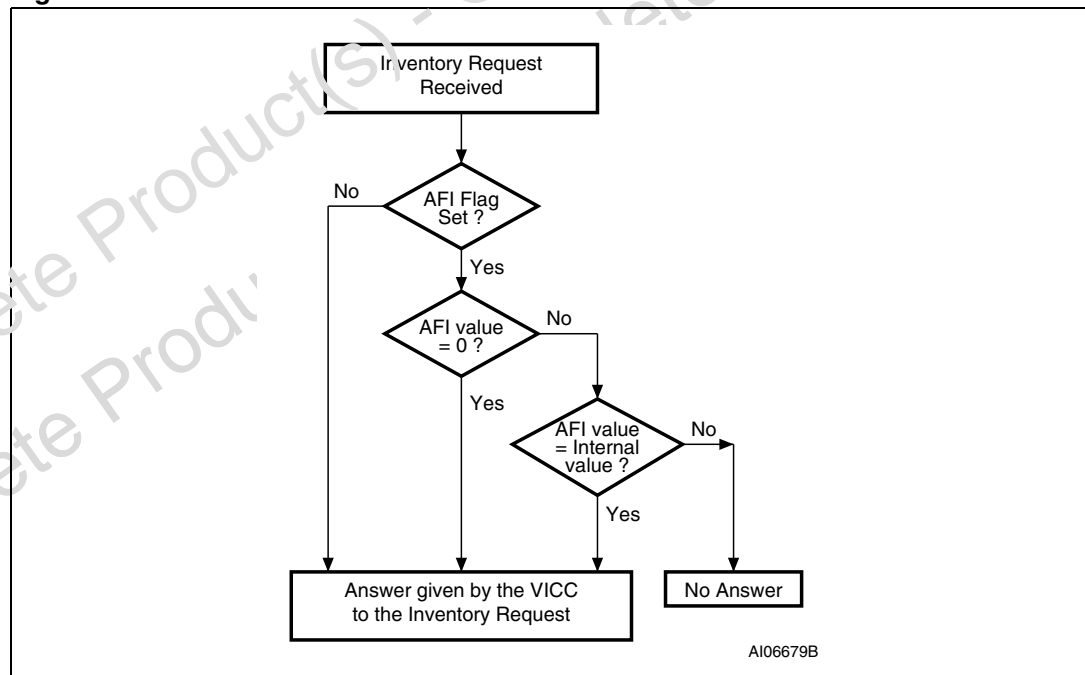


Figure 14. Decision tree for AFI



10.2 Application family identifier (AFI)

The application family identifier (AFI) indicates the type of application targeted by the VCD, and is used to select only those LRI64 devices meeting the required application criteria (as summarized in [Figure 14](#)). The value is programmed by the LRI64 issuer in the AFI register. Once programmed, it cannot be modified.

The most significant nibble of the AFI is used to indicate one specific application, or all families. The least significant nibble of the AFI is used to code one specific subfamilies, or all subfamilies. Subfamily codes, other than 0, are proprietary (as described in ISO 15693 and ISO 18000-3 Mode 1 documentation).

10.3 Data storage format identifier (DSFID)

The data storage format identifier (DSFID) indicates how the data is structured in the LRI64 memory. It is coded on one byte. It allows for quick and brief knowledge on the logical organization of the data. It is programmed by the LRI64 issuer in the DSFID register. Once programmed, it cannot be modified.

10.4 Cyclic redundancy code (CRC)

The cyclic redundancy code (CRC) is calculated as defined in ISO/IEC 13239, starting from an initial register content of all ones: FFFFh.

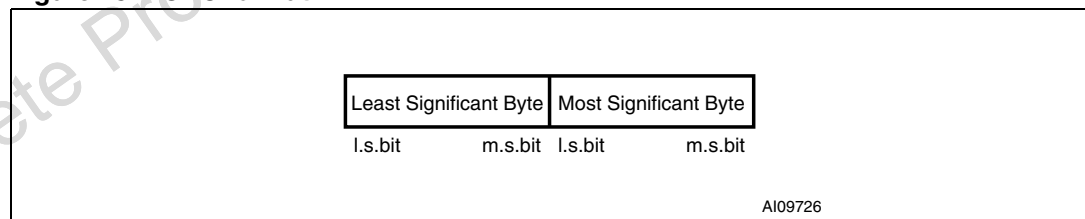
The 2-byte CRC is appended to each request and each response, within each frame, before the EOF. The CRC is calculated on all the bytes after the SOF, up to the CRC field.

Upon reception of a request from the VCD, the LRI64 verifies that the CRC value is valid. If it is invalid, it discards the frame, and does not answer the VCD.

Upon reception of a response from the LRI64, it is recommended that the VCD verify that the CRC value is valid. If it is invalid, the actions that need to be performed are up to the VCD designer.

The CRC is transmitted least significant byte first. Each byte is transmitted Least Significant Bit first, as shown in [Figure 15](#).

Figure 15. CRC format



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11 LRI64 protocol description

The Transmission protocol defines the mechanism to exchange instructions and data between the VCD and the LRI64, in each direction. Based on “VCD talks first”, the LRI64 does not start transmitting unless it has received and properly decoded an instruction sent by the VCD.

The protocol is based on an exchange of:

- a request from the VCD to the LRI64
- a response from the LRI64 to the VCD

Each request and each response are contained in a frame. The frame delimiters (SOF, EOF) are described in the previous paragraphs.

Each request ([Figure 16](#)) consists of:

- Request SOF ([Figure 7](#))
- Request flags ([Table 3](#) to [Table 5](#))
- Command code
- Parameters (depending on the command)
- Application data
- 2-byte CRC ([Figure 15](#))
- Request EOF ([Figure 8](#))

Each response ([Figure 17](#)) consists of:

- Response SOF ([Figure 11](#))
- Response flags ([Table 6](#))
- Parameters (depending on the command)
- Application data
- 2-byte CRC ([Figure 15](#))
- Response EOF ([Figure 12](#))

The number of bits transmitted in a frame is a multiple of eight, and thus always an integer number of bytes.

Single-byte fields are transmitted least significant bit first.

Multiple-byte fields are transmitted least significant byte first, with each byte transmitted least significant bit first.

The setting of the flags indicates the presence of any optional fields. When the flag is set, 1, the field is present. When the flag is reset, 0, the field is absent.

Figure 16. VCD request frame format

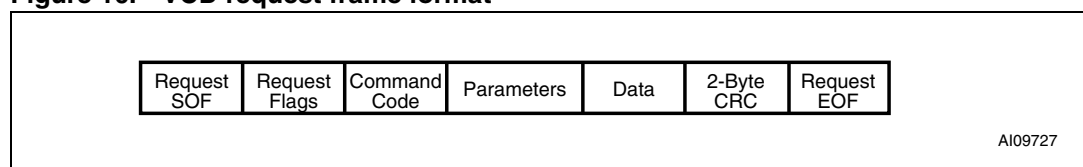


Figure 17. LRI64 response frame format

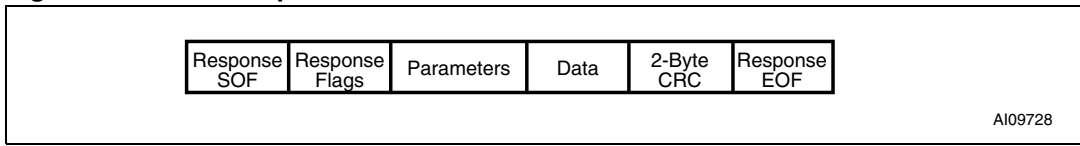
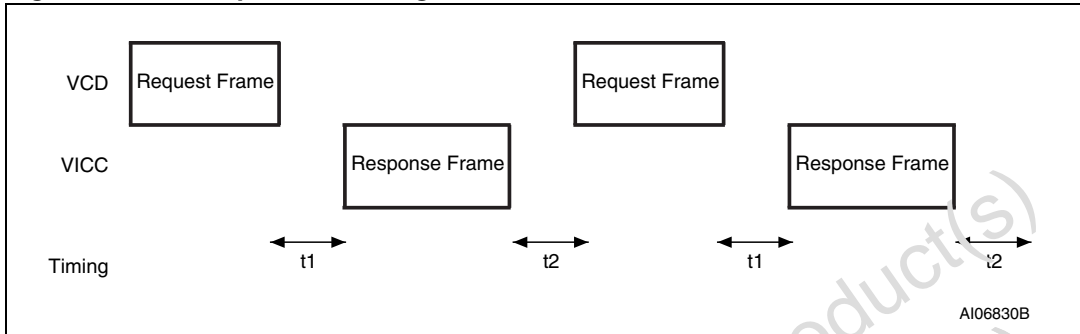


Figure 18. LRI64 protocol timing



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12 LRI64 states

A LRI64 can be in any one of three states:

- Power-off
- Ready
- Quiet

Transitions between these states are as specified in [Figure 19](#).

12.1 Power-off state

The LRI64 is in the Power-off state when it receives insufficient energy from the VCD.

12.2 Ready state

The LRI64 is in the Ready state when it receives enough energy from the VCD. It answers to any request in Addressed and Non-addressed modes.

12.3 Quiet state

When in the Quiet state, the LRI64 answers to any request in Addressed mode.

13 Modes

The term mode refers to the mechanism for specifying, in a request, the set of LRI64 devices that shall answer to the request.

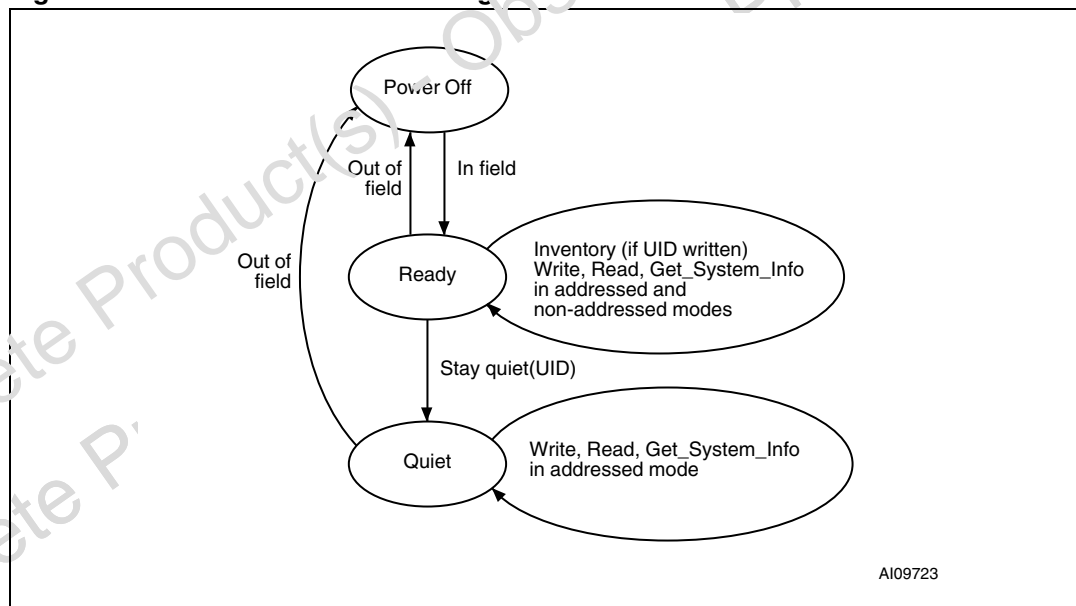
13.1 Addressed mode

When the Address_flag is set to 1 (Addressed mode), the request contains the unique ID (UID) of the addressed LRI64 device (such as an LRI64 device). Any LRI64 receiving a request in which the Address_flag is set to 1, compares the received Unique ID to its own UID. If it matches, it execute the request (if possible) and returns a response to the VCD, as specified by the command description. If it does not match, the LRI64 device remains silent.

13.2 Non-addressed mode (general request)

When the Address_flag is set to 0 (Non-addressed mode), the request does not contain a Unique ID field. Any LRI64 device receiving a request in which the Address_flag is set to 0, executes the request and returns a response to the VCD as specified by the command description.

Figure 19. LRI64 state transition diagram.



14 Flags and error codes

14.1 Request flags

In a request, the 8-bit flags field specifies the actions to be performed by the LRI64, and whether corresponding fields are present or not.

Flag bit 3 (the Inventory_flag) defines the way the four most significant flag bits (5 to 8) are used. When bit 3 is reset (0), bits 5 to 8 define the LRI64 selection criteria. When bit 3 is set (1), bits 5 to 8 define the LRI64 Inventory parameters.

Table 3. Request flags 1 to 4

Bit	Name	Value ⁽¹⁾	Description
1	Subcarrier flag	0	Single subcarrier frequency mode. (Option 1 is not supported)
2	Data_rate flag	1	High data rate mode. (Option 0 is not supported)
3	Inventory flag	0	Flags 5 to 8 meaning are according to Table 4
		1	Flags 5 to 8 meaning are according to Table 5
4	Protocol extension flag	0	No Protocol format extension. Must be set to 0. (Option 1 is not supported)

1. If the value of the request flag is a non authorized value, the LRI64 does not execute the command, and does not respond to the request.

Table 4. Request flags 5 to 8 (when bit 3 = 0)

Bit	Name	Value ⁽¹⁾	Description
5	Select flag	0	No selection mode. Must be set to 0. (Option 1 is not supported)
6	Address flag	0	Non addressed mode. The UID field is not present in the request. All LRI64 shall answer to the request.
		1	Addressed mode. The UID field is present in the request. Only the LRI64 that matches the UID answers the request.
7	Option flag ⁽¹⁾	0	No option. Must be set to 0. (Option 1 is not supported)
8	RFU ⁽¹⁾	0	No option. Must be set to 0. (Option 1 is not supported)

1. Only bit 6 (Address flag) can be configured for the LRI64. All others bits (5, 7 and 8) must be reset to 0.

Table 5. Request flags 5 to 8 (when bit 3 = 1)

Bit	Name	Value ⁽¹⁾	Description
5	AFI flag	0	AFI field is not present
		1	AFI field is present
6	Nb_slots flag	0	16 slots
		1	1 slot
7	Option flag	0	No option. Must be set to 0. (Option 1 is not supported)
8	RFU	0	No option. Must be set to 0. (Option 1 is not supported)

1. Bits 7 and 8 must be reset to 0.

14.2 Response flags

In a response, the 8-bit flags field indicates how actions have been performed by the LRI64, and whether corresponding fields are present or not.

Table 6. Response flags 1 to 8

Bit	Name	Value	Description
1	Error flag	0	No error
		1	Error detected. Error code is in the "Error" field.
2	RFU	0	
3	RFU	0	
4	RFU	0	
5	RFU	0	
6	RFU	0	
7	RFU	0	
8	RFU	0	

14.3 Response error code

If the Error flag is set by the LRI64 in the response, the error code field is present and provides information about the error that occurred. [Table 7](#) shows the one error code that is supported by the LRI64.

Table 7. Response error code

Error code	Meaning
0Fh	Error with no specific information given

15 Anticollision

The purpose of the anticollision sequence is to allow the VCD to compile a list of the LRI64 devices that are present in the VCD field, each one identified by its unique ID (UID).

The VCD is the master of the communication with one or multiple LRI64 devices. It initiates the communication by issuing the Inventory request ([Figure 22](#)).

15.1 Request flags

The Nb_slots_flag needs to be set appropriately. The AFI flag needs to be set, if the Optional AFI Field is to be present.

15.2 Mask length and mask value

The mask length defines the number of significant bits in the mask value.

The mask value is contained in an integer number of bytes.

The least significant bit of each is transmitted first.

If the mask length is not a multiple of 8 (bits), the most significant end of the mask value is padded with the required number of null bits (set to 0) so that the mask value is contained in an integer number of bytes, so that the next field (the 2-byte CRC) starts at the next byte boundary.

In the example of [Figure 20](#), the mask length is 11 bits. The mask value, 10011001111, is padded out at the most significant end with five bits set to 0. The 11-bit mask plus the current slot number is compared to the UID.

15.3 Inventory responses

Each LRI64 sends its response in a given time slot, or else remains silent.

The first slot starts immediately after the reception of the request EOF.

To switch to the next slot, the VCD sends another EOF.

The following rules and restrictions apply:

- if no LRI64 answer is detected, the VCD may switch to the next slot by sending an EOF
- if one or more LRI64 answers are detected, the VCD waits until the complete frame has been received before sending an EOF, to switch to the next slot.

The pulse shall be generated according to the definition of the EOF in ISO 15693 and ISO 18000-3 Mode 1 standards.