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LS1088A

QorIQ LS1088A Data Sheet

Features

- LS1088A contains eight ARM® Cortex®-A53 (32/64 bit) cores with the following capabilities:
  - Speed up to 1.6 GHz
  - Arranged as two clusters of four cores
  - 32 KB L1 instruction cache (ECC protection) and 32 KB L1 data cache (ECC protection)
  - Two 1 MB unified I/D L2 cache (ECC protection), one per Cortex-A53 core cluster
  - NEON™ SIMD coprocessor
  - ARMv8 cryptography extensions
- Hierarchical interconnect fabric:
  - Hardware-managed data coherency
  - Up to 700 MHz operation
- One 32/64-bit DDR4 SDRAM memory controller:
  - ECC and interleaving support
  - Up to 2.1 GT/s
- Datapath acceleration architecture 2.0 (DPAA2) incorporates acceleration for the following functions:
  - Packet parsing, classification, and distribution (WRIOP)
  - Queue management for scheduling, packet sequencing, and congestion management (QMan)
  - Hardware buffer management for buffer allocation and de-allocation (BMan)
  - Cryptography acceleration (SEC)
  - IEEE 1588 support
  - Advanced I/O processor (AIOP)
- Parallel Ethernet interfaces:
  - Up to two RGMII interfaces
- Eight SerDes lanes for high-speed peripheral interfaces:
  - Three PCI Express 3.0 controllers (one supporting x4 operation)
  - One serial ATA (SATA 3.0) controller supporting 6 Gbps
  - Up to two SGMII supporting 2500 Mbps
  - Up to four SGMII supporting 1000 Mbps
  - Up to two XFI (10 GbE) interfaces
  - Up to two QSGMII
  - Supports 1000Base-KX
  - Supports 10GBase-KR
- Additional peripheral interfaces include:
  - One quad serial peripheral interface (QSPI) controller, one serial peripheral interface (SPI) controller
  - Integrated flash controller (IFC) supporting NAND and NOR flash with 28-bit addressing and 16-bit data
  - Two USB 3.0 controllers with integrated PHY
  - Enhanced secure digital host controller supporting SD 3.0, eMMC 4.4, and eMMC 4.5 modes
  - uQE supporting TDM/HDLC
  - Four I2C controllers
  - Two 16550-compliant DUARTs
  - General purpose IO (GPIO), four FlexTimers, and nine watchdog timers
  - Trust architecture
  - Debug support with run control, data acquisition, high-speed trace, and performance/event monitoring
- 780 FC-PBGA package, 23 mm x 23 mm, 0.8 mm pitch

Table of Contents

1 Overview

A member of the Layerscape (LS1) series, the LS1088A is a cost-effective, power-efficient, and highly integrated system-on-chip (SoC) device featuring eight extremely power-efficient 64-bit ARM® Cortex®-A53 cores with ECC-protected L1 and L2 cache memories for high reliability, running up to 1.6 GHz.

The LS1088A family of devices can be used for enterprise and service provider routers, Virtual CPE, industrial communications, security appliance and military and aerospace applications.

This figure shows the LS1088A block diagram.

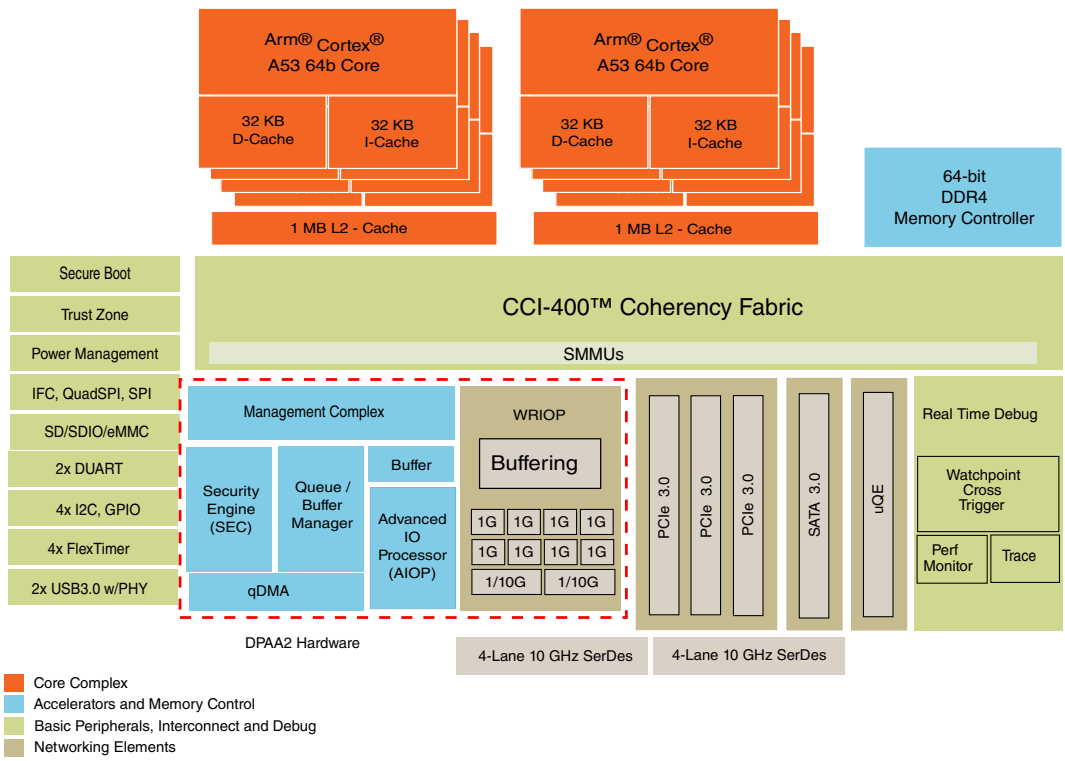

Figure 1. LS1088A block diagram

2 Pin assignments

NOTE: Information given in this section is preliminary and is subject to change.

2.1 780 BGA ball layout diagrams

This figure shows the complete view of the LS1088A BGA ball map diagram. Figure 3, Figure 4, Figure 5, and Figure 6 show quadrant views.

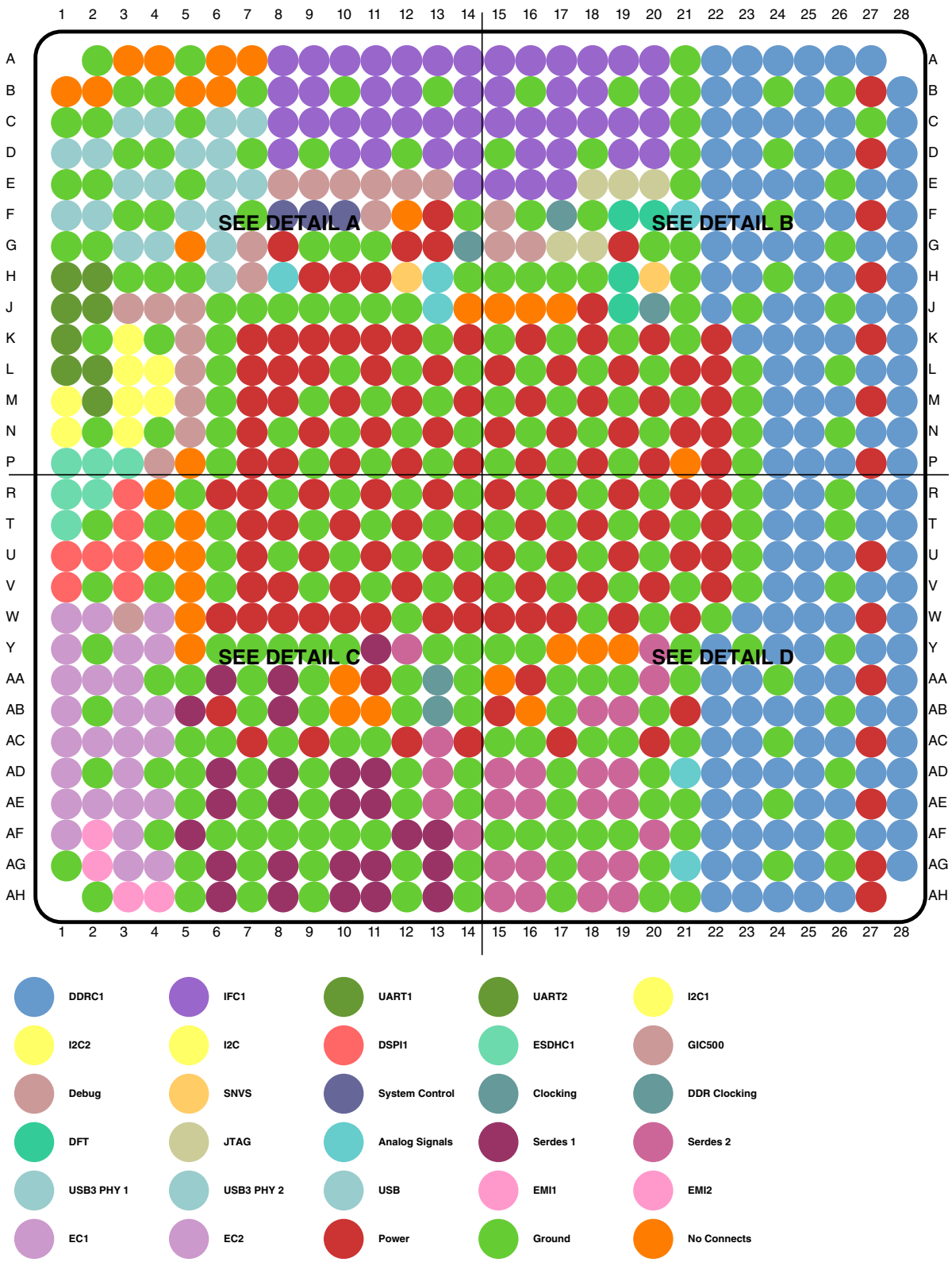

Figure 2. Complete BGA Map for the LS1088A

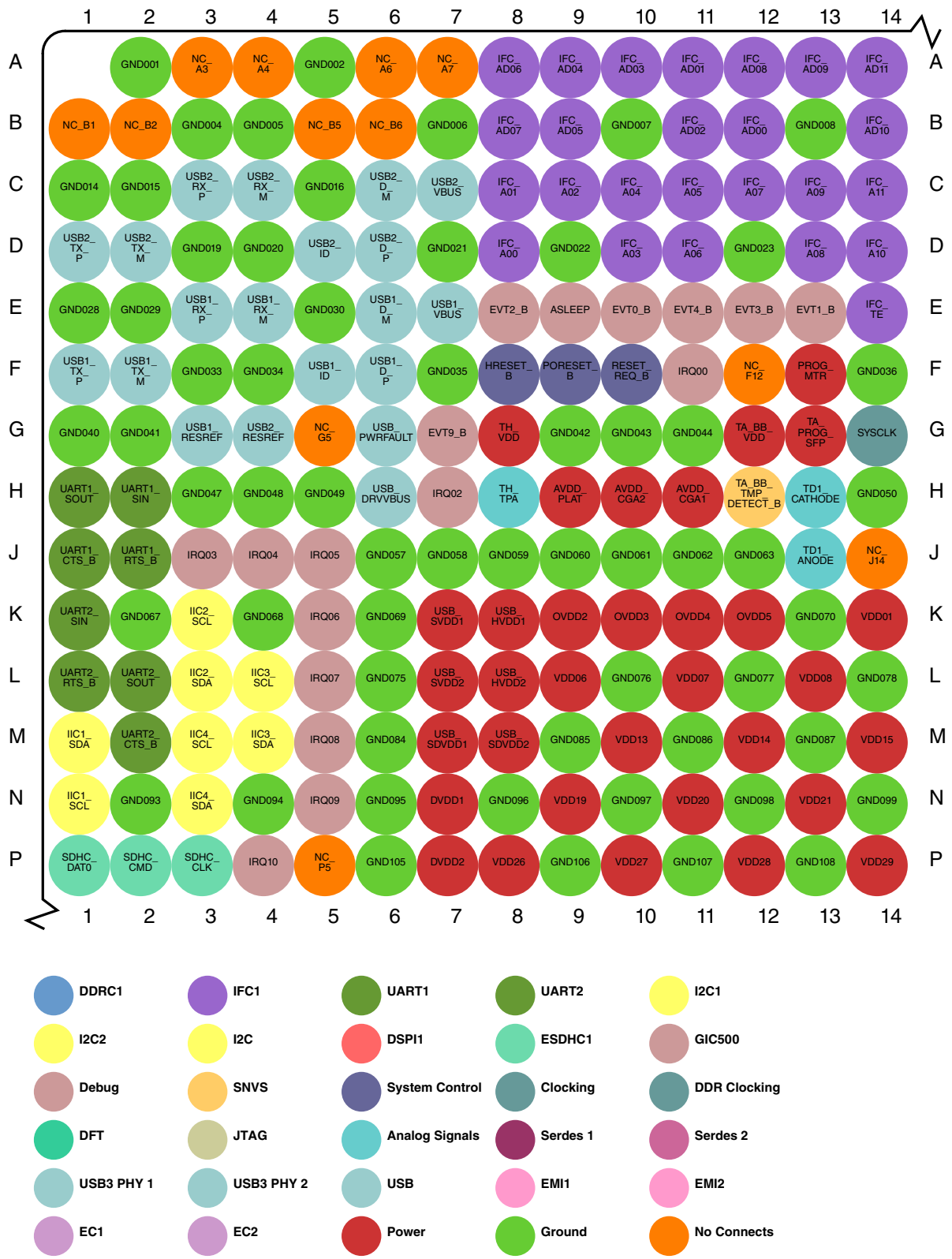

Figure 3. Detail A

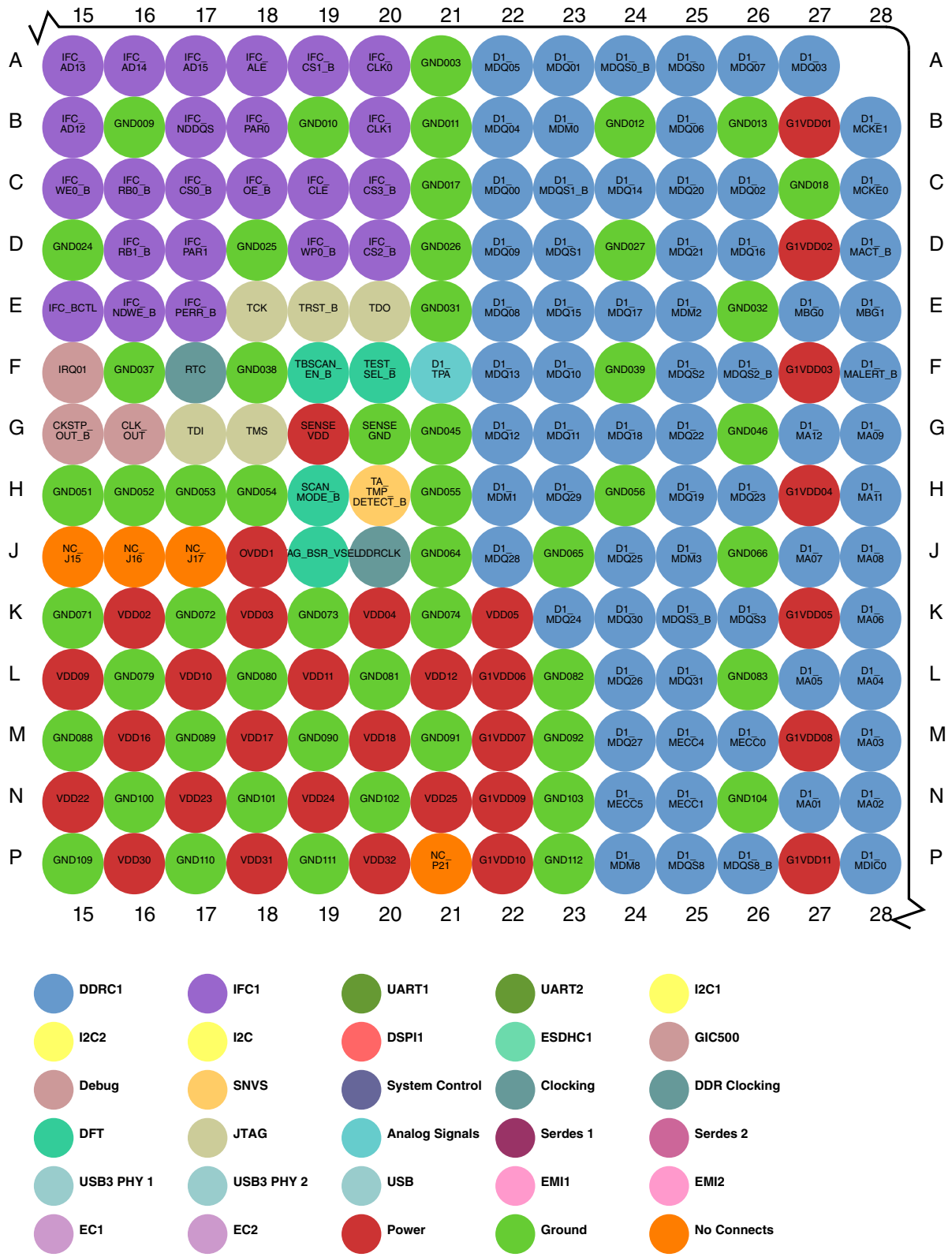

Figure 4. Detail B

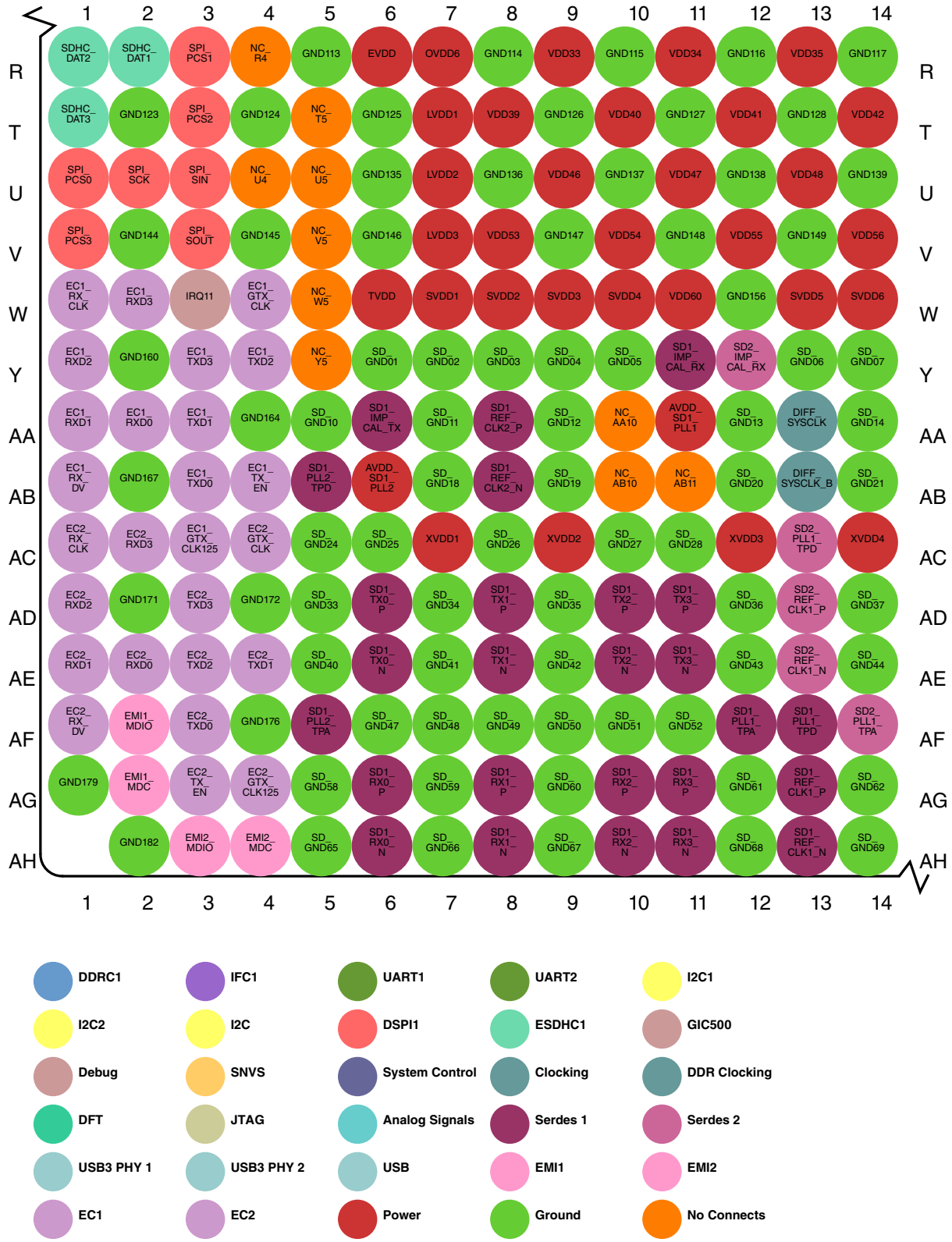

Figure 5. Detail C

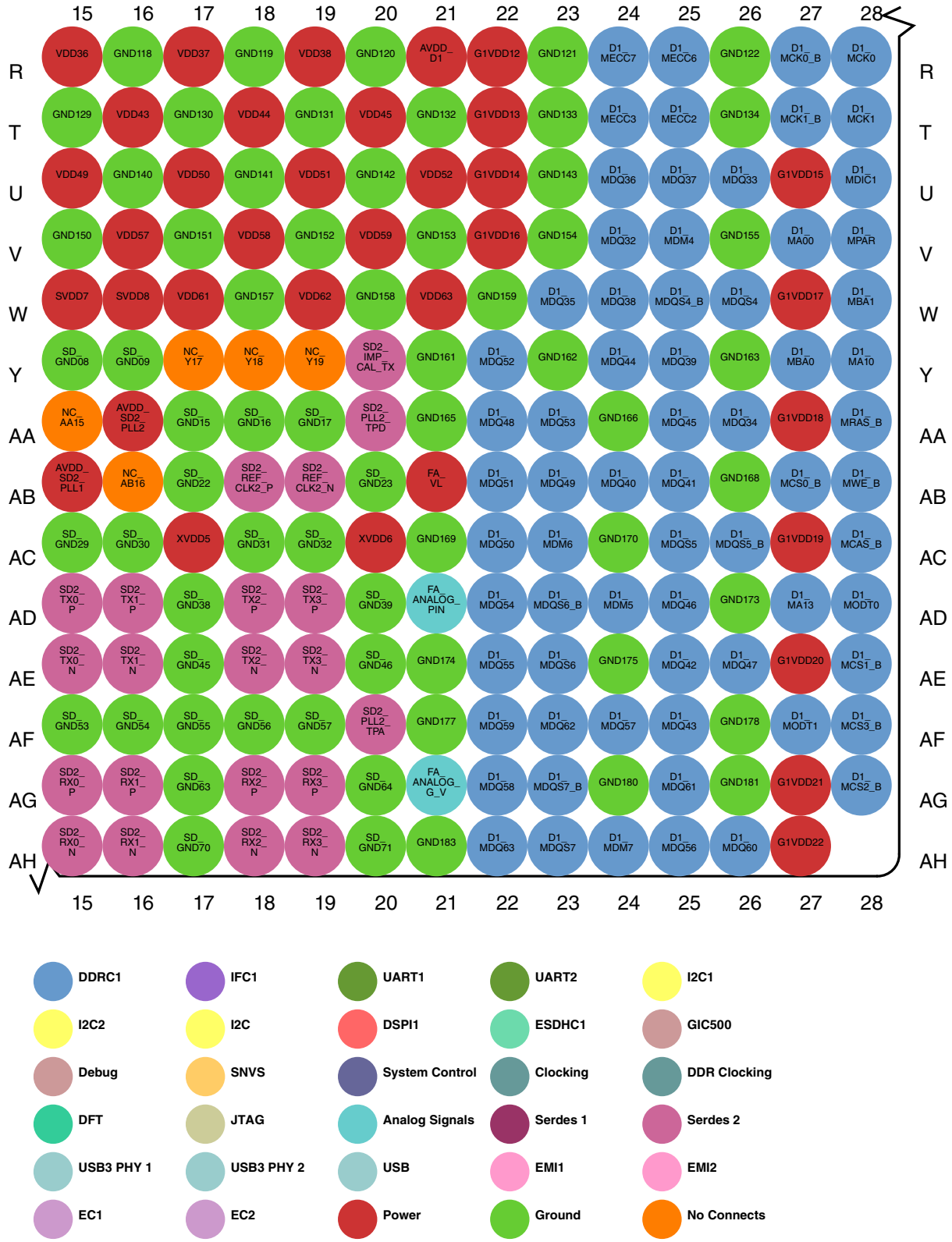

Figure 6. Detail D

2.2 Pinout list

This table provides the pinout listing for the LS1088A by bus. Primary functions are **bolded** in the table.

Table 1. Pinout list by bus

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
DDR SDRAM Memory Interface 1					
D1_MA00	Address	V27	O	$G1V_{DD}$	1
D1_MA01	Address	N27	O	$G1V_{DD}$	1
D1_MA02	Address	N28	O	$G1V_{DD}$	1
D1_MA03	Address	M28	O	$G1V_{DD}$	1
D1_MA04	Address	L28	O	$G1V_{DD}$	1
D1_MA05	Address	L27	O	$G1V_{DD}$	1
D1_MA06	Address	K28	O	$G1V_{DD}$	1
D1_MA07	Address	J27	O	$G1V_{DD}$	1
D1_MA08	Address	J28	O	$G1V_{DD}$	1
D1_MA09	Address	G28	O	$G1V_{DD}$	1
D1_MA10	Address	Y28	O	$G1V_{DD}$	1
D1_MA11	Address	H28	O	$G1V_{DD}$	1
D1_MA12	Address	G27	O	$G1V_{DD}$	1
D1_MA13	Address	AD27	O	$G1V_{DD}$	1
D1_MACT_B	Activate	D28	O	$G1V_{DD}$	1
D1_MALERT_B	Alert	F28	I	$G1V_{DD}$	1, 6
D1_MBA0	Bank Select	Y27	O	$G1V_{DD}$	1
D1_MBA1	Bank Select	W28	O	$G1V_{DD}$	1
D1_MBG0	Bank Group	E27	O	$G1V_{DD}$	1
D1_MBG1	Bank Group	E28	O	$G1V_{DD}$	1
D1_MCAS_B	Column Address Strobe / MA[15]	AC28	O	$G1V_{DD}$	1
D1_MCK0	Clock	R28	O	$G1V_{DD}$	---
D1_MCK0_B	Clock Complement	R27	O	$G1V_{DD}$	---
D1_MCK1	Clock	T28	O	$G1V_{DD}$	---
D1_MCK1_B	Clock Complement	T27	O	$G1V_{DD}$	---
D1_MCKE0	Clock Enable	C28	O	$G1V_{DD}$	1
D1_MCKE1	Clock Enable	B28	O	$G1V_{DD}$	1
D1_MCS0_B	Chip Select	AB27	O	$G1V_{DD}$	1
D1_MCS1_B	Chip Select	AE28	O	$G1V_{DD}$	1
D1_MCS2_B	Chip Select	AG28	O	$G1V_{DD}$	1

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
D1_MCS3_B	Chip Select	AF28	O	$G1V_{DD}$	1
D1_MDIC0	Driver Impedence Calibration	P28	IO	$G1V_{DD}$	3
D1_MDIC1	Driver Impedence Calibration	U28	IO	$G1V_{DD}$	3
D1_MDM0	Data Mask	B23	O	$G1V_{DD}$	---
D1_MDM1	Data Mask	H22	O	$G1V_{DD}$	---
D1_MDM2	Data Mask	E25	O	$G1V_{DD}$	---
D1_MDM3	Data Mask	J25	O	$G1V_{DD}$	---
D1_MDM4	Data Mask	V25	O	$G1V_{DD}$	---
D1_MDM5	Data Mask	AD24	O	$G1V_{DD}$	---
D1_MDM6	Data Mask	AC23	O	$G1V_{DD}$	---
D1_MDM7	Data Mask	AH24	O	$G1V_{DD}$	---
D1_MDM8	Data Mask	P24	O	$G1V_{DD}$	---
D1_MDQ00	Data	C22	IO	$G1V_{DD}$	---
D1_MDQ01	Data	A23	IO	$G1V_{DD}$	---
D1_MDQ02	Data	C26	IO	$G1V_{DD}$	---
D1_MDQ03	Data	A27	IO	$G1V_{DD}$	---
D1_MDQ04	Data	B22	IO	$G1V_{DD}$	---
D1_MDQ05	Data	A22	IO	$G1V_{DD}$	---
D1_MDQ06	Data	B25	IO	$G1V_{DD}$	---
D1_MDQ07	Data	A26	IO	$G1V_{DD}$	---
D1_MDQ08	Data	E22	IO	$G1V_{DD}$	---
D1_MDQ09	Data	D22	IO	$G1V_{DD}$	---
D1_MDQ10	Data	F23	IO	$G1V_{DD}$	---
D1_MDQ11	Data	G23	IO	$G1V_{DD}$	---
D1_MDQ12	Data	G22	IO	$G1V_{DD}$	---
D1_MDQ13	Data	F22	IO	$G1V_{DD}$	---
D1_MDQ14	Data	C24	IO	$G1V_{DD}$	---
D1_MDQ15	Data	E23	IO	$G1V_{DD}$	---
D1_MDQ16	Data	D26	IO	$G1V_{DD}$	---
D1_MDQ17	Data	E24	IO	$G1V_{DD}$	---
D1_MDQ18	Data	G24	IO	$G1V_{DD}$	---
D1_MDQ19	Data	H25	IO	$G1V_{DD}$	---
D1_MDQ20	Data	C25	IO	$G1V_{DD}$	---
D1_MDQ21	Data	D25	IO	$G1V_{DD}$	---
D1_MDQ22	Data	G25	IO	$G1V_{DD}$	---
D1_MDQ23	Data	H26	IO	$G1V_{DD}$	---
D1_MDQ24	Data	K23	IO	$G1V_{DD}$	---
D1_MDQ25	Data	J24	IO	$G1V_{DD}$	---

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
D1_MDQ26	Data	L24	IO	$G1V_{DD}$	---
D1_MDQ27	Data	M24	IO	$G1V_{DD}$	---
D1_MDQ28	Data	J22	IO	$G1V_{DD}$	---
D1_MDQ29	Data	H23	IO	$G1V_{DD}$	---
D1_MDQ30	Data	K24	IO	$G1V_{DD}$	---
D1_MDQ31	Data	L25	IO	$G1V_{DD}$	---
D1_MDQ32	Data	V24	IO	$G1V_{DD}$	---
D1_MDQ33	Data	U26	IO	$G1V_{DD}$	---
D1_MDQ34	Data	AA26	IO	$G1V_{DD}$	---
D1_MDQ35	Data	W23	IO	$G1V_{DD}$	---
D1_MDQ36	Data	U24	IO	$G1V_{DD}$	---
D1_MDQ37	Data	U25	IO	$G1V_{DD}$	---
D1_MDQ38	Data	W24	IO	$G1V_{DD}$	---
D1_MDQ39	Data	Y25	IO	$G1V_{DD}$	---
D1_MDQ40	Data	AB24	IO	$G1V_{DD}$	---
D1_MDQ41	Data	AB25	IO	$G1V_{DD}$	---
D1_MDQ42	Data	AE25	IO	$G1V_{DD}$	---
D1_MDQ43	Data	AF25	IO	$G1V_{DD}$	---
D1_MDQ44	Data	Y24	IO	$G1V_{DD}$	---
D1_MDQ45	Data	AA25	IO	$G1V_{DD}$	---
D1_MDQ46	Data	AD25	IO	$G1V_{DD}$	---
D1_MDQ47	Data	AE26	IO	$G1V_{DD}$	---
D1_MDQ48	Data	AA22	IO	$G1V_{DD}$	---
D1_MDQ49	Data	AB23	IO	$G1V_{DD}$	---
D1_MDQ50	Data	AC22	IO	$G1V_{DD}$	---
D1_MDQ51	Data	AB22	IO	$G1V_{DD}$	---
D1_MDQ52	Data	Y22	IO	$G1V_{DD}$	---
D1_MDQ53	Data	AA23	IO	$G1V_{DD}$	---
D1_MDQ54	Data	AD22	IO	$G1V_{DD}$	---
D1_MDQ55	Data	AE22	IO	$G1V_{DD}$	---
D1_MDQ56	Data	AH25	IO	$G1V_{DD}$	---
D1_MDQ57	Data	AF24	IO	$G1V_{DD}$	---
D1_MDQ58	Data	AG22	IO	$G1V_{DD}$	---
D1_MDQ59	Data	AF22	IO	$G1V_{DD}$	---
D1_MDQ60	Data	AH26	IO	$G1V_{DD}$	---
D1_MDQ61	Data	AG25	IO	$G1V_{DD}$	---
D1_MDQ62	Data	AF23	IO	$G1V_{DD}$	---
D1_MDQ63	Data	AH22	IO	$G1V_{DD}$	---

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
D1_MDQS0	Data Strobe	A25	IO	$G1V_{DD}$	---
D1_MDQS0_B	Data Strobe	A24	IO	$G1V_{DD}$	---
D1_MDQS1	Data Strobe	D23	IO	$G1V_{DD}$	---
D1_MDQS1_B	Data Strobe	C23	IO	$G1V_{DD}$	---
D1_MDQS2	Data Strobe	F25	IO	$G1V_{DD}$	---
D1_MDQS2_B	Data Strobe	F26	IO	$G1V_{DD}$	---
D1_MDQS3	Data Strobe	K26	IO	$G1V_{DD}$	---
D1_MDQS3_B	Data Strobe	K25	IO	$G1V_{DD}$	---
D1_MDQS4	Data Strobe	W26	IO	$G1V_{DD}$	---
D1_MDQS4_B	Data Strobe	W25	IO	$G1V_{DD}$	---
D1_MDQS5	Data Strobe	AC25	IO	$G1V_{DD}$	---
D1_MDQS5_B	Data Strobe	AC26	IO	$G1V_{DD}$	---
D1_MDQS6	Data Strobe	AE23	IO	$G1V_{DD}$	---
D1_MDQS6_B	Data Strobe	AD23	IO	$G1V_{DD}$	---
D1_MDQS7	Data Strobe	AH23	IO	$G1V_{DD}$	---
D1_MDQS7_B	Data Strobe	AG23	IO	$G1V_{DD}$	---
D1_MDQS8	Data Strobe	P25	IO	$G1V_{DD}$	---
D1_MDQS8_B	Data Strobe	P26	IO	$G1V_{DD}$	---
D1_MECC0	Error Correcting Code	M26	IO	$G1V_{DD}$	---
D1_MECC1	Error Correcting Code	N25	IO	$G1V_{DD}$	---
D1_MECC2	Error Correcting Code	T25	IO	$G1V_{DD}$	---
D1_MECC3	Error Correcting Code	T24	IO	$G1V_{DD}$	---
D1_MECC4	Error Correcting Code	M25	IO	$G1V_{DD}$	---
D1_MECC5	Error Correcting Code	N24	IO	$G1V_{DD}$	---
D1_MECC6	Error Correcting Code	R25	IO	$G1V_{DD}$	---
D1_MECC7	Error Correcting Code	R24	IO	$G1V_{DD}$	---
D1_MODT0	On Die Termination	AD28	O	$G1V_{DD}$	1
D1_MODT1	On Die Termination	AF27	O	$G1V_{DD}$	1
D1_MPAR	Address Parity Out	V28	O	$G1V_{DD}$	1
D1_MRAS_B	Row Address Strobe / MA[16]	AA28	O	$G1V_{DD}$	1
D1_MWE_B	Write Enable / MA[14]	AB28	O	$G1V_{DD}$	1
Integrated Flash Controller					
IFC_A00/GPIO1_16/ QSPI_A_CS0	IFC Address	D8	O	OV_{DD}	1, 5
IFC_A01/GPIO1_17/ QSPI_A_CS1	IFC Address	C8	O	OV_{DD}	1, 5
IFC_A02/GPIO1_18/ QSPI_A_SCK	IFC Address	C9	O	OV_{DD}	1, 5

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
IFC_A03/GPIO1_19/ QSPI_B_CS0	IFC Address	D10	O	OV_{DD}	1, 5
IFC_A04/GPIO1_20/ QSPI_B_CS1	IFC Address	C10	O	OV_{DD}	1, 5
IFC_A05/GPIO1_21/ QSPI_B_SCK/cfg_dram_type	IFC Address	C11	O	OV_{DD}	1, 4
IFC_A06/GPIO2_00/ IFC_WP1_B/QSPI_A_DATA0	IFC Address	D11	O	OV_{DD}	1
IFC_A07/GPIO2_01/ IFC_WP2_B/QSPI_A_DATA1	IFC Address	C12	O	OV_{DD}	1
IFC_A08/GPIO2_02/ IFC_WP3_B/QSPI_A_DATA2	IFC Address	D13	O	OV_{DD}	1
IFC_A09/GPIO2_03/ IFC_RB2_B/IFC_CS_B4/ QSPI_A_DATA3	IFC Address	C13	O	OV_{DD}	1
IFC_A10/GPIO2_04/ IFC_RB3_B/IFC_CS_B5/ QSPI_A_DQS	IFC Address	D14	O	OV_{DD}	1
IFC_A11/GPIO2_05/ IFC_CS_B6/QSPI_B_DQS	IFC Address	C14	O	OV_{DD}	1
IFC_AD00/GPIO1_00/ cfg_gpinput0	IFC Address / Data	B12	IO	OV_{DD}	4, 9
IFC_AD01/GPIO1_01/ cfg_gpinput1	IFC Address / Data	A11	IO	OV_{DD}	4, 9
IFC_AD02/GPIO1_02/ cfg_gpinput2	IFC Address / Data	B11	IO	OV_{DD}	4, 9
IFC_AD03/GPIO1_03/ cfg_gpinput3	IFC Address / Data	A10	IO	OV_{DD}	4, 9
IFC_AD04/GPIO1_04/ cfg_gpinput4	IFC Address / Data	A9	IO	OV_{DD}	4, 9
IFC_AD05/GPIO1_05/ cfg_gpinput5	IFC Address / Data	B9	IO	OV_{DD}	4, 9
IFC_AD06/GPIO1_06/ cfg_gpinput6	IFC Address / Data	A8	IO	OV_{DD}	4, 9
IFC_AD07/GPIO1_07/ cfg_gpinput7	IFC Address / Data	B8	IO	OV_{DD}	4, 9
IFC_AD08/GPIO1_08/ cfg_rcw_src1	IFC Address / Data	A12	IO	OV_{DD}	4, 9
IFC_AD09/GPIO1_09/ cfg_rcw_src2	IFC Address / Data	A13	IO	OV_{DD}	4, 9
IFC_AD10/GPIO1_10/ cfg_rcw_src3	IFC Address / Data	B14	IO	OV_{DD}	4, 9
IFC_AD11/GPIO1_11/ cfg_rcw_src4	IFC Address / Data	A14	IO	OV_{DD}	4, 9

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
IFC_AD12/GPIO1_12/ cfg_rcw_src5	IFC Address / Data	B15	IO	OV_{DD}	4, 9
IFC_AD13/GPIO1_13/ cfg_rcw_src6	IFC Address / Data	A15	IO	OV_{DD}	4, 9
IFC_AD14/GPIO1_14/ cfg_rcw_src7	IFC Address / Data	A16	IO	OV_{DD}	4, 9
IFC_AD15/GPIO1_15/ cfg_rcw_src8	IFC Address / Data	A17	IO	OV_{DD}	4, 9
IFC_ALE/GPIO1_24	IFC Address Latch Enable	A18	O	OV_{DD}	1, 5
IFC_BCTL/GPIO2_12	IFC Buffer control	E15	O	OV_{DD}	1
IFC_CLE/GPIO1_25/ cfg_rcw_src0	IFC NAND Command Latch Enable / Write Enable 1 / NOR Address active-low Valid	C19	O	OV_{DD}	1, 4
IFC_CLK0/GPIO2_17	IFC Clock	A20	O	OV_{DD}	1
IFC_CLK1/GPIO2_18	IFC Clock	B20	O	OV_{DD}	1
IFC_CS0_B/GPIO2_08	IFC Chip Select	C17	O	OV_{DD}	1, 6
IFC_CS1_B/GPIO2_09	IFC Chip Select	A19	O	OV_{DD}	1, 6
IFC_CS2_B/GPIO2_10	IFC Chip Select	D20	O	OV_{DD}	1, 6
IFC_CS3_B/GPIO2_11/ QSPI_B_DATA3/ QSPI_A_DATA7	IFC Chip Select	C20	O	OV_{DD}	1, 6
IFC_CS_B4/**IFC_A09**/ GPIO2_03/IFC_RB2_B/ QSPI_A_DATA3	IFC Chip Select	C13	O	OV_{DD}	1
IFC_CS_B5/**IFC_A10**/ GPIO2_04/IFC_RB3_B/ QSPI_A_DQS	IFC Chip Select	D14	O	OV_{DD}	1
IFC_CS_B6/**IFC_A11**/ GPIO2_05/QSPI_B_DQS	IFC Chip Select	C14	O	OV_{DD}	1
IFC_NDDQS/GPIO2_13	IFC DQS Strobe	B17	IO	OV_{DD}	9
IFC_NDWE_B/GPIO2_19	IFC NAND Write Enable / NAND DDR Clock	E16	O	OV_{DD}	1
IFC_OE_B/GPIO1_26/ cfg_eng_use1	IFC Output Enable	C18	O	OV_{DD}	1, 5
IFC_PAR0/GPIO2_06/ QSPI_B_DATA0/ QSPI_A_DATA4	IFC Address & Data Parity	B18	IO	OV_{DD}	9
IFC_PAR1/GPIO2_07/ QSPI_B_DATA1/ QSPI_A_DATA5	IFC Address & Data Parity	D17	IO	OV_{DD}	9
IFC_PERR_B/GPIO2_16/ QSPI_B_DATA2/ QSPI_A_DATA6	IFC Parity Error	E17	I	OV_{DD}	1
IFC_RB0_B/GPIO2_14	IFC Ready/Busy CS0	C16	I	OV_{DD}	1, 6

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
IFC_RB1_B/GPIO2_15	IFC Ready/Busy CS1	D16	I	OV_{DD}	1, 6
IFC_RB2_B/**IFC_A09**/ GPIO2_03/IFC_CS_B4/ QSPI_A_DATA3	IFC Ready/Busy CS 2	C13	I	OV_{DD}	1
IFC_RB3_B/**IFC_A10**/ GPIO2_04/IFC_CS_B5/ QSPI_A_DQS	IFC Ready/Busy CS 3	D14	I	OV_{DD}	1
IFC_TE/GPIO1_23/cfg_ifc_te	IFC External Transceiver Enable	E14	O	OV_{DD}	1, 4
IFC_WE0_B/GPIO1_22/ cfg_eng_use0	IFC Write Enable 0 / Start of Frame	C15	O	OV_{DD}	1, 4, 19
IFC_WP0_B/GPIO1_27/ cfg_eng_use2	IFC Write Protect	D19	O	OV_{DD}	1, 5
IFC_WP1_B/**IFC_A06**/ GPIO2_00/QSPI_A_DATA0	IFC Write Protect	D11	O	OV_{DD}	1
IFC_WP2_B/**IFC_A07**/ GPIO2_01/QSPI_A_DATA1	IFC Write Protect	C12	O	OV_{DD}	1
IFC_WP3_B/**IFC_A08**/ GPIO2_02/QSPI_A_DATA2	IFC Write Protect	D13	O	OV_{DD}	1
DUART1					
UART1_CTS_B/GPIO3_10/ UART3_SIN	Clear To Send	J1	I	DV_{DD}	1
UART1_RTS_B/GPIO3_08/ UART3_SOUT	Ready to Send	J2	O	DV_{DD}	1
UART1_SIN	Receive Data	H2	I	DV_{DD}	1
UART1_SOUT	Transmit Data	H1	O	DV_{DD}	1
DUART2					
UART2_CTS_B/GPIO3_11/ UART4_SIN	Clear To Send	M2	I	DV_{DD}	1
UART2_RTS_B/GPIO3_09/ UART4_SOUT	Ready to Send	L1	O	DV_{DD}	1
UART2_SIN/GPIO3_07	Receive Data	K1	I	DV_{DD}	1
UART2_SOUT/GPIO3_06	Transmit Data	L2	O	DV_{DD}	1
DUART3 and 4					
UART3_SIN/**UART1_CTS_B**/ GPIO3_10	Receive Data	J1	I	DV_{DD}	1
UART3_SOUT/ **UART1_RTS_B**/GPIO3_08	Transmit Data	J2	O	DV_{DD}	1
UART4_SIN/**UART2_CTS_B**/ GPIO3_11	Receive Data	M2	I	DV_{DD}	1
UART4_SOUT/ **UART2_RTS_B**/GPIO3_09	Transmit Data	L1	O	DV_{DD}	1
I2C1					

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
IIC1_SCL	Serial Clock	N1	IO	DV_{DD}	7, 8
IIC1_SDA	Serial Data	M1	IO	DV_{DD}	7, 8
I2C2					
IIC2_SCL/GPIO3_12/ SDHC_CD_B/CLK9/BRGO2	Serial Clock	K3	IO	DV_{DD}	7, 8
IIC2_SDA/GPIO3_13/ SDHC_WP/CLK10/BRGO3	Serial Data	L3	IO	DV_{DD}	7, 8
I2C3 and 4					
IIC3_SCL/GPIO4_28/EVT5_B/ USB2_DRVVBUS/BRGO4/ CLK11	Serial Clock	L4	IO	DV_{DD}	7, 8
IIC3_SDA/GPIO4_29/EVT6_B/ USB2_PWRFAULT/BRGO1/ CLK12_CLK8	Serial Data	M4	IO	DV_{DD}	7, 8
IIC4_SCL/GPIO4_30/EVT7_B/ TDMA_RQ/UC1_CDB_RXER	Serial Clock	M3	IO	DV_{DD}	7, 8
IIC4_SDA/GPIO4_31/EVT8_B/ TDMB_RQ/UC3_CDB_RXER	Serial Data	N3	IO	DV_{DD}	7, 8
SPI Interface					
SPI_PCS0/GPIO3_17/ SDHC_DAT4/SDHC_VS	SPI Chip Select	U1	IO	OV_{DD}	---
SPI_PCS1/GPIO3_18/ SDHC_DAT5/ SDHC_CMD_DIR	SPI Chip Select	R3	O	OV_{DD}	1
SPI_PCS2/GPIO3_19/ SDHC_DAT6/ SDHC_DAT0_DIR	SPI Chip Select	T3	O	OV_{DD}	1
SPI_PCS3/GPIO3_20/ SDHC_DAT7/ SDHC_DAT123_DIR	SPI Chip Select	V1	O	OV_{DD}	1
SPI_SCK/GPIO3_16/ SDHC_GATE_IN	SPI Clock	U2	IO	OV_{DD}	---
SPI_SIN/GPIO3_15/ SDHC_CLK_SYNC_IN	Master In Slave Out	U3	I	OV_{DD}	1
SPI_SOUT/GPIO3_14/ SDHC_CLK_SYNC_OUT	Master Out Slave In	V3	O	OV_{DD}	1
eSDHC					
SDHC_CD_B/**IIC2_SCL**/ GPIO3_12/CLK9/BRGO2	Command	K3	I	DV_{DD}	1
SDHC_CLK/GPIO3_26	Host to Card Clock	P3	O	EV_{DD}	1
SDHC_CLK_SYNC_IN/ **SPI_SIN**/GPIO3_15	IN	U3	I	OV_{DD}	1
SDHC_CLK_SYNC_OUT/ **SPI_SOUT**/GPIO3_14	OUT	V3	O	OV_{DD}	1

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
SDHC_CMD/GPIO3_21	Command/Response	P2	IO	EV_{DD}	6
SDHC_CMD_DIR/**SPI_PCS1**/ GPIO3_18/SDHC_DAT5	DIR	R3	O	OV_{DD}	1
SDHC_DAT0/GPIO3_22	Data	P1	IO	EV_{DD}	6
SDHC_DAT0_DIR/**SPI_PCS2**/ GPIO3_19/SDHC_DAT6	DIR	T3	O	OV_{DD}	1
SDHC_DAT1/GPIO3_23	Data	R2	IO	EV_{DD}	6
SDHC_DAT123_DIR/ **SPI_PCS3**/GPIO3_20/ SDHC_DAT7	DIR	V1	O	OV_{DD}	1
SDHC_DAT2/GPIO3_24	Data	R1	IO	EV_{DD}	6
SDHC_DAT3/GPIO3_25	Data	T1	IO	EV_{DD}	6
SDHC_DAT4/**SPI_PCS0**/ GPIO3_17/SDHC_VS	Data	U1	IO	OV_{DD}	---
SDHC_DAT5/**SPI_PCS1**/ GPIO3_18/SDHC_CMD_DIR	Data	R3	IO	OV_{DD}	---
SDHC_DAT6/**SPI_PCS2**/ GPIO3_19/SDHC_DAT0_DIR	Data	T3	IO	OV_{DD}	---
SDHC_DAT7/**SPI_PCS3**/ GPIO3_20/ SDHC_DAT123_DIR	Data	V1	IO	OV_{DD}	---
SDHC_GATE_IN/**SPI_SCK**/ GPIO3_16	IN	U2	I	OV_{DD}	1
SDHC_VS/**SPI_PCS0**/ GPIO3_17/SDHC_DAT4	VS	U1	O	OV_{DD}	1
SDHC_WP/**IIC2_SDA**/ GPIO3_13/CLK10/BRGO3	Write Protect	L3	I	DV_{DD}	1
Interrupt Controller					
EVT9_B/GPIO4_10	Interrupt Output	G7	IO	OV_{DD}	7, 9
IRQ00	External Interrupt	F11	I	OV_{DD}	1
IRQ01	External Interrupt	F15	I	OV_{DD}	1
IRQ02	External Interrupt	H7	I	OV_{DD}	1
IRQ03/GPIO3_27/ TDMB_TSYNC/ UC3_RTSB_TXEN	External Interrupt	J3	I	DV_{DD}	1
IRQ04/GPIO3_28/ TDMA_RXD/UC1_RXD7/ TDMA_TXD	External Interrupt	J4	I	DV_{DD}	1
IRQ05/GPIO3_29/ TDMA_RSYNC/ UC1_CTSB_RXDV	External Interrupt	J5	I	DV_{DD}	1
IRQ06/GPIO4_04/ TDMA_RXD_EXC/ TDMA_TXD/UC1_TXD7	External Interrupt	K5	I	DV_{DD}	1

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
IRQ07/GPIO4_05/ TDMA_TSYNC/ UC1_RTSB_TXEN	External Interrupt	L5	I	DV_{DD}	1
IRQ08/GPIO4_06/ TDMB_RXD/UC3_RXD7/ TDMB_TXD	External Interrupt	M5	I	DV_{DD}	1
IRQ09/GPIO4_07/ TDMB_RSYNC/ UC3_CTSB_RXDV	External Interrupt	N5	I	DV_{DD}	1
IRQ10/GPIO4_08/ TDMB_RXD_EXC/ TDMB_TXD/UC3_TXD7	External Interrupt	P4	I	DV_{DD}	1
IRQ11/GPIO4_09	External Interrupt	W3	I	LV_{DD}	1
Debug					
ASLEEP/GPIO1_28/ cfg_soc_use	Asleep	E9	O	OV_{DD}	1, 4
CKSTP_OUT_B	Checkstop Out	G15	O	OV_{DD}	1, 6, 7
CLK_OUT	Clock Out	G16	O	OV_{DD}	2
EVT0_B	Event 0	E10	IO	OV_{DD}	9
EVT1_B	Event 1	E13	IO	OV_{DD}	9
EVT2_B	Event 2	E8	IO	OV_{DD}	9
EVT3_B	Event 3	E12	IO	OV_{DD}	9
EVT4_B	Event 4	E11	IO	OV_{DD}	9
EVT5_B/**IIC3_SCL**/GPIO4_28/ USB2_DRVVBUS/BRGO4/ CLK11	Event 5	L4	IO	DV_{DD}	---
EVT6_B/**IIC3_SDA**/GPIO4_29/ USB2_PWRFAULT/BRGO1/ CLK12_CLK8	Event 6	M4	IO	DV_{DD}	---
EVT7_B/**IIC4_SCL**/GPIO4_30/ TDMA_RQ/UC1_CDB_RXER	Event 7	M3	IO	DV_{DD}	---
EVT8_B/**IIC4_SDA**/GPIO4_31/ TDMB_RQ/UC3_CDB_RXER	Event 8	N3	IO	DV_{DD}	---
Trust					
TA_BB_TMP_DETECT_B	Battery Backed Tamper Detect	H12	I	$TA\_BB\_V_{DD}$	---
TA_TMP_DETECT_B	Tamper Detect	H20	I	OV_{DD}	---
System Control					
HRESET_B	Hard Reset	F8	IO	OV_{DD}	6, 7
PORESET_B	Power On Reset	F9	I	OV_{DD}	---
RESET_REQ_B	Reset Request (POR or Hard)	F10	O	OV_{DD}	1, 5
Clocking					
DIFF_SYSCLK	Single Source System Clock Differential (positive)	AA13	I	SV_{DD}	20

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
DIFF_SYSCLK_B	Single Source System Clock Differential (negative)	AB13	I	SV_{DD}	20
RTC/GPIO3_30	Real Time Clock	F17	I	OV_{DD}	1
SYSCLK	System Clock	G14	I	OV_{DD}	---
DDR Clocking					
DDRCLK	DDR Controller Clock	J20	I	OV_{DD}	---
DFT					
JTAG_BSR_VSEL	Reserved	J19	I	OV_{DD}	15
SCAN_MODE_B	Reserved	H19	I	OV_{DD}	10
TBSCAN_EN_B	Test Boundary Scan Enable	F19	I	OV_{DD}	6
TEST_SEL_B	Reserved	F20	I	OV_{DD}	10
JTAG					
TCK	Test Clock	E18	I	OV_{DD}	---
TDI	Test Data In	G17	I	OV_{DD}	9
TDO	Test Data Out	E20	O	OV_{DD}	2
TMS	Test Mode Select	G18	I	OV_{DD}	9
TRST_B	Test Reset	E19	I	OV_{DD}	9
Analog Signals					
D1_TPA	Reserved	F21	IO		12
FA_ANALOG_G_V	Reserved	AG21	IO		15
FA_ANALOG_PIN	Reserved	AD21	IO		15
TD1_ANODE	Thermal diode anode	J13	IO		17
TD1_CATHODE	Thermal diode cathode	H13	IO		17
TH_TPA	Reserved	H8	-	-	12
SerDes 1					
SD1_IMP_CAL_RX	SerDes Receive Impedence Calibration	Y11	I	SV_{DD}	11
SD1_IMP_CAL_TX	SerDes Transmit Impedance Calibration	AA6	I	XV_{DD}	16
SD1_PLL1_TPA	SerDes PLL 1 Test Point Analog	AF12	O	AVDD_SD1_PLL1	12
SD1_PLL1_TPD	SerDes Test Point Digital	AF13	O	XV_{DD}	12
SD1_PLL2_TPA	SerDes PLL 2 Test Point Analog	AF5	O	AVDD_SD1_PLL2	12
SD1_PLL2_TPD	SerDes Test Point Digital	AB5	O	XV_{DD}	12
SD1_REF_CLK1_N	SerDes PLL 1 Reference Clock Complement	AH13	I	SV_{DD}	---
SD1_REF_CLK1_P	SerDes PLL 1 Reference Clock	AG13	I	SV_{DD}	---
SD1_REF_CLK2_N	SerDes PLL 2 Reference Clock Complement	AB8	I	SV_{DD}	---

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
SD1_REF_CLK2_P	SerDes PLL 2 Reference Clock	AA8	I	SV_{DD}	---
SD1_RX0_N	SerDes Receive Data (negative)	AH6	I	SV_{DD}	---
SD1_RX0_P	SerDes Receive Data (positive)	AG6	I	SV_{DD}	---
SD1_RX1_N	SerDes Receive Data (negative)	AH8	I	SV_{DD}	---
SD1_RX1_P	SerDes Receive Data (positive)	AG8	I	SV_{DD}	---
SD1_RX2_N	SerDes Receive Data (negative)	AH10	I	SV_{DD}	---
SD1_RX2_P	SerDes Receive Data (positive)	AG10	I	SV_{DD}	---
SD1_RX3_N	SerDes Receive Data (negative)	AH11	I	SV_{DD}	---
SD1_RX3_P	SerDes Receive Data (positive)	AG11	I	SV_{DD}	---
SD1_TX0_N	SerDes Transmit Data (negative)	AE6	O	XV_{DD}	---
SD1_TX0_P	SerDes Transmit Data (positive)	AD6	O	XV_{DD}	---
SD1_TX1_N	SerDes Transmit Data (negative)	AE8	O	XV_{DD}	---
SD1_TX1_P	SerDes Transmit Data (positive)	AD8	O	XV_{DD}	---
SD1_TX2_N	SerDes Transmit Data (negative)	AE10	O	XV_{DD}	---
SD1_TX2_P	SerDes Transmit Data (positive)	AD10	O	XV_{DD}	---
SD1_TX3_N	SerDes Transmit Data (negative)	AE11	O	XV_{DD}	---
SD1_TX3_P	SerDes Transmit Data (positive)	AD11	O	XV_{DD}	---
SerDes 2					
SD2_IMP_CAL_RX	SerDes Receive Impedence Calibration	Y12	I	SV_{DD}	11
SD2_IMP_CAL_TX	SerDes Transmit Impedance Calibration	Y20	I	XV_{DD}	16
SD2_PLL1_TPA	SerDes PLL 1 Test Point Analog	AF14	O	AVDD_SD2_PLL1	12
SD2_PLL1_TPD	SerDes Test Point Digital	AC13	O	XV_{DD}	12
SD2_PLL2_TPA	SerDes PLL 2 Test Point Analog	AF20	O	AVDD_SD2_PLL2	12
SD2_PLL2_TPD	SerDes Test Point Digital	AA20	O	XV_{DD}	12

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
SD2_REF_CLK1_N	SerDes PLL 1 Reference Clock Complement	AE13	I	SV_{DD}	---
SD2_REF_CLK1_P	SerDes PLL 1 Reference Clock	AD13	I	SV_{DD}	---
SD2_REF_CLK2_N	SerDes PLL 2 Reference Clock Complement	AB19	I	SV_{DD}	---
SD2_REF_CLK2_P	SerDes PLL 2 Reference Clock	AB18	I	SV_{DD}	---
SD2_RX0_N	SerDes Receive Data (negative)	AH15	I	SV_{DD}	---
SD2_RX0_P	SerDes Receive Data (positive)	AG15	I	SV_{DD}	---
SD2_RX1_N	SerDes Receive Data (negative)	AH16	I	SV_{DD}	---
SD2_RX1_P	SerDes Receive Data (positive)	AG16	I	SV_{DD}	---
SD2_RX2_N	SerDes Receive Data (negative)	AH18	I	SV_{DD}	---
SD2_RX2_P	SerDes Receive Data (positive)	AG18	I	SV_{DD}	---
SD2_RX3_N	SerDes Receive Data (negative)	AH19	I	SV_{DD}	---
SD2_RX3_P	SerDes Receive Data (positive)	AG19	I	SV_{DD}	---
SD2_TX0_N	SerDes Transmit Data (negative)	AE15	O	XV_{DD}	---
SD2_TX0_P	SerDes Transmit Data (positive)	AD15	O	XV_{DD}	---
SD2_TX1_N	SerDes Transmit Data (negative)	AE16	O	XV_{DD}	---
SD2_TX1_P	SerDes Transmit Data (positive)	AD16	O	XV_{DD}	---
SD2_TX2_N	SerDes Transmit Data (negative)	AE18	O	XV_{DD}	---
SD2_TX2_P	SerDes Transmit Data (positive)	AD18	O	XV_{DD}	---
SD2_TX3_N	SerDes Transmit Data (negative)	AE19	O	XV_{DD}	---
SD2_TX3_P	SerDes Transmit Data (positive)	AD19	O	XV_{DD}	---
USB PHY 1					
USB1_D_M	USB PHY HS Data (-)	E6	IO	-	---
USB1_D_P	USB PHY HS Data (+)	F6	IO	-	---
USB1_ID	USB PHY ID Detect	F5	I	-	---

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
USB1_RESREF	USB PHY Impedance Calibration	G3	IO	-	---
USB1_RX_M	USB PHY SS Receive Data (-)	E4	I	-	---
USB1_RX_P	USB PHY SS Receive Data (+)	E3	I	-	---
USB1_TX_M	USB PHY SS Transmit Data (-)	F2	O	-	---
USB1_TX_P	USB PHY SS Transmit Data (+)	F1	O	-	---
USB1_VBUS	USB PHY VBUS	E7	I	-	---
USB PHY 2					
USB2_D_M	USB PHY HS Data (-)	C6	IO	-	---
USB2_D_P	USB PHY HS Data (+)	D6	IO	-	---
USB2_ID	USB PHY ID Detect	D5	I	-	---
USB2_RESREF	USB PHY Impedance Calibration	G4	IO	-	---
USB2_RX_M	USB PHY SS Receive Data (-)	C4	I	-	---
USB2_RX_P	USB PHY SS Receive Data (+)	C3	I	-	---
USB2_TX_M	USB PHY SS Transmit Data (-)	D2	O	-	---
USB2_TX_P	USB PHY SS Transmit Data (+)	D1	O	-	---
USB2_VBUS	USB PHY VBUS	C7	I	-	---
USB1 and 2					
USB2_DRVVBUS/**IIC3_SCL**/ GPIO4_28/EVT5_B/BRGO4/ CLK11	DRV VBus	L4	O	DV_{DD}	1
USB2_PWRFAULT/**IIC3_SDA**/ GPIO4_29/EVT6_B/BRGO1/ CLK12_CLK8	PWR Fault	M4	I	DV_{DD}	1
USB_DRVVBUS/GPIO4_02	USB_DRVVBUS	H6	O	DV_{DD}	1
USB_PWRFAULT/GPIO4_03	USB_PWRFAULT	G6	I	DV_{DD}	1
Ethernet Management Interface 1					
EMI1_MDC/GPIO4_00	Management Data Clock	AG2	O	LV_{DD}	1, 13
EMI1_MDIO/GPIO4_01	Management Data In/Out	AF2	IO	LV_{DD}	13
Ethernet Management Interface 2					
EMI2_MDC/GPIO2_20	Management Data Clock	AH4	O	TV_{DD}	1
EMI2_MDIO/GPIO2_21	Management Data In/Out	AH3	IO	TV_{DD}	---
Ethernet Controller 1					
EC1_GTX_CLK/GPIO2_27	Transmit Clock Out	W4	O	LV_{DD}	1
EC1_GTX_CLK125/GPIO2_28	Reference Clock	AC3	I	LV_{DD}	1
EC1_RXD0/GPIO4_12	Receive Data	AA2	I	LV_{DD}	1
EC1_RXD1/GPIO4_11	Receive Data	AA1	I	LV_{DD}	1

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
EC1_RXD2/GPIO2_30	Receive Data	Y1	I	LV_{DD}	1
EC1_RXD3/GPIO2_29	Receive Data	W2	I	LV_{DD}	1
EC1_RX_CLK/GPIO4_13	Receive Clock	W1	I	LV_{DD}	1
EC1_RX_DV/GPIO4_14	Receive Data Valid	AB1	I	LV_{DD}	1
EC1_TXD0/GPIO2_25	Transmit Data	AB3	O	LV_{DD}	1
EC1_TXD1/GPIO2_24	Transmit Data	AA3	O	LV_{DD}	1
EC1_TXD2/GPIO2_23	Transmit Data	Y4	O	LV_{DD}	1
EC1_TXD3/GPIO2_22	Transmit Data	Y3	O	LV_{DD}	1
EC1_TX_EN/GPIO2_26	Transmit Enable	AB4	O	LV_{DD}	1, 14
Ethernet Controller 2					
EC2_GTX_CLK/GPIO4_20	Transmit Clock Out	AC4	O	LV_{DD}	1
EC2_GTX_CLK125/GPIO4_21	Reference Clock	AG4	I	LV_{DD}	1
EC2_RXD0/GPIO4_25/ TSEC_1588_TRIG_IN2	Receive Data	AE2	I	LV_{DD}	1
EC2_RXD1/GPIO4_24/ TSEC_1588_PULSE_OUT1	Receive Data	AE1	I	LV_{DD}	1
EC2_RXD2/GPIO4_23	Receive Data	AD1	I	LV_{DD}	1
EC2_RXD3/GPIO4_22	Receive Data	AC2	I	LV_{DD}	1
EC2_RX_CLK/GPIO4_26/ TSEC_1588_CLK_IN	Receive Clock	AC1	I	LV_{DD}	1
EC2_RX_DV/GPIO4_27/ TSEC_1588_TRIG_IN1	Receive Data Valid	AF1	I	LV_{DD}	1
EC2_TXD0/GPIO4_18/ TSEC_1588_PULSE_OUT2	Transmit Data	AF3	O	LV_{DD}	1
EC2_TXD1/GPIO4_17/ TSEC_1588_CLK_OUT	Transmit Data	AE4	O	LV_{DD}	1
EC2_TXD2/GPIO4_16/ TSEC_1588_ALARM_OUT1	Transmit Data	AE3	O	LV_{DD}	1
EC2_TXD3/GPIO4_15/ TSEC_1588_ALARM_OUT2	Transmit Data	AD3	O	LV_{DD}	1
EC2_TX_EN/GPIO4_19	Transmit Enable	AG3	O	LV_{DD}	1, 14
General Purpose Input/Output					
GPIO1_00/**IFC_AD00**/ cfg_gpinput0	General Purpose Input/Output	B12	O	OV_{DD}	1, 4
GPIO1_01/**IFC_AD01**/ cfg_gpinput1	General Purpose Input/Output	A11	O	OV_{DD}	1, 4
GPIO1_02/**IFC_AD02**/ cfg_gpinput2	General Purpose Input/Output	B11	O	OV_{DD}	1, 4
GPIO1_03/**IFC_AD03**/ cfg_gpinput3	General Purpose Input/Output	A10	O	OV_{DD}	1, 4
GPIO1_04/**IFC_AD04**/ cfg_gpinput4	General Purpose Input/Output	A9	O	OV_{DD}	1, 4

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
GPIO1_05/**IFC_AD05**/ cfg_gpinput5	General Purpose Input/Output	B9	O	OV_{DD}	1, 4
GPIO1_06/**IFC_AD06**/ cfg_gpinput6	General Purpose Input/Output	A8	O	OV_{DD}	1, 4
GPIO1_07/**IFC_AD07**/ cfg_gpinput7	General Purpose Input/Output	B8	O	OV_{DD}	1, 4
GPIO1_08/**IFC_AD08**/ cfg_rcw_src1	General Purpose Input/Output	A12	O	OV_{DD}	1, 4
GPIO1_09/**IFC_AD09**/ cfg_rcw_src2	General Purpose Input/Output	A13	O	OV_{DD}	1, 4
GPIO1_10/**IFC_AD10**/ cfg_rcw_src3	General Purpose Input/Output	B14	O	OV_{DD}	1, 4
GPIO1_11/**IFC_AD11**/ cfg_rcw_src4	General Purpose Input/Output	A14	O	OV_{DD}	1, 4
GPIO1_12/**IFC_AD12**/ cfg_rcw_src5	General Purpose Input/Output	B15	O	OV_{DD}	1, 4
GPIO1_13/**IFC_AD13**/ cfg_rcw_src6	General Purpose Input/Output	A15	O	OV_{DD}	1, 4
GPIO1_14/**IFC_AD14**/ cfg_rcw_src7	General Purpose Input/Output	A16	O	OV_{DD}	1, 4
GPIO1_15/**IFC_AD15**/ cfg_rcw_src8	General Purpose Input/Output	A17	O	OV_{DD}	1, 4
GPIO1_16/**IFC_A00**/ QSPI_A_CS0	General Purpose Input/Output	D8	O	OV_{DD}	1, 5
GPIO1_17/**IFC_A01**/ QSPI_A_CS1	General Purpose Input/Output	C8	O	OV_{DD}	1, 5
GPIO1_18/**IFC_A02**/ QSPI_A_SCK	General Purpose Input/Output	C9	O	OV_{DD}	1, 5
GPIO1_19/**IFC_A03**/ QSPI_B_CS0	General Purpose Input/Output	D10	O	OV_{DD}	1, 5
GPIO1_20/**IFC_A04**/ QSPI_B_CS1	General Purpose Input/Output	C10	O	OV_{DD}	1, 5
GPIO1_21/**IFC_A05**/ QSPI_B_SCK/cfg_dram_type	General Purpose Input/Output	C11	O	OV_{DD}	1, 4
GPIO1_22/**IFC_WE0_B**/ cfg_eng_use0	General Purpose Input/Output	C15	O	OV_{DD}	1, 4, 19
GPIO1_23/**IFC_TE**/cfg_ifc_te	General Purpose Input/Output	E14	O	OV_{DD}	1, 4
GPIO1_24/**IFC_ALE**	General Purpose Input/Output	A18	O	OV_{DD}	1, 5
GPIO1_25/**IFC_CLE**/ cfg_rcw_src0	General Purpose Input/Output	C19	O	OV_{DD}	1, 4
GPIO1_26/**IFC_OE_B**/ cfg_eng_use1	General Purpose Input/Output	C18	O	OV_{DD}	1, 5
GPIO1_27/**IFC_WP0_B**/ cfg_eng_use2	General Purpose Input/Output	D19	O	OV_{DD}	1, 5

Table continues on the next page...