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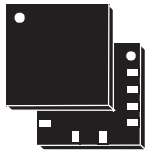
LSM303C

Ultra-compact high-performance eCompass module: 3D accelerometer and 3D magnetometer

Datasheet - production data



LGA-12 (2.0x2.0x1.0 mm)

Features

- 3 magnetic field channels and 3 acceleration channels
- ±16 gauss magnetic full scale
- ±2/±4/±8 *g* selectable acceleration full scale
- 16-bit data output
- SPI / I^2C serial interfaces
- Analog supply voltage 1.9 V to 3.6 V
- Power-down mode / low-power mode
- Programmable interrupt generators for free-fall, motion detection and magnetic field detection
- Embedded temperature sensor
- Embedded FIFO
- ECOPACK®, RoHS and “Green” compliant

Applications

- Tilt-compensated compasses
- Map rotation
- Position detection
- Motion-activated functions
- Free-fall detection
- Click/double-click recognition
- Pedometer
- Intelligent power saving for handheld devices
- Display orientation
- Gaming and virtual reality input devices
- Impact recognition and logging
- Vibration monitoring and compensation

Description

The LSM303C is a system-in-package featuring a 3D digital linear acceleration sensor and a 3D digital magnetic sensor.

The LSM303C has linear acceleration full scales of ±2 *g* / ±4 *g* / ±8 *g* and a magnetic field full scale of ±16 gauss.

The LSM303C includes an I^2C serial bus interface that supports standard and fast mode (100 kHz and 400 kHz) and an SPI serial standard interface.

The system can be configured to generate an interrupt signal for free-fall, motion detection and magnetic field detection.

The magnetic and accelerometer blocks can be enabled or put into power-down mode separately.

The LSM303C is available in a plastic land grid array package (LGA) and is guaranteed to operate over an extended temperature range from -40 °C to +85 °C.

Table 1. Device summary

Part number	Temperature range [°C]	Package	Packaging
LSM303C	-40 to +85	LGA-12	Tray
LSM303CTR	-40 to +85	LGA-12	Tape and reel

Contents

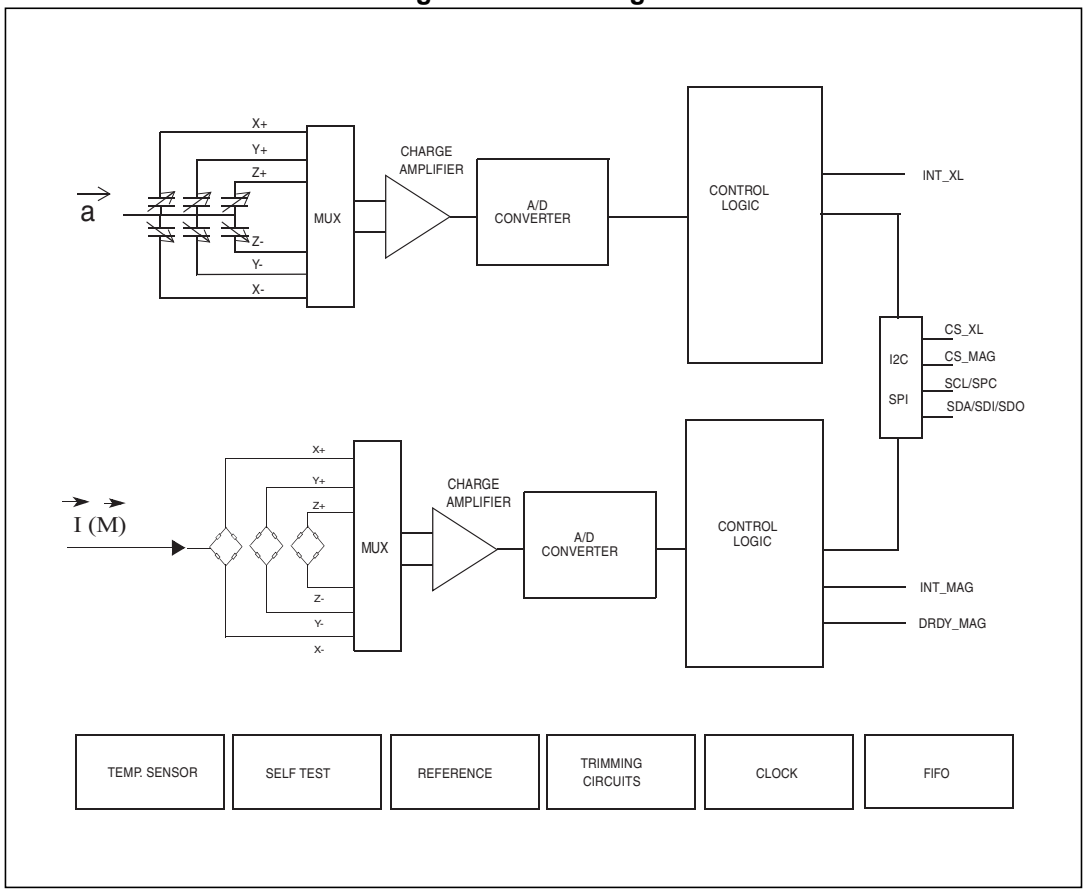
List of tables

List of figures

1 Block diagram and pin description

1.1 Block diagram

Figure 1. Block diagram



1.2 Pin description

Figure 2. Pin connections

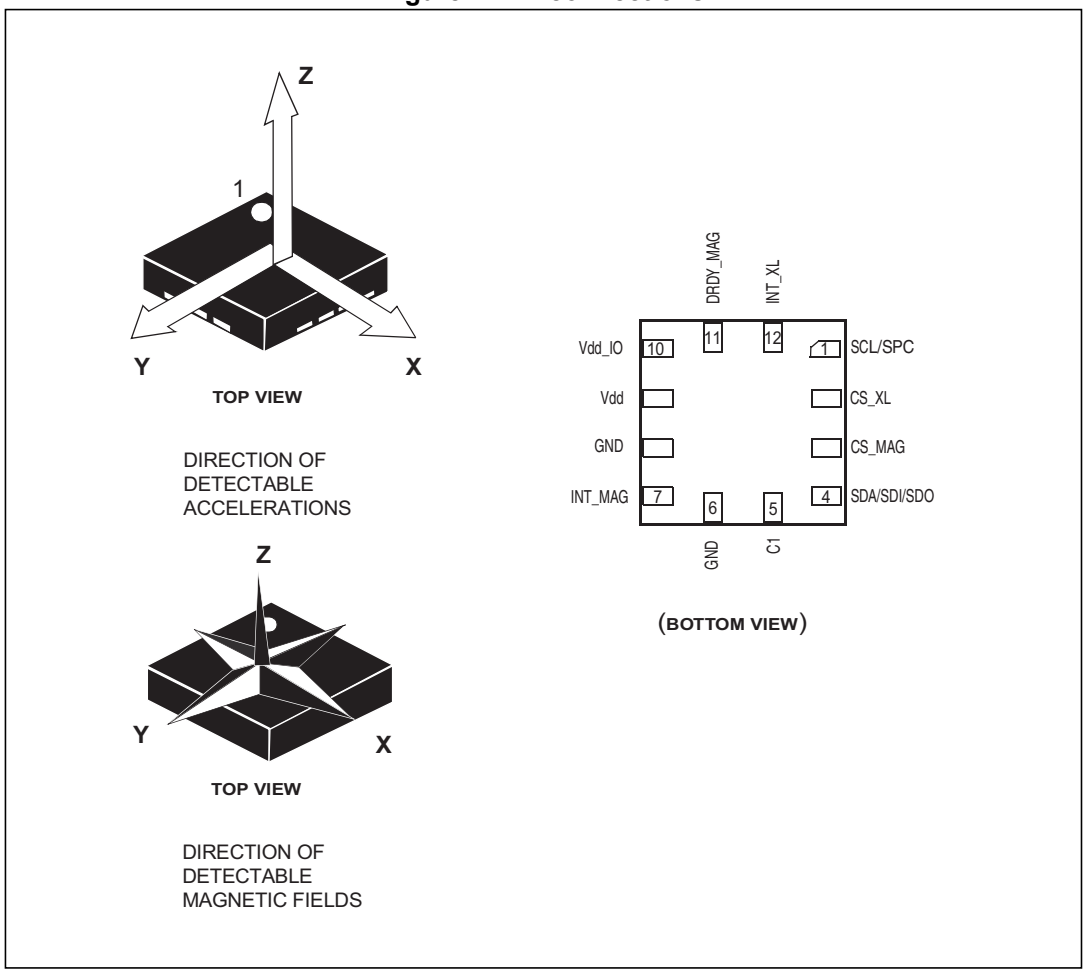


Table 2. Pin description

Pin#	Name	Function
1	SCL SPC	I^2C serial clock (SCL) SPI serial port clock (SPC)
2	CS_XL	Accelerometer: SPI enable I^2C/SPI mode selection 1: SPI idle mode / I^2C communication enabled; 0: SPI communication mode / I^2C disabled
3	CS_MAG	Magnetometer: SPI enable I^2C/SPI mode selection 1: SPI idle mode / I^2C communication enabled; 0: SPI communication mode / I^2C disabled
4	SDA SDI SDO	I^2C serial data (SDA) SPI serial data input (SDI) 3-wire interface serial data output (SDO)
5	C1	Capacitor connection (C1 = 100 nF)
6	GND	Connected to GND
7	INT_MAG	Magnetometer interrupt signal
8	GND	Connected to GND
9	Vdd	Power supply
10	Vdd_IO	Power supply for I/O pins
11	DRDY_MAG	Magnetometer data ready
12	INT_XL	Accelerometer interrupt signal

2 Module specifications

2.1 Sensor characteristics

@ Vdd = 2.5 V, T = 25 °C unless otherwise noted [a].

Table 3. Sensor characteristics

Symbol	Parameter	Test conditions	Min.	Typ.(1)	Max.	Unit
LA_FS	Linear acceleration measurement range(2)			±2		*g*
				±4		
				±8		
M_FS	Magnetic measurement range			±16		gauss
LA_So	Linear acceleration sensitivity	Linear acceleration FS = ±2 g		0.061		mg/LSB
		Linear acceleration FS = ±4 g		0.122		
		Linear acceleration FS = ±8 g		0.244		
M_GN	Magnetic sensitivity	Magnetic FS = ±16 gauss		0.58		mgauss/ LSB
LA_TCSo	Linear acceleration sensitivity change vs. temperature			0.01		%/°C
LA_TyOff	Typical zero-*g* level offset accuracy(3),(4)			±40		mg
M_TyOff	Typical zero-*gauss* level offset accuracy			±1		gauss
LA_TCOff	Zero-*g* level change vs. temp.	Max. delta from 25 °C		±0.5		mg/°C
LA_An	Linear acceleration RMS noise	ODR = 100 Hz, BW = 50 Hz, FS = ±2 *g*		1		mg (RMS)
M_R	Magnetic RMS noise	Ultra-high-performance mode		3.5		mgauss (RMS)
DF	Magnetic disturbance field	Zero-gauss offset starts to degrade			50	gauss
LA_ST	Linear acceleration self-test positive difference(5)		70		1500	mg
M_ST	Magnetic self-test(6)	X, Y-axis	-1		-3	gauss
		Z-axis	-0.1		-1	
Top	Operating temperature range		-40		+85	°C

1. Typical specifications are not guaranteed.
2. Verified by wafer level test and measurement of initial offset and sensitivity.
3. Typical zero-*g* level offset value after MSL3 preconditioning.
4. Offset can be eliminated by enabling the built-in high-pass filter.
5. Accelerometer “Self-test positive difference” is defined as: $OUTPUT[mg]_{(CTRL\_REG5\_A\ ST2,\ ST1\ bits=01)}$ - $OUTPUT[mg]_{(CTRL\_REG5\_A\ ST2,\ ST1\ bits=00)}$.
6. Magnetic “self-test” is defined as: $OUTPUT[gauss]_{(CTRL\_REG1\_M\ ST\ bit=1)}$ - $OUTPUT[gauss]_{(CTRL\_REG1\_M\ ST\ bit=0)}$.

a. The product is factory calibrated at 2.5 V. The operational power supply range is from 1.9 V to 3.6 V.

2.2 Temperature sensor characteristics

@ Vdd = 2.5 V, T = 25 °C unless otherwise noted[b].

Table 4. Temperature sensor characteristics

Symbol	Parameter	Test conditions	Min.	Typ.[1]	Max.	Unit
TSDr	Temperature sensor output change vs. temp.			8		digit/°C
TODR	Temperature refresh rate[2]			ODR		Hz
Top	Operating temperature range		-40		+85	°C

1. Typical specifications are not guaranteed.
2. If the TEMP_EN bit in *CTRL_REG1_M (20h)* is set to '1', temperature data is acquired at each conversion cycle. Refer to *Table 73: Output data rate configuration*

2.3 Electrical characteristics

@ Vdd = 2.5 V, T = 25 °C unless otherwise noted.[b]

Table 5. Electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.[1]	Max.	Unit
Vdd	Supply voltage		1.9		3.6	V
Vdd_IO	Module power supply for I/O		1.71	1.8	Vdd+0.1	V
LA_Idd_NM	Linear acceleration current consumption in active mode. Magnetic sensor in power-down mode.	ODR = 100 - 800 Hz		180		µA
		ODR = 50 Hz		120		
		ODR =10 Hz		50		
M_Idd_HR	Magnetic current consumption in ultra-high resolution mode Linear acceleration in power-down mode.	ODR = 20 Hz		270		µA
M_Idd_LP	Magnetic current consumption in low-power mode Linear acceleration in power-down mode.	ODR = 20 Hz		40		µA
Idd_PD	Current consumption in power-down			6		µA
T_{OP}	Operating temperature range		-40		+85	°C
Trise	Time for power supply rising[2]		0.01		100	ms
Twait	Time delay between Vdd_IO and Vdd[2]		0		10	ms

1. Typical specifications are not guaranteed.
2. Please refer to *Section 2.3.1: Recommended power-up sequence* for more details.

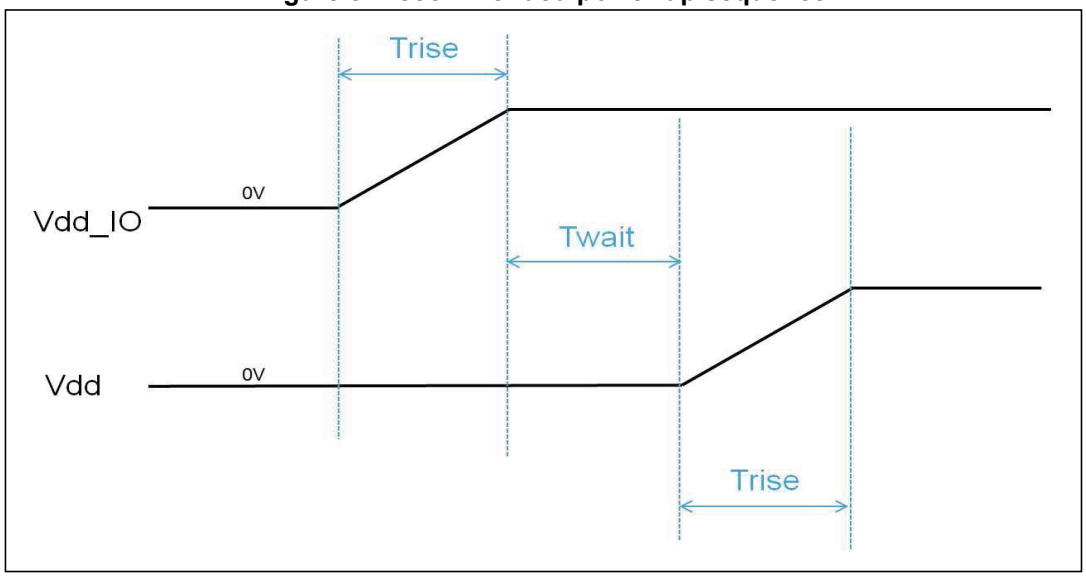
b. The product is factory calibrated at 2.5 V.The operational power supply range is from 1.9 V to 3.6 V.

2.3.1 Recommended power-up sequence

For the power-up sequence please refer to the following figure, where:

- Trise is the time for the power supply to rise from 10% to 90% of its final value
- Twait is the time delay between the end of the Vdd_IO ramp (90% of its final value) and the start of the Vdd ramp

Figure 3. Recommended power-up sequence



2.4 Communication interface characteristics

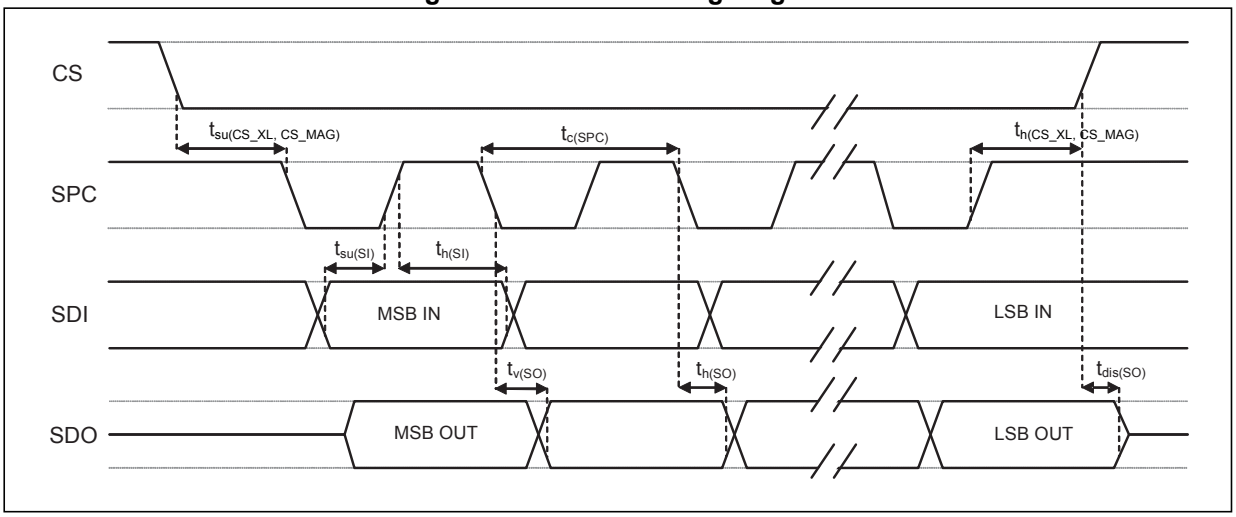
2.4.1 SPI - serial peripheral interface

Subject to general operating conditions for Vdd and Top.

Table 6. SPI slave timing values

Symbol	Parameter	Value (1)		Unit
		Min	Max	
$t_{c(SPC)}$	SPI clock cycle	100		ns
$f_{c(SPC)}$	SPI clock frequency		10	MHz
$t_{su(CS\_XL,\ CS\_MAG)}$	CS setup time	6		ns
$t_{h(CS\_XL,\ CS\_MAG)}$	CS hold time	8		
$t_{su(SI)}$	SDI input setup time	5		
$t_{h(SI)}$	SDI input hold time	15		
$t_{v(SO)}$	SDO valid output time		50	
$t_{h(SO)}$	SDO output hold time	9		
$t_{dis(SO)}$	SDO output disable time		50	

Figure 4. SPI slave timing diagram



Note: Values are guaranteed at 10 MHz clock frequency for SPI with 3 wires, based on characterization results, not tested in production.

Measurement points are done at 0.2·Vdd_IO and 0.8·Vdd_IO, for both input and output ports.

2.4.2 I²C - inter-IC control interface

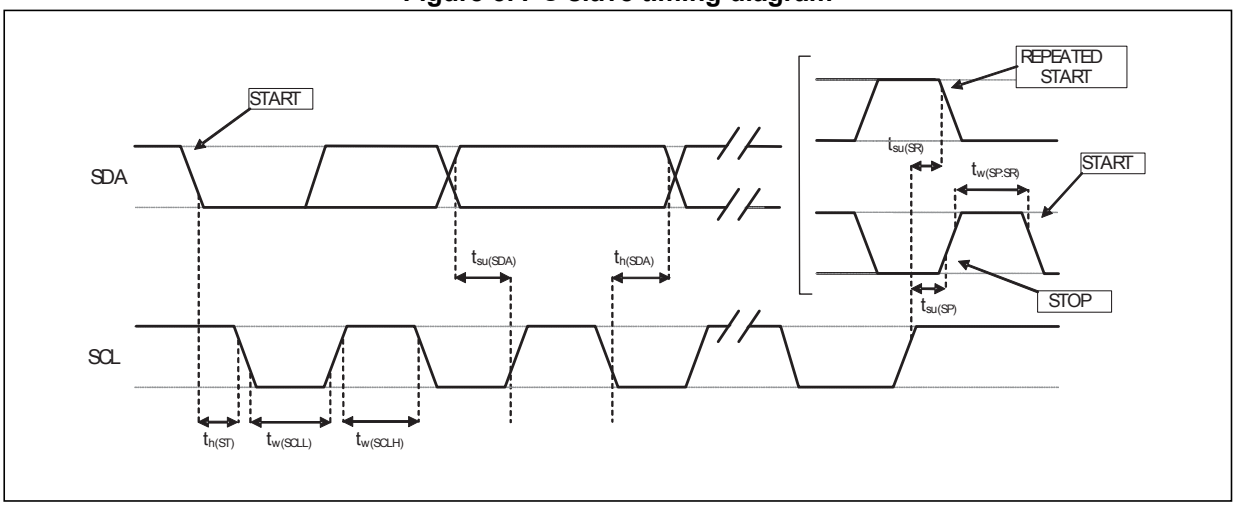
Subject to general operating conditions for Vdd and Top.

Table 7. I²C slave timing values

Symbol	Parameter	I²C standard mode (1)		I²C fast mode (1)		Unit
		Min	Max	Min	Max	
$f_{(SCL)}$	SCL clock frequency	0	100	0	400	kHz
$t_{w(SCLL)}$	SCL clock low time	4.7		1.3		µs
$t_{w(SCLH)}$	SCL clock high time	4.0		0.6		
$t_{su(SDA)}$	SDA setup time	250		100		ns
$t_{h(SDA)}$	SDA data hold time	0	3.45	0	0.9	µs
$t_{h(ST)}$	START condition hold time	4		0.6		µs
$t_{su(SR)}$	Repeated START condition setup time	4.7		0.6		
$t_{su(SP)}$	STOP condition setup time	4		0.6		
$t_{w(SP:SR)}$	Bus free time between STOP and START condition	4.7		1.3		

1. Data based on standard I²C protocol requirement, not tested in production

Figure 5. I²C slave timing diagram



Note: Measurement points are done at 0.2·Vdd_IO and 0.8·Vdd_IO, for both ports.

2.5 Absolute maximum ratings

Stresses above those listed as “absolute maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 8. Absolute maximum ratings

Symbol	Ratings	Maximum value	Unit
Vdd	Supply voltage	-0.3 to 4.8	V
Vdd_IO	I/O pins supply voltage	-0.3 to 4.8	V
Vin	Input voltage on any control pin (CS_XL, CS_MAG, SCL/SPC, SDA/SDI/SDO)	-0.3 to Vdd_IO +0.3	V
A_{POW}	Acceleration (any axis, powered, Vdd = 2.5 V)	3000 for 0.5 ms	*g*
		10000 for 0.1 ms	*g*
A_{UNP}	Acceleration (any axis, unpowered)	3000 for 0.5 ms	*g*
		10000 for 0.1 ms	*g*
M_{EF}	Maximum exposed field	1000	gauss
T_{OP}	Operating temperature range	-40 to +85	°C
T_{STG}	Storage temperature range	-40 to +125	°C
ESD	Electrostatic discharge protection (HBM)	2	kV

Note: Supply voltage on any pin should never exceed 4.8 V

This device is sensitive to mechanical shock, improper handling can cause permanent damage to the part

This device is sensitive to electrostatic discharge (ESD), improper handling can cause permanent damage to the part

3 Terminology

3.1 Sensitivity

3.1.1 Linear acceleration sensor sensitivity

Sensitivity describes the gain of the sensor and can be determined by applying 1 *g* acceleration to it. As the sensor can measure DC accelerations this can be done easily by pointing the axis of interest towards the center of the Earth, noting the output value, rotating the sensor by 180 degrees (pointing to the sky) and noting the output value again. By doing so, ±1 *g* acceleration is applied to the sensor. Subtracting the larger output value from the smaller one, and dividing the result by 2, leads to the actual sensitivity of the sensor. This value changes very little over temperature and time. The sensitivity tolerance describes the range of sensitivities of a large population of sensors.

3.1.2 Magnetic sensor sensitivity

Sensitivity describes the gain of the sensor and can be determined, for example, by applying a magnetic field of 1 *gauss* to it.

3.2 Zero-*g* level

The zero-*g* level offset (LA_TyOff) describes the deviation of an actual output signal from the ideal output signal if no acceleration is present. A sensor in a steady state on a horizontal surface will measure 0 *g* for the X-axis and 0 *g* for the Y-axis whereas the Z-axis will measure 1 *g*. The output is ideally in the middle of the dynamic range of the sensor (content of OUT registers 00h, data expressed as two's complement number). A deviation from the ideal value in this case is called zero-*g* offset. Offset is to some extent a result of stress to MEMS sensor and therefore the offset can slightly change after mounting the sensor onto a printed circuit board or exposing it to extensive mechanical stress. Offset changes little with temperature, see *Table 3* "Zero-*g* level change vs. temperature" (LA_TCOff). The zero-*g* level tolerance (TyOff) describes the standard deviation of the range of zero-*g* levels of a population of sensors.

3.3 Zero-*gauss* level

Zero-*g*auss level offset (M_TyOff) describes the deviation of an actual output signal from the ideal output if no magnetic field is present.

4 Functionality

4.1 Self-test

The self-test allows checking the linear acceleration functionality without moving it. The self-test function is off when the self-test bits (ST) are programmed to ‘00’. When the self-test bits are changed, an actuation force is applied to the sensor, simulating a definite input acceleration. In this case the sensor outputs will exhibit a change in their DC levels which are related to the selected full scale through the device sensitivity. When the self-test is activated, the device output level is given by the algebraic sum of the signals produced by the acceleration acting on the sensor and by the electrostatic test force. If the output signals change within the amplitude limits specified inside *Table 3*, then the sensor is working properly and the parameters of the interface chip are within the defined specifications.

The self-test function is also available for the magnetic sensor. When the magnetic self-test is enabled, a current is forced into a coil near the sensor. This current will generate a magnetic field that will produce a variation of the magnetometer output signals. If the output signals change within the amplitude limits specified in *Table 3*, then the sensor is working properly and the parameters of the interface chip are within the defined specifications.

4.2 FIFO

The LSM303C embeds an acceleration data FIFO for each of the three output channels, X, Y and Z. This allows consistent power saving for the system, since the host processor does not need to continuously poll data from the sensor, but it can wake up only when needed and burst the significant data out from the FIFO. This buffer can work accordingly to the following different modes: Bypass mode, FIFO mode, Stream mode, Stream-to-FIFO mode, Bypass-to-Stream, Bypass-to-FIFO. Each mode is selected by the FIFO_MODE bits in the FIFO_CTRL register. Programmable FIFO threshold level, FIFO empty or FIFO overrun events are in the FIFO_SRC register and can be set to generate a dedicated interrupt on the INT_XL pin.

FIFO_SRC (EMPTY) is equal to '1' when no samples are available.

FIFO_SRC (FTH) goes to '1' if new data arrives and FIFO_SRC(FSS [4:0]) is greater than or equal to FIFO_CTRL (FTH [4:0]). FIFO_SRC (FTH) goes to '0' if reading a X, Y, Z data slot from FIFO and FIFO_SRC (FSS [4:0]) is less than or equal to FIFO_CTRL (FTH [4:0]).

FIFO_SRC (OVR) is equal to '1' if a FIFO slot is overwritten.

The FIFO feature is enabled by writing a '1' to the FIFO_EN bit in CTRL_REG3_A.

To guarantee the correct acquisition of data during the switching into and out of FIFO, the first sample acquired must be discarded.

4.2.1 Bypass mode

In Bypass mode (FIFO_CTRL (FMODE [2:0])= 000), the FIFO is not operational and it remains empty.

Bypass mode is also used to reset the FIFO when in FIFO mode.

4.2.2 FIFO mode

In FIFO mode (FIFO_CTRL (FMODE [2:0]) = 001) data from the X, Y and Z channels are stored in the FIFO until it is full. An overrun interrupt can be enabled, CTRL_REG3_A (INT_XL_OVR) = '1', in order to be raised when the FIFO stops collecting data. When the overrun interrupt occurs, the first set of data has been overwritten and the FIFO stops collecting data from the input channels. To reset the FIFO content, Bypass mode should be written in FIFO_CTRL (FMODE [2:0]) as '000'. After this reset command it is possible to restart FIFO mode by writing '001' to FIFO_CTRL (FMODE [2:0]).

The FIFO buffer can memorize 32 levels of X, Y and Z data, but the depth of the FIFO can be reduced by means of the CTRL_REG3_A (STOP_ FTH) bit. Setting the STOP_FTH bit to '1', the FIFO depth is limited to FIFO_CTRL (FTH [4:0]) - 1.

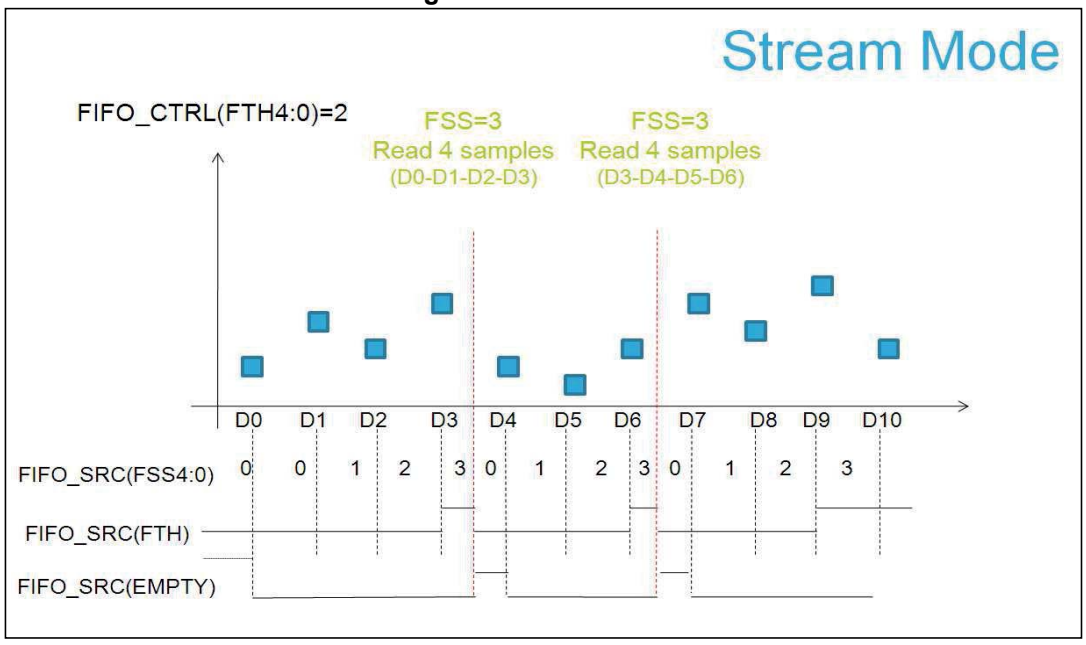
4.2.3 Stream mode

Stream mode (FIFO_CTRL (FMODE [2:0]) = 010) provides a continuous FIFO update. As new data arrives the older data is discarded.

An overrun interrupt can be enabled, CTRL_REG3_A (INT_XL_OVR) = '1', in order to read the entire content of the FIFO at once. If in the application no data can be lost and it is not possible to read at least one sample for each axis within one ODR period, a watermark interrupt can be enabled in order to read partially the FIFO and leave free memory slots for incoming data. Setting the FIFO_CTRL (FTH [4:0]) to an N value, the number of X, Y and Z data samples that should be read at the rise of the watermark interrupt is up to (N+1).

In the latter case, reading all FIFO content before an overrun interrupt has occurred, the first data read is equal to the last data already read in the previous burst, so the number of new data available in FIFO depends on the previous reading (see FIFO_SRC behavior depicted in the following figure).

Figure 6. Stream mode



Stream mode is intended to be used to read all 32 samples of FIFO within an ODR after receiving an overrun signal.

A watermark interrupt CTRL_REG3_A (INT_XL_FTH) can be enabled in order to read data from the FIFO and leave a free memory slot for incoming data. Setting the FIFO_CTRL (FTH [4:0]) to an N value, the number of X, Y and Z data samples that should be read at the rise of the watermark interrupt, in order to read the entire content of the FIFO, is N + 1.

4.2.4 Stream-to-FIFO mode

In Stream-to-FIFO mode (FIFO_CTRL(FMODE2:0) = 011), FIFO behavior changes according to the IG_SRC1_A (IA) bit. When the IG_SRC1_A(IA) bit is equal to '1', FIFO operates in FIFO mode, when the IG_SRC1_A (IA) bit is equal to '0', FIFO operates in Stream mode.

The interrupt generator 1 should be set to the desired configuration by means of IG_CFG1_A, IG_THS_X1_A, IG_THS_Y1_A and IG_THS_Z1_A.

The CTRL_REG7_A (LIR1) bit should be set to '1' in order to have latched interrupt.

4.2.5 Bypass-to-Stream mode

In Bypass-to-Stream mode (FIFO_CTRL (FMODE [2:0]) = '100'), X, Y and Z measurement storage inside FIFO operates in Stream mode when the IG_SRC1_A (IA) is equal to '1', otherwise FIFO content is reset (Bypass mode).

The interrupt generator 1 should be set to the desired configuration by means of IG_CFG1_A, IG_THS_X1_A, IG_THS_Y1_A and IG_THS_Z1_A.

The CTRL_REG7_A (LIR1) bit should be set to '1' in order to have latched interrupt.

4.2.6 Bypass-to-FIFO mode

In Bypass-to-FIFO mode (FIFO_CTRL (FMODE [2:0]) = '111', FIFO behavior changes according to the IG_SRC1_A(IA) bit. When the IG_SRC1_A(IA) bit is equal to '1,' FIFO operates in FIFO mode. When the IG_SRC1_A(IA) bit is equal to '0', FIFO operates in Bypass mode (FIFO content reset). If a latched interrupt is generated, FIFO starts collecting data until the first data into the FIFO buffer is overwritten. The interrupt generator 1 should be set to the desired configuration by means of IG_CFG1_A, IG_THS_X1_A, IG_THS_Y1_A and IG_THS_Z1_A.

The CTRL_REG7_A (LIR1) bit should be set to '1' in order to have latched interrupt.

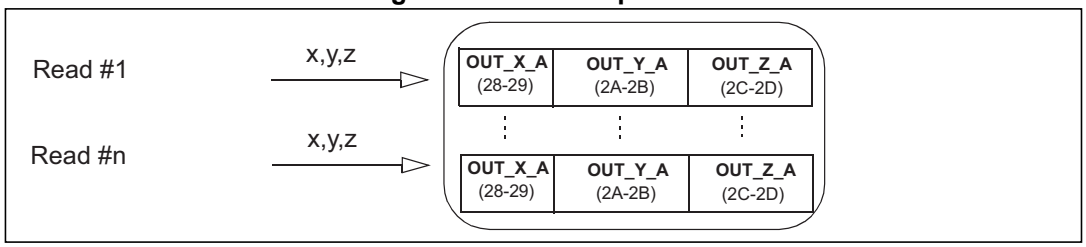
4.2.7 Retrieving data from FIFO

FIFO data is read from the OUT_X_A, OUT_Y_A and OUT_Z_A registers. A read operation using a serial interface of the OUT_X_A, OUT_Y_A or OUT_Z_A output registers provides the data stored in the FIFO. Each time data is read from the FIFO, the oldest X, Y and Z data are placed in the OUT_X_A, OUT_Y_A and OUT_Z_A registers and both single read and read_burst operations can be used.

4.2.8 FIFO multiple read (burst)

Starting from Addr 28h multiple reads can be performed. Once the read reaches Addr 2Dh the system automatically restarts from Addr 28h.

Figure 7. FIFO multiple read



4.3 Activity/Inactivity function

The Activity/Inactivity recognition function allows reducing the power consumption of the accelerometer block in order to supply other smart applications.

When the Activity/Inactivity recognition function is activated, accelerometer is able to automatically go to 10 Hz sampling rate and to wake up as soon as the interrupt event has been detected, increasing the output data rate and bandwidth.

With this feature the system may be efficiently switched from/to low-power mode to full performance depending on user-selectable positioning and acceleration events, thus ensuring power saving and flexibility.

The Activity/Inactivity recognition function is activated by writing the desired threshold in the ACT_THS_A register. The high-pass filter is automatically enabled.

Table 9. Activity/Inactivity function control registers

Register	LSB value
ACT_THS_A	Full Scale / 128 [mg]
ACT_DUR_A	8/ODR [s]

When the acceleration becomes smaller than the threshold for at least (8 ACT_DUR +1)/ODR time, the CTRL_REG1_A (ODR [2:0]) bits of CTRL_REG1_A are bypassed (Inactivity) and internally set to 10 Hz (ODR [2:0] = 001), but the content of the CTRL_REG1_A (ODR [2:0]) bits are left untouched.

When the acceleration becomes bigger than the threshold (ACT_THS_A), CTRL_REG1_A is restored immediately (Activity).

Once the Activity/Inactivity detection function is enabled, it will be applied to the INT_XL pin by setting the CTRL_REG3_A (INT_XL_INACT) bit to ‘1’.

To disable the Activity/Inactivity detection function, set the content of ACT_THS_A register to 00h.

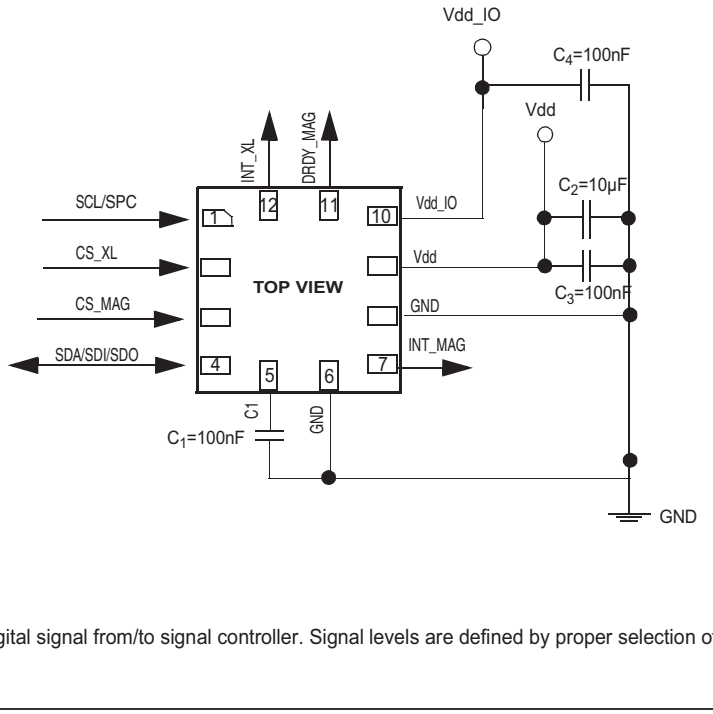
4.4 Factory calibration

The IC interface is factory calibrated for sensitivity (LA_So, M_GN), Zero-*g* level (LA_TyOff) and Zero-*gauss* level (M_TyOff).

The trim values are stored inside the device in non-volatile memory. Anytime the device is turned on, the trim parameters are downloaded into the registers to be used during active operation. This allows using the device without further calibration.

5 Application hints

Figure 8. LSM303C electrical connections



The device core is supplied through the Vdd line while the I/O pads are supplied through the Vdd_IO line. Power supply decoupling capacitors (100 nF ceramic, 10 µF aluminum) should be placed as near as possible to pin 9 of the device (common design practice).

All the voltage and ground supplies must be present at the same time to have proper behavior of the IC (refer to *Figure 8*). It is possible to remove Vdd, maintaining Vdd_IO, without blocking the communication bus, in this condition the measurement chain is powered off.

The functionality of the device and the measured acceleration data are selectable and accessible through the I^2C or SPI interfaces. When using the I^2C, CS must be tied high (i.e. connected to Vdd_IO).

The functions, the threshold and the timing of the two interrupt pins (INT_XL and INT_MAG) can be completely programmed by the user through the I^2C/SPI interface.

5.1 Soldering information

The LGA package is compliant with the ECOPACK®, RoHS and “Green” standards.
It is qualified for soldering heat resistance according to JEDEC J-STD-020.

Leave “Pin 1 Indicator” unconnected during soldering.

Land pattern and soldering recommendations are available at www.st.com.

5.2 High current wiring effects

High current in wiring and printed circuit traces can be culprits in causing errors in magnetic field measurements for compassing.

Conductor-generated magnetic fields will add to the Earth's magnetic field, leading to errors in compass heading computation.

Keep currents higher than 10 mA a few millimeters away from the sensor IC.

6 Digital interfaces

The registers embedded inside the LSM303C may be accessed through both the I^2C and SPI serial interfaces. The latter may be SW-configured to operate in 3-wire interface mode.

The serial interfaces are mapped onto the same pads. To select/exploit the I^2C interface, the CS line must be tied high (i.e. connected to Vdd_IO).

Table 10. Serial interface pin description

Pin name	Pin description
CS_XL, CS_MAG	SPI enable I2C/SPI mode selection (1: SPI idle mode / I^2C communication enabled; 0: SPI communication mode / I^2C disabled)
SCL SPC	I^2C serial clock (SCL) SPI serial port clock (SPC)
SDA SDI SDO	I^2C serial data (SDA) SPI serial data input (SDI) 3-wire interface serial data output (SDO)

6.1 I^2C serial interface

The LSM303C I^2C is a bus slave. The I^2C is employed to write data into registers whose content can also be read back.

The relevant I^2C terminology is given in the table below.

Table 11. Serial interface pin description

Term	Description
Transmitter	The device which sends data to the bus
Receiver	The device which receives data from the bus
Master	The device which initiates a transfer, generates clock signals and terminates a transfer
Slave	The device addressed by the master

There are two signals associated with the I^2C bus: the serial clock line (SCL) and the serial data line (SDA). The latter is a bidirectional line used for sending and receiving the data to/from the interface. Both the lines must be connected to Vdd_IO through an external pull-up resistor. When the bus is free, both the lines are high.

The I^2C interface is compliant with fast mode (400 kHz) I^2C standards as well as with the normal mode.

In order to disable the I^2C block for the accelerometer, CTRL_REG4_A (I2C_DISABLE) must be written to ‘1’, while for magnetometer CTRL_REG3_M (I2C_DISABLE) must be written to ‘1’.

6.1.1 I²C operation

The transaction on the bus is started through a START (ST) signal. A START condition is defined as a HIGH-to-LOW transition on the data line while the SCL line is held HIGH. After this has been transmitted by the master, the bus is considered busy. The next byte of data transmitted after the start condition contains the address of the slave in the first 7 bits and the eighth bit tells whether the master is receiving data from the slave or transmitting data to the slave. When an address is sent, each device in the system compares the first seven bits after a start condition with its address. If they match, the device considers itself addressed by the master.

Data transfer with acknowledge is mandatory. The transmitter must release the SDA line during the acknowledge pulse. The receiver must then pull the data line LOW so that it remains stable low during the HIGH period of the acknowledge clock pulse. A receiver which has been addressed is obliged to generate an acknowledge after each byte of data received.

The I²C embedded inside the LSM303C behaves like a slave device and the following protocol must be adhered to. In the I²C of the accelerometer sensor, after the START condition (ST) a slave address is sent, once a slave acknowledge (SAK) has been returned, an 8-bit sub-address (SUB) is transmitted. The 7 LSb represent the actual register address while the CTRL_REG4_A (IF_ADD_INC) bit defines the address increment. In the I²C of the magnetometer sensor, after the START condition (ST) a slave address is sent, once a slave acknowledge (SAK) has been returned, an 8-bit sub-address (SUB) is transmitted. The 7 LSb represent the actual register address while the MSB enables the address auto increment. The SUB (register address) is automatically increased to allow multiple data read/write.

Table 12. Transfer when master is writing one byte to slave

Master	ST	SAD + W		SUB		DATA		SP
Slave			SAK		SAK		SAK	

Table 13. Transfer when master is writing multiple bytes to slave

Master	ST	SAD + W		SUB		DATA		DATA		SP
Slave			SAK		SAK		SAK		SAK	

Table 14. Transfer when master is receiving (reading) one byte of data from slave

Master	ST	SAD + W		SUB		SR	SAD + R			NMAK	SP
Slave			SAK		SAK			SAK	DATA		

Table 15. Transfer when master is receiving (reading) multiple bytes of data from slave

Master	ST	SAD+W		SUB		SR	SAD+R			MAK		MAK		NMAK	SP
Slave			SAK		SAK			SAK	DATA		DAT A		DATA		

Data are transmitted in byte format (DATA). Each data transfer contains 8 bits. The number of bytes transferred per transfer is unlimited. Data is transferred with the Most Significant bit