Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

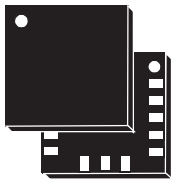
Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

LSM303D

Ultra-compact high-performance eCompass module: 3D accelerometer and 3D magnetometer

Datasheet - production data



LGA-16 (3x3x1 mm)

Features

- 3 magnetic field channels and 3 acceleration channels
- ±2/±4/±8/±12 gauss magnetic full scale
- ±2/±4/±6/±8/±16 *g* linear acceleration full scale
- 16-bit data output
- SPI / I^2C serial interfaces
- Analog supply voltage 2.16 V to 3.6 V
- Power-down mode / low-power mode
- Programmable interrupt generators for free-fall, motion detection and magnetic field detection
- Embedded temperature sensor
- Embedded FIFO
- ECOPACK®, RoHS and “Green” compliant

Applications

- Tilt-compensated compasses
- Map rotation
- Position detection
- Motion-activated functions
- Free-fall detection
- Click/double-click recognition
- Pedometers
- Intelligent power saving for handheld devices
- Display orientation
- Gaming and virtual reality input devices
- Impact recognition and logging
- Vibration monitoring and compensation

Description

The LSM303D is a system-in-package featuring a 3D digital linear acceleration sensor and a 3D digital magnetic sensor.

The LSM303D has linear acceleration full scales of ±2*g* / ±4*g* / ±6*g* / ±8*g* / ±16*g* and a magnetic field full scale of ±2 / ±4 / ±8 / ±12 gauss.

The LSM303D includes an I^2C serial bus interface that supports standard and fast mode (100 kHz and 400 kHz) and SPI serial standard interface.

The system can be configured to generate an interrupt signal for free-fall, motion detection and magnetic field detection. Thresholds and timing of interrupt generators are programmable by the end user.

Magnetic and accelerometer blocks can be enabled or put into power-down mode separately.

The LSM303D is available in a plastic land grid array package (LGA) and is guaranteed to operate over an extended temperature range from -40 °C to +85 °C.

Table 1. Device summary

Part number	Temperature range [°C]	Package	Packaging
LSM303D	-40 to +85	LGA-16	Tray
LSM303DTR	-40 to +85	LGA-16	Tape and reel

Contents

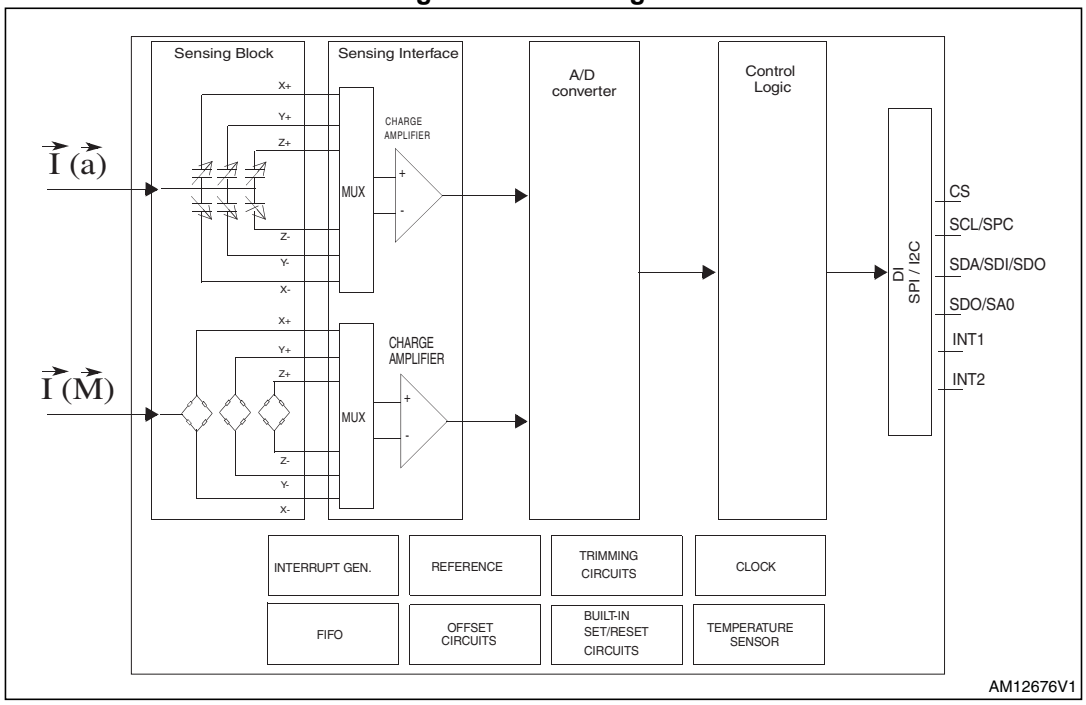
List of tables

List of figures

1 Block diagram and pin description

1.1 Block diagram

Figure 1. Block diagram



1.2 Pin description

Figure 2. Pin connections

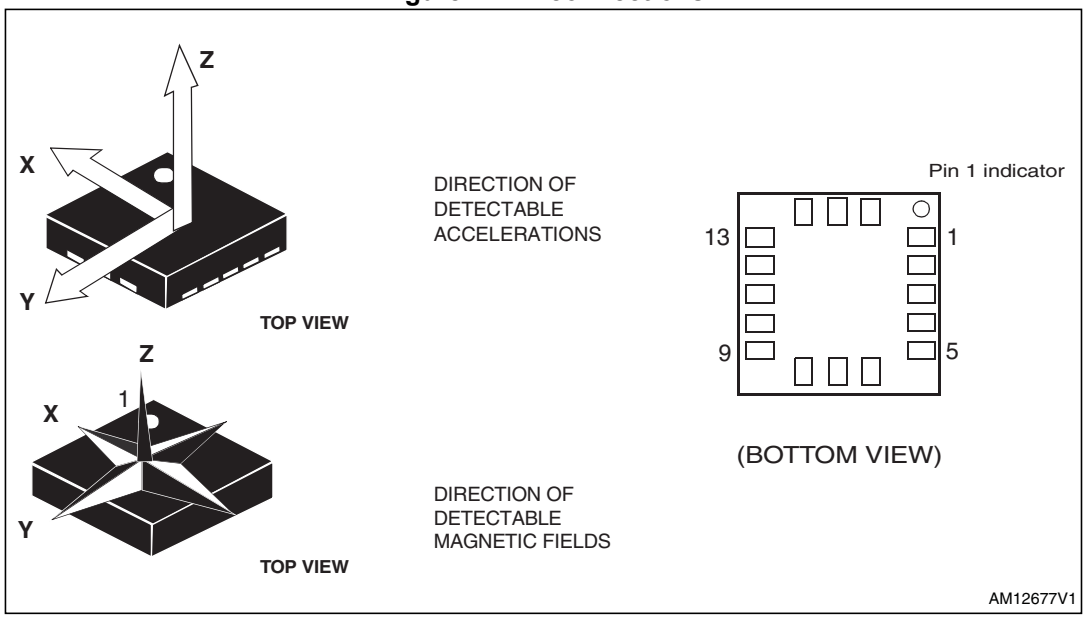


Table 2. Pin description

Pin#	Name	Function
1	Vdd_IO	Power supply for I/O pins
2	SETC	S/R capacitor connection (C_2)
3	SETP	S/R capacitor connection (C_2)
4	SCL SPC	I^2C serial clock (SCL) SPI serial port clock (SPC)
5	GND	0 V supply
6	SDA SDI SDO	I^2C serial data (SDA) SPI serial data input (SDI) 3-wire interface serial data output (SDO)
7	SDO SA0	SPI serial data output (SDO) I^2C less significant bit of the device address (SA0)
8	CS	SPI enable I^2C/SPI mode selection (1: SPI idle mode / I^2C communication enabled; 0: SPI communication mode / I^2C disabled)
9	INT 2	Interrupt 2
10	Reserved	Connect to GND
11	INT 1	Interrupt 1
12	GND	0 V supply
13	GND	0 V supply
14	Vdd	Power supply
15	C1	Capacitor connection (C_1)
16	GND	0 V supply

2 Module specifications

2.1 Sensor characteristics

@ Vdd = 2.5 V, T = 25 °C unless otherwise noted [a].

Table 3. Sensor characteristics

Symbol	Parameter	Test conditions	Min.	Typ.(1)	Max.	Unit
LA_FS	Linear acceleration measurement range(2)			±2		*g*
				±4		
				±6		
				±8		
				±16		
M_FS	Magnetic measurement range			±2		gauss
				±4		
				±8		
				±12		
LA_So	Linear acceleration sensitivity	Linear acceleration FS = ±2 *g*		0.061		mg/LSB
		Linear acceleration FS = ±4 *g*		0.122		
		Linear acceleration FS = ±6 *g*		0.183		
		Linear acceleration FS = ±8 *g*		0.244		
		Linear acceleration FS = ±16 *g*		0.732		
M_So	Magnetic sensitivity	Magnetic FS = ±2 gauss		0.080		mgauss/ LSB
		Magnetic FS = ±4 gauss		0.160		
		Magnetic FS = ±8 gauss		0.320		
		Magnetic FS = ±12 gauss		0.479		
LA_TCSo	Linear acceleration sensitivity change vs. temperature			±0.01		%/°C
M_TCSo	Magnetic sensitivity change vs. temperature			±0.05		%/°C
LA_TyOff	Linear acceleration typical zero-*g* level offset accuracy(3),(4)			±60		m*g*
LA_TCOff	Linear acceleration zero-*g* level change vs. temperature	Max delta from 25 °C		±0.5		m*g*/°C
LA_An	Linear acceleration noise density	Linear acceleration FS = 2*g*; ODR = 100 Hz		150		$ug/(\sqrt{Hz})$
M_R	Magnetic noise density	Magnetic FS = 2 gauss; LR setting CTRL5 (M_RES [1,0]) = 00b		5		mgauss/ RMS

a. The product is factory calibrated at 2.5 V. The operational power supply range is from 2.16 V to 3.6 V.

Table 3. Sensor characteristics (continued)

Symbol	Parameter	Test conditions	Min.	Typ.(1)	Max.	Unit
M_CAS	Magnetic cross-axis sensitivity	Cross field = 0.5 gauss Applied = ±3 gauss		±1		%FS/ gauss
M_EF	Maximum exposed field	No permanent effect on sensor performance			10000	gauss
M_DF	Magnetic disturbance field	Sensitivity starts to degrade. Automatic S/R pulse restores the sensitivity(5)			20	gauss
LA_ST	Linear acceleration self-test positive difference(6)	±2 *g* range, X-, Y-axis AST = 1 see *Table 37*	70		1700	mg
		±2 *g* range, Z-axis AST = 1 see *Table 37*	70		1700	
Top	Operating temperature range		-40		+85	°C

1. Typical specifications are not guaranteed.
2. Verified by wafer level test and measurement of initial offset and sensitivity.
3. Typical zero-*g* level offset value after MSL3 preconditioning.
4. Offset can be eliminated by enabling the built-in high-pass filter.
5. Set/reset pulse is automatically applied at each conversion cycle.
6. “Self-test output change” is defined as: $OUTPUT[mg]_{(CTRL2\ AST\ bit\ =1)}$ - $OUTPUT[mg]_{(CTRL2\ AST\ bit\ =0)}$.

2.2 Temperature sensor characteristics

@ Vdd = 2.5 V, T = 25 °C unless otherwise noted(b).

Table 4. Temperature sensor characteristics

Symbol	Parameter	Test conditions	Min.	Typ.(1)	Max.	Unit
TSDr	Temperature sensor output change vs. temperature	-		8		LSB/°C
TODR	Temperature refresh rate			M_ODR [2:0](2)		Hz
Top	Operating temperature range		-40		+85	°C

1. Typical specifications are not guaranteed.
2. Refer to *Table 47: Magnetic data rate configuration*.

b. The product is factory calibrated at 2.5 V.

2.3 Electrical characteristics

@ Vdd = 2.5 V, T = 25 °C unless otherwise noted.

Table 5. Electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.(1)	Max.	Unit
Vdd	Supply voltage		2.16		3.6	V
Vdd_IO	Module power supply for I/O		1.71	1.8	Vdd+0.1	
Idd	eCompass(2) current consumption in normal mode(3)	LR setting CTRL5 (M_RES [1,0]) = 00b, see *Table 45*		300		µA
IddSL	Current consumption in power-down mode(4)			1		µA
Top	Operating temperature range		-40		+85	°C

1. Typical specifications are not guaranteed.
2. eCompass: accelerometer and magnetic sensor.
3. Magnetic sensor setting ODR = 6.25 Hz, accelerometer sensor ODR = 50 Hz and magnetic high-resolution setting.
4. Linear accelerometer and magnetic sensor in power-down mode.

2.4 Communication interface characteristics

2.4.1 SPI - serial peripheral interface

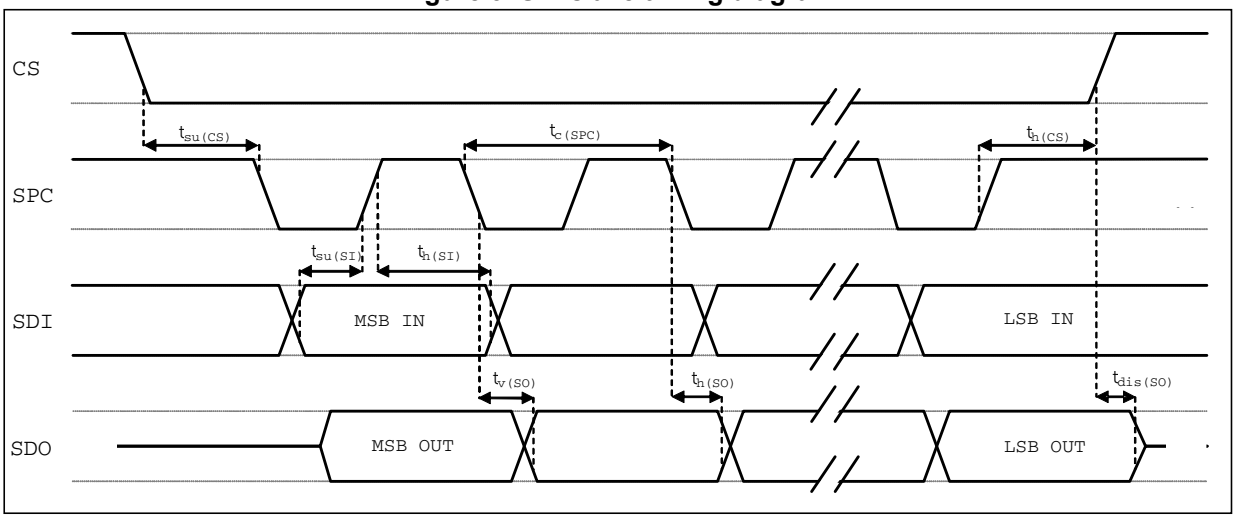
Subject to general operating conditions for Vdd and Top.

Table 6. SPI slave timing values

Symbol	Parameter	Value (1)		Unit
		Min.	Max.	
$t_{c(SPC)}$	SPI clock cycle	100		ns
$f_{c(SPC)}$	SPI clock frequency		10	MHz
$t_{su(CS)}$	CS setup time	5		ns
$t_{h(CS)}$	CS hold time	20		
$t_{su(SI)}$	SDI input setup time	5		
$t_{h(SI)}$	SDI input hold time	15		
$t_{v(SO)}$	SDO valid output time		50	
$t_{h(SO)}$	SDO output hold time	5		
$t_{dis(SO)}$	SDO output disable time		50	

1. Values are guaranteed at 10 MHz clock frequency for SPI with both 4 and 3 wires, based on characterization results, not tested in production.

Figure 3. SPI slave timing diagram



Note: Measurement points are done at 0.2·Vdd_IO and 0.8·Vdd_IO for both input and output ports.

2.4.2 Sensor I²C - inter-IC control interface

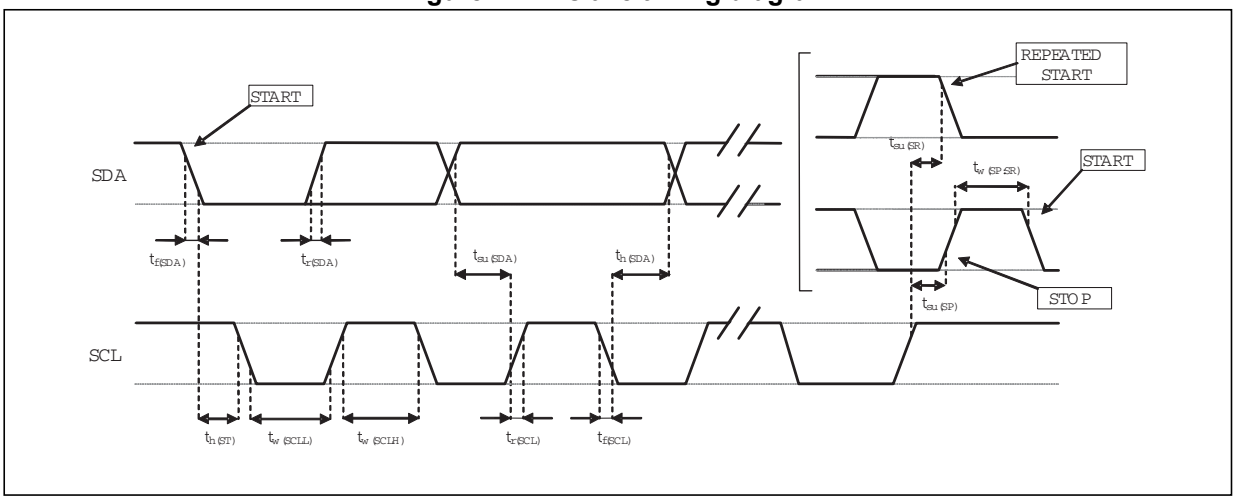
Subject to general operating conditions for Vdd and Top.

Table 7. I²C slave timing values

Symbol	Parameter	I²C standard mode (1)		I²C fast mode (1)		Unit
		Min.	Max.	Min.	Max.	
$f_{(SCL)}$	SCL clock frequency	0	100	0	400	kHz
$t_{w(SCLL)}$	SCL clock low time	4.7		1.3		µs
$t_{w(SCLH)}$	SCL clock high time	4.0		0.6		
$t_{su(SDA)}$	SDA setup time	250		100		ns
$t_{h(SDA)}$	SDA data hold time	0	3.45	0	0.9	µs
$t_{r(SDA)}$ $t_{r(SCL)}$	SDA and SCL rise time		1000	$20 + 0.1C_b$ (2)	300	ns
$t_{f(SDA)}$ $t_{f(SCL)}$	SDA and SCL fall time		300	$20 + 0.1C_b$ (2)	300	
$t_{h(ST)}$	START condition hold time	4		0.6		µs
$t_{su(SR)}$	Repeated START condition setup time	4.7		0.6		
$t_{su(SP)}$	STOP condition setup time	4		0.6		
$t_{w(SP:SR)}$	Bus free time between STOP and START condition	4.7		1.3		

1. Data based on standard I²C protocol requirement, not tested in production.
2. C_b = total capacitance of one bus line, in pF.

Figure 4. I²C slave timing diagram



Note: Measurement points are done at 0.2·Vdd_IO and 0.8·Vdd_IO for both ports.

2.5 Absolute maximum ratings

Stresses above those listed as “absolute maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 8. Absolute maximum ratings

Symbol	Ratings	Maximum value	Unit
Vdd	Supply voltage	-0.3 to 4.8	V
Vdd_IO	I/O pins supply voltage	-0.3 to 4.8	V
Vin	Input voltage on any control pin (SCL/SPC, SDA/SDI/SDO, SDO/SA0, CS)	-0.3 to Vdd_IO +0.3	V
A_{POW}	Acceleration (any axis, powered, Vdd = 2.5 V)	3,000 for 0.5 ms	*g*
		10,000 for 0.1 ms	*g*
A_{UNP}	Acceleration (any axis, unpowered)	3,000 for 0.5 ms	*g*
		10,000 for 0.1 ms	*g*
T_{OP}	Operating temperature range	-40 to +85	°C
T_{STG}	Storage temperature range	-40 to +125	°C
ESD	Electrostatic discharge protection	2 (HBM)	kV

Note: Supply voltage on any pin should never exceed 4.8 V.

This device is sensitive to mechanical shock, improper handling can cause permanent damage to the part.

This device is sensitive to electrostatic discharge (ESD), improper handling can cause permanent damage to the part.

3 Terminology

3.1 Set/reset pulse

The set/reset pulse is an automatic operation performed before each magnetic acquisition cycle to recover the initial magnetization state of the sensor and therefore the linearity of the sensor itself.

3.2 Sensitivity

3.2.1 Linear acceleration sensor sensitivity

Sensitivity describes the gain of the sensor and can be determined, for example, by applying 1 *g* acceleration to it. As the sensor can measure DC accelerations this can be done easily by pointing the axis of interest towards the center of the Earth, noting the output value, rotating the sensor by 180 degrees (pointing to the sky) and noting the output value again. By doing so, ±1 *g* acceleration is applied to the sensor. Subtracting the larger output value from the smaller one, and dividing the result by 2, leads to the actual sensitivity of the sensor. This value changes very little over temperature and time. The sensitivity tolerance describes the range of sensitivities of a large population of sensors.

3.2.2 Magnetic sensor sensitivity

Sensitivity describes the gain of the sensor and can be determined, for example, by applying a magnetic field of 1 *gauss* to it.

3.3 Zero-*g* level

Zero-*g* level offset (TyOff) describes the deviation of an actual output signal from the ideal output signal if no acceleration is present. A sensor in a steady-state on a horizontal surface measures 0 *g* on the X-axis and 0 *g* on the Y-axis, whereas the Z-axis measures 1 *g*. The output is ideally in the middle of the dynamic range of the sensor (content of OUT registers 00h, data expressed as two's complement). A deviation from the ideal value in this case is called Zero-*g* offset. Offset is, to some extent, a result of stress to MEMS sensor and therefore the offset can slightly change after mounting the sensor onto a printed circuit board or exposing it to extensive mechanical stress. Offset changes little over temperature, see "Zero-*g* level change vs. temperature". The Zero-*g* level tolerance (TyOff) describes the standard deviation of the range of Zero-*g* levels of a population of sensors.

3.4 Zero-*gauss* level

Zero-*g*auss level offset describes the deviation of an actual output signal from the ideal output if no magnetic field is present. Thanks to the set/reset pulse and to the magnetic sensor read-out chain, the offset is dynamically cancelled. The Zero-*g*auss level does not show any dependencies on temperature and power supply.

4 Functionality

4.1 Self-test

The self-test allows checking the linear acceleration sensor functionality without moving the sensor. The self-test function is off when the self-test bit (AST) is programmed to ‘0‘. When the self-test bit is programmed to ‘1’, an actuation force is applied to the sensor, simulating a definite input acceleration. In this case the sensor outputs exhibit a change in their DC levels which are related to the selected full scale through the device sensitivity. When the self-test is activated, the device output level is given by the algebraic sum of the signals produced by the acceleration acting on the sensor and by the electrostatic test-force. If the output signals change within the amplitude specified inside *Section 2.1*, then the sensor is working properly and the parameters of the interface chip are within the defined specifications.

4.2 Temperature sensor

The LSM303D features an internal temperature sensor. Temperature data can be enabled by setting the TEMP_EN bit on the *CTRL5 (24h)* register to 1.

Both the TEMP_OUT_H and TEMP_OUT_L registers must be read.

Temperature data is stored inside *TEMP_OUT_L (05h), TEMP_OUT_H (06h)* as two’s complement data in 12-bit format, right-justified.

The output data rate of the temperature sensor is set by M_ODR [2:0] in *CTRL5 (24h)* and is equal to the magnetic sensor output data rate.

4.3 FIFO

The LSM303D embeds an acceleration data FIFO for each of the three output channels, X, Y and Z. This allows consistent power saving for the system, as the host processor does not need to continuously poll data from the sensor, but it can wake up only when needed and burst the significant data out from the FIFO. This buffer can work according to four different modes: Bypass mode, FIFO mode, Stream mode and Stream-to-FIFO mode. Each mode is selected by the FIFO_MODE bits. Programmable threshold level, FIFO_empty or FIFO_Full events can be enabled to generate dedicated interrupts on the INT 1 or INT 2 pin.

Bypass mode

In Bypass mode, the FIFO is not operational and for this reason it remains empty. As described in *Figure 5*, for each channel only the first address is used. The remaining FIFO slots are empty.

FIFO mode

In FIFO mode, data from X, Y and Z channels are stored in the FIFO. A FIFO threshold interrupt can be enabled in order to be raised when the FIFO is filled to the level specified by the internal register. The FIFO continues filling until it is full. When full, the FIFO stops collecting data from the input channels.

Stream mode

In Stream mode, data from X, Y and Z measurements are stored in the FIFO. A FIFO threshold interrupt can be enabled and set as in FIFO mode.The FIFO continues filling until it's full. When full, the FIFO discards the older data as the new arrive.

Stream-to-FIFO mode

In Stream-to-FIFO mode, data from X, Y and Z measurements are stored in the FIFO. A FIFO threshold interrupt can be enabled in order to be raised when the FIFO is filled to the level specified by the internal register. The FIFO continues filling until it's full. When full, the FIFO discards the older data as the new arrive. Once a trigger event occurs, the FIFO starts operating in FIFO mode.

Bypass-to-Stream mode

In Bypass-to-Stream mode, the FIFO starts operating in Bypass mode and once a trigger event occurs (related to *IG_CFG1 (30h)* register events), the FIFO starts operating in Stream mode.

Retrieving data from FIFO

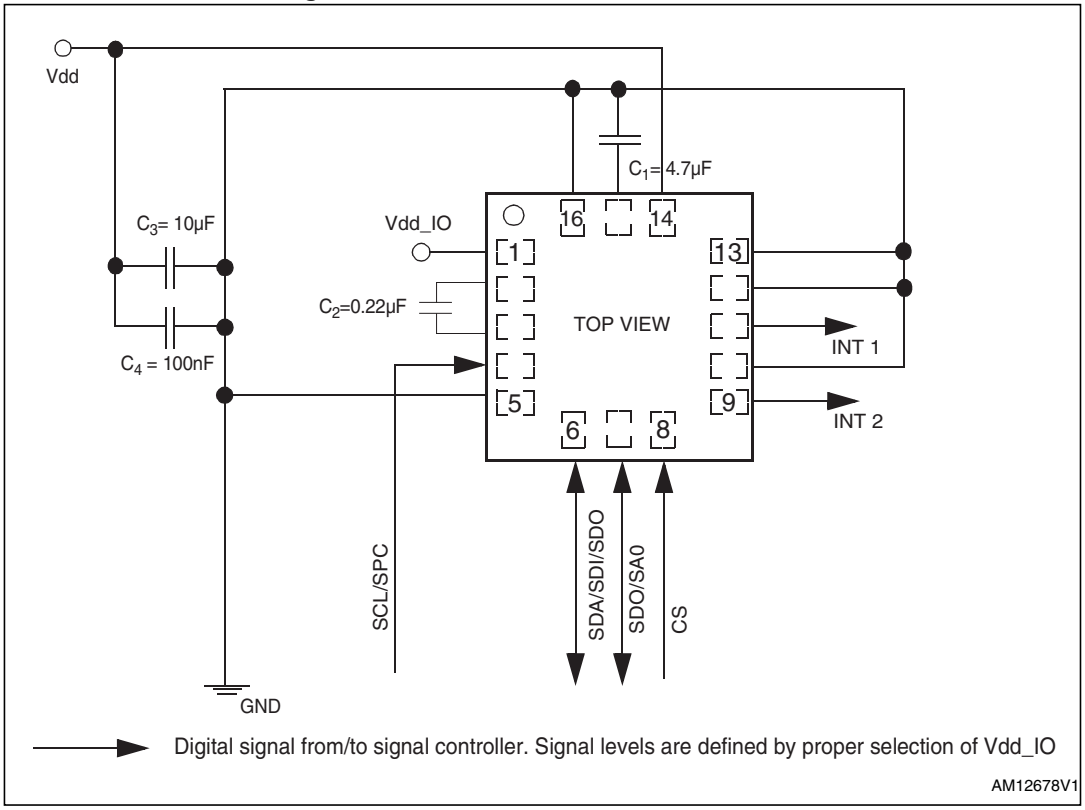
FIFO data is read from the OUT_X_A, OUT_Y_A and OUT_Z_A registers. When the FIFO is in Stream, Stream-to-FIFO, Bypass-to-Stream or FIFO mode, a read operation to the OUT_X_A, OUT_Y_A or OUT_Z_A registers provides the data stored in the FIFO. Each time data is read from the FIFO, the oldest X, Y and Z data are placed in the OUT_X_A, OUT_Y_A and OUT_Z_A registers and both single read and read_burst operations can be used.

4.4 Factory calibration

The IC interface is factory calibrated. The trim values are stored inside the device in nonvolatile memory. Anytime the device is turned on, the trimming parameters are downloaded into the registers to be used during normal operation. This allows the user to use the device without further calibration.

5 Application hints

Figure 5. LSM303D electrical connections



5.1 External capacitors

The C_1 and C_2 external capacitors should be low SR value ceramic type construction (typ. recommended value 200 mΩ). Reservoir capacitor C_1 is nominally 4.7 µF in capacitance, with the set/reset capacitor C_2 nominally 0.22 µF in capacitance.

The device core is supplied through the Vdd line. Power supply decoupling capacitors (C_4 = 100 nF ceramic, C_3 = 10 µF Al) should be placed as near as possible to the supply pin of the device (common design practice). All the voltage and ground supplies must be present at the same time to have proper behavior of the IC (refer to *Figure 5*).

The functionality of the device and the measured acceleration/magnetic field data is selectable and accessible through the I^2C/SPI interfaces.

The functions, the threshold and the timing of the two interrupt pins (INT 1 and INT 2) can be completely programmed by the user through the I^2C/SPI interfaces.

5.2 Pull-up resistors

If an I^2C interface is used, pull-up resistors (recommended value 10 kΩ) must be placed on the two I^2C bus lines.

5.3 Digital Interface power supply

This digital interface, dedicated to the linear acceleration and to the magnetic field signal, is capable of operating with a standard power supply (Vdd) or using a dedicated power supply (Vdd_IO).

5.4 Soldering information

The LGA package is compliant with ECOPACK®, RoHS and “Green” standards.
It is qualified for soldering heat resistance according to JEDEC J-STD-020.

Leave “Pin 1 Indicator” unconnected during soldering.

Land pattern and soldering recommendations are available at www.st.com/mems.

5.5 High-current wiring effects

High current in wiring and printed circuit traces can be the cause of errors in magnetic field measurements for compassing.

Conductor-generated magnetic fields add to the Earth’s magnetic field creating errors in compass heading computations.

Keep currents higher than 10 mA a few millimeters further away from the sensor IC.

6 Digital interfaces

The registers embedded in the LSM303D may be accessed through both the I^2C and SPI serial interfaces. The latter may be SW-configured to operate either in 3-wire or 4-wire interface mode.

The serial interfaces are mapped onto the same pins. To select/exploit the I^2C interface, the CS line must be tied high (i.e connected to Vdd_IO).

Table 9. Serial interface pin description

Pin name	Pin description
CS	I^2C/SPI mode selection (1: SPI idle mode / I^2C communication enabled; 0: SPI communication mode / I^2C disabled)
SCL/SPC	I^2C serial clock (SCL) SPI serial port clock (SPC)
SDA/SDI/SDO	I^2C serial data (SDA) SPI serial data input (SDI) 3-wire interface serial data output (SDO)
SDO/SA0	SPI serial data output (SDO) I^2C less significant bit of the device address (SA0)

6.1 I^2C serial interface

The LSM303D I^2C is a bus slave. The I^2C is employed to write data into registers whose content can also be read back.

The relevant I^2C terminology is given in the table below.

Table 10. I^2C terminology

Term	Description
Transmitter	The device which sends data to the bus
Receiver	The device which receives data from the bus
Master	The device which initiates a transfer, generates clock signals and terminates a transfer
Slave	The device addressed by the master

There are two signals associated with the I^2C bus: the serial clock line (SCL) and the serial data line (SDA). The latter is a bi-directional line used for sending and receiving the data to/from the interface. Both lines must be connected to Vdd_IO through external pull-up resistors. When the bus is free, both lines are high.

The I^2C interface is compliant with fast mode (400 kHz) I^2C standards as well as with normal mode.

6.1.1 I²C operation

The transaction on the bus is started through a START (ST) signal. A START condition is defined as a high-to-low transition on the data line while the SCL line is held high. After this has been transmitted by the master, the bus is considered busy. The next byte of data transmitted after the START condition contains the address of the slave in the first 7 bits and the eighth bit tells whether the master is receiving data from the slave or transmitting data to the slave. When an address is sent, each device in the system compares the first seven bits after a START condition with its address. If they match, the device considers itself addressed by the master.

The slave address (SAD) associated to the LSM303D is 00111xxb, whereas the xx bits are modified by the SDO/SA0 pin in order to modify the device address. If the SDO/SA0 pin is connected to the voltage supply, the address is 0011101b, otherwise, if the SDO/SA0 pin is connected to ground, the address is 0011110b. This solution permits the connection and addressing of two different accelerometers to the same I²C lines.

Data transfer with acknowledge is mandatory. The transmitter must release the SDA line during the acknowledge pulse. The receiver must then pull the data line low so that it remains stable low during the high period of the acknowledge clock pulse. A receiver which has been addressed is obliged to generate an acknowledge after each byte of data received.

The I²C embedded in the LSM303D behaves as a slave device and the following protocol must be adhered to. After the START condition (ST) a slave address is sent, once a slave acknowledge (SAK) has been returned, an 8-bit sub-address is transmitted: the 7 LSb represent the actual register address while the MSb enables address auto-increment. If the MSb of the SUB field is 1, the SUB (register address) is automatically incremented to allow multiple data read/write.

The slave address is completed with a read/write bit. If the bit is ‘1’ (read), a repeated START (SR) condition must be issued after the two sub-address bytes; if the bit is ‘0’ (write) the master transmits to the slave with direction unchanged. *Table 11* explains how the SAD+read/write bit pattern is composed, listing all the possible configurations.

Table 11. SAD+read/write patterns

Command	SDO/SA0 pin	SAD[6:2]	SAD[1:0]	R/W	SAD+R/W
Read	0	00111	10	1	3D
Write	0	00111	10	0	3C
Read	1	00111	01	1	3B
Write	1	00111	01	0	3A

Table 12. Transfer when master is writing one byte to slave

Master	ST	SAD + W		SUB		DATA		SP
Slave			SAK		SAK		SAK	

Table 13. Transfer when master is writing multiple bytes to slave

Master	ST	SAD + W		SUB		DATA		DATA		SP
Slave			SAK		SAK		SAK		SAK	

Table 14. Transfer when master is receiving (reading) one byte of data from slave

Master	ST	SAD + W		SUB		SR	SAD + R			NMAK	SP
Slave			SAK		SAK			SAK	DATA		

Table 15. Transfer when master is receiving (reading) multiple bytes of data from slave

Master	ST	SAD+W		SUB		SR	SAD+R			MAK		MAK		NMAK	SP
Slave			SAK		SAK			SAK	DATA		DATA		DATA		

Data is transmitted in byte format (DATA). Each data transfer contains 8 bits. The number of bytes sent per transfer is unlimited. Data is transferred with the most significant bit (MSb) first. If a receiver cannot receive another complete byte of data until it has performed some other function, it can hold the clock line, SCL, low to force the transmitter into a wait state. Data transfer only continues when the receiver is ready for another byte and releases the data line. If a slave receiver does not acknowledge the slave address (i.e. it is not able to receive because it is performing some real-time function) the data line must be left high by the slave. The master can then abort the transfer. A low-to-high transition on the SDA line while the SCL line is high is defined as a STOP condition. Each data transfer must be terminated by the generation of a STOP (SP) condition.

In order to read multiple bytes, it is necessary to assert the most significant bit of the sub-address field. In other words, SUB(7) must be equal to ‘1’ while SUB(6-0) represents the address of the first register to be read.

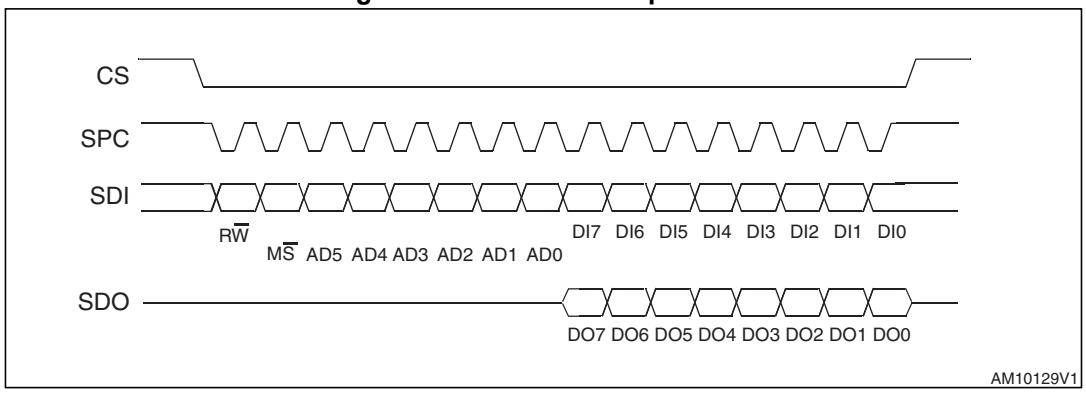
In the communication format presented, MAK is master acknowledge and NMAK is no master acknowledge.

6.2 SPI bus interface

The SPI is a bus slave. The SPI allows writing and reading the registers of the device.

The serial interface interacts with the outside world through 4 wires: **CS**, **SPC**, **SDI** and **SDO**.

Figure 6. Read and write protocol



CS is the serial port enable and is controlled by the SPI master. It goes low at the start of the transmission and goes back high at the end. **SPC** is the serial port clock and it is controlled by the SPI master. It is stopped high when **CS** is high (no transmission). **SDI** and **SDO** are respectively the serial port data input and output. These lines are driven at the falling edge of **SPC** and should be captured at the rising edge of **SPC**.

Both the read register and write register commands are completed in 16 clock pulses or in multiples of 8 in the case of multiple read/write bytes. Bit duration is the time between two falling edges of **SPC**. The first bit (bit 0) starts at the first falling edge of **SPC** after the falling edge of **CS** while the last bit (bit 15, bit 23, ...) starts at the last falling edge of **SPC** just before the rising edge of **CS**.

bit 0: R$\overline{W}$ bit. When 0, the data DI(7:0) is written to the device. When 1, the data DO(7:0) from the device is read. In the latter case the chip drives **SDO** at the start of bit 8.

bit 1: M$\overline{S}$ bit. When 0, the address remains unchanged in multiple read/write commands. When 1, the address is auto-incremented in multiple read/write commands.

bit 2-7: address AD(5:0). This is the address field of the indexed register.

bit 8-15: data DI(7:0) (write mode). This is the data that is written to the device (MSb first).

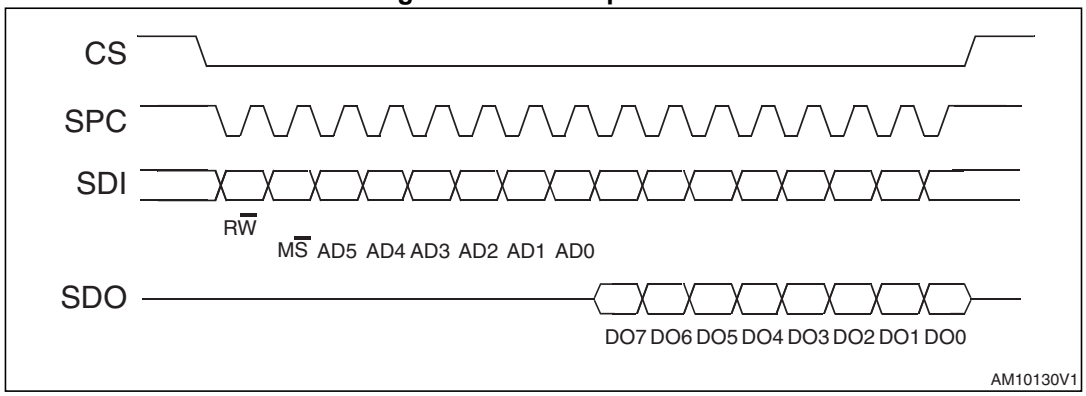
bit 8-15: data DO(7:0) (read mode). This is the data that is read from the device (MSb first).

In multiple read/write commands, further blocks of 8 clock periods are added. When the M$\overline{S}$ bit is 0, the address used to read/write data remains the same for every block. When the M$\overline{S}$ bit is 1, the address used to read/write data is incremented at every block.

The function and the behavior of **SDI** and **SDO** remain unchanged.

6.2.1 SPI read

Figure 7. SPI read protocol



The SPI read command is performed with 16 clock pulses. The multiple byte read command is performed by adding blocks of 8 clock pulses to the previous one.

bit 0: READ bit. The value is 1.

bit 1: MS bit. When 0, does not increment the address; when 1, increments the address in multiple reads.

bit 2-7: address AD(5:0). This is the address field of the indexed register.

bit 8-15: data DO(7:0) (read mode). This is the data that is read from the device (MSb first).

bit 16-... : data DO(...-8). Further data in multiple byte reads.

Figure 8. Multiple byte SPI read protocol (2-byte example)