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Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
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LSM320DL

Linear sensor module
3D accelerometer sensor and 2D gyroscope sensor

Preliminary data

Features

- Analog supply voltage 2.4 V to 3.6 V
- Digital supply voltage IOs, 1.8 V
- Low power mode
- Power-down mode
- 3 independent acceleration channels and 2 angular rate channels (pitch and yaw)
- ±2g/±4g/±8/±16g dynamically selectable full-scale
- ±250/±500/±2000 dps dynamically selectable full-scale
- Embedded temperature sensor
- SPI/I^2C serial interface (16-bit data output)
- Programmable interrupt generator for free-fall and motion detection
- ECOPACK® RoHS and “Green” compliant

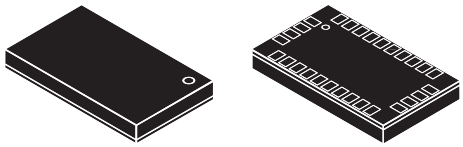
Applications

- GPS navigation systems
- Impact recognition and logging
- Gaming and virtual reality input devices
- Motion activated functions
- Intelligent power saving for handheld devices
- Vibration monitoring and compensation
- Free-fall detection
- 6D orientation detection

Description

The LSM320DL is a system-in-package featuring a 3D digital accelerometer and a 2D digital gyroscope.

The ST modules family uses a robust and mature manufacturing process already used for the production of micromachined accelerometers.



LGA 28L 7.5 x 4.4 x 1.1 mm

The various sensing elements are manufactured using specialized micromachining processes, while the IC interfaces are realized using a CMOS technology that allows to design a dedicated circuit which is trimmed to better match the sensing element characteristics.

LSM320DL has a dynamic user selectable full-scale acceleration range of ±2*g*/±4*g*/±8/±16*g* and angular rate of ±250/±500/±2000 deg/sec.

The accelerometer and gyroscope sensors can be either activated or put in low power/power-down mode separately for application optimized power saving.

The LSM320DL is available in a plastic land grid array (LGA) package.

Several years ago ST successfully pioneered the use of this package for accelerometers. Today, ST has the widest manufacturing capability and strongest expertise in the world for production of sensors in a plastic LGA package.

Table 1. Device summary

Order codes	Temperature range [°C]	Package	Packing
LSM320DL	-40 to +85	LGA 28L	Tray
LSM320DLTR			Tape and reel

Contents

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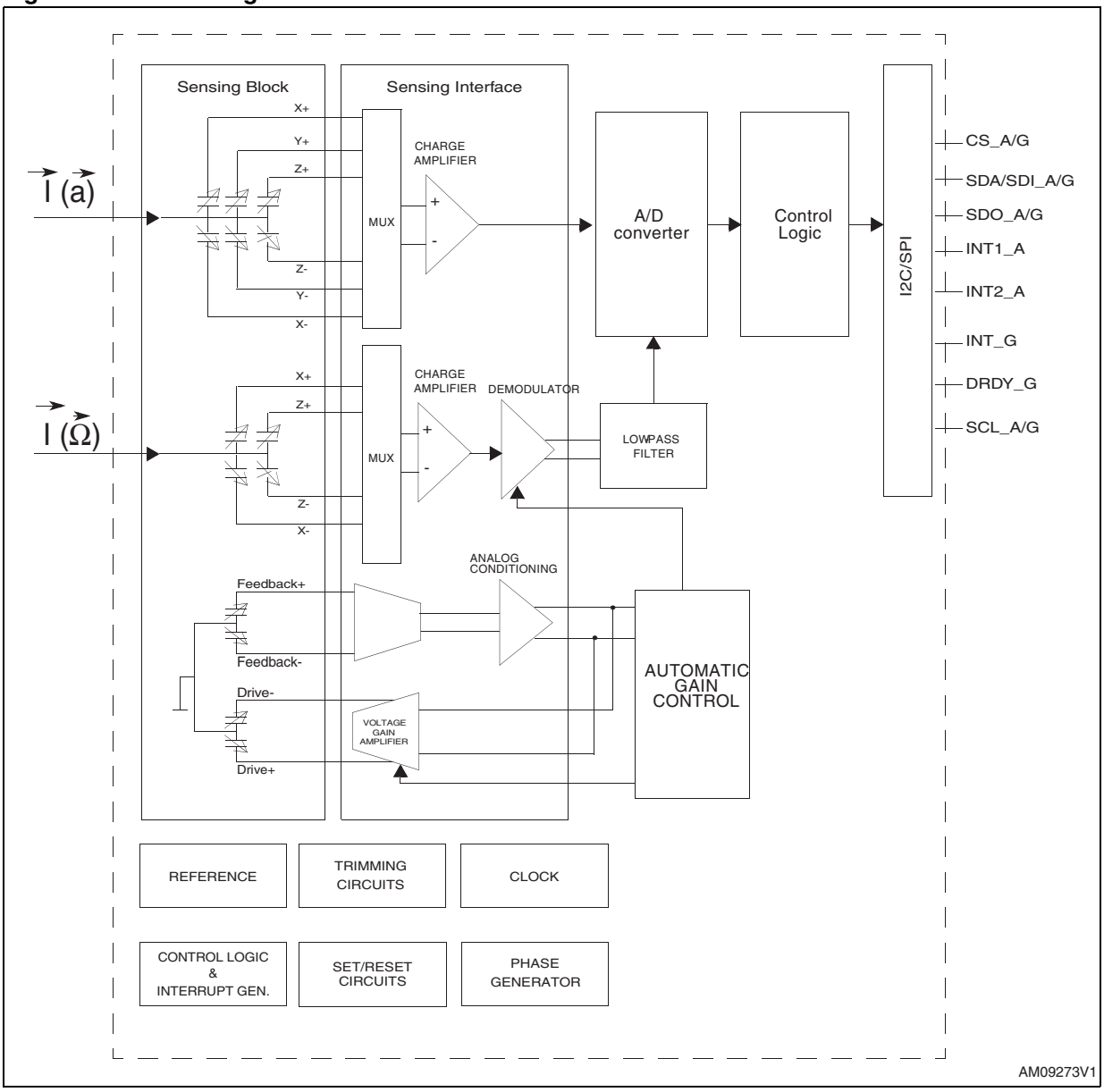
1 Block diagram and pin description

1.1 Block diagram

Figure 1. Block diagram



1.2 Pin description

Figure 2. Pin connection

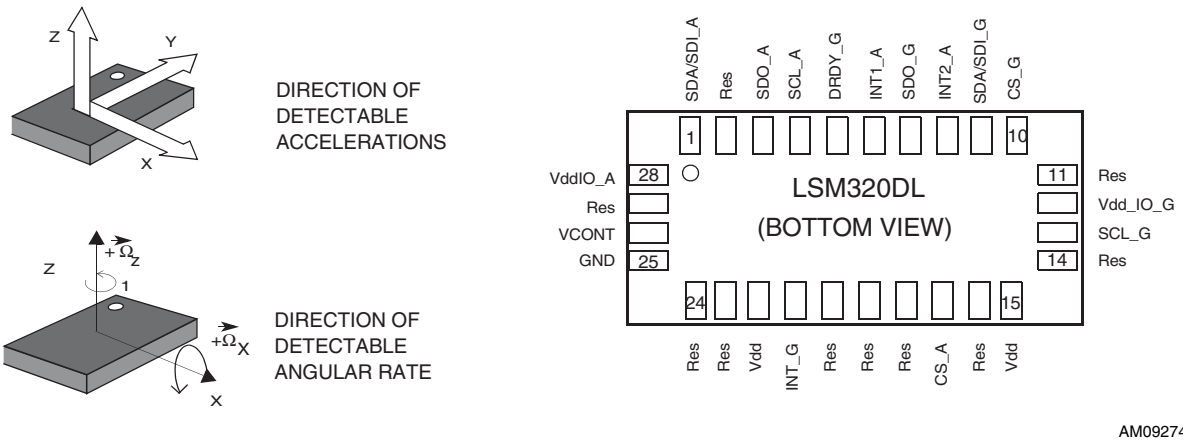


Table 2. Pin description

Pin#	Name	Function
1	SDA/SDI_A	Accelerometer: I^2C serial data (SDA) SPI serial data input (SDI) 3-wire interface serial data output (SDO)
2	Res	Reserved connect to GND
3	SDO_A	Accelerometer: SPI serial data output (SDO) I^2C least significant bit of the device address (SA0)
4	SCL_A	Accelerometer: I^2C serial clock (SCL) SPI serial port clock (SPC)
5	DRDY_G	Gyroscope data ready
6	INT1_A	Accelerometer interrupt signal
7	SDO_G	Gyroscope: SPI serial data output (SDO) I^2C least significant bit of the device address (SA0)
8	INT2_A	Accelerometer interrupt signal
9	SDA/SDI_G	Gyroscope: I^2C serial data (SDA) SPI serial data input (SDI) 3-wire interface serial data output (SDO)

Table 2. Pin description (continued)

Pin#	Name	Function
10	CS_G	Gyroscope: SPI enable I^2C/SPI mode selection (1: SPI idle mode / I^2C communication enabled; 0: SPI communication mode / I^2C disabled)
11	Res	Reserved connect to GND
12	VddIO_G	Gyroscope power supply for IO pins
13	SCL_G	Gyroscope: I^2C serial clock (SCL) SPI serial port clock (SPC)
14	Res	Reserved connect to GND
15	Vdd	Power supply
16	Res	Reserved connect to GND
17	CS_A	Accelerometer: SPI enable I^2C/SPI mode selection (1: SPI idle mode / I^2C communication enabled; 0: SPI communication mode / I^2C disabled)
18	Res	Reserved connect to GND
19	Res	Reserved connect to GND
20	Res	Reserved connect to GND
21	INT_G	Gyroscope interrupt signal
22	Vdd	Power supply
23	Res	Reserved connect to GND
24	Res	Reserved connect to GND
25	GND	0 V power supply
26	VCONT	PLL filter connection
27	Res	Reserved connect to GND
28	VddIO_A	Accelerometer power supply for IO pins

2 Module specifications

2.1 Mechanical characteristics

@ Vdd = 3V, T = 25 °C unless otherwise noted[a].

Table 3. Mechanical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.[1]	Max.	Unit
LA_FS	Linear acceleration measurement range[2]	FS bit set to 00		±2.0		*g*
		FS bit set to 01		±4.0		
		FS bit set to 10		±8.0		
		FS bit set to 11		±16.0		
G_FS	Angular rate measurement range[2]	FS bit set to 00		±250		dps
		FS bit set to 01		±500		
		FS bit set to 10		±2000		
LA_So	Linear acceleration sensitivity	FS bit set to 00		1		m*g*/digit
		FS bit set to 01		2		
		FS bit set to 10		4		
		FS bit set to 11		12		
G_So	Angular rate sensitivity	FS bit set to 00		8.75		mdps/ digit
		FS bit set to 01		17.5		
		FS bit set to 10		70		
LA_So	Linear acceleration sensitivity change vs. temperature	FS bit set to 00		±0.05		%/°C
G_So	Angular rate sensitivity change vs. temperature	From -40 to +85 °C		±2		%
LA_TyOff	Typical Zero-*g* level offset accuracy[3]	FS bit set to 00		±60		m*g*
G_TyOff	Typical zero-rate level[4]	FS bit set to 00		10		LSb
LA_TCOff	Zero-*g* level change vs. temperature	Max. delta from 25 °C		±0.5		m*g*/°C
G_TCOff	Zero-rate level change vs. temperature	FS bit set to 00 from -40 to +85 °C		±0.03		dps/°C
An	Acceleration noise density	FS bit set to 00 Normal mode, ODR bit set to 1001		220		µ*g*/$\sqrt{Hz}$
Rn	Rate noise density	FS bit set to 00		0.03		°/s/$\sqrt{Hz}$
Top	Operating temperature range		-40		+85	°C

a. The product is factory calibrated at 3 V. The operational power supply range is from 2.4 V to 3.6 V.

1. Typical specifications are not guaranteed.
2. Verified by wafer level test and measurement of initial offset and sensitivity.
3. Typical Zero-*g* level offset value after MSL3 preconditioning.
4. Offset can be eliminated by enabling the built-in high pass filter.

2.2 Electrical characteristics

@ Vdd = 3 V, T = 25 °C unless otherwise noted.

Table 4. Electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.(1)	Max.	Unit
Vdd	Supply voltage		2.4		3.6	V
Vdd_IO	Power supply for I/O		1.71		Vdd+0.1	V
LA_Idd	LA current consumption in normal mode	ODR = 50Hz		11		µA
		ODR = 1Hz		2		
LA_IddLowP	LA current consumption in low power mode	ODR = 50Hz		6		µA
LA_IddPdn	LA current consumption in power-down mode	T = 25°C		0.5		µA
G_Idd	AR current consumption in normal mode			6		mA
G_IddSL	Supply current in sleep mode(2)			1.5		mA
G_IddPdn	AR current consumption in power-down mode	T = 25 °C		5		µA
VIH	Digital high level input voltage		0.8*Vdd_IO			V
VIL	Digital low level input voltage				0.2*Vdd_IO	V
VOH	High level output voltage		0.9*Vdd_IO			V
VOL	Low level output voltage				0.1*Vdd_IO	V
Top	Operating temperature range		-40		+85	°C

1. Typical specifications are not guaranteed.
2. Sleep mode introduces a faster turn-on time compared to power-down mode.

2.3 Temperature sensor characteristics

@ Vdd =3.0 V, T= 25 °C, unless otherwise noted.[b]

Table 5. Temperature sensor characteristics

Symbol	Parameter	Test condition	Min.	Typ.[1]	Max.	Unit
TSDr	Temperature sensor output change vs. temperature	-		-1		°C/digit
TODR	Temperature refresh rate			1		Hz
Top	Operating temperature range		-40		+85	°C

1. Typical specifications are not guaranteed.

b. The product is factory calibrated at 3.0 V.

2.4 Communication interface characteristics

2.4.1 SPI - serial peripheral interface

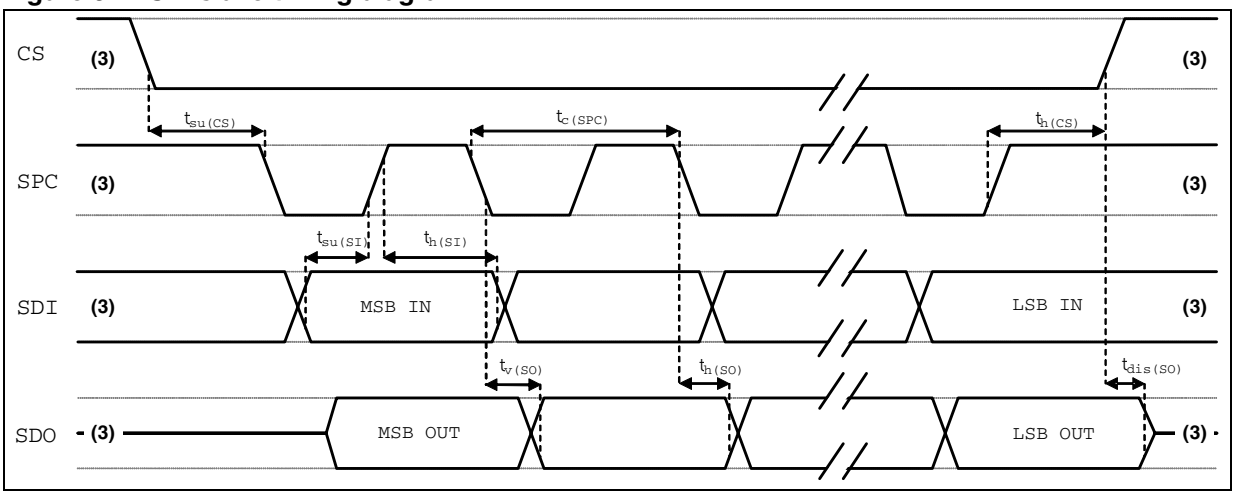
Subject to general operating conditions for Vdd and Top.

Table 6. SPI slave timing values

Symbol	Parameter	Value (1)		Unit
		Min.	Max.	
tc(SPC)	SPI clock cycle	100		ns
fc(SPC)	SPI clock frequency		10	MHz
tsu(CS)	CS setup time	6		ns
th(CS)	CS hold time	8		
tsu(SI)	SDI input setup time	5		
th(SI)	SDI input hold time	15		
tv(SO)	SDO valid output time		50	
th(SO)	SDO output hold time	9		
tdis(SO)	SDO output disable time		50	

1. Values are guaranteed at 10 MHz clock frequency for SPI with both 4 and 3 wires, based on characterization results, not tested in production.

Figure 3. SPI slave timing diagram (c)



3. When no communication is on-going, data on CS, SPC, SDI, and SDO are driven by internal pull-up resistors.

c. Measurement points are done at 0.2·Vdd_IO and 0.8·Vdd_IO, for both input and output ports.

2.4.2 I²C - inter IC control interface

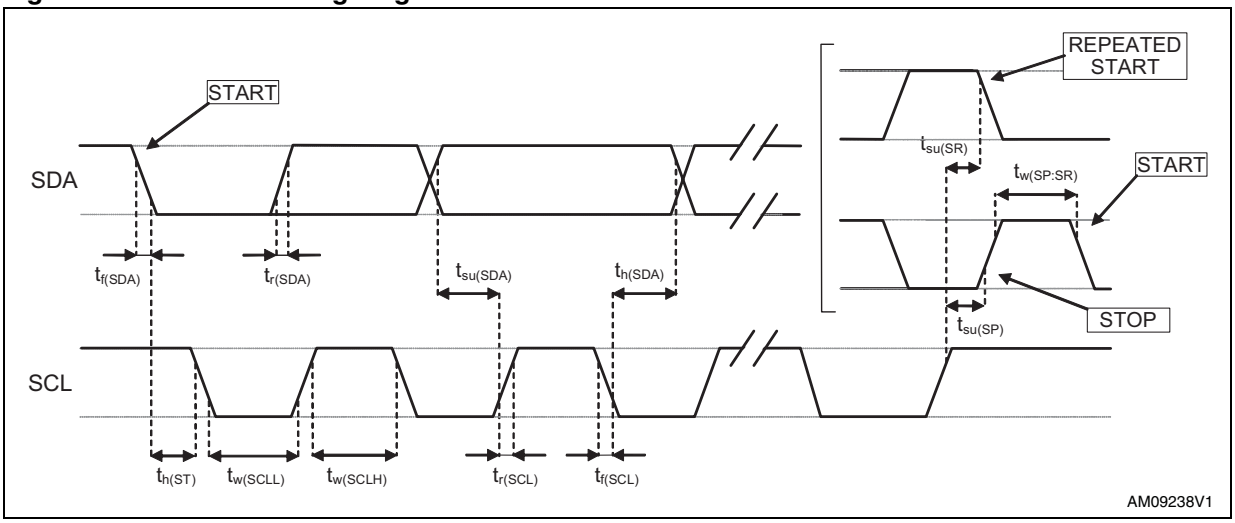
Subject to general operating conditions for Vdd and Top.

Table 7. I²C slave timing values

Symbol	Parameter	I²C standard mode(1)		I²C fast mode (1)		Unit
		Min.	Max.	Min.	Max.	
$f_{(SCL)}$	SCL clock frequency	0	100	0	400	KHz
$t_{w(SCLL)}$	SCL clock low time	4.7		1.3		µs
$t_{w(SCLH)}$	SCL clock high time	4.0		0.6		
$t_{su(SDA)}$	SDA setup time	250		100		ns
$t_{h(SDA)}$	SDA data hold time	0,01	3.45	0	0.9	µs
$t_{r(SDA)}$ $t_{r(SCL)}$	SDA and SCL rise time		1000	$20 + 0.1C_b$ (2)	300	ns
$t_{f(SDA)}$ $t_{f(SCL)}$	SDA and SCL fall time		300	$20 + 0.1C_b$ (2)	300	
$t_{h(ST)}$	START condition hold time	4		0.6		µs
$t_{su(SR)}$	Repeated START condition setup time	4.7		0.6		
$t_{su(SP)}$	STOP condition setup time	4		0.6		
$t_{w(SP:SR)}$	Bus free time between STOP and START condition	4.7		1.3		

1. Data based on standard I²C protocol requirement, not tested in production.
2. Cb = total capacitance of one bus line, in pF.

Figure 4. I²C slave timing diagram (d)



d. Measurement points are done at 0.2·Vdd_IO and 0.8·Vdd_IO, for both ports.

2.5 Absolute maximum ratings

Stresses above those listed as “absolute maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 8. Absolute maximum ratings

Symbol	Ratings	Maximum value	Unit
Vdd	Supply voltage	-0.3 to 4.8	V
Vdd_IO	I/O pins supply voltage	-0.3 to 4.8	V
Vin	Input voltage on any control pin (SCL, SDA/SDI)	-0.3 to Vdd_IO +0.3	V
A_{POW}	Acceleration (any axis, powered, Vdd = 3 V)	3000 *g* for 0.5 ms	
		10000 *g* for 0.1 ms	
A_{UNP}	Acceleration (any axis, unpowered)	3000 *g* for 0.5 ms	
		10000 *g* for 0.1 ms	
T_{OP}	Operating temperature range	-40 to +85	°C
T_{STG}	Storage temperature range	-40 to +125	°C
ESD	Electrostatic discharge protection	2 (HBM)	kV

This is a mechanical shock sensitive device, improper handling can cause permanent damage to the part

This is an ESD sensitive device, improper handling can cause permanent damage to the part

2.6 Terminology

2.6.1 Sensitivity

Linear acceleration sensitivity can be determined, for example, by applying 1 *g* acceleration to the device. As the sensor can measure DC accelerations this can be done easily by pointing the axis of interest towards the center of the Earth, noting the output value, rotating the sensor by 180 degrees (pointing to the sky) and noting the output value again. By doing so, ±1 *g* acceleration is applied to the sensor. Subtracting the larger output value from the smaller one, and dividing the result by 2, leads to the actual sensitivity of the sensor. This value changes very little over temperature and also very little over time. The sensitivity tolerance describes the range of sensitivities of a large population of sensors.

Angular rate sensitivity describes the angular rate gain of the sensor and can be determined by applying a defined angular velocity to it. This value changes very little over temperature and also very little over time.

2.6.2 Zero level

Linear acceleration Zero-*g* level offset (TyOff) describes the deviation of an actual output signal from the ideal output signal if no acceleration is present. A sensor in a steady-state on a horizontal surface measures 0 *g* in the X axis and 0 *g* in the Y axis, whereas the Z axis measures 1 *g*. The output is ideally in the middle of the dynamic range of the sensor (content of OUT registers 00h, data expressed as 2's complement number). A deviation from the ideal value in this case is called Zero-*g* offset. Offset is, to some extent, a result of stress to the MEMS sensor and therefore the offset can slightly change after mounting the sensor onto a printed circuit board or exposing it to extensive mechanical stress. The offset changes little over temperature, see "Zero-*g* level change vs. temperature". The Zero-*g* level tolerance (TyOff) describes the standard deviation of the range of Zero-*g* levels of a population of sensors.

Angular rate zero-rate level describes the actual output value if there is no angular rate present. The zero-rate level of precise MEMS sensors is, to some extent, a result of stress to the sensor and therefore zero-rate level can slightly change after mounting the sensor onto a printed circuit board or after exposing it to extensive mechanical stress. This value changes very little over temperature and also very little over time.

3 Functionality

The LSM320DL is a system-in-package featuring a 3D digital accelerometer and a 2D digital gyroscope.

The complete device includes specific sensing elements and two IC interfaces able to measure both the acceleration and angular rate applied to the module and to provide a signal to the external world through an SPI/I^2C serial interface.

The various sensing elements are manufactured using specialized micromachining processes, while the IC interfaces are realized using a CMOS technology that allows to design a dedicated circuit which is trimmed to better match the sensing element characteristics.

The LSM320DL may also be configured to generate an inertial wake-up and free-fall interrupt signal according to a programmed acceleration event along the enabled axes.

3.1 Factory calibration

The IC interface is factory calibrated for sensitivity and zero level. The trimming values are stored inside the device by a non-volatile memory. Any time the device is turned on, the trimming parameters are downloaded into the registers to be used during the normal operation. This allows the user to use the device without further calibration.

4 Application hints

Figure 5. LSM320DL electrical connection

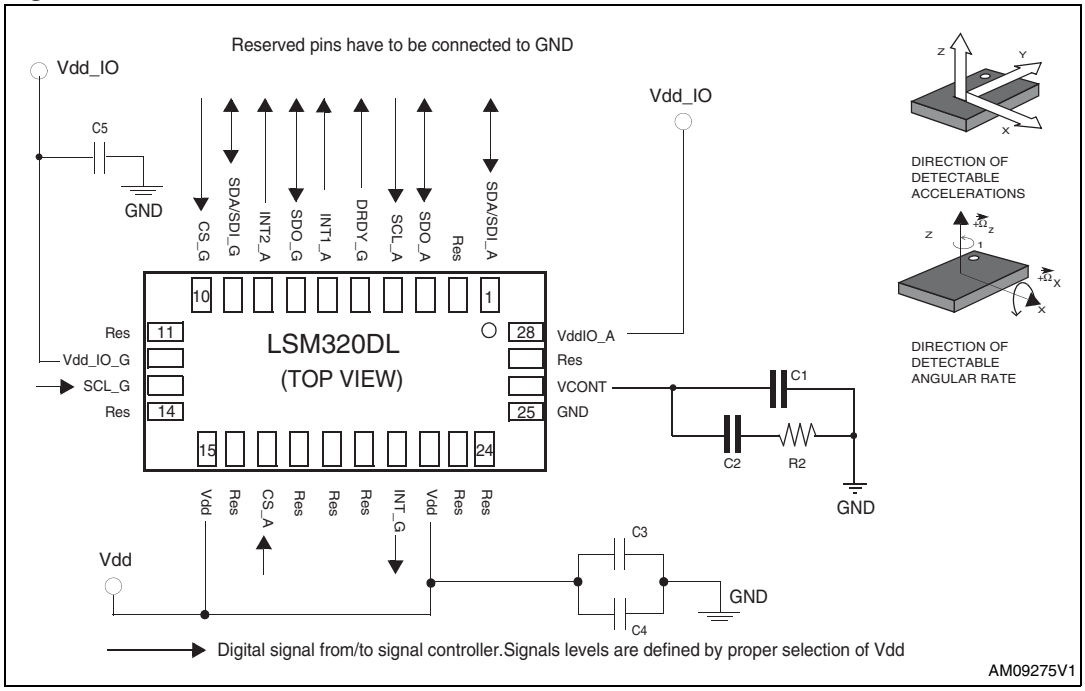


Table 9. Part list

Component	Typical value
C1	10 nF
C2	470 nF
C3	10 µF
C4	100 nF
C5	100 nF
R2	10 kOhm

4.1 External capacitors

The device core is supplied through Vdd line. Power supply decoupling capacitors (C4=100 *nF* ceramic, C3=10 *µF* Al) should be placed as near as possible to the supply pin of the device (common design practice).

All the voltage and ground supplies must be present at the same time to have proper behavior of the IC (refer to *Figure 5*).

The functionality of the device and the measured acceleration/angular rate data is selectable and accessible through the SPI/I^2C interface.

The functions, the threshold, and the timing of the two interrupt pins for each sensor can be completely programmed by the user though the SPI/I^2C interface.

4.2 Soldering information

The LGA package is compliant with the ECOPACK®, RoHS and “Green” standard.
It is qualified for soldering heat resistance according to JEDEC J-STD-020D.

Leave “Pin 1 Indicator” unconnected during soldering.

Land pattern and soldering recommendations are available at www.st.com/mems.

5 Digital interfaces

The registers embedded inside the LSM320DL may be accessed through both the I^2C and SPI serial interfaces. The latter may be SW configured to operate either in 3-wire or 4-wire interface mode.

To select/exploit the I^2C interface, CS line must be tied high (i.e. connected to Vdd_IO).

Table 10. Serial interface pin description

Pin name	Pin description
CS_A	Linear acceleration SPI enable Linear acceleration I^2C/SPI mode selection (1: I^2C mode; 0: SPI enabled)
CS_G	Angular Rate SPI enable Angular Rate I^2C/SPI mode selection (1: I^2C mode; 0: SPI enabled)
SCL_A SCL_G	I^2C serial clock (SCL) SPI serial port clock (SPC)
SDA/SDI_A SDA/SDI_G	I^2C serial data (SDA) SPI serial data input (SDI) 3-wire interface serial data output (SDO)
SDO_A SDO_G	I^2C less significant bit of the device address (SA0) SPI serial data output (SDO)

5.1 I^2C serial interface

The LSM320DL I^2C is a bus slave. The I^2C is employed to write the data into the registers whose content can also be read back.

The relevant I^2C terminology is given in the table below.

Table 11. Serial interface pin description

Term	Description
Transmitter	The device which sends data to the bus
Receiver	The device which receives data from the bus
Master	The device which initiates a transfer, generates clock signals and terminates a transfer
Slave	The device addressed by the master

There are two signals associated with the I^2C bus: the serial clock line (SCL) and the serial data line (SDA). The latter is a bidirectional line used for sending and receiving the data to/from the interface.

5.1.1 I²C operation

The transaction on the bus is started through a START (ST) signal. A START condition is defined as a HIGH to LOW transition on the data line while the SCL line is held HIGH. After this has been transmitted by the master, the bus is considered busy. The next byte of data transmitted after the start condition contains the address of the slave in the first 7 bits and the eighth bit tells whether the master is receiving data from the slave or transmitting data to the slave. When an address is sent, each device in the system compares the first seven bits after a start condition with its address. If they match, the device considers itself addressed by the master.

Data transfer with acknowledge is mandatory. The transmitter must release the SDA line during the acknowledge pulse. The receiver must then pull the data line LOW so that it remains stable low during the HIGH period of the acknowledge clock pulse. A receiver which has been addressed is obliged to generate an acknowledge after each byte of data received.

The I²C embedded inside the LSM320DL behaves as a slave device and the following protocol must be adhered to. After the start condition (ST), a slave address is sent, once a slave acknowledge (SAK) has been returned, an 8-bit sub-address (SUB) is transmitted: the 7 LSb represent the actual register address while the MSB enables address auto increment. If the MSb of the SUB field is '1', the SUB (register address) is automatically increased to allow multiple data read/write.

Table 12. Transfer when master is writing one byte to slave

Master	ST	SAD + W		SUB		DATA		SP
Slave			SAK		SAK		SAK	

Table 13. Transfer when master is writing multiple bytes to slave:

Master	ST	SAD + W		SUB		DATA		DATA		SP
Slave			SAK		SAK		SAK		SAK	

Table 14. Transfer when master is receiving (reading) one byte of data from slave:

Master	ST	SAD + W		SUB		SR	SAD + R			NMAK	SP
Slave			SAK		SAK			SAK	DATA		

Table 15. Transfer when master is receiving (reading) multiple bytes of data from slave

Master	ST	SAD+W		SUB		SR	SAD+R			MAK		MAK		NMAK	SP
Slave			SAK		SAK			SAK	DATA		DATA		DATA		

Data are transmitted in byte format (DATA). Each data transfer contains 8 bits. The number of bytes transferred per transfer is unlimited. Data is transferred with the most significant bit (MSb) first. If a receiver can't receive another complete byte of data until it has performed some other function, it can hold the clock line, SCL LOW, to force the transmitter into a wait

state. Data transfer only continues when the receiver is ready for another byte and releases the data line. If a slave receiver doesn't acknowledge the slave address (i.e. it is not able to receive because it is performing some real time function), the data line must be left HIGH by the slave. The master can then abort the transfer. A LOW to HIGH transition on the SDA line while the SCL line is HIGH is defined as a STOP condition. Each data transfer must be terminated by the generation of a STOP (SP) condition.

In order to read multiple bytes, it is necessary to assert the most significant bit of the sub-address field. In other words, SUB(7) must be equal to 1 while SUB(6-0) represents the address of the first register to be read.

In the presented communication format, MAK is Master Acknowledge, and NMAK is No Master Acknowledge.

Default address:

The **SDO**/**SA0** pad can be used to modify less significant bits of the device address. If the SA0 pad is connected to voltage supply, LSb is '1' (ex. address 0011001b), or else, if the SA0 pad is connected to ground, the LSb value is '0' (ex address 0011000b).

The slave address is completed with a Read/Write bit. If the bit is '1' (Read), a repeated START (SR) condition must be issued after the two sub-address bytes; if the bit is '0' (Write) the master transmits to the slave with direction unchanged. *Table 16* and *Table 17* explain how the SAD+Read/Write bit pattern is composed, listing all the possible configurations.

Linear acceleration address: the default (factory) 7-bit slave address is 001100xb.

Table 16. Linear acceleration SAD+Read/Write patterns

Command	SAD[6:1]	SAD[0] = SA0	R/W	SAD+R/W
Read	001100	0	1	00110001 (31h)
Write	001100	0	0	00110000 (30h)
Read	001100	1	1	00110011 (33h)
Write	001100	1	0	00110010 (32h)

Angular rate sensor: the default (factory) 7-bit slave address is 110100xb.

Table 17. Angular rate SAD+Read/Write patterns

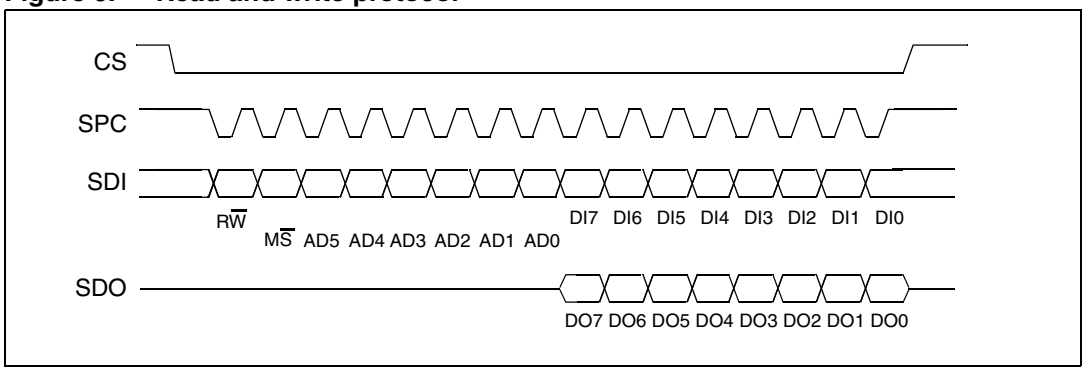
Command	SAD[6:1]	SAD[0] = SA0	R/W	SAD+R/W
Read	110100	0	1	11010001 (F1h)
Write	110100	0	0	11010000 (F0h)
Read	110100	1	1	11010011 (F3h)
Write	110100	1	0	11010010 (F2h)

5.2 SPI bus interface

The LSM320DL SPI is a bus slave. The SPI allows to write and read the registers of the device.

The serial interface interacts with the outside world with 4 wires: **CS**, **SPC**, **SDI**, and **SDO**.(SPC, SDI, SD0 are common)

Figure 6. Read and write protocol



CS is the serial port enable and it is controlled by the SPI master. It goes low at the start of the transmission and returns to high at the end. **SPC** is the serial port clock and it is controlled by the SPI master. It is stopped high when **CS** is high (no transmission). **SDI** and **SDO** are respectively the serial port data input and output. Those lines are driven at the falling edge of **SPC** and should be captured at the rising edge of **SPC**.

Both the read register and write register commands are completed in 16 clock pulses or in multiples of 8 in case of multiple bytes read/write. Bit duration is the time between two falling edges of **SPC**. The first bit (bit 0) starts at the first falling edge of **SPC** after the falling edge of **CS** while the last bit (bit 15, bit 23, ...) starts at the last falling edge of SPC just before the rising edge of **CS**.

bit 0: R$\overline{W}$ bit. When 0, the data DI(7:0) is written into the device. When 1, the data DO(7:0) from the device is read. In the latter case, the chip drives **SDO** at the start of bit 8.

bit 1: M$\overline{S}$ bit. When 0, the address remains unchanged in multiple read/write commands. When 1, the address is auto incremented in multiple read/write commands.

bit 2-7: address AD(5:0). This is the address field of the indexed register.

bit 8-15: data DI(7:0) (write mode). This is the data that is written into the device (MSb first).

bit 8-15: data DO(7:0) (read mode). This is the data that is read from the device (MSb first).

In multiple read/write commands, further blocks of 8 clock periods are added. When the M$\overline{S}$ bit is ‘0’, the address used to read/write data remains the same for every block. When the M$\overline{S}$ bit is ‘1’, the address used to read/write data is increased at every block.

The function and the behavior of **SDI** and **SDO** remain unchanged.